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Design and Implementation of Soft Switching Boost Converter

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***Abstract*—**The design and implementation of closed loop soft switching boost DC-DC converter have been proposed. The staedy state analysis of open loop converter with operational modes are evaluated. Equations for the design of all the circuit parametrs are attainted and discussed in details for simulation and experimental purpose. The proposed circuit has resonant circuit which has one inductor and two capacitor to achieve soft switching of converter by operating it at zero voltage condition..

***Keywords*—** *Positive output voltage, Voltage, stability, voltage stress.*

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1. INTRODUCTION

A boost converter is generally a DC-DC converter that produces output voltage based on the supplied input voltage. Lower voltage gain is a drawback for stepping converters in several applications. Various converter technologies are established to meet the limitations. DC/DC converters are widely used in many applications.
In special applications, such as military affairs, aerospace, winches,sensitive control instrumentation, renewable energy interfacedevices, and motor speed control, dc/dc converters are efficientlybeing utilised [1–4]
Reducing or eliminating the switching losses will be possible if the product of the voltage and current of the switch is zero right before the transition . In order to realise the soft-switching feature, many techniques have been presented in the literature, which all are based on three main categories: zero-voltage switching (ZVS), zero-current switching (ZCS), and zero-voltage zero-current switching . By ZVS, high-frequency switching is possible for the MOSFETs. Thus, the size of the converter is decreased, without any increase in switching losses . In addition, insulatedgate bipolar transistors (IGBTs) are the most appropriate switches for providing ZCS conditions[5]
By adding a clamp diode, voltage oscillations on the diode will be removed, but the ZVS range for both switches decreases. The clamp diode increases the freewheeling current, which results in higher conduction losses . The main switch in series with auxiliary one leads to high conduction losses . In the structure presented in , the clamping circuit is complicated, and there are many elements. Moreover, because of high-voltage stress on the clamping diode, costs and conduction losses are accordingly high. By adding a resonant circuit, ZVS conditions are provided , but the auxiliary circuits are complicated and have very high-voltage stresses.[5-9]
In , a soft-switching bidirectional dc/dc converter has been presented, which utilises an auxiliary active lossless snubber circuit, in order to provide softswitching conditions. In this converter, the switches are turned on with ZVS, but due to not having ZCS conditions, the turning off transitions are lossy. In this structure, the large number of the semiconductors and energy storage devices lead to more complexity, high losses, and high costs. In this paper, according to the usage of auxiliary elements and resonant circuit, ZVS conditions have been provided for the switches. Theoretical analysis of the operating modes shows that high current and voltage stresses can significantly be reduced, during the transitions. The design considerations have been proposed in detail. [10]

2. Soft Switch DC-DC Boost converter

In Fig. 1, V_i is the input dc voltage, S_1 is the auxiliary switch, C_1 parallel capacitor of S_1, D_1 and D_2 are auxiliary elements for resonant circuit, L_1 is the resonant inductor, S_2 is the main switch, C_2 is the parallel capacitor of S_2, D_o

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is the output diode, L is the filter inductor, C_o is the filter capacitor, and R is the load resistance.

2.1 Analysis of the converter

Mode 1 *($0 \le t < t_1$)*

In this operating mode, S_1, S_2, and D_o are on, while D_1 and D_2 are off. The voltages across S_1 and C_1 ($vS_1 = vC_1$),S_2 and C_2 ($vS_2 = vC_2$), and D_o (v_{Do}) are zero, as well as the currents through C_1 (iC_1), C_2 (iC_2), D_1 (iD_1), and D_2 (iD_2). Moreover, accordingto this figure, it can be written as

$$vL_1 = -vD_1 = -vD_2 = V_o \qquad (1)$$

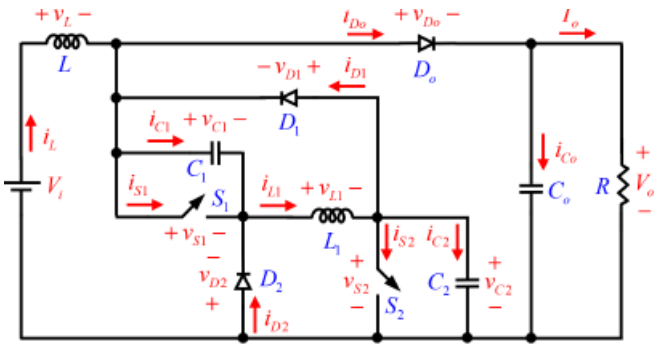

Fig1: Soft switch DC-DC converter

Mode 2 *($t_1 \le t < t_2$)*

In this operating mode, S_1 and S_2 are on, while D_1, D_2, and D_o are off. According to Fig. 1*b*, vS_1 and vS_2 are zero, as well as iC_1, iC_2, iD_1, iD_2, and i_{Do}. In addition, iS_1, iS_2, and iL_1 are equal to I_i.The current through L_1 has a constant value, thus the voltage across it (vL_1) will be zero. Consequently, based on Fig. 1*b*, vD_1 and vD_2 will be zero, too. Therefore, according to KVL, v_{Do} will be $-V_o$.

Mode 3 *($t_2 \le t < t_3$)*

In this operating mode, S_1 and D_1 are on, while S_2, D_2, and D_o are off. According to Fig. 1*b*, vS_1 and vD_1 are zero, as well as iS_2, iC_1, iD_1, iD_2, and i_{Do}. In addition, iS_1, iC_2, and iL_1 are equal to I_i.The current through L_1 has a constant value. Thus, the voltage across it (vL_1) will be zero.The current through C_2 has a constant value, so according to KVL, the voltage across it (vC_2) can be calculated as follows:

$$Vs2 = Vc2 = -VD2 = \frac{Ii}{C2}t \qquad (2)$$

Mode 4 *($t_3 \le t < t_4$)*

In this operating mode, S_1, D_1, and D_o are on, while S_2 and D_2 are off. According to Fig. 1*b*, vS_1, vD_1, and v_{Do} are zero, as well as iS_2,iC_1, and iD_2. In addition, iS_1, iD_1, i_{Do}, and iL_1 are equal to I_i. The voltage across C_2 is equal to V_o, which means the current through it is zero.

Mode 5 *($t_4 \le t < t_5$)*

In this operating mode, D_1 and D_o are on, while S_1, S_2, and D_2 are off. Noticing Fig. 1*b*, vD_1 and v_{Do} are zero, as well as iS_1, iS_2, and iD_2. The voltage across C_2 is equal to V_o, which means the current through it is zero. Therefore, according to KCL, the current through D_o will be equal to I_i.

$$Vc1 = Vs1 = Ii\sqrt{\frac{L1}{C1}}\sin\omega_{r1}t \qquad (3)$$

$$Vd2 = Ii\sqrt{\frac{L1}{C1}}\sin\omega_{r1}t - V0 \qquad (4)$$

Mode 6 *($t_5 \le t < t_6$)*

In this operating mode D_1, D_2, and D_o are on, while S_1 and S_2 are off. Noticing Fig. 1*b*, vD_1, vD_2, and v_{Do} are zero, as well as iS_1 and iS_2. In addition, vS_1 and vS_2 are equal to V_o. The voltages across C_1 and C_2 have constant values, which means the current through them are zero.

$$iD1 = iD2 = iL1 = Ii\sqrt{1 - \frac{C1V0^2}{L1Ii^2} - \frac{V0}{L1}t} \qquad (5)$$

Mode 7 *($t_6 \le t \le t_7$)*

In this operating mode D_o is on, while S_1, S_2, D_1, and D_2 are off. According to Fig. 1*b*, v_{Do} is zero, as well as is_1, is_2, iD_1, and iD_2. In this operating mode, L_1 resonates with C_1 and C_2

$$Ic1 = ic2 = iL1 = -V0\sqrt{\frac{C1}{2L1}}\sin\omega_{r2t} \qquad (6)$$

$$Vs1 = Vc1 = Vs2 = Vc2 = \frac{V0}{2}(1 + cos\omega_{r2t}) \qquad (7)$$

$$iD0 = Ii - iC2 = Ii + V0\sqrt{\frac{C1}{2L1}}\sin\omega_{r2t} \qquad (8)$$

conventional ones for satisfying the industrial oriented requirements is very valuable and important.

3. DESIGN CONSIDERATION

$$R = \frac{V0^2}{P0} = \frac{18^2}{30} = 12\Omega$$

$$Ii = \frac{V0^2}{RVi} = \frac{P0}{Vi} = 2.25A$$

$$C1 = \frac{1}{(2\pi fsk)^2 L1} = \frac{4.06e-15}{L1}$$

$$L1 = \sqrt{\frac{4.06e-15}{1.5e-4}} = 0.1mH$$

$$C1 = \frac{4.06e-15}{5e-6} = 0.4\mu F$$

Figure 3: simulation results in MATLAB: (a) simulink model of soft switching DC-DC boost converter, (b)

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output voltage and current, (c)&(d) ZVS condition across main switch and auxillary switch, (e) closed loop circuit of soft switch dc-dc converter,(f) bode plot of the converter in open loop,(g) step response of the converter in open loop,(h) outpower,(j) gate to source voltage across switch s1, (k) gate to source voltage of switch s2,(l) drain to source voltag e of switch s1, (m)drain to source voltage of switch s2, (n) hardware model of soft switching DC-DC boost converter,(o)simulink model of AC-DC boost converer,(p)primary and the secondary voltage across the transformer,(q)voltage and current across the bridge rectifier ,(r)output voltage and current of the AC-DC soft switching boost converter ,(s) total harmonic distortion of the input current without fiter circuit,(t)total harmonic distortion with LC filter circuit ,(u)hardware model of the AC-DC soft switching boost converter,(v 12volts dc voltage from the rectifier bridge ,(w) output voltage of the AC-DC softswitchingboostconverter

According to Fig. 3*b*, by turning S_1 off, the voltage across it sinusoidally rises to 18 V, during the first resonant

According to Fig. 3*c*, by turning S_1 off, the voltage across it sinusoidally rises to 18 V, during the first resonant mode. While S_1 is off, vS_1 is fixed on 8 V until the second resonant mode, which makes vS_1 decrease to zero, sinusoidally. At the end of this mode, S_1 turns on by ZVS.

According to Fig. 3*d and fig 3l* , by turning S_2 off, the voltage across it sinusoidally increases to 8 V, during the first resonant mode.

According to Fig 3e and fig 3m, the bode plot of the soft switching dc-dc boost converter is obtained. It is found that the converter in open loop operation is unstable.

According to Fig 5f, the step reponse of the converter in open loop is obatined.it is found that the converter has high stady state error

From fig 3i the output voltage of 18 volts is shown in the CRO it is verified with the simulation result and the theoretical calculation

From fig 3p the primary and secondary voltage of the step down is shown it is found that the primary voltage is 30 volts AC and it is stepdown to 12 volts AC

From fig 3q the 12 volt AC voltage is rectified to 12 volts DC using the recifier bridge.

From fig 3r the output voltage of the 18 volts DC is obtained in the MATLAB simulink.

From fig 3s the input AC current has the toltal harmonic distortion of 44.9%

From fig 3t the total harmonic distortion of input AC current is reduced to 0.19% using a LC filter at the input side.

From fig 3 the DC 12volts is seen in the CRO from the rectifier bridge which is given as the input to the converter circuit.

From fig 3w the output voltage of 18 volts of the converter is seen in the CRO.which is verified from the MATLAB simulink and the theoretical calculation.

However, for the output powers between 26 and 33W the switching loss of the main switch is lower than the conduction loss of the auxiliary elements, which recommends that the usage of the auxiliary elements for achieving soft-switching feature is useful, and will lead to loss reduction for the proposed converter. Similarly, for output powers >33 W the conduction loss is higher than the switching loss, which means using auxiliary elements does not make any sense for having ZVS.

The hardware model is developed using the designed values. As shown in the design procedure.the gate pulses aree generated using the 555 timer for both the switches of duty cycle 76% and 54% with 10khz as the frequency.

A AC-DC boost converter is also developed and simulated using the MATLAB simulation. The AC voltage of 230 volts is step down to 12volts AC using step down transformer then it is rectified to 12 volts DC with the bridge rectifier.the main advantage of this circuit is we can operate the boost converter with AC voltage.

The harware model are developed with the following specifications as shown in the table below.

Mosfet, S1 and S2	Irf540, Irfz44n
Diode,D1,D2,D0,D3	1n5819
Input voltage, Vin	12v
Output voltage, Vout	18v
Switching frequency	10KHz
Capacitor C1 ,C2 and C0	0.4µf, 500µf
Inductor L and L1	1mH, 0.1MH

Table 1: stability analysis of open loop and closed loop

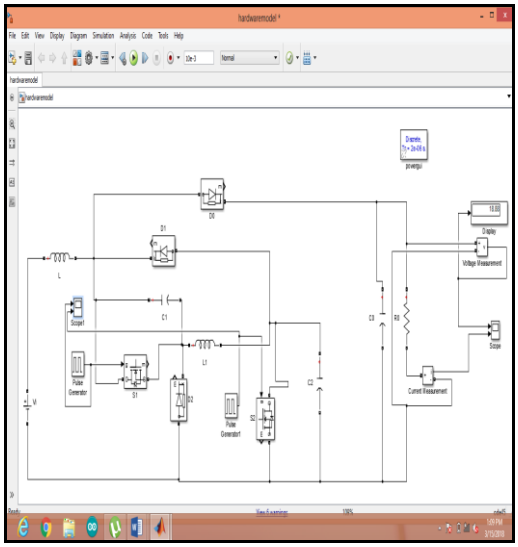

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Figure 3

	Rise time(sec)	Settling time (sec)	Steady state error	stability	Phase Margin	Gain margin
Open loop	0.0032	0.0429	0.5	unstable	-37.5	-88.1

(a)

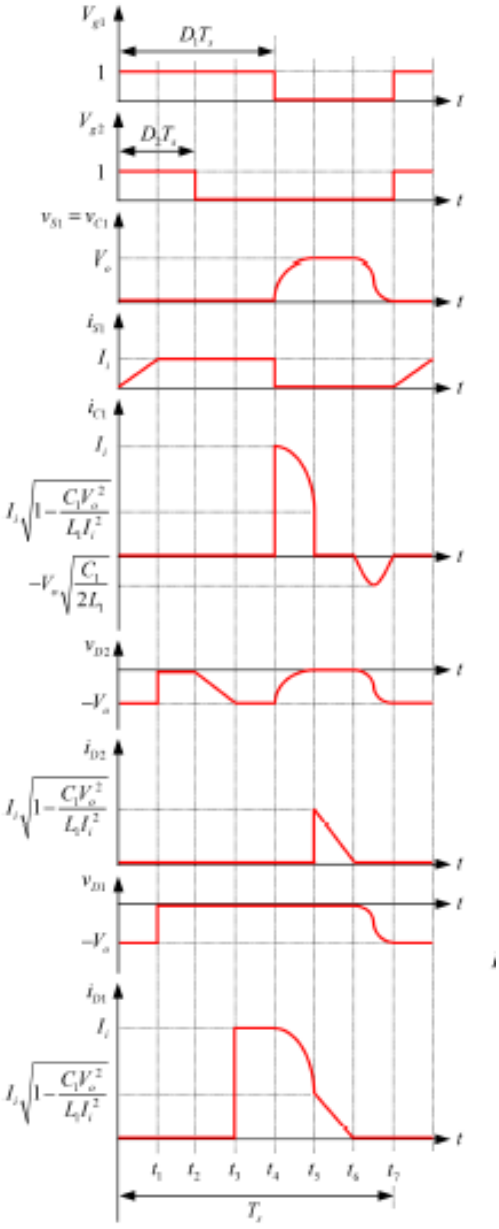
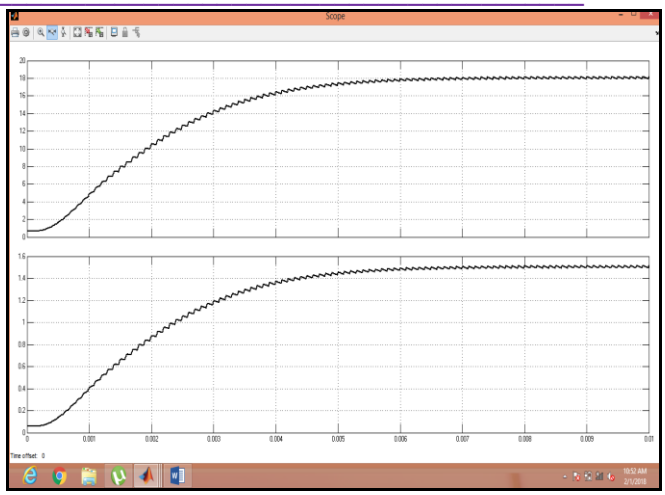


Fig. 2 Ideal waveforms of the voltages of DC-DC converter



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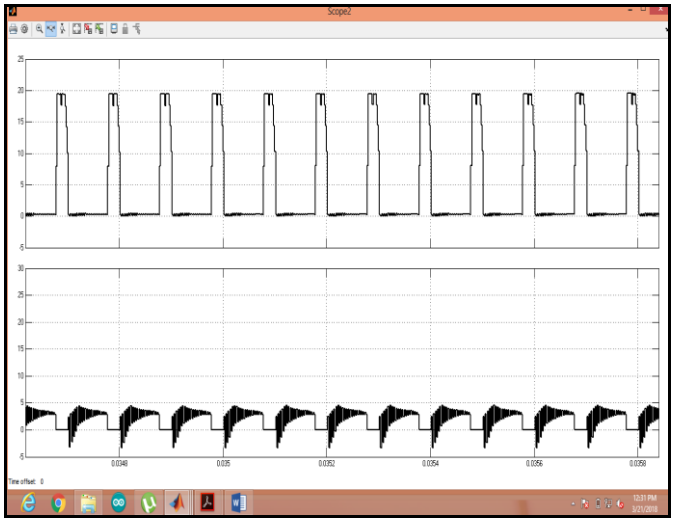

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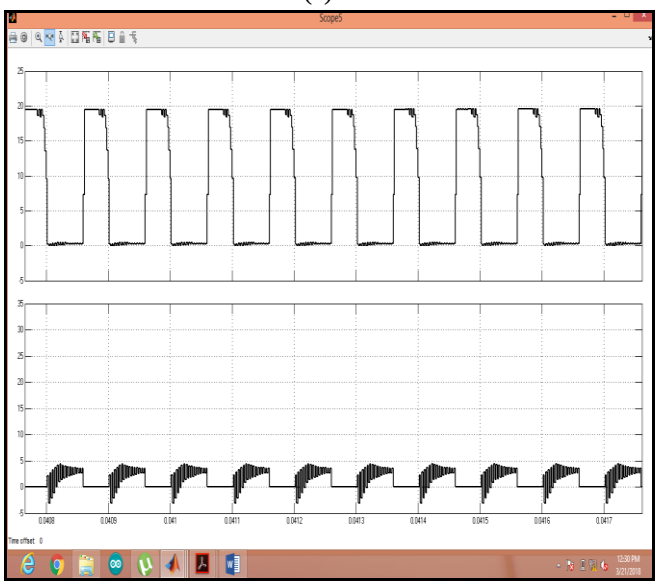

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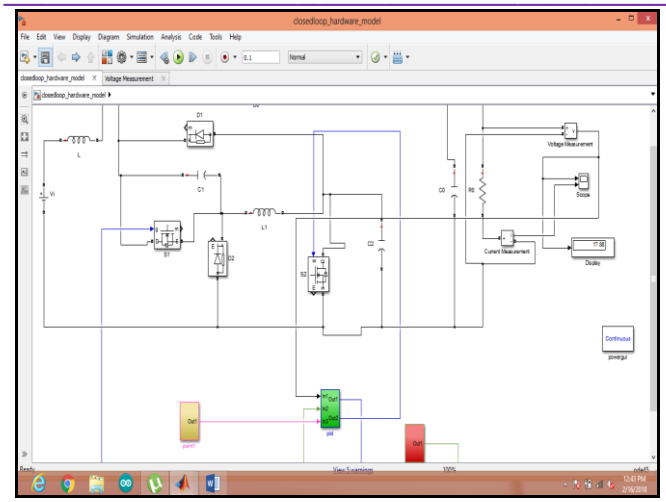

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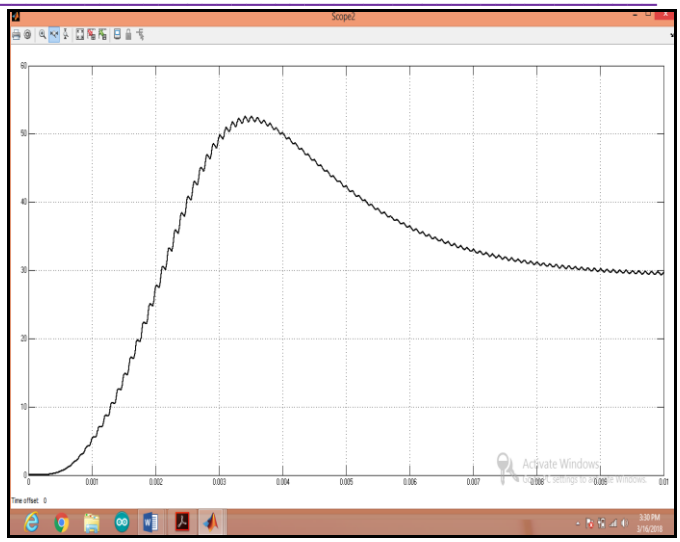

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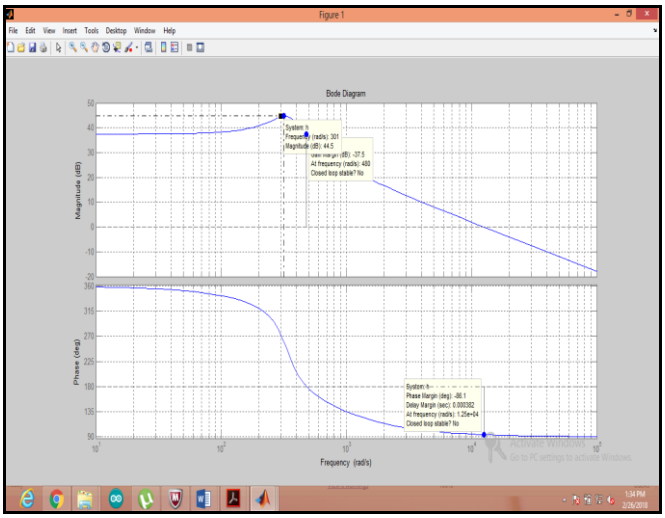

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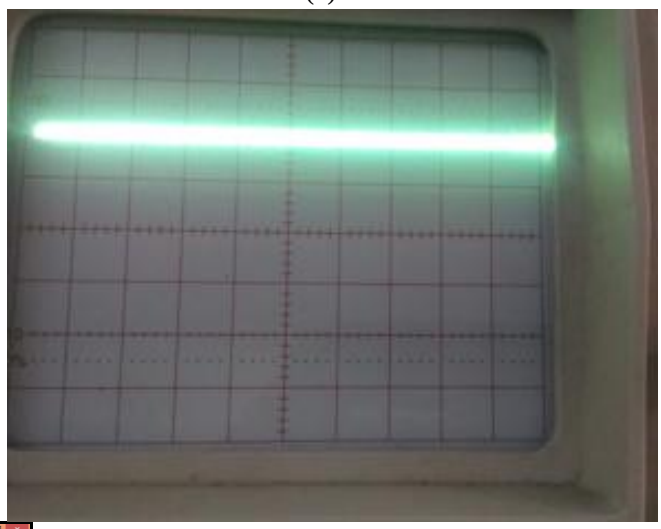

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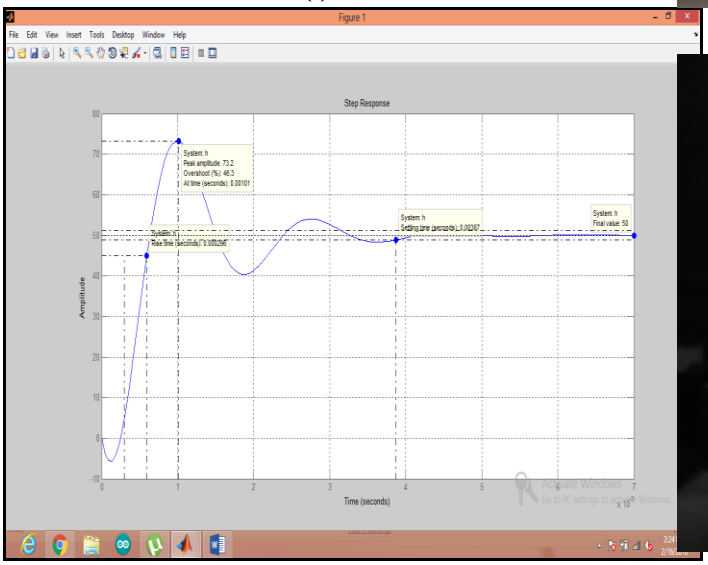

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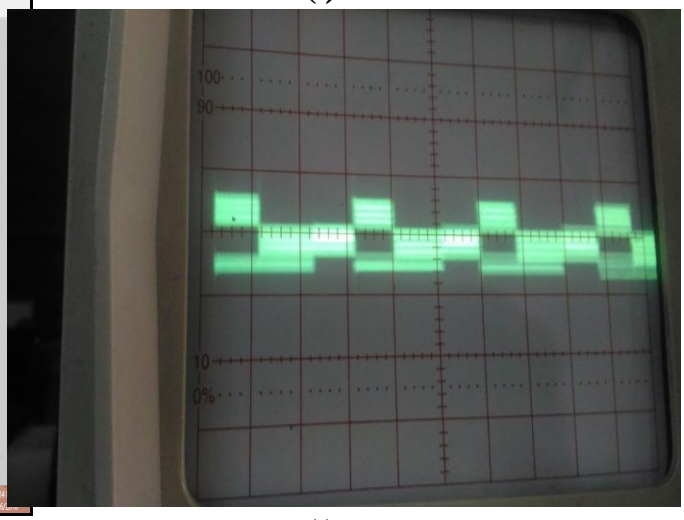

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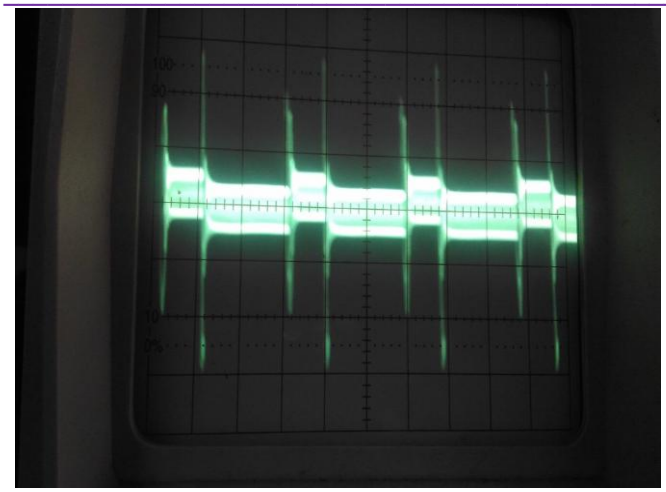

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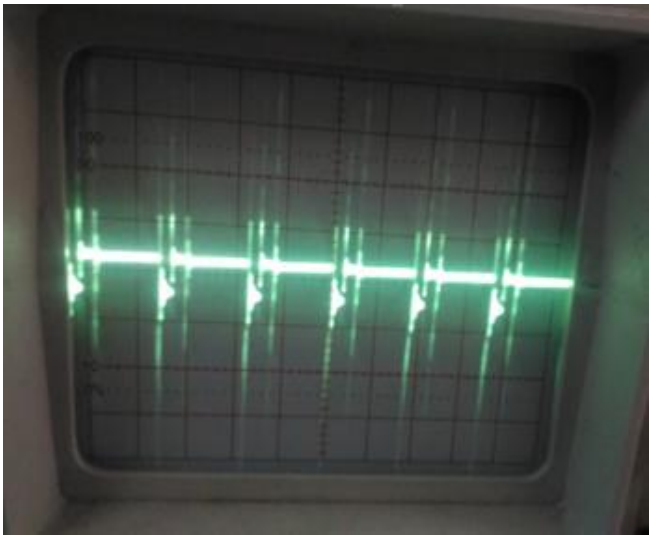

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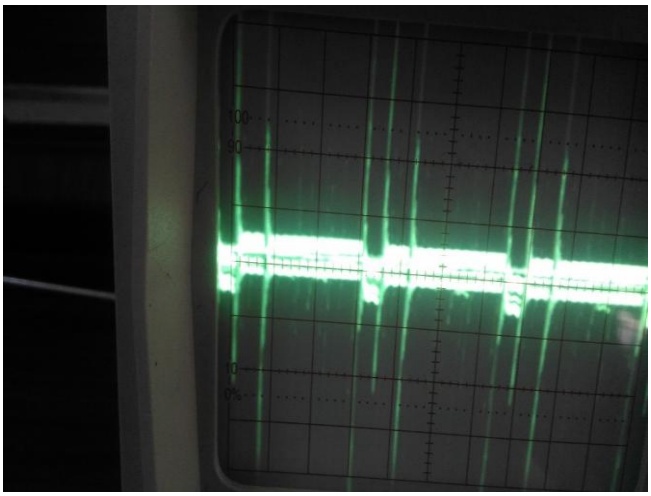

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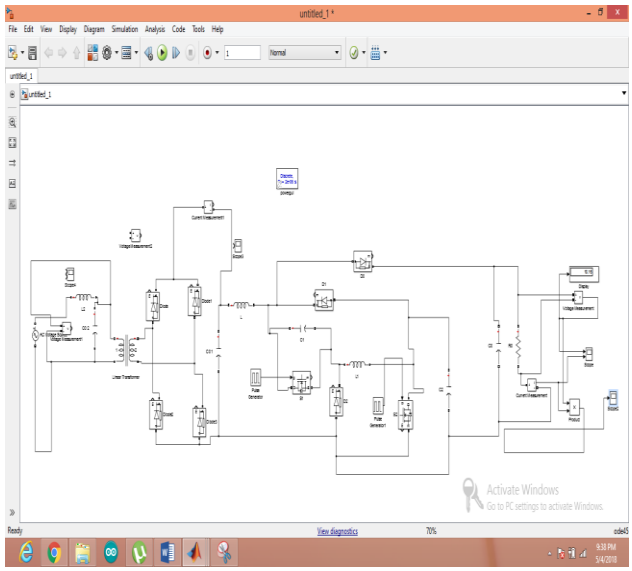

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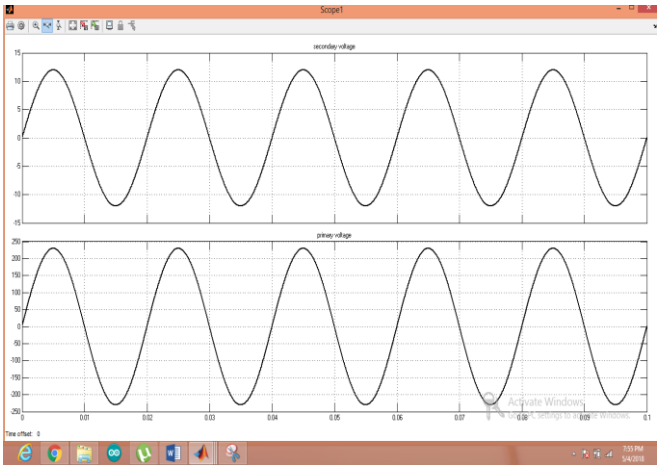

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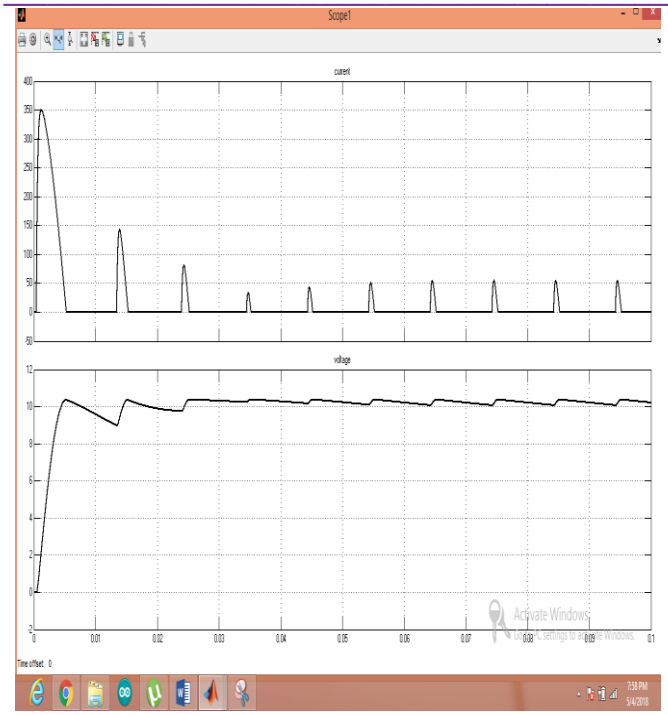

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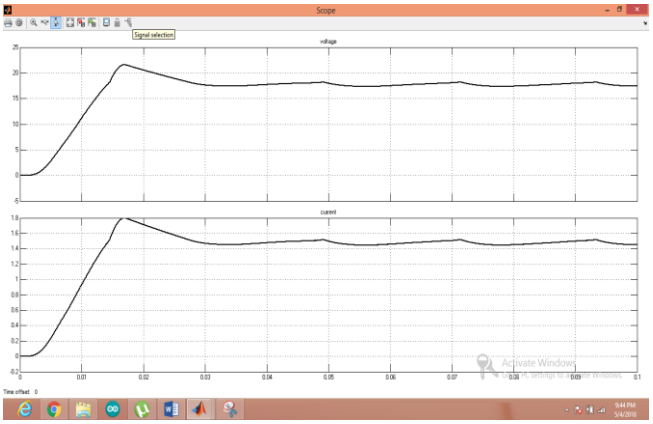

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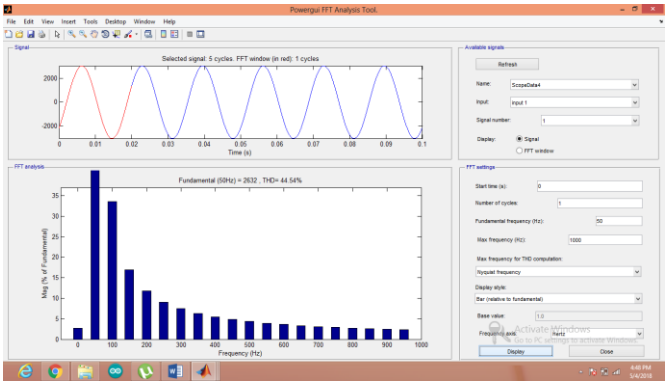

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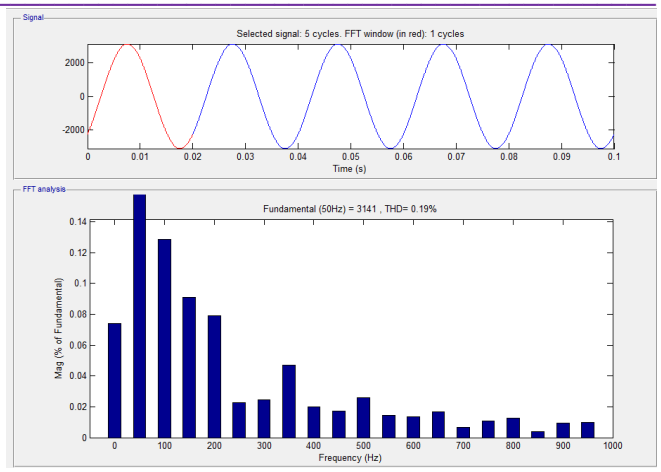

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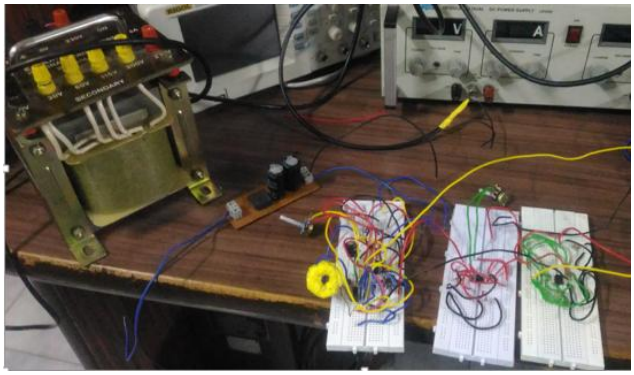

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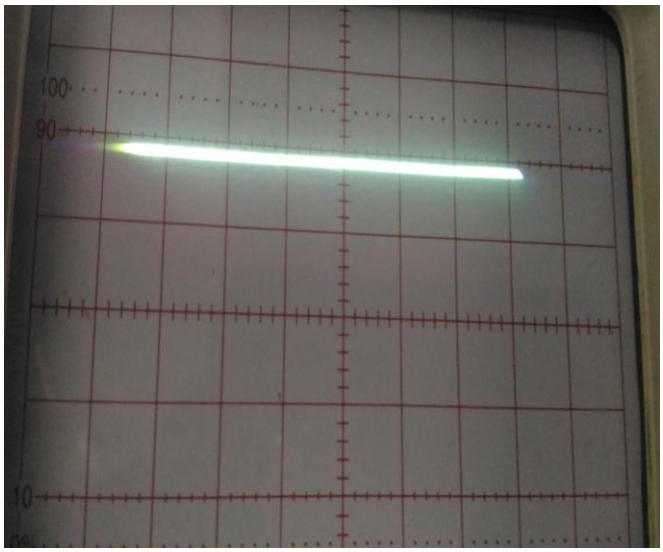

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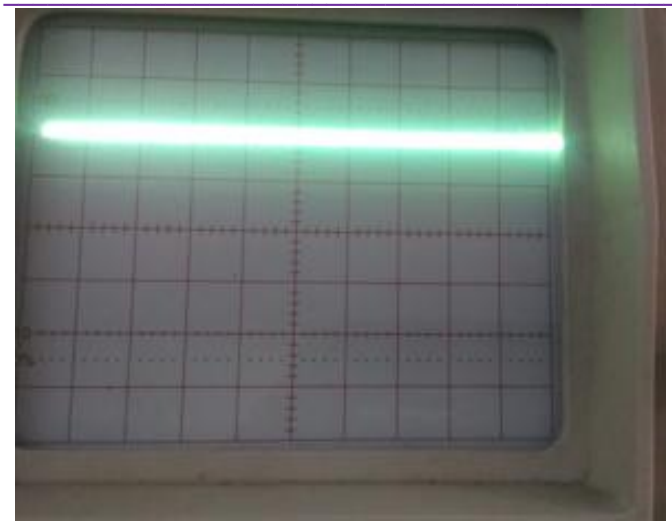

(w)

5. Conclusion

In this paper, analysis, design, experimental, and simulation results of soft-switching boost ac-dc and dc/dc converter have been presented. By using the soft-switching technique, voltage and current stresses are reduced. At the end of the seventh operating mode, due to the resonant circuit, the voltage across the switches reduce to zero, which allows both switches. However, both switches have hard switching at the turning off transitions, due to the absence of ZCS conditions. Design considerations and device selection have been proposed in thorough details, using the equations obtained in analysis.. The proposed structure provided ZVS conditions at ON transitions, and decreased the voltage and current stresses of both main and auxiliary switches increase.from the simulation reults is evident that the stabity of the system inreases to stsbe from unstable. The output is maintained constant with the help of controller.The stady state error of the system is decreased.

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