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A Low Power Asynchronous Viterbi Decoder using LEDR Encoding

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***Abstract*—** With the consumer demand for increased content and as a result, increasing high data bandwidth continuing to drive communications systems, coding for error control has become extraordinarily important. One way to improve the Bit Error Rate (BER), while maintaining high data reliability, is to use an error correction technique like the Viterbi algorithm. Originally conceived by Andrew Viterbi as an error-correction scheme for noisy digital communication, the Viterbi algorithm provides an efficient method for Forward Error Correction (FEC) that improves channel reliability. Today, it is used in many digital communications systems in applications as diverse as LTE Physical Downlink Control Channel (PDCCH), CDMA and GSM, digital cellular, dial up modems, satellite, deep-space communications, and 802.11 wireless LANs.

Though it is useful for error correction it dissipates large power. A lot many researches were carried out at architectural as well as algorithmic level to optimize the ACS (Add compare and Select) unit and Survival Memory Management in Synchronous Viterbi Decoders. But still there is a problem of power dissipation which requires more technical solutions. Due to requirements of high speed, low power, low weight and long battery life a low power Viterbi decoders has a great demand in the communication field. This paper proposed the method for survivor path storage and decoding as Minimum Transition Hybrid Register Exchange Method along with handshaking protocol as Level Encoded dual rail (LEDR) encoding to make the system asynchronous. The whole system has been designed on algorithmic level and Simulation is done on Xilinx Tool for Asynchronous Viterbi Decoder using MTHREM.

Keywords- *Asynchronous Viterbi decoder, MTHREM, LEDR Encoding.*

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I. INTRODUCTION

In 1967 Andrew J. Viterbi invented a Viterbi decoder algorithm. The Viterbi Algorithm has vast usage to decode the Convolutional codes even if the medium is noisy. Viterbi decoder algorithm is a recursive algorithm which is applicable

to find the shortest path through a trellis. Therefore it is an ideal Trellis Decoder. It has capability to handle extremely high speeds. In Mobile station baseband modem Viterbi decoder occupies large space and hence more power dissipation. Therefore, practical implementations of a low-power Viterbi decoder is a needbased matter.

There are two methods for survivor path storage and decoding, the Trace- back method (TBM) and Register Exchange method (REM). Memory requirement is high in Traceback Method. TBM is the traditional decoding method used in Viterbi decoders .It is mostly used where there is a large requirement of constraint length and also high performance. But this method has drawbacks, like it requires last-in-first-out (LIFO) buffer and also it has to use multiple read operations whenevere there is requirement for high speed operations. Due to multiple operation complex logic circuits are required .The REM requires registers to save the data of every cycle. Due to huge switching activity, it will consume large power and area. If we combine the TB and REM, problem of switching activity of viterbi decoder is reduced comparatively and that is Hybrid Register Exchange Method (HREM).

This paper is arranged in sections as follows .In section II the Design Flow of the whole system has been discussed. The Convolutional Encoder and Viterbi Decoder and their components in sections III & IV. Section V gives detailed idea of decoding methods using REM, HREM and MTHREM .In section VI we have presented the Handshaking protocols i,e. 4 phase and 2 Phase dual rail encoding (LEDR) to make the system asynchronous for low power consumption. In section VII & VIII the simulation results are discussed by using MTHREM method.

II. DESIGN FLOW OF VITERBI DECODER

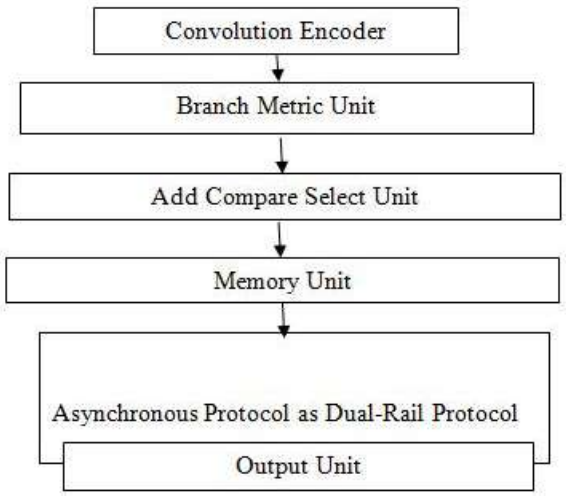

Figure 1. Design Flow

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III. CONVOLUTIONAL ENCODER

Convolutional encoder is generating the data bit streams which acts as input data for Viterbi Decoder to transmit in wireless medium. A convolutional encoder encodes single bit data and generate two bit code word. As shown in Figure 1 two memory elements FF1 and FF0 which holds and shifts input data and generates Out0 and Out1 by Ex-ORing operations. The designed Convolutional encoder has three terms : n, k and K, where n is termed as code rate=1/2, k is the number of input bits and K is called constraint length. The encoder accepts one bit as input and generates two bit codeword at every cycle of operation

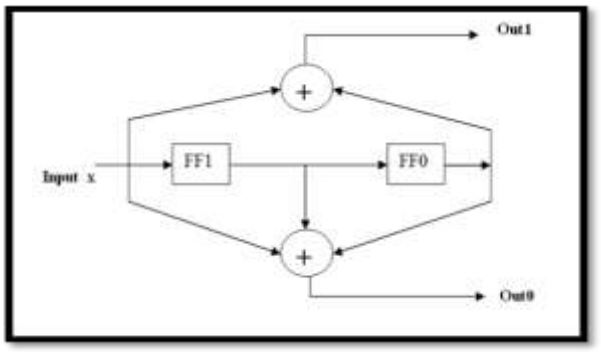

Figure 2. Block diagram of convolutional encoder

K=3, k=1, n=2

The encoded sequence is generated by following as

$$Out0 = Input \oplus FF1 \oplus FF0 \quad (1)$$

$$Out1 = Input \oplus FF0 \quad (2)$$

A. Units

- Use either SI (MKS) or CGS as primary

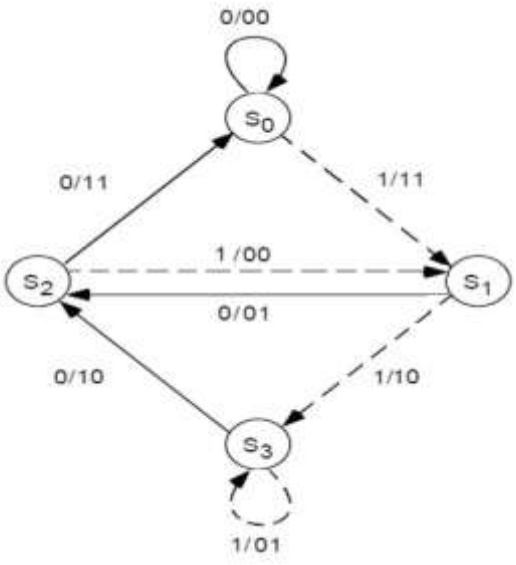

Figure 3. State Diagram of Encoder

From figure 2 it is observed that it has two memory storage (m) as FF1 and FF0 where the data bits saved temporarily. As two memories therefore it has four states as S_0 S_1, S_2, S_3 (2^m). Input bits alongwith the contents of flip flops does the Ex-oring operation and generates the encoded two bit output code for every incoming single bit and therefore the code rate is ½.

IV. VITERBI DECODER

Once the data is transmitted by Convolutional encoder it is received by the Receivers at the destination. With the help of the trellis diagram, Viterbi Decoder decodes the received bit streams by finding the sequence with the maximum likelihood. Viterbi decoder consists of three basic building blocks.

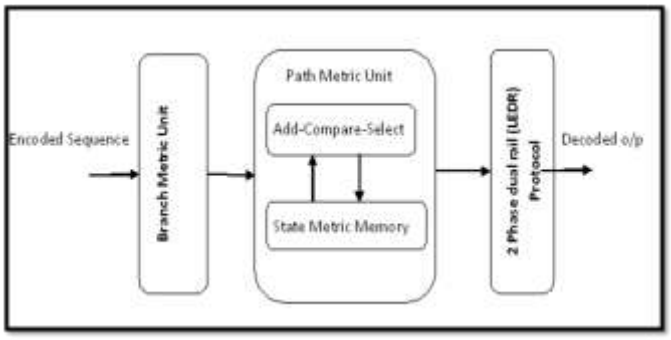

Figure 4. Block diagram of the proposed Asynchronous Viterbi decoder

The branch metric Unit (BMU), the Add-Compare-Select Unit (ACSU) and the Trace Back Unit (TBU). The BMU compares the received bits and the expected bits and generates the differ bits. The ACS unit adds the branch metrics with previous state metrics and generates path metrics. After this summation the value of each state is updated, both the path metrics are compared and lower metric path is selected as the survivor path. With the changes of BMU and ACSU decision processing is done by TB unit and decoded data accordingly.

V. DECODING METHODS:

1 REGISTER EXCHANGE METHOD

Traceback & Register-exchange methods are used to record survivor branches. As shown in Figure 4, there are total four states and to every state one register is assigned which contains information bits for the survivor path. At every cycle of trellis the information bits are recorded. As two memory elements are used therefore total states are 4 and the corresponding registers required are 2^m .Every register stored the partially decoded data while processing. As the data copies from previous register at t=1 to next register at t +1 instant therefore the register exchange method doesn't require to process the data from back to front. As the data processed throughout the trellis therefore the register of final state stores the decoded output. As memory requirement is

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high the REM is more complex. As data is copied from one register to next register at every cycle switching activity increases and so power consumption of the decoder is very high.

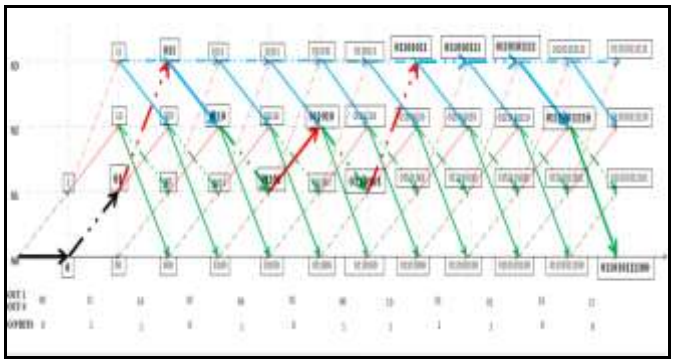

Figure 5. Register Exchange Method

2 HYBRID REGISTER EXCHANGE METHOD

To remove the drawbacks of REM we combine the Traceback and Register Exchange method called Hybrid Register Exchange method. In HREM the data is processed in alternate cycles but not in every cycle. As data is not switched frequently from one register to other the power is comparatively reduced. As shown in figure 6, every state holds the corresponding data bits and trellis progresses in alternate cycles from t=2, t=4, t=6, to t=12. First we have to traceback through trellis of encoder for survival memory locations and then the partial decoded data is transferred from initial state to next state. At t=2 , '01' are the corresponding state bits which is transferred at state S2 in t=4 cycle therefore the total bits of S2 at t=4 are "0110".The data is copied from S1 to S2 and so on till t=12 instant where finally all the decoded data gets accumulated. Here the operation is in alternate cycles and not in every cycle like REM therefore the dynamic power is comparatively reduced.

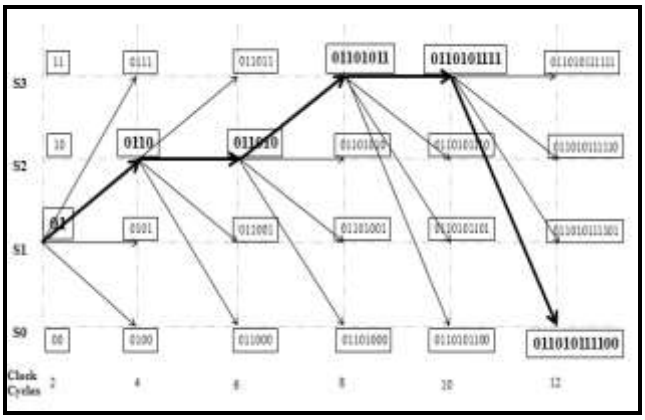

Figure 6. Hybrid Register Exchange Method

3 MINIMUM HYBRID REGISTER EXCHANGE METHOD

The drawback of REM and HREM can be reduced by avoiding unwanted transitions that leads to more power consumption. Therefore we further tried to get low power consumption than REM and HREM.

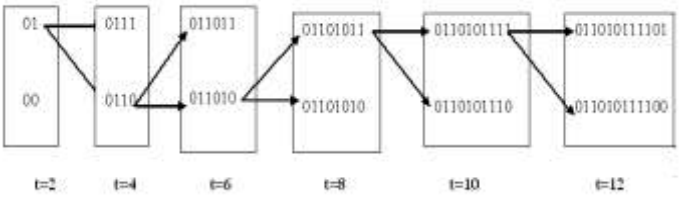

Figure 7. Minimum Hybrid Register Exchange Method

In minimum transition algorithms (MTHREM) we utilized a free distance property of Encoder. Free distance gives information about the errors in the received bits which can be corrected by the Viterbi decoder. We set up these errors as a threshold and observed that above the threshold the error cannot be corrected, so there is no need for storing the survivors which has a path metric above this threshold. In our Viterbi decoder the error correcting capability is 2 .Therefore we skip those transitions whose metric is greater than 2 .The decoder gets rid of those unnecessary data transfer which happened in REM and HREM. Registers requirement for data transfer is half than REM and HREM i.e. $2^m/2$. Here data transfer and traceback operations are placed at m^{th} instant, therefore switching activity and power dissipation further reduces.

From the state diagram shown in figure 2, we can obtain a closed form expression.The expansion of these expressions gives all distant information directly. In figure 8, we have labeled the branches emerging from their nodes i.e states as D2, D and D0 = 1. The exponent is nothing but the distance of particular branch from the corresponding branch of all zero paths. As shown in figure 8, if we starts adding the branch exponents, the path S0-S1-S2-S0 is at distance 5 from the correct path, and S0-S1-S3-S2-S0 and S0-S1-S2-S1-S0 has distance 6 respectively.

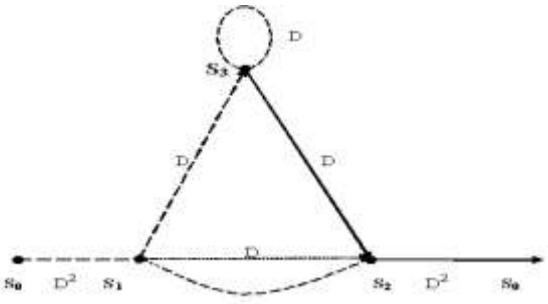

Figure 8. Free Distance property of Encoder

So the free distance is nothing but the minimum Hamming distance which is 5. Therefore number of error bits calculated by formula 2t+1< = 5, gives value of t=2 .Therefore our decoder has error correcting capability is 2.

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VI. ASYNCHRONOUS VITERBI DECODER

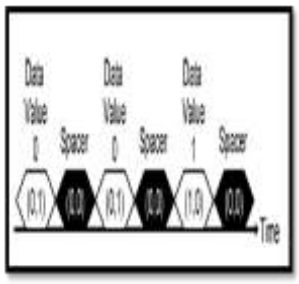
In synchronous a global clock should provide the clock signal to all the receivers to carry out different operations for data transfer. Till the completion of operation Synchronous systems provide the clock signal even if the device under operation is working or in standby mode. To remove this drawback clock-gating was used. But the system itself proved complex. So to get rid of such problems low power asynchronous architectures were used where timing is managed locally. Instead of providing a global clock we can use local clocks to reduce power consumption. In Asynchronous System there is a mutual agreement between sender and receiver on data transfer speed. Here sender provides a synchronization signals to receiver before sending the message signal and as soon as receiver acknowledges the data transfer starts .Here the devices which are taking part in process only utilizes the clock signals and thus helps to reduce power of the system.

Therefore Handshaking Protocols is one of the solutions to make the system Asynchronous for low power dissipation.

Delay encoding can be represented by two ways:

I) **4 Phase Dual Rail Encoding** :

Here each bit data is represented by two wires. "01"represents logic 0, while "10" represents logic 1. "00" state is a null state. After a data value Sender sends spacer (0, 0). The receiver came to know the arrival of a data value by detecting the change of either bit 0 to 1.Addition of spacer in 4-phase dual-rail encoding gives low throughput and this is the major drawback.

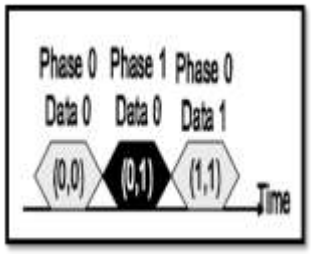


	Codeword (t, f)
Data 0	(0,1)
Data 1	(1,0)
Spacer	(0,0)

Figure 9. 4 phase dual Rail Encoding

II) Level-encoded dual-rail encoding (LEDR):

The another delay insensitive data encoding scheme is LEDR that encodes two wires, or "rails", to encode one bit of data. Here no spacer is required. Each data value has two types of code words with different phases. Here sender sends data values alternately in phase 0 and phase 1. As no spacer is required, the number of signal transitions is half as compared to four-phase dual-rail encoding. So it results in high throughout and low power consumption.



		Code word (V, R)
Phase 0	Data 0	(0,0)
	Data 1	(1,1)
Phase 1	Data 0	(0,1)
	Data 1	(1,0)

Figure 10. LEDR encoding

we have implemented LEDR encoding to make the Viterbi decoder Asynchronous for futher reduction of dynamic power In designing of Asynchronous Viterbi decoder the system clock called global clock which is of 5 Mhz is divided into two local clocks which is of 2.5 Mhz .Both the local signals works on handshaking between all units of viterbi decoder and maintain synchronization to decode the sequence even if error bit occurs. At last the complete design is simulated and power analysis is done on Quartus Power play power analyzer and it observed that the dynamic power is less in Asynchronous system as compared to Synchronous Viterbi decoder

VI Proposed Architecture of Asynchronous Viterbi Decoder

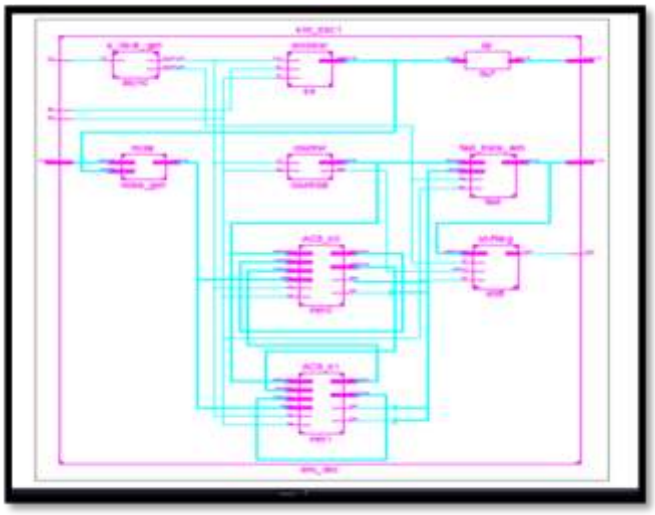


Figure 11. RTL View of Asynchronous Viterbi Decoder

As shown in figure 11 a controller named e_clock_gen has been designed which generates two local signals of 2.5 MHz.

VII.SIMULATION RESULTS:

The Asynchronous Viterbi Decoder is designed and simulated using decoding method MTHREM and handshaking protocol as LEDR encoding. As shown in figure 12, input 12 bit sequence 011010111100 has been applied to asynchronous Viterbi decoder and after 13th clock cycles we received the decoded data serially at Sout pin. As shown in figure 13, 14 and 15, we introduced a one bit, two bit and two consecutive bit error in the above 12 bit input sequence and applied to Asynchronous Viterbi decoder and still we received the exact sequence whatever transmitted at

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Sout pin of decoder. As the error correcting capability of decoder is 2 therefore simulation results of Figure 13, 14 and 15 shows that the two bit error at transmitter side has been corrected at receiver i,e the correct data is received at Sout pin of decoder.

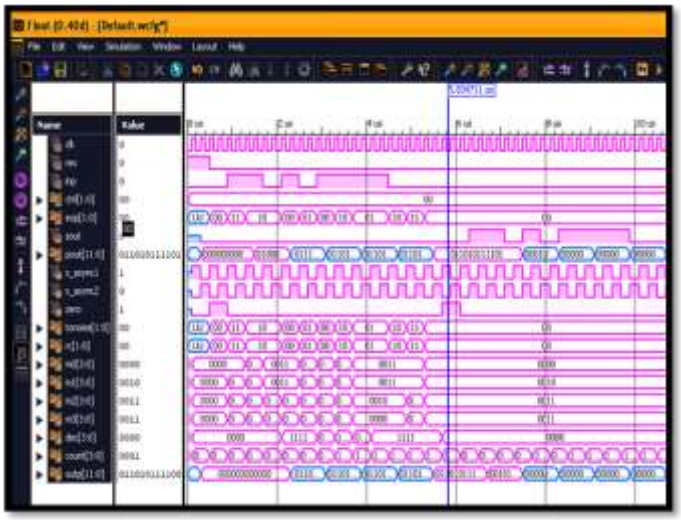

Figure 12 Asynchronous Viterbi decoder using MTHREM

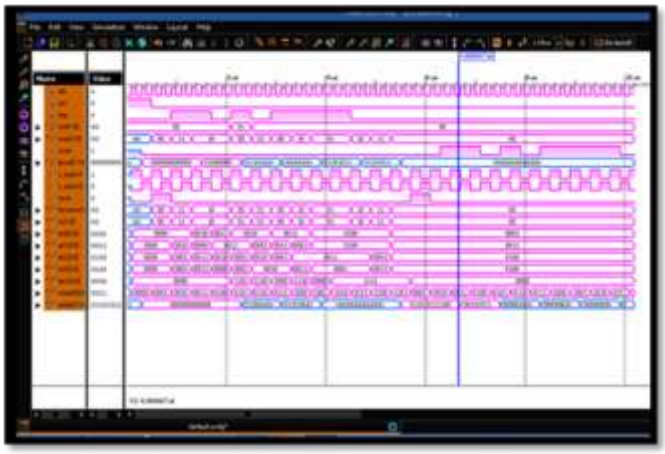

Figure13: Simulation of one bit error, ctrl<= "00","01" after 2100ns,"00" after 2500ns;

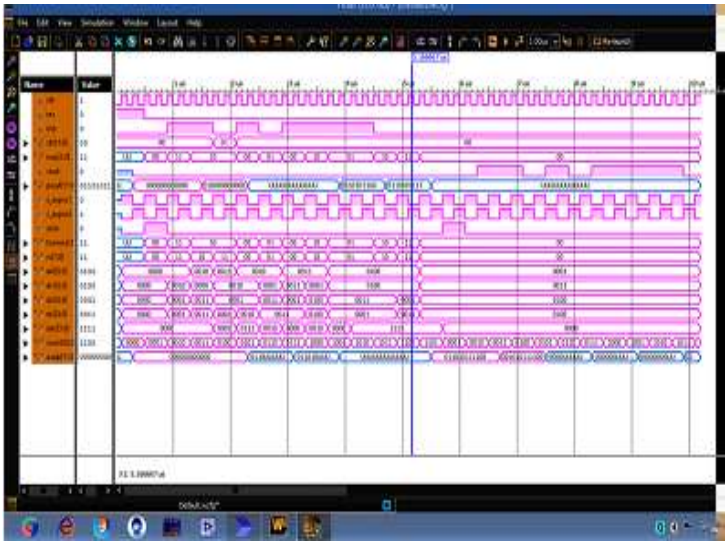

Figure14: Simulation of two bit error, ctrl<= "00","01" after 1700ns,"00" after 2100ns;

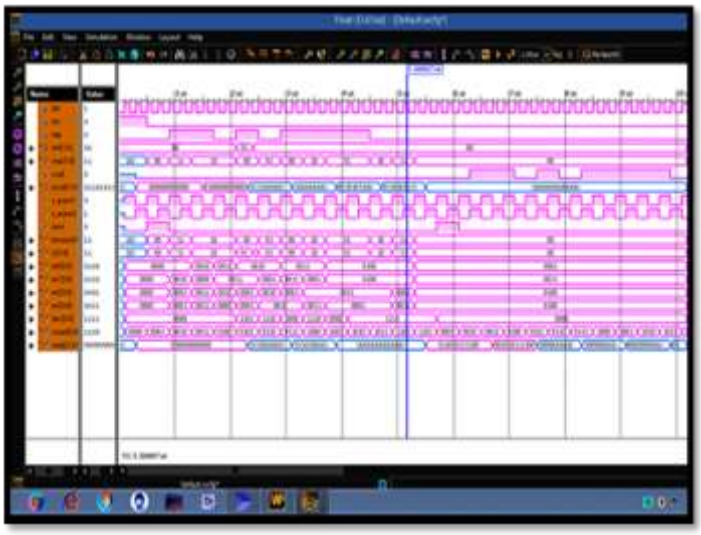

Figure 15: Simulation of two consecutive bit error, ctrl<= "00","01" after 2100ns,"00" after 2400ns,"00" after 2900ns;

CONCLUSION

In this paper we have designed Low power Asynchronous Viterbi decoder using Level Encoded Dual Rail encoding for Minimum Hybrid Register Exchange methods for constraint length K=3 and code rate 1/2.The design of Asynchronous viterbi decoder for 12 bit input sequence 011010111100 has been simulated for one bit ,two bit and two consecutive error bits and it has been proved that even if two bit error has introduced while transmission of data the decoder removed the error and provides the exact sequence at the receiver.

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