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A 3.4 Gbps 2^7-1 Pseudo Random Bit Sequence generator for Serial-Data Communications in 0.18µm CMOS

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***Abstract*—**This paper presents a 3.4 Gbps Pseudo Random Bit Sequence (PRBS) generator with sequence length of 2^7-1. The circuit uses 7- Bit shift register with a linear current mode XOR gate and current mode D flip-flop and works up to data rates of 3.4 Gbps. The simulated data jitter of the 3.4 Gbps output is 2.75ps with full swing output voltage of 1.8V and the binary-sequence repeats itself after 127 cycles PRBS generator implemented in Cadence 0.18µm CMOS technology.

Keywords- *Flip-Flop, CML, LFSR, PRBS.*

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I. INTRODUCTION

Pseudo Random Binary Sequence (PRBS) generators are needed as test signals for a high-speed serial link systems such as High-Definition Multimedia Interface (HDMI) ,DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays.HDMI carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats.HDMI is a digital replacement for existing analog video standards.At its heart, HDMI is a high-speed, serial, digital signalling system that is designed to transport extremely large amounts of digital data over a long cable length with very high accuracy and reliability[1].To avoid using expensive high-speed test equipment , on-chip PRBS generators have been developed to provide a cost effective way to serial-data transmitter.The jitter performance of the serial-data transmitter can be measured through the received eye diagrams produced by the PRBS generator.

In this paper , we present a 3.4 Gbps PRBS gererator implemented in 0.18µm CMOS technology.The implemented PRBS gererator is designed for testing the digital data circuits up to 3.4 Gbps.

II. PRBS GENERATOR

A. Requirement for PRBS Generator

In order to test the designed transmitter circuit, a differential data signals at the rate of 3.4 Gb/s is required. In order to generate this test input signal, we require a Pseudo Random Binary Sequence (PRBS) generator. The PRBS generator should produce an almost-random differential binary sequence at the required operating frequency of 3.4 GHz. The output of the PRBS generator is to be fed to the input terminals of the transmitter; a 7-bit PRBS Generator was designed as described in the following section.

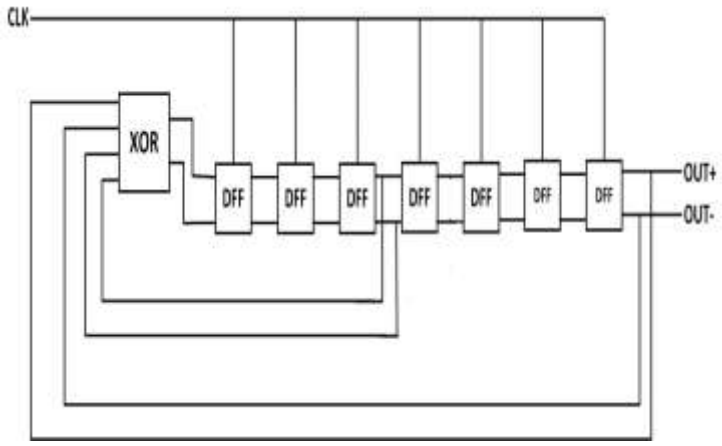

Fig 1. LFSR for Polynomial P(x) = X^7+X^3+1

B. Design and development of PRBS generator

The PRBS generator is realized by means of a Linear Feedback Shift Register (LFSR). Since we require a differential output bit stream, the LFSR should also be differential in nature. Thus, current-mode XOR gate and current-mode D Flip-flops were used for building the PRBS Generator. The block diagram of the 7-bit differential PRBS Generator is shown in fig 1. The seven D-Flip flops are connected serially to form a shift register. The output of the seventh flop-flop and third flip-flop are feedback as inputs to the current-mode XOR-gate. The output of the XOR gate is fed as input to the first flip-flop. A clock signal at 3.4GHz is given to all the flip-flops. The PRBS then generates a random bit-stream at the same frequency**.** A conventional current-mode XOR gate is implemented as shown in fig 2.

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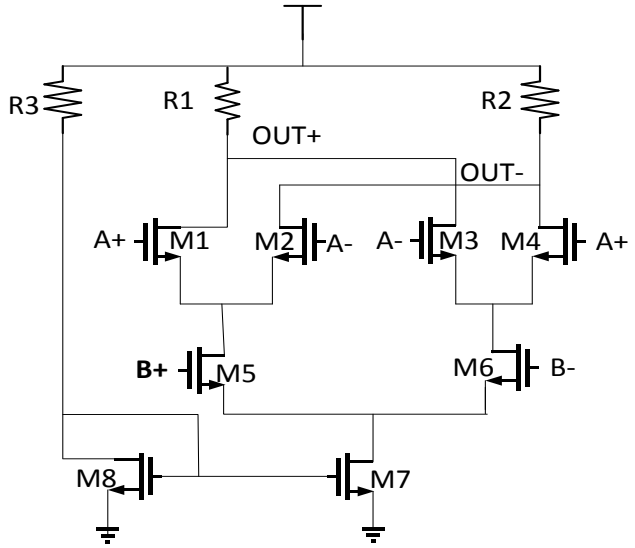

Fig 2 .Current-mode XOR gate

The PRBS Generator is realized by means of a Linear Feedback Shift Register (LFSR). Sense Amplifier based Flip-flops and Current-mode XOR gate were used for building the PRBS Generator.

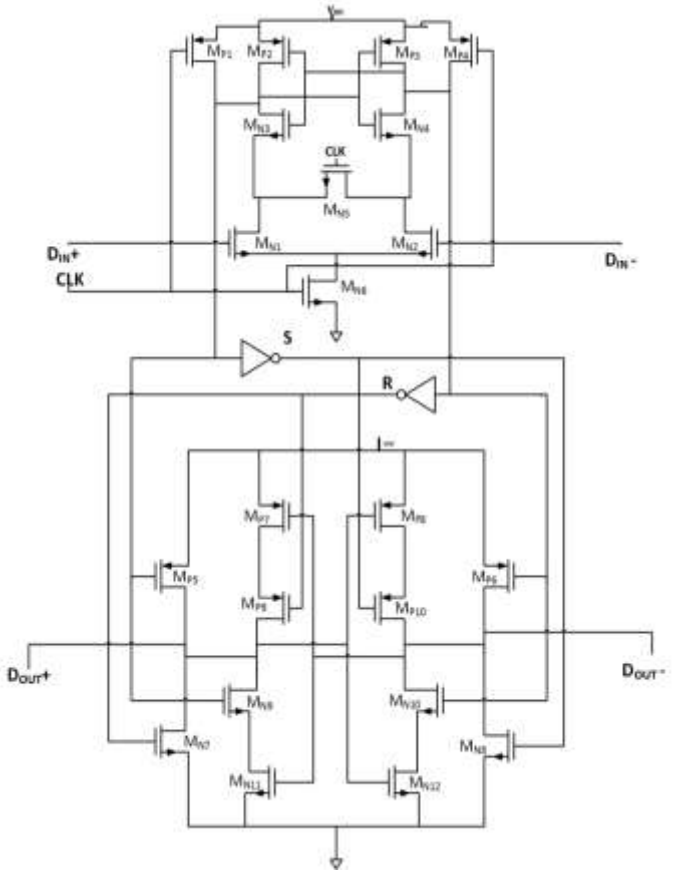

Fig 3 .Sense amplifier based flip-flop [2]

The sense amplifier based flip-flop uses a output stage latch topology shown in fig 3 that significantly reduces delay and improves driving capability [2]. Every flip flops were optimized for minimum delay and reduced output transistor sizes. The seven Flip flops are connected serially to form a shift register. The tap is formed with the Current-mode XOR gate. A clock signal at 3.4GHz generated from PLL is driving all the flip-flops. The PRBS then generates a random bit-stream of length at the same frequency.

III. SIMULATION RESULTS

The single ended output waveform of the PRBS Generator is shown in fig 4. The binary-sequence repeats itself after 127 cycles. The V_{high} and V_{low} for the single-ended outputs are 1.8V and 0V respectively. The eye diagram of the PRBS Generator is shown in fig 5 which operates at 3.4GB/s the measured jitter of PRBS generator is 2.75ps.Table I shows the performance summary of the designed PRBS Generator.

Table I. Performance summary of the designed PRBS Generator.

Parameter	Value
Frequency	3.4 GB/s
Output Voltage Swing	1.8V
Jitter (ps)	2.75
Length of random sequence	127
D-Flip-flop Power(µW)	6.28
PRBS generator Power(mW)	21.21

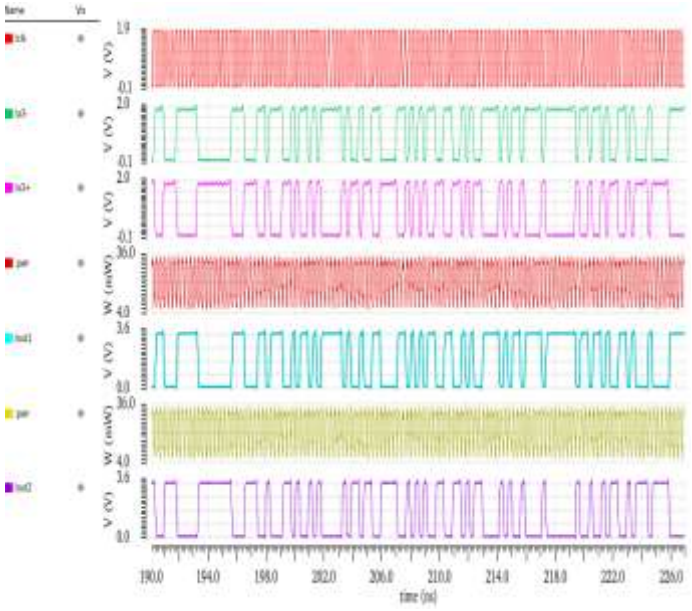

Fig 4.Single ended output waveforms of the PRBS Generator.

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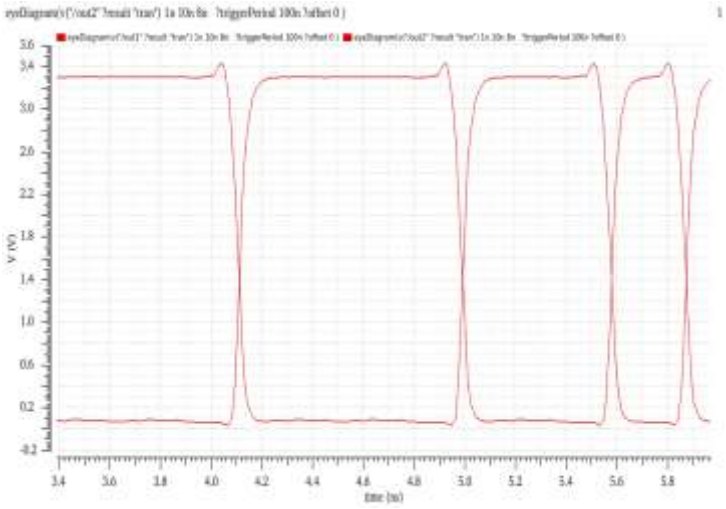

Fig 5.Eye diagram of the PRBS Generator.

IV. CONCLUSION

The test data was generated by means of a 7-bit PRBS generator which is used a 3.4 GHz clock signal provided by a Phase Locked Loop and sense amplifier based flip-flop. The PRBS generator is simulated with 1.8 V, 0.18µm CMOS process which takes into account the device parasitic and second order effects.

References

[1] The High Definition Multimedia Interface Specification version 1.4a, http://www.hdmi.org.

[2] Nikolic, B., Oklobdzija, V. G., Stojanovic, V., Jia, W., Chiu, J. K. S., & Leung, M. M. T. (2000). Improved sense-amplifier-based flip-flop: Design and measurements. *IEEE Journal of Solid-State Circuits*, *35*(6), 876-884.