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Low-voltage Low-power Bulk-driven CMOS Op-Amp Using Negative Miller Compensation for ECG

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Highlights:

- Two operational amplifier topologies and two compensation strategies were compared in this study ECG as the application of focus.
- The bulk-driven MOS transistor technique was used to provide a low supply voltage and avoid voltage threshold effects.
- The first operational amplifier design was a typical two-stage amplification design with standard Miller compensation, while the second design was a two-stage amplification design with two integrated compensation approaches (standard Miller and negative Miller compensation).
- To improve the unity gain frequency and phase margin of the second -amp while keeping power consumption constant, negative Miller compensation was applied by connecting a capacitor between the input and output nodes of the bulk-driven first stage as well as standard Miller compensation in the second stage.

Abstract: Two bulk-driven CMOS (Complementary Metal Oxide Semiconductor) operational amplifier (op-amp) designs for electrocardiogram (ECG) application are presented and compared in this paper. Both op-amps are based on two-stage amplification, where bulk-driven differential input is the first stage, while additional DC gain is the second stage. Different compensation techniques were integrated in each op-amp design. Standard Miller compensation was used for the first op-amp parallel with the second stage. The novelty of the second op-amp is that it utilizes negative Miller compensation between the bulk-driven input node and the output node of the first stag, while standard Miller compensation was used in the second stage. The purpose of this work was to compare DC gain, phase margin (PM) and unit gain frequency (UGF) obtained through different simulated compensation strategies and test results. The op-amps were simulated using 0.25 μm CMOS technology. The simulation results are presented using the standard model libraries from Tanner EDA tools, operating on a single rail +0.8V power supply.

Keywords: *bulk-driven; ECG; low power; Miller compensation; negative Miller compensation; op-amp; unity gain frequency.*

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1 Introduction

An electrocardiogram (ECG) is a classic test to detect cardiac problems. The ECG technique is completely non-invasive, painless, and provides doctors and patient with immediate results. Nowadays, ECG is a technology that must be smaller and more portable, easier to use, affordable to create, and have a long battery life [1]. The basic diagram of an ECG is shown in Figure 1, where sensors E1 and E2 detect the electrical pulse of the heart, which is used to determine the ECG signal from the human body. In Figure 1, the control circuit of the ECG design contains two parts: firstly, the analog front-end ECG component (an integrated circuitop-amp) that is used to amplify the ECG signal; secondly, an analog to digital converter (ADC) for digitizing the analog ECG signal and a digital to analog converter (DAC) for the display system for tracking the heart rate of the patient. Other elements that help connect the ECG signal are based on using either electronic programmable device such as a microcontroller (μC) [2], an Arduino [3], a digital signal processor (DSP) [4, and a field-programmable gate array (FPGA) [5].

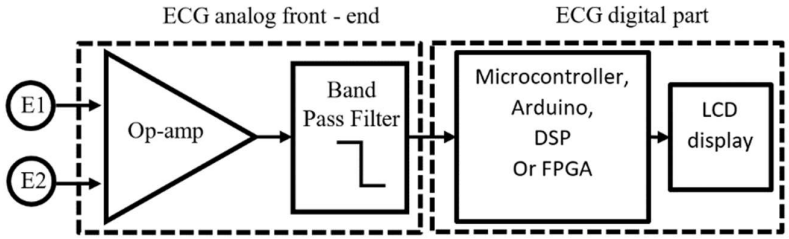

Figure 1 Traditional ECG sensor design.

One of these electronic parts is the operational amplifier (op-amp. The greatest challenge in designing the op-amp is dealing with a situation where power and voltage diminish, prompting a decrease in the performance of the amplifier. For example, reduced power consumption leading to a decreased frequency response performance (such as unity gain frequency (UGF) or slew rate (SR)) at high speed [6, because UGF and SR are current dependent [7].

The simple analog front-end consists primarily of an instrumentation amplifier and band pass filter circuits. These circuits have an op-amp design that is considered a basic incorporated circuit in their design, while the band pass filter can be operated by utilizing one of the op-amp's circuits or a digital filter can be used. The op-amp is usually based on Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology (see Figure 2(a)). There are several different strategies and methods for designing an op-amp [8,9]. These strategies are based

on the performance and attributes required for signal amplification in an electronic integrated circuit.

A large portion of these designs utilize the gate terminal as input node, as can be seen in Figure 2 (b). It requires a high voltage to achieve the required performance, which prompts an increase in power consumption, thus reducing the battery life. Thus, the bulk terminal is used as input signal for the MOSFET circuit (see Figure 2(c)). One of the attributes of this technique is that it produces a current regardless of whether the voltage of the gate source (V_{GS}) is greater than the voltage threshold (V_{Th}) or not, as it does not rely on the limit voltage.

Power supply reduction may reduce the input voltage range and, even worse, its linearity [10] and the frequency response. This can be overcome by applying a bulk-driven technique, however, the frequency response will still remain challenging. The drawbacks and benefits of bulk-driven MOSFETs are both clear. The V_{Th} requirement in the signal path is avoided by bulk-driven MOSFET supporting features, hence increasing voltage swings under decreased voltage-power operation. However, bulk-driven MOSFETs have disadvantages such as transconductance of the body (bulk) (gmb) around five times smaller than the transconductance of the gate (gm). This makes it possible to reduce the unit gain frequency (UGF) value when UGF affects the frequency response performance. In addition, this structure also has large parasitic capacitance and high input noise [1112], which also contributes to reduction of UGF and PM.

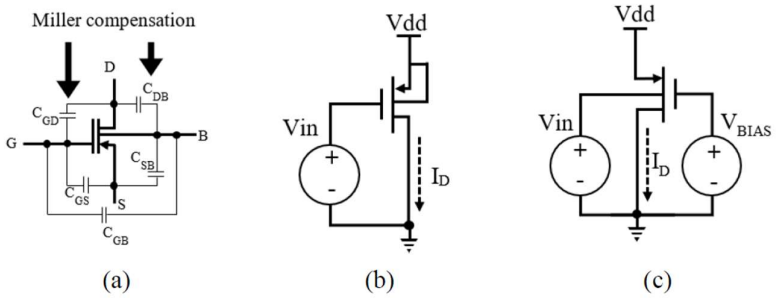

Figure 2 (a) Structure of the MOSFET, (b) simple gate-driven PMOS, (c) conventional bulk-driven PMOS.

Miller compensation or Miller capacitance is a technique used in many op-amp designs to improve the stability (phase margin PM) in a closed loop configuration. However, it causes reduction of the frequency response, so the input node and the output node are connected with a normal capacitor (Cc) [11, 13, 14], creating Miller compensation. Another compensation technique is negative Miller compensation, which is utilized to improve UGF by reducing or

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removing parasitic capacitance at the input nodes. At high frequencies, particularly for transistor capacity, their impact is noticeable since unwanted phase changes may occur that are not observed at lower frequencies.

The aim of the present work was to improve the frequency response (UGF) and margin stability (PM) for low-voltage low-power bulk-driven CMOS op-amps by applying and combining two compensation techniques. Figure 3 presents a diagram of the proposed work. Two stages were designed, where the first stage is a bulk-driven differential input stage and the second stage provides additional open loop gain (DC gain). Standard Miller capacitance is connected in the second stage (see Figure 3) to provide stabilization (PM). Negative Miller capacitance is connected in the differential input stage to increase UGF. The obtainable op-amp was simulated in 0.25µm CMOS technology; the results are shown using the standard model libraries from Tanner EDA tools. The power supply operation was reduced to +0.8 V.

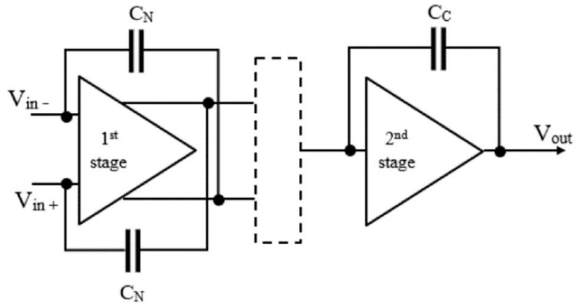

Figure 3 Op-amp diagram of the two-stage Miller compensation (standard (C_c) Miller and negative Miller (C_N) compensation).

The rest of this paper is organized as follows. In Section 2, on the basis of bulk CMOS technology, the traditional two-stage amplification technique is presented, including organizational theory, key benefits and technological consequences. Section 3 shows the compensation techniques established with the standard Miller and negative Miller compensation designs. Section 4 presents the simulation and its results, including their evaluation. Lastly, Section 5 concludes the paper.

2 Standard Bulk-Driven Folded Cascode Technique

Bulk-driven CMOS blends low-voltage and low-power ICs and tends to be a beneficial strategy. Compatibility with the traditional CMOS process [15,16] is the primary benefit of this technology. The configuration of the typical MOS

transistor is not modified. In the equivalent, the need to solve the MOS transistor input $V_{GS} > V_{Th}$ voltages is suppressed, improving the voltage headroom. MOS transistors are used as signal input for the bulk node, while the gates are fitted with V_{BIAS} voltage. To explain further, the theory of the technique is the configuration of the MOS transistor itself. There are four nodes in total: gate, drain, source, and bulk. As described in Figure 2, the system uses the bulk as the signal input (V_{in}), which ensures that the MOS transistor input threshold voltage is surpassed [17], where a bulk-to-source junction may function under condition of negative, zero, or positive bias [18]. This will contribute to a larger input common mode voltage range, in addition to voltage swing, which otherwise cannot be accomplished with low voltage supply.

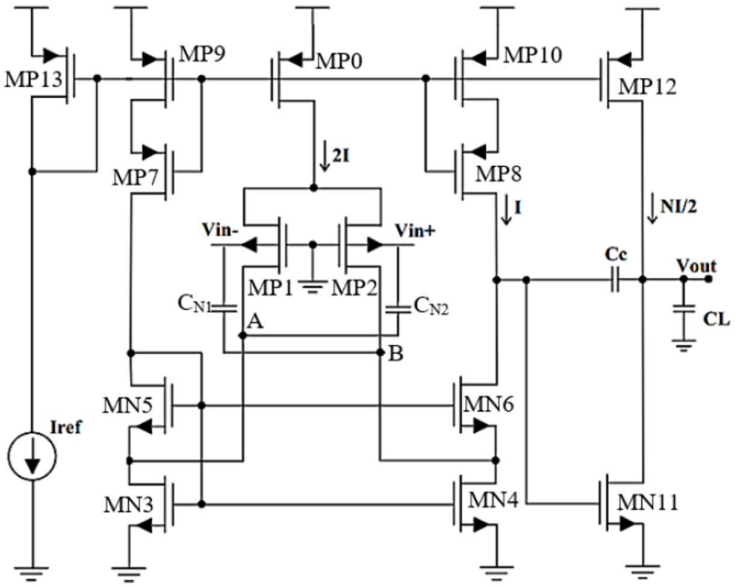

Figure 4 Diagram of the suggested standard two-stage bulk-driven folded cascode op-amp with negative Miller compensation (C_N).

The standard two-stage Bulk-Driven-Folded Cascode (BD-FC) op-amp was first proposed in Ref. [10]. Figure 4 shows the proposed circuit architecture for this work. The first stage consists of transistors MN1 and MN2 and the second stage is presented by MN11 and MP12. The input signals are also shown. Since transistors MN3 and MN4 are typically used as biased current sources at the initial stage of the Folded Cascode Operational Transconductance Amplifier (FC-OTA), the effective g_m can be better exploited. Furthermore, the transistors MN3 and MN4 (MP1 and MP2) can be used as the driving transistors [19]. The

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transistors MN3 and MN4 are also fitted with the highest DC current for the largest g_m. The input signal for these transistors will then be used to further improve the transconductance [20]. If the transistor current (MP0) is 2I, the input transistor current (MP1 and MP2) is I. The transistors of the tail current need high input resistance, low noise, and low offset. It also has an effect on the UGF to reach a certain g_m as well as g_{mb}. The control g_{mb} of the input stages is due to the tail current.

3 Compensation and Stability Techniques

The open-loop design can then have a phase margin of 45° or greater, which can be accomplished by the use of a compensation technique. Different compensation techniques, such as standard Miller and negative Miller compensation, may be utilized to provide the required frequency response and stability. These compensation strategies may be used alone or in combination.

3.1 Standard Miller Compensation

The compensation [21] (or Miller) effect is based on the following principle: the gain (A) of the inverting amplifier is defined as negative and the feedback capacity is set between the output and the input, as shown in Figure 5 (a). Input capacitance node ($C_{1(Miller)}$) and output capacitance node ($C_{2(Miller)}$) with regard to ground are shown as the Miller effect, as shown in Figure 5(b). Input and output are influenced by the capacitance. The capacitance effect of the input is ($C_{1(Miller)}$) = C_C (1+|A|). The output capacitance effect is closer to C_C [14] and is provided by ($C_{2(Miller)}$) = C_C (1+1/|A|).

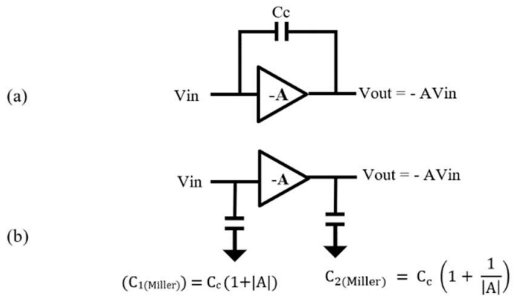

Figure 5 (a) Inverting amplifier with regular capacitor, (b) standard Miller theory equivalent circuit.

According to the bulk-driven op-amp structure in Figure 4, the output node (drains of MP12 and MN11) of the second stage is connected to a Miller capacitator (Cc) and the output node of the first stage (drains of MP8 and MN6). In other words, the Miller compensation capacitor (Cc) is connected in parallel

with the second stage [14], resulting in a two-stage bulk-driven CMOS op-amp, which is commonly known to have two poles [22,23]. The Miller compensation technology moves the first low-frequency pole (p1) to the origin (to the lower frequency), which makes the pole more dominant. In addition, the second high-frequency pole (p2), which is separated from the origin (to the higher frequency), becomes less dominant, creating a bandwidth far greater than that reached by connecting one node to the ground through the compensation capacitor [24]. This is aimed at attaining a suitable PM by forcing the system transfer function to behave identical to a single-pole system. The signal from the output to the input is then compensated by a feedback capacitance. However, this results in a positive zero [25] in the RHP (right hand plane) and slows down the speed of operation (UGF).

3.2 Negative Miller Compensation

The ability to have negative Miller compensation is based on the Miller effect. A noninverting amplifier as identified in [26] can be used to achieve negative Miller compensation. The influence of negative Miller compensation can be seen in Figure 6, in which A is the amplifier gain. The Miller effect causes a negative capacitance value at the amplification stage's input node, with a gain greater than 1 (unit) (see Figure 6(b)). The input capacitance of the amplifier is given by:

$$C_{in} = C_{bs} + C_{bsub} + C_{bd} \quad (1)$$

In addition, the equivalent input capacitance of negative Miller compensation (Eq. (2)), when the gain is greater than 1, the equivalent input capacitance ($C_{1(NM)}$) is a negative value, which is called the negative capacitance:

$$C_{1(NM)} = C_N (1 - A) \quad (2)$$

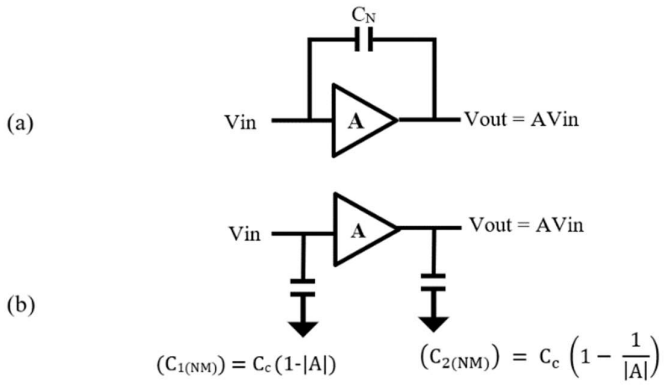

Figure 6 (a) Non-inverting amplifier with regular capacitor, (b) corresponding circuit of negative Miller compensation.

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The parasitic capacitance of a bulk-driven-NMOS is presented in Figure 1(a) with the purpose of promoting the knowledge of the small signal model of the bulk-driven NMOS common source and the impact of parasitic capacitance on the parameters of the bulk-driven NMOS, as mentioned in Ref. [27]. Figure 7 shows the small signal equivalent circuit of the common source amplifier dependent bulk-driven NMOS at high frequencies. The UGF of the bulk input stage is therefore provided by:

$$\mathrm{UGF_b} = \frac{1}{2\pi}\frac{\mathrm{g_{mb}}}{\mathrm{C_{bs}} + \mathrm{C_{bsub}} + \mathrm{C_{bd}}} \tag{3}$$

where, C_{bs}, C_{bsub} and C_{bd} are the bulk-source, bulk-substrate and bulk-drain parasitic capacitances, respectively. The parasitic capacitances are caused by the transistor well and substrate structure. In Figure 7, the C_{bd} capacitance provides feedback between the bulk (input node) and the drain (output node) [14].

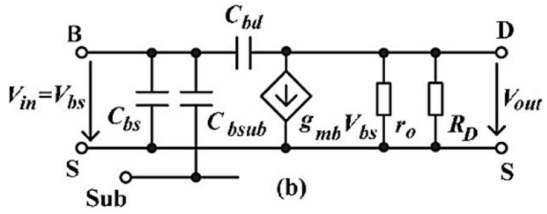

Figure 7 Bulk-driven input DC small-signal equivalent circuit [27].

However, C_{bd} provides the Miller effect, decreasing the operating speed (UGF), while C_{bd} boosts the input capacitance and reduces the capacitance of the output counterpart. The Miller effect (transistor at input node) must be canceled or at least minimized in order to increase UGF at a high frequency. By using Eqs. (2) and (3), the value of the input capacitance (C_{bs}+ C_{bsub}+ C_{bd}) will be reduced by adding negative capacitance (-$C_{1(NM}$ and UGF is given:

$$\mathrm{UGF_b} = \frac{1}{2\pi}\frac{\mathrm{g_{mb}}}{(\mathrm{C_{bs}} + \mathrm{C_{bsub}} + \mathrm{C_{bd}}) + (-C_{1(NM)})} \tag{4}$$

4 Simulation and Results

Figure 4 shows the first op-amp, which is a bulk-driven op-amp that only employs standard Miller compensation, and the second op-amp, which is a bulk-driven op-amp that uses both standard Miller and negative capacitance. Adding a capacitor to the input transistor stage is necessary to generate negative Miller capacitance. C_{N1} is attached between the input transistor level (the inverting node (V_{IN-})) and the output node of the first stage (node (B)), while C_{N2} is attached between the non-inverting node (V_{IN-}) and the input transistor stage output node (node (A)).

The op-amp architecture was developed using CMOS technologies using the standard model libraries from Tanner EDA tools at 0.25 µm and was simulated using corner analysis (typical-typical (TT), fast-fast (FF), slow-slow (SS), slow-fast (SF) and fast-slow (FS)). For this production process, the voltage supply (V_{dd}) operation is usually +2.5 V, but the supply voltage in this process was reduced to +0.8 V. Table 1 lists the transistor sizes as well as the other components used in the simulation of the bulk-driven op-amp. Table 2 shows the frequency response of the op-amp using only Miller compensation (i.e., no negative Miller capacitors incorporated).

Table 1 Transistors and other elements of the bulk-driven op-amp.

Transistor	Type	Width/length
MP0 (µm/ µm)	PMOS	16.10/2.5
MP1, MP2(µm/ µm)	PMOS	20.6/ 3.25
MN3, MN4 (µm/ µm)	NMOS	20.2/5
MN5, MN6 (µm/ µm)	NMOS	1.25/1.5
MP7, MP8 (µm/ µm)	PMOS	15/5
MP9, MP10 (µm/ µm)	PMOS	35/0.25
MN11 (µm/ µm)	NMOS	1.5/2.5
MP12 (µm/ µm)	PMOS	6.75/2.5
MP13 (µm/ µm)	PMOS	5/2.5
Cc (fF)		200
CN (fF)		600
Iref (nA)		140

Table 2 Different Miller capacitor values for the configuration of the first op-amp design.

Cc (fF)	DC gain (dB)	UGF (kHz)	PM (degree)	Power consumption (µW)
0	63.13	2954.2	-15.32	0.996
200	63.13	184.43	75.81	0.996
400	63.13	93.88	80.92	0.996
600	63.13	62.58	82.77	0.996
800	63.13	47.21	83.66	0.996
1000	63.13	37.79	84.23	0.996

Capacitor C_c varied from 0 pF (no compensation) to 1 pF and it was found that PM increased with increased Miller compensation (increasing the value of Cc), however, UGF decreased. DC gain and power consumption held the same values with Cc changing. The gain frequency and PM for various Miller capacitance values are shown in Figures 8 and 9 respectively.

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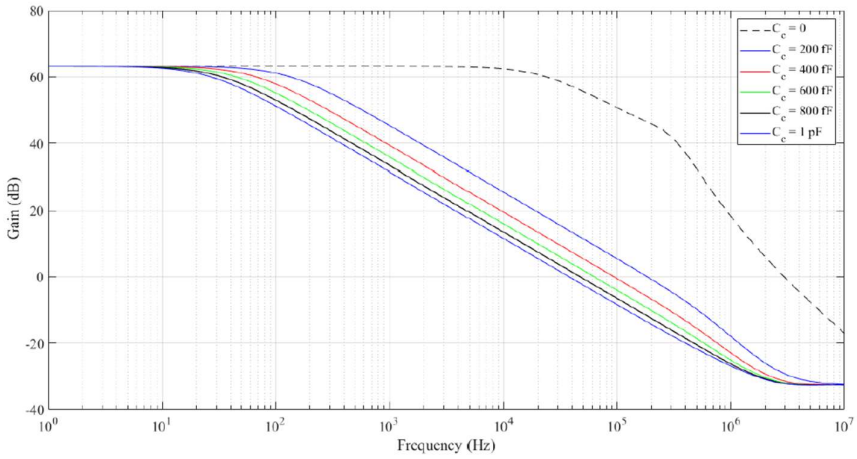

Figure 8 Frequency response diagram (open-loop op-amp gain magnitude) (no output load (V_{dd} = +0.8 V)) for the first op-amp.

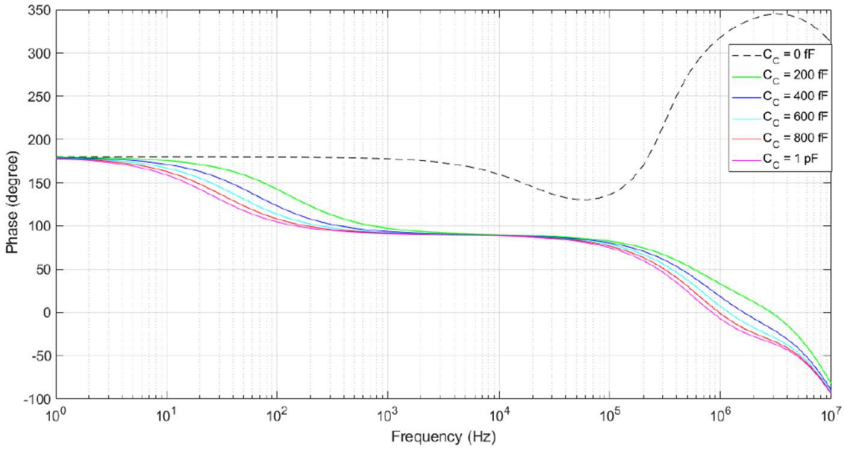

Figure 9 Frequency response diagram (open-loop op-amp phase) (no output load (V_{dd}= + 0.8 V)) for the first op-amp.

As the next step in this work, the various values of C_N with a fixed C_c value of 200 fF are shown in Table 3. As the value of C_N increased, UGF increased while PM also showed an increase. DC gain and power consumption kept very similar values with C_N changing. Figures 10 and 11 show the frequency and phase of gain for various capacitances of the negative Miller capacitator.

Table 3 The second op-amp design with different negative Miller capacitor values (fixed Miller capacitor value = 200 fF).

C_N (fF)	DC Gain (dB)	UGF (kHz)	PM (degree)	Power consumption (μW)
0	63.14	185.90	75.73	0.99
200	63.14	184.43	83.98	0.99
400	63.14	186.78	92.10	0.99
600	63.14	193.22	100.23	0.99
800	63.14	206.06	108.54	0.99
1p	63.13	230.21	117.27	0.99

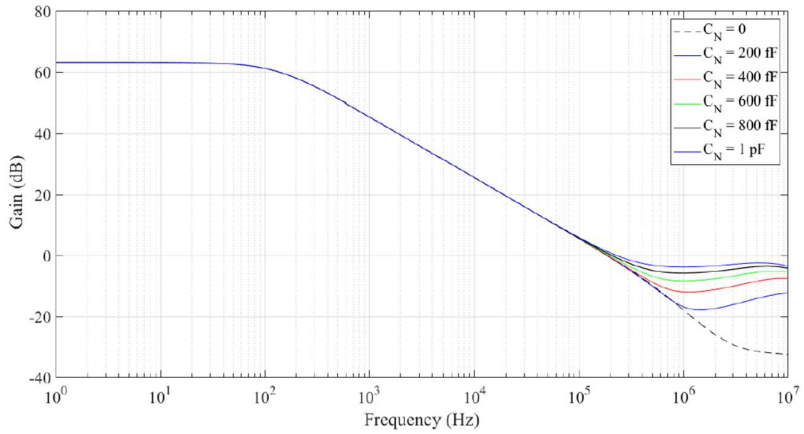

Figure 10 Frequency response diagram (open-loop op-amp gain magnitude) (no output load (V_{dd}= +0.8 V)) for the second op-amp design.

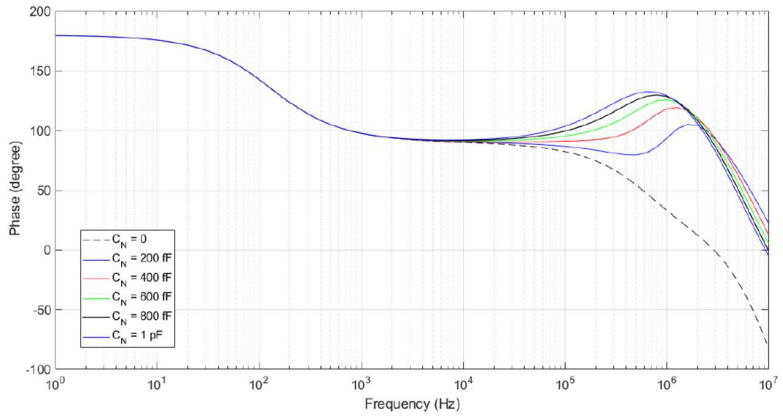

Figure 11 Frequency response diagram (open-loop op-amp phase) (no output load (V_{dd}= +0.8 V)) for the second op-amp design.

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A comparison of the first and second op-amp is shown in Table 4.

Table 4 Comparison of op-amp performance: first and second op-amp design (no output load (V_{dd} = +0.8 V)).

	First op-amp (Cc= 200 fF)	**Second op-amp (Cc= 200fF within C_N = 600fF)**
Power supply (V)	0.8	0.8
Technology (µm)	0.25	0.25
DC gain (dB)	63.14	63.14
UFG (kHz)	181.9	193.10
PM (degree)	75.73	100.1195
Power consumption (µW)	0.99	0.99
High output swing (V)	0.795	0.795
Low output swing (V)	0.018	0.018
CMRR (dB)	108.86	108.86

Additionally, the simulation results were evaluated without output load. Only UGF and PM were different, while all the other parameters stayed the same. Figures 12 and 13 show a comparison of the first and the second op-amp output for op-amp gain and phase, respectively.

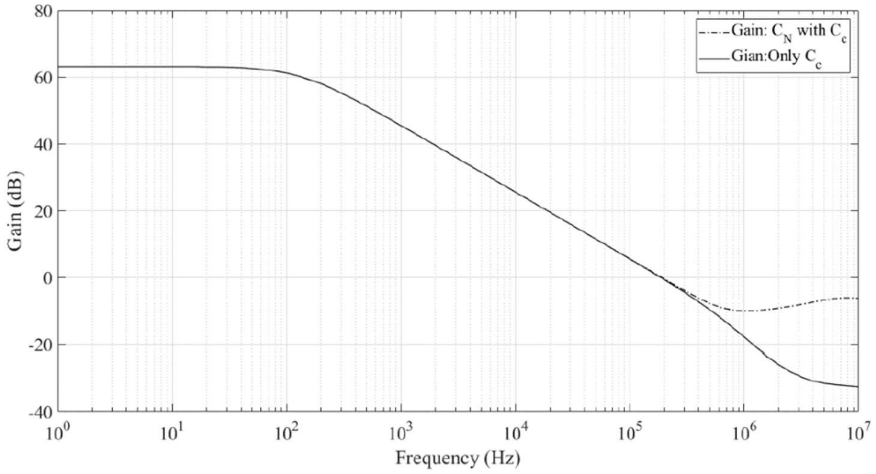

Figure 12 Comparison of op-amp gain performance: first and second op-amp design (no output load (V_{dd}= +0.8 V)).

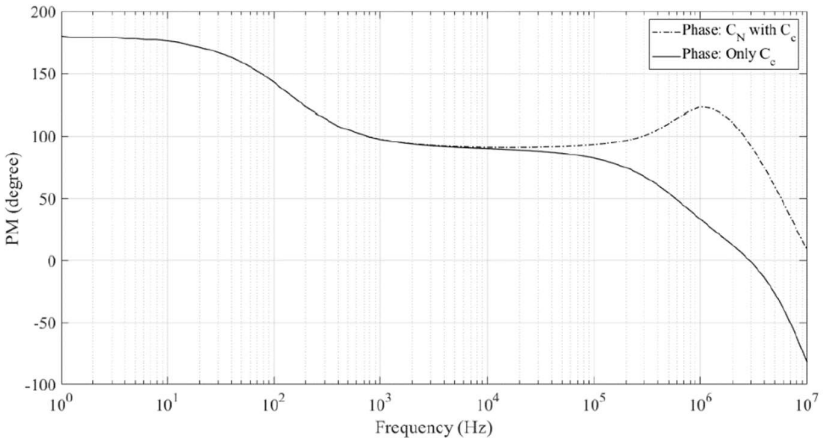

Figure 13 Comparison of op-amp phase performance: first and second op-amp design (no output load (V_{dd}= +0.8 V)).

The negative Miller capacitance difference with unit gain frequency for the second op-amp is presented in Figure 14; it varied from 0 pF (no negative Miller capacitor, etc.) to 1 pF. The UGF ranged from 185 kHz to around 230 kHz. The same difference was used with negative Miller capacitor to vary with the phase margin. The outcome of phase margin varied from 76° to around 117°, as can be seen in Figure 15.

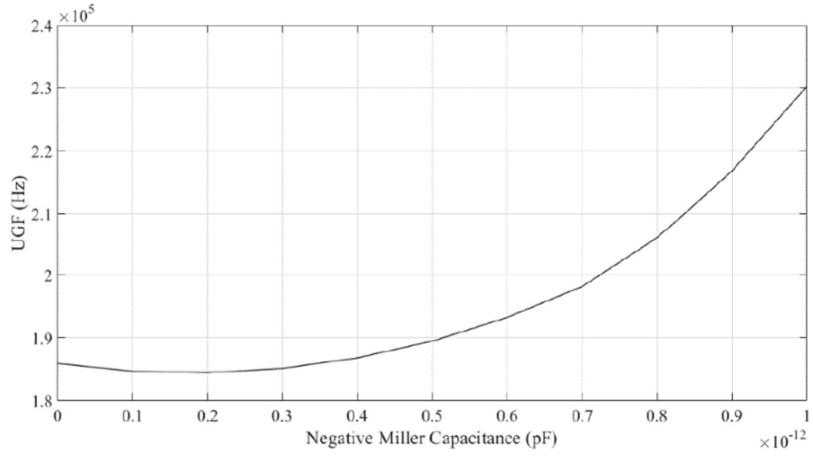

Figure 14 Negative Miller capacitance variation with unity gain frequency (second op-amp).

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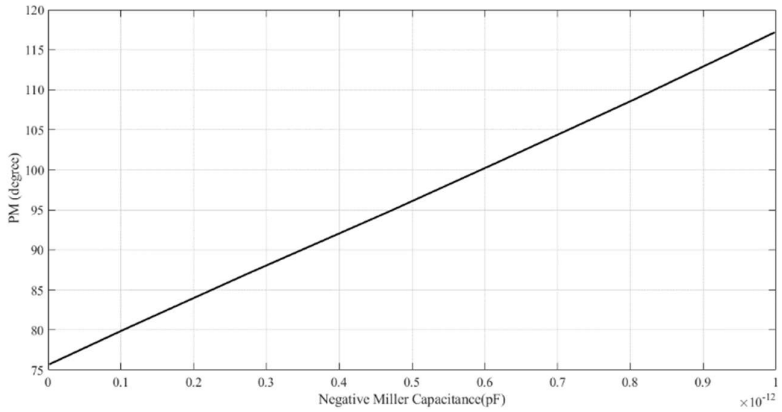

Figure 15 Negative Miller capacitance variation with phase margin (second op-amp).

The simulated output and input waveforms of the second op-amp are shown in Figure 16 as a voltage follower circuit, at 100 kHz and 0.1 mV input sinusoidal wave amplitude. This figure shows that an input/output swing for rail-to-rail is attainable. The simulation results for the corner analysis (SS, FF, SF and FS) variations are given in Table 5 to show the global process variations on key requirements of the aimed bulk-driven op-amp. Different load capacitors were applied, as presented in Table 5.

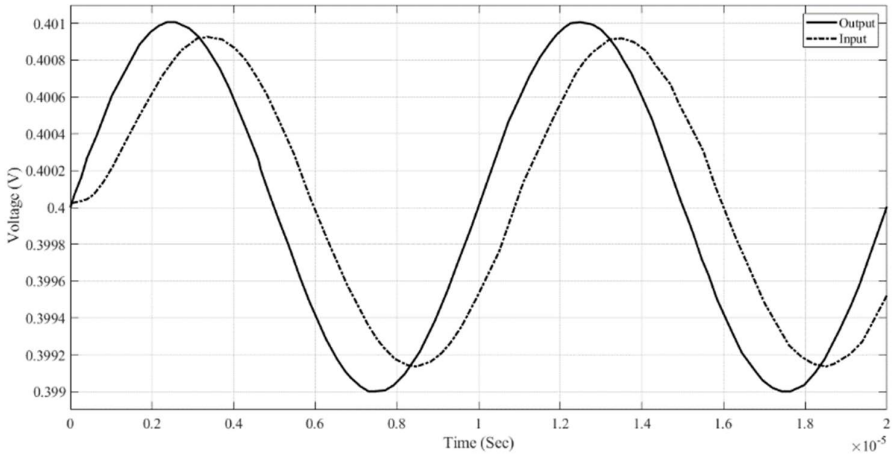

Figure 16 The input/output signals of the second op-amp with rail-to-rail input signal at 100 kHz and amplitude 0.1 mV.

Table 5 Review of corner analysis open-loop frequency response and power consumption for second op-amp (Cc = 200 fF, CN=600 fF, V_{dd} = +0.8 V).

Corner analysis					Load variations	
	SS	FF	SF	FS	C_L=1 pF	C_L=5 pF
DC gain (dB)	62.34	60.79	62.71	54.56	59.88	59.88
UFG (kHz)	173.68	225.03	207.69	188.86	406.01	300.16
PM (degree)	99.27	100.80	95.95	98.07	67.08	40.43
Power consumption (μW)	0.999	0.994	0.99	1	6.76	6.76

The performance of the simulated second op-amp was evaluated to six published op-amp designs functioning at varied power supply voltages and different technology processes, as shown in Table 6.

Table 6 Performance of bulk-driven op-amp with negative Miller compensation in comparison with other works.

	Proposed	[10]	[28]	[29]	[30]	[31]	[32]
Power supply (V)	0.8	0.6	0.8	0.9	±0.5	0.5	0.8
Technology (μm)	0.25	0.18	0.18	0.18	0.35	0.18	0.18
DC gain (dB)	63.14	82	56	58.4	59.1	52	68
UFG (kHz)	193.10	19.1	3200	5150	5900	2500	8100
Input bias current (nA)	730	-	-	<1	2.15		-
Output load (pF)	5	-	20	-	-	20	1
PM (degree)	100.2	60	45	71	63	45	89
CMRR (dB)	108.86	130.2	100	55.6	70.5	78	-
High output swing (V)	0.795	560	-	-	-	-	-
Low output swing (V)	0.018	40	-	-	-	-	-
Power consumption (μW)	0.99	0.4	100	261	197	110	94

Typical process parameters and no output load were used to get the simulated results. Using typical 0.25 μm CMOS technology, the design blends negative Miller and standard Miller compensation, showing an increase in frequency performance at a power supply voltage 0.8 V. Previous other op-amp designs [10, 28-32], which were intended for specific purposes, were also compared.

5 Conclusions

Two bulk-driven op-amp architectures were implemented and evaluated in the present paper. The op-amps were planned to apply the 0.25 μm CMOS process. Both op-amp schemes were operated at +0.8 V power supply voltage. Techniques of standard and negative Miller compensation were proposed. The first bulk-driven op-amp was compensated employing standard Miller compensation. The second bulk-driven op-amp was compensated using standard and negative Miller compensation. Simulation results were obtained using the standard model libraries from Tanner's EDA tools. The second op-amp model showed a

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considerable improvement in UGF and PM while keeping power consumption constant. Future research will look at design layout difficulties such as evaluating the design performance with layout-induced parasitic aspects (both resistance and capacitance). Before the concept can be produced and actual prototypes tested, further evaluation is required.

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