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Design of an Efficient Memristor-based Dynamic Exclusive-OR gate.

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***Abstract*— In this paper, an efficient memristor-based dynamic logic design for an Exclusive-OR gate is proposed. The proposed realization reduces the number of cascaded stages and component count thereby providing an overall performance improvement. The performance of the proposed design is compared with the most recent existing design through LTspice software simulations at 32 nm technology node in terms of total power consumption, average propagation delay, and number of components used in the implementation. The outcomes depict that the proposed design consumes 57 % reduced power and provides faster operation with 5.09 % improvement in propagation delay in comparison to its existing counterpart. Further, the robustness of the proposed design is verified by performing technology and capacitance variation. The results show the impeccable performance of proposed design across different load capacitance and technology nodes.**

Keywords*— *memristor, domino logic, dynamic logic, dynamic circuits, domino logic gates, Exclusive-OR.

I. INTRODUCTION

The dynamic CMOS circuits have become an integral part of modern portable electronics systems. The transition to dynamic CMOS based circuits occurred gradually as the static CMOS logic styles were volatile in nature. The dynamic CMOS based circuit design is a more reliable choice since the output node voltage is based on the transient storage of charge in parasitic capacitances. The dynamic logic circuit offers numerous benefits over the static logic design in terms of high speed and low area characteristics [1,2]. However, with the scaling of technology, a design space involving the use of new materials is being created that makes it necessary for thedesigner to adopt new technologies. At a device level, a Fourth fundamental circuit element named as Memristor has been extensively used in circuit design. It is a nano-scale two- terminal device that has the ability to execute both logic and memory operations. Hence, a Memristor-based circuit has its application in crossbar circuits, programmable analog ICs, and unbalanced ternary logic gates [3,4]. Thus, there is a paradigm shift in digital CMOS logic design. In this paper a novel form of hybrid model wherein memristors incorporated in a dynamic CMOS circuit are worked upon.

This paper introduces a recent efficient methodology to design a domino CMOS Exclusive-OR gate. An approach to design a memristor-based dynamic Exclusive-OR gate design is recently presented in [7]. The design achieves better performance than the existing CMOS based dynamic Exclusive-OR gate design. However, the multi-stage implementation results in increased power consumption and propagation delay, thus, making it an unattractive choice. This paper therefore presents an Exclusive-OR gate design with reduced number of stages thereby showing performance improvement with regard to component count, power and delay.

In the following section II, an outline of the previous works in comparison to dynamic CMOS logic and memristor is presented. The existing memristor-based dynamic Exclusive-OR gate design is discussed in section III. The proposed efficient memristor-based dynamic Exclusive-OR gate design is put forward in Section IV. Section V introduces the simulation results of the proposed design and its comparison with the existing design. The results for technology and capacitance variations are also included for completeness. In the end, section VI concludes the paper.

II. OUTLINE OF PREVIOUS WORK

The scope of the paper is to provide valuable insight into the use of memristor for designing dynamic CMOS logic styles. Thus, in this section, a brief review on domino CMOS logic gates and memristors is presented.

A. Domino CMOS logic

Domino CMOS logic gates are a class of CMOS circuit design, which rely on temporary storage of charge on parasitic capacitances. A Domino logic module is made up of an n-type Dynamic logic block and a static inverter. These gates work on the principle of pre-charge and evaluate logic depending on the input clock (CLK) signal value. The representation of a Domino buffer is indicated in Fig. 1.

The PMOS and NMOS transistors (MP1 and MN1) driven by CLK are responsible for executing the pre-charge and evaluate phase respectively. In the pre-charge phase, when CLK is LOW, MP1 conducts and pre-charge the dynamic node X1 to HIGH logic level, which in turn discharges the output of the CMOS inverter (MP2-MN3) VOUT to LOW value. In this situation, the pull-down network consisting of NMOS transistor MN2 has no effect on the node X1 as transistor MN1 is OFF. Alternatively, during the evaluation phase, the pre-charge transistor MP1 is OFF while evaluation transistor MN1 conducts. The input V_{IN}, thus, drives the node X1 to either HIGH or LOW logic levels during this phase.

By following the CMOS design principles, the circuit realization of 2-input OR gate, 2-input AND gate, and 2-input Exclusive-OR gate are drawn in Fig. 2-4. The domino OR gate shown in Fig. 2 comprises of a cascade of dynamic OR gate (MN1, MN2, MN3, MP1) and a CMOS inverter (MN2, MN4) with load capacitor C.

At the time of pre-charge phase, when the input CLK is LOW, MP1 turns ON and charges the dynamic node X1 to HIGH logic level. This turns the transistor MN4 ON and discharges output node VOUT to LOW voltage level. When CLK becomes HIGH during the evaluation phase, then MP1 turns OFF whereas MN3 conducts. The node X1 remains HIGH or discharges to LOW voltage level according to the input applied at nodes A and B. When both the inputs A and B are LOW then the dynamic node X1 stays HIGH and output node, VOUT, remains LOW. As the inputs A and B become HIGH, the dynamic node X1 discharges to LOW level whereas output node VOUT charges to HIGH voltage level. When either of the inputs A or B is HIGH, then node X1 is pulled down towards LOW logic level and VOUT becomes HIGH. Similar functionality can be derived for Domino AND (Fig. 3), and Exclusive-OR (Fig. 4) gates.

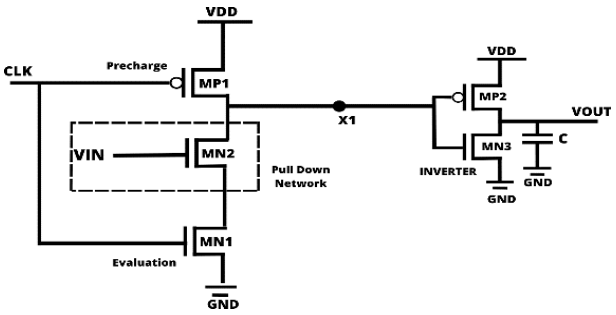

Fig. 1. CMOS Based Domino Buffer

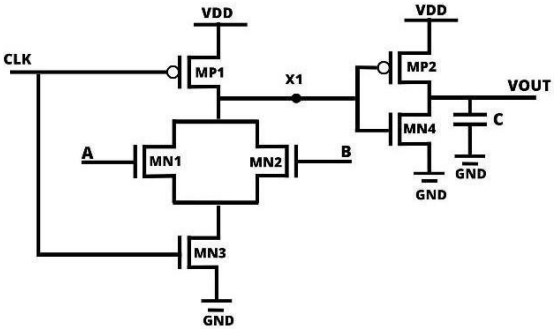

Fig. 2. CMOS based Domino OR gate

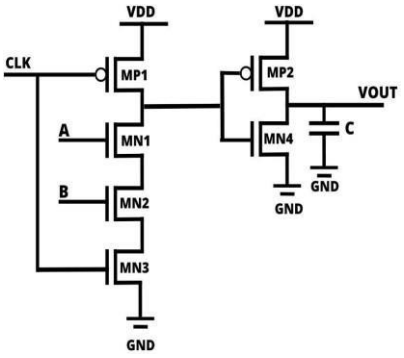

Fig. 3. CMOS based Domino AND gate

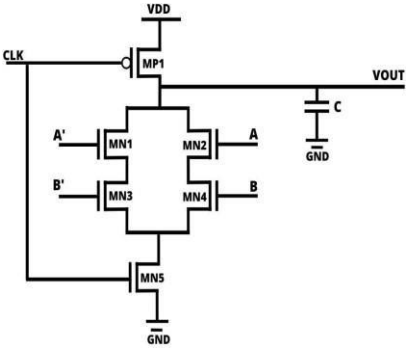

Fig. 4. CMOS based Domino Exclusive-OR gate

B. Memristors

Chua predicted the memristor as a two-terminal passive circuit device based on the mathematical symmetry of the L resistor R, capacitor C, and inductor L [3]. In 2008, Hewlett-Packard (HP) laboratories proved that a metal-insulator-metal (MIM) structure such as TiO2/TiO2-x sandwiched between two metallic nanowires such as Platinum (Pt) produces memristive behaviour [4–6]. The schematic symbol of memristor is shown in Fig. 5. It can be used to limit the flow of electrical current in a circuit. Since it also stores the amount of charge that has previously flowed through it therefore it is now being used as computational elements in circuit design.

The memristor can attain two distinct values of resistance i.e., R_{on} and R_{off} state. The R_{on} state is known as the low resistance (LR) state which is attained by the memristor while R_{off} implies the high resistance (HR) state of the memristor. When the current flows from terminal A to terminal B (from n to p), the width of the doped region increases while that of an un- doped region decreases, which reduces the resistance to R_{on} and results in LR state of the memristor. Alternatively, when the current flows from p terminal to n terminal, then due to reverse flow of current, the width of un-doped region increases and that of doped region decreases which increases the resistance of device to R_{off} and leads the memristor to its HR state.

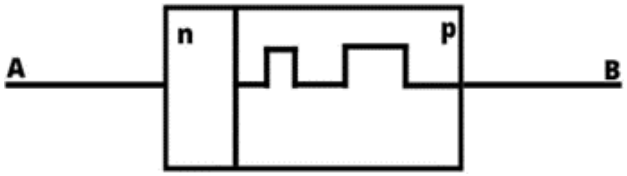

Fig. 5. Schematic symbol of memristor

III. EXISTING MEMRISTOR BASED DYNAMIC EXCLUSIVE OR GATE DESIGN

The existing memristor-based dynamic Exclusive-OR gate [7] with inputs: CLK, A, B and output: VOUT is shown in Fig. 6. It comprises of two stage domino gates and implements the Boolean expression shown in equation (1). The first stage in Fig. 6 implements the AND terms of the Boolean expression while the second stage performs the OR operation.

$$VOUT = A'.B + A.B' \qquad (1)$$

The working of the existing memristor-based dynamic Exclusive-OR gate is explained further.

A. Working

During the pre-charge phase, CLK becomes LOW and nodes N3, N4 and N8 are pre-charged HIGH resulting in LOW values at nodes N5, N6 and output node, VOUT. During the evaluation phase, CLK is pulled HIGH and now the output at node VOUT depends upon the inputs at node A and B.

When the inputs A and B are LOW, in such a case, there exists a potential difference between input nodes A' and B and thus current flows through memristor X1 (from p to n) and X2 (from n to p) such that X1 and X2 are driven into HR and LR states respectively. The node N1, thus, becomes LOW and nodes N3 and N5 remain HIGH and LOW respectively. Similar situation exists in lower part of the circuit wherein memristors X3 and X4 are driven into LR and HR states respectively. Thus, node N4 remains HIGH whereas N6 remains LOW. As both N5 and N6 are at LOW level therefore the values at nodes N8 and VOUT remains HIGH and LOW respectively. Similar observation can be derived for other input combinations of A and B.

The existing memristor-based dynamic Exclusive-OR circuit design depicted in Fig. 6 comprises of 6 memristors and 19 CMOS transistors.

The transistors required to implement A' and B' from A and B respectively are not shown in the Figure. The use of several CMOS transistors negatively affects the overall performance of the circuit with reference to area overhead and increased power consumption [7]. Further, the dual stage implementation requires two clock pulses, which results in increased average propagation delay. Therefore, an efficient memristor-based dynamic Exclusive-OR gate design is needed that can provide improved performance without the trade-offs of the existing design. One such design is proposed in the next section.

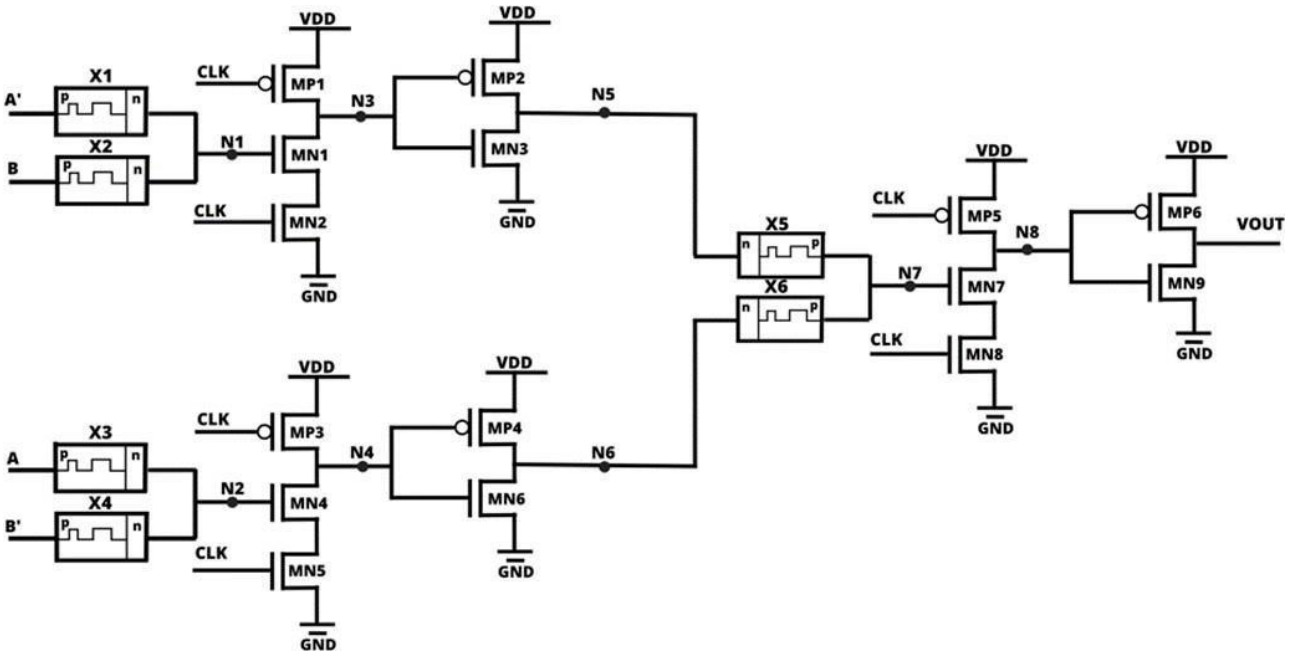

Fig. 6. Existing memristor-based dynamic Exclusive-OR gate

IV. PROPOSED EFFICIENT MEMRISTOR BASED DYNAMIC EXCLUSIVE-OR GATE DESIGN

In this section, a new efficient memristor-based dynamic Exclusive OR gate design is presented with its circuit shown in Fig. 7. The proposed design has inputs as CLK, A, B and an output, VOUT. It consists of only single stage Domino gates and arranges memristors in an AND-OR manner. The memristor pairs X1-X2 and X3-X4 perform an AND operation while their respective outputs are further fed as inputs to the memristor pair X5-X6 connected to realize the OR functionality.

The equation representing the proposed Exclusive-OR functionality is given below.

$$VOUT = (A.B + A'.B')' \quad \text{.....(2)}$$

The working of the proposed memristor-based dynamic Exclusive-OR gate design is explained next.

A. Working

During the pre-charge phase, the output node VOUT is pre-charged to HIGH voltage level as input CLK is LOW. As the CLK is pulled HIGH during evaluation phase, the voltage at node VOUT now depends upon the input values at node A and B. For the case when both the inputs A and B are at LOW logic level, in such a case, there is no potential difference between nodes A to B and hence memristor pair X1-X2 attains the HR state resulting in LOW voltage level at node N1. Simultaneously, the node N2 is pulled HIGH as the memristor pair X3-X4 attains the LR state. The values at nodes N1 (LOW) and N2 (HIGH) are fed as input to memristor pair X5-X6. Due to the flow of current from n to p terminal in X6 and p to n terminal in X5, the memristor X6 attains LR state whereas memristor X5 attains LR state. This results in HIGH voltage level at node N3. The transistor MN1 conducts and discharges the output load capacitor C towards GND to generate LOW voltage level at output node VOUT.

Similarly, for the case when both the inputs A and B are at HIGH logic level, node N1 is pulled HIGH whereas node N2 remains LOW. Now, this time X5 attains LR state and X6 moves to HR state resulting in HIGH voltage level at node N3. The capacitor C discharges through conducting transistors MN1 and MN2 to make output VOUT as LOW.

When the inputs A and B change to HIGH and LOW voltage levels, there is a difference in potential set up across the memristor pairs X1-X2 and X3-X4. This brings the memristors X1 and X4 in the HR state whereas memristors X2 and X3 moves to the LR state. Hence, LOW logic value is generated at both the nodes N1 and N2. As both X5 and X6 are in the HR state therefore the voltage at node N3 remains LOW. The transistor MN1 does not conduct and hence VOUT is maintained at HIGH logic level.

Similarly, when input A is LOW and input B is HIGH, the nodes N1 and N2 are pulled LOW through the low-resistance path provided by memristors X1 and X4 respectively. The voltage at node N3 remains at LOW logic level due to the HR state of memristors X5 and X6. The transistor MN1 remains in the cut-off region resulting in HIGH voltage level at output node VOUT. Table I summarizes the voltage levels at nodes N1, N2, N3 and VOUT for distinct combinations of inputs A and B.

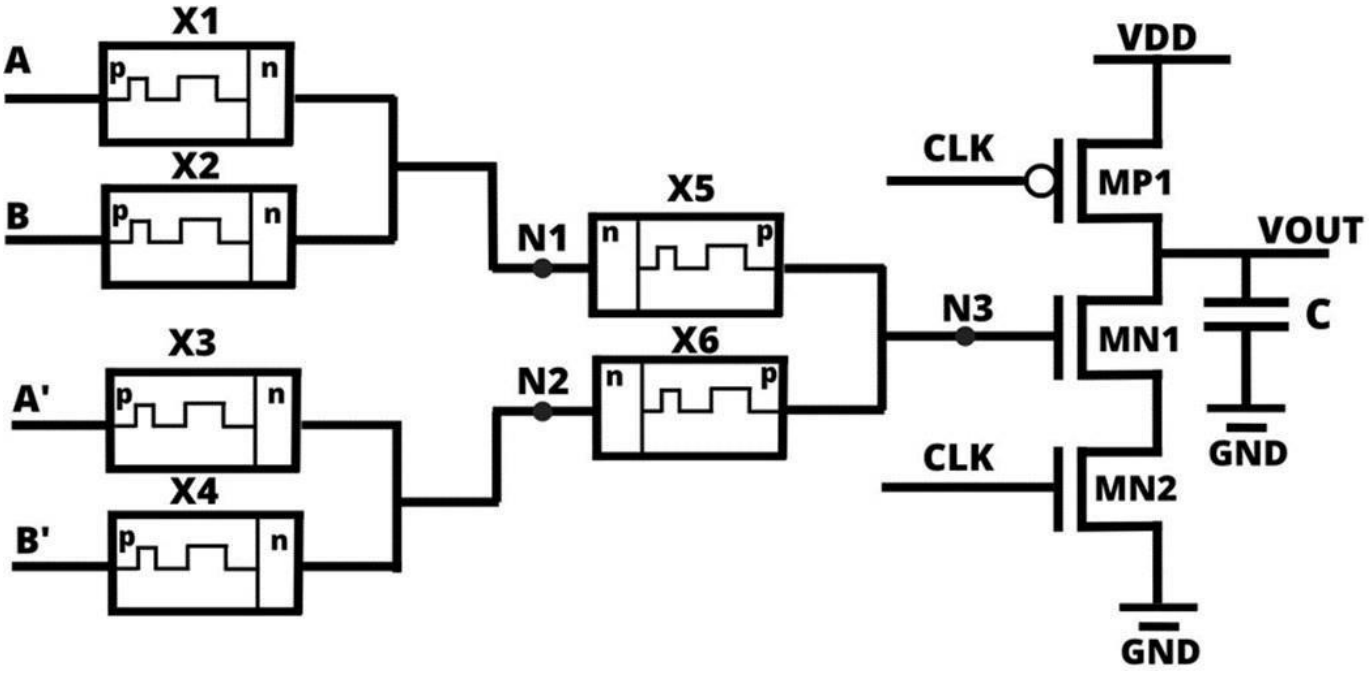

Fig. 7. Proposed Memristor-based Dynamic Exclusive-OR gate

TABLE I. NODE VOLTAGE LEVELS FOR DIFFERENT INPUT VALUES

INPUTS		NODE VOLTAGES			
A	**B**	**N1**	**N2**	**N3**	**VOUT**
0	**0**	**0**	**1**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**
1	**0**	**0**	**0**	**0**	**1**
1	**1**	**1**	**0**	**1**	**0**

Fig. 8. Timing waveforms for Proposed Memristor-based Dynamic Exclusive-OR gate

V. SIMULATION RESULTS

In this section, the proposed memristor-based dynamic Exclusive-OR gate design is simulated and analyzed at 32 nm technology node. In addition, the performance of proposed design is compared with the existing design [7] on the basis of different performance parameters [8] using LTspice XVIItool. The R_{on} and R_{off} values for memristors are 200 Ω and 1.5kΩ respectively. The typical threshold voltages for NMOS and PMOS transistors are 0.397 and -0.339 respectively. The frequency of the applied clock is 50 MHz for transient analysis with 50 % Duty cycle. The analysis results are summarized in Table II- IV with best performance values highlighted in bold font.

A. Functional Verification of Proposed Design

The timing waveform of the proposed Exclusive-OR gate design is depicted in Fig. 8. The waveform shows distinct combinations of input node values at A and B and the respective output node voltage level VOUT during pre-charge (CLK = '0') and evaluation phase (CLK = '1'). During pre-charge phase output node VOUT is pre-charged to HIGH voltage level irrespective of input node values. However, during evaluation phase, VOUT either discharges or remains HIGH depending upon the input values at nodes A and B. When the inputs A and B are at same logic levels, that is, when both A = '0' and B = '0' or when A = '1' and B = '1', the output load capacitor discharges and output node attain LOW voltage level in the evaluation phase. Alternatively, when input nodes A and B are at different voltage levels, that is, when either A = '1' and B = '0' or when A = '0' and B = '1' then HIGH logic level at output VOUT is obtained.

It is worth mentioning that in the proposed design the output VOUT is generated in one clock cycle in contrast to the existing design where the values propagate through two stages and so the output is generated after two clock cycles. The proposed design, thus, is more efficient in terms of propagation delay compared to the existing one.

B. Performance Comparison

The performance of the proposed design is examined and contrasted with the existing design [7] in terms of total power consumption, average propagation delay and number of components (transistors and memristors) required to implement the respective designs. Both the circuit designs are simulated under similar operating conditions with a load capacitor of 100 fF. The results of simulation are summarized in Table II with the improved values highlighted in bold font. It can be inferred from the results that the proposed design consumes 57 % less power and provides 5.06 % improvement in propagation delay when contrasted with the existing design. In addition, the proposed design requires less transistors for implementation thus providing significant advantage in terms of area occupied [8].

TABLE II. PERFORMANCE COMPARISON

Performance Parameter	*Total Power Consumption (μW)*	*Average propagation delay (ns)*	*Transistor count*	*Memristor count*
Existing Memristor based Dynamic Exclusive-OR Gate	**3.99**	**6.258**	**19**	**6**
Proposed Memristor based Dynamic Exclusive-OR Gate	**1.716**	**5.941**	**7**	**6**
Improvement (%)	**57**	**5.06**	**12**	**-**

TABLE III. CAPACITANCE VARIATION

	50fF		*100fF*		*250fF*	
Performance Parameter	***Total Power Consumption (µW)***	***Average Propagation Delay (ns)***	***Total Power Consumption (µW)***	***Average Propagation Delay (ns)***	***Total Power Consumption (µW)***	***Average Propagation Delay (ns)***
Existing Memristor based Dynamic Exclusive-OR Gate	**3.993**	**6.258**	**5.108**	**6.672**	**8.181**	**7.767**
Proposed Memristor based Dynamic Exclusive-OR Gate	**1.716**	**5.940**	**3.384**	**6.574**	**8.068**	**7.449**
Improvement (%)	**57.03**	**5.08**	**33.75**	**1.47**	**1.38**	**4.09**

TABLE IV. TECHNOLOGY VARIATION

	32nm		*45nm*		*65nm*	
Performance Parameter	***Total Power Consumption (µW)***	***Average Propagation Delay (ns)***	***Total Power Consumption (µW)***	***Average Propagation Delay (ns)***	***Total Power Consumption (µW)***	***Average Propagation Delay (ns)***
Existing Memristor based Dynamic Exclusive-OR Gate	**3.993**	**6.258**	**4.044**	**5.720**	**4.326**	**5.819**
Proposed Memristor based Dynamic Exclusive-OR Gate	**1.285**	**5.917**	**1.715**	**5.520**	**1.728**	**5.527**
Improvement (%)	**67.82**	**5.45**	**57.59**	**3.50**	**60.05**	**5.09**

C. Capacitance Variation

To prove the efficacy of proposed design the simulations are also carried out under capacitance variation wherein the load capacitance is varied from 50 ff to 250 ff. Table III summarizes the performance results for total power consumption and propagation delay as the load capacitance is varied. For load capacitance of 250 ff, the proposed design provides 1.38 % and 4.09 % improvement in power consumption and propagation delay respectively. However, as the load capacitance reduces to 50 ff, the % age improvement with proposed design also increases to 57.03 % and 5.08 % in power and propagation delay in comparison to existing design.

B. Technology Variation

With the advancement in technology, the size of the transistors used to implement VLSI circuits is shrinking. As the technology node decreases, the length of the transistor also shortens which improves the efficiency of the circuit. Hence, both the circuits are simulated at different technology nodes to see the impact of technology variation on design performance. The results of technology variations are captured at 32 nm, 45nm and 65 nm technology nodes and are summarized in TableIV for comparison. At 65 nm technology node, the proposed design shows 60.05 % and 5.09 % improvement in power and propagation delay. As the

technology scales down to 32 nm node, the % age improvement also increases to 67.82 % and 5.45 % in power and propagation delay in comparison to existing design. The results, thus, reveal the impeccable performance of proposed design compared to the existing design across all technology nodes

VI. CONCLUSION

An Efficient design for Memristor-based Dynamic Exclusive-OR gate is presented in this paper at 32 nm technology node. The proposed design provides significant improvement in terms of total power consumption and propagation delay in comparison to existing design under different operating conditions. In addition, the proposed design uses less components for its implementation and thus occupies less chip area. The results show that the proposed design consumes 57% less power and provides 5. 1 % faster operation. To verify the robustness of the proposed design, the simulations are also carried at different load capacitance values. As the load capacitance is varied from 250 ff to 50 ff, the % age improvement in total power consumption increases from 1.38 % at 250 ff to 33.75 % at 100 ff which further increases to 57.03 % at 50 ff. Similarly, an improvement from 4.09 % with load capacitance of 250 ff to 5.08 % with 50 ff is also achieved in propagation delay in comparison to existing design. To show the versatility of the proposed design, the results are also captured at different technology nodes (65 nm to 32 nm). It is observed that the proposed design provides significant improvement of 60.05 % in power consumption at 65 nm technology node. As the technology scales, the performance further improves to 57.59 % at 45 nm and 67.82 % at 32 nm node. Similar improvement is also observed in propagation delay wherein the proposed design shows 5.09 % improvement at 65 nm which further increases to 5.45 % at 32 nm node. The proposed design with less area overhead and improved performance, thus, provides an attractive alternative to be used at lower technology nodes for implementing different computational blocks.

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