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Development of Medium Power High Efficiency Multi-Level Buck-Boost DC-DC Converter

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***Abstract*— Power DC/DC converters or regulators form the backbone of different portable electronic devices like cellular phones, laptops, portable electronic devices which are using batteries as their power supply. Portable devices usually comprise of several sub-circuits that should be supplied with different voltage levels, which are not the same as battery's voltage level which is the main supply voltage. A new approach of buck-boost converter is presented in this paper, that automatically detects the zero-inductor current & compels the convertor to deliberately switch from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM), once the inductor current attempts towards negative values, restricting the inductor current to approach towards negative value, and thus enhancing the convertor's performance and efficiency at low load conditions. The converter steps down 200 V input voltage to 187 V and steps up to 211 V simultaneously at 100 Ω load resistance using PSIM software at switching frequency of 100 KHz. The comprehensive analysis of the topology is carried out and the simulated results are compared with the earlier designs at variable loads to verify the performance of the converter.**

Keywords- Buck-boost converter, zero current switching, continuous conduction mode, dc/dc convertor, switching mode power supply, negative inductor current.

I. INTRODUCTION

In the field of power engineering and drives, DC-DC conversion technologies are a hot topic of study. Such devices have electronic platforms for efficiently customizing DC electric voltage [1]. The majority of the time, these converters are utilized to switch between different voltage levels [2][3]. DC-DC convertors are used whenever we want to change some input DC voltage from one level to some other output voltage level which may be either higher or lower in magnitude than the input voltage level. DC-DC convertors form the Backbone of many portable electronic devices which are using batteries as their source of energy. These devices include microgrid application [4], electrical components [5], renewable energy devices [6], internet of things [7], electric vehicle (EV) chargers [8], photovoltaic system (PV) [9], PV and fuel cell-based EV [10], and telecommunication power supply [11]. In addition, portable devices usually are composed of many sub-circuits each of which requires different voltage levels. Since every device uses a single battery source with given rating, so a single battery source cannot fulfil the voltage requirements of all the sub-circuits.

Hence, there is a requirement of a circuit which is capable of giving both greater than and lower than the magnitude of source voltage simultaneously that is buck-boost converter. Such circuits have a large number of applications such as voltage supply to various power islands on the electronic device simultaneously where each power source needs different voltage level from the input. Since DC-DC convertors are used in portable devices where the battery life is the main concern. So, their power efficiency needs to be very high. We can't effort to have decrease in their power efficiency. This is the main motivation behind the paper.

The objective of this paper is to develop a buck-boost convertor that will automatically switch from CCM to DCM prohibiting the inductor current to go negative resulting in the improvement of efficiency. These devices are capable of generating both buck and boost voltages simultaneously. The paper emphasis on DC-DC Buck-Boost convertor, and is designed with a switching frequency of 100 KHz, source voltage Vs = 200 V, and the output buck and boost voltages are 187 V and 211 V respectively at the load resistance of 100 Ω. The main goal is to learn about Switching Mode Power Supplies (SMPS) and the many control methods that are used in them, and then to build a Buck-Boost converter that can generate both buck and boost voltages at the same time.

The paper has been divided into different section where section 2 mainly consists of the basic overview and the working mechanism of buck boost convertor. section 3 covers the proposed topology, validation, simulation of experiments, and the values are compared accordingly. Section 4 spots light on the advantages of proposed architecture. Section 4 covers the future prospect of work, and is followed by conclusion.

II. General overview of DC-DC Buck-Boost Convertor

DC-DC Buck-Boost convertor is one of the types of the SMPS, which produces the output DC voltage that is either less in magnitude or large in magnitude than the input voltage i.e., it either steps down or steps up the input voltage level to some desired output voltage level [12]. Both are utilized to generate several voltage levels out of a given DC supply voltage, and are required to power the handheld products and other components. Using DC-DC converters to generate different voltages levels out of single power supply can significantly reduce gadget size. One can explore the domains and deep insights of convertors basic working and methodology [13]. It consists of two main parts; the power circuit block and the feedback control block for controlling the output voltage of the power circuit block.

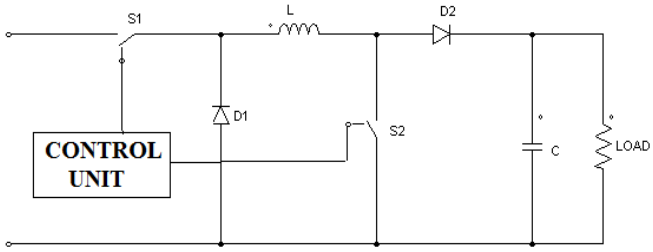

Figure 1. Basic DC-DC buck-boost converter topology

The basic circuit topology of the Buck-Boost Convertor is shown in figure 1. The power circuit or topology consists of semiconductor switches S1 and S2 (which can be MOSFET, BJT etc.), Inductor (L), Capacitor (C) and freewheeling diodes (D1 and D2) while as switch controller together with feedback loop forms feedback block.

The convertor accepts the DC input and uses either Pulse Width Modulation (PWM) or the Pulse Frequency Modulation (PFM) to control the conduction period of MOSFET in order to regulate the output voltage. The external inductor (L), external capacitor (C) forms a low pass filter (LPF) to remove the voltage ripples and generate a regulated DC output voltage. A simple explanation of the converter, working, and its types is widely covered in [12][14].

Operation of Buck-Boost Convertor: The simplified structure of buck boost convertor is shown in figure 2 (a). There are two states in which the buck-boost convertor operates i.e., ON state and OFF state. These two states are discussed in detail below.

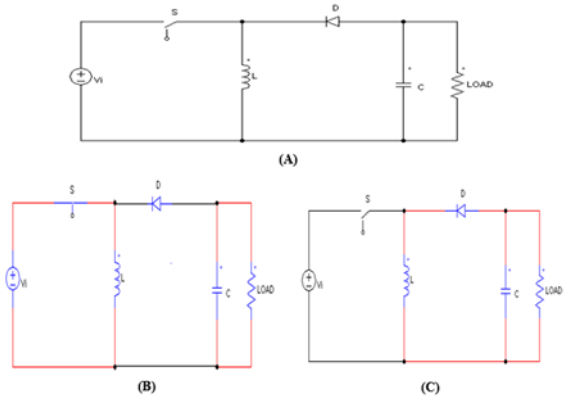

Figure 2. (A) Show general structure of buck boost converter, (B) show equivalent ON state circuit, (C) depicts the equivalent OFF state circuit.

The working mechanism of Buck-Boost convertor is very easy to understand. Here the ON state refers to the ON state of power switch (transistor). once the power switch is turned ON, input voltage supply is immediately linked with inductor. As a result, energy starts building up in inductor. The capacitor provides energy towards the load connected at this point. The equivalent diagram of the buck-boost convertor during the ON state is shown in figure 2 (b). When the power switch is in ON state, the diode D essentially is reverse biased, and is equivalent to the open circuit. So, the current IL through the inductor starts increasing linearly and a voltage drop of VL occurs across the inductor L. Therefore, current in load and charge on the capacitor C begins to decrease gradually during the ON time. Also, during ON period, the inductor L stores the electrical energy in the form of magnetic field.

The equivalent diagram of buck-boost convertor when the power switch is in OFF state is shown in figure 2 (c). When the power switch is in OFF state, the energy stored by the inductor during ON state is released back into the circuit and the inductor current IL starts falling linearly. This causes the polarity of voltage across the inductor opposite to the polarity that was during the ON state. The stored energy in an inductor now delivers current to the load through the diode D which is now in conduction mode. Since the voltage across the capacitor can't change instantaneously, thus the change in the output voltage is prevented by the capacitor C and reduces the percentage of ripples in the output voltage as a result of fluctuating inductor current. Thus, we get a perfect DC voltage waveform at the output with some ripples instead of a square wave.

III. Proposed Topology and Results

There is a requirement of a circuit which is capable of giving both greater than and lower than the magnitude of source voltage simultaneously with high efficiency that is

buck-boost converter. Such circuits have a large number of applications such as voltage supply to various power levels on the device simultaneously where each power sources need different voltage levels from the input. The proposed architecture of buck-boost converter is shown in Figure 3.

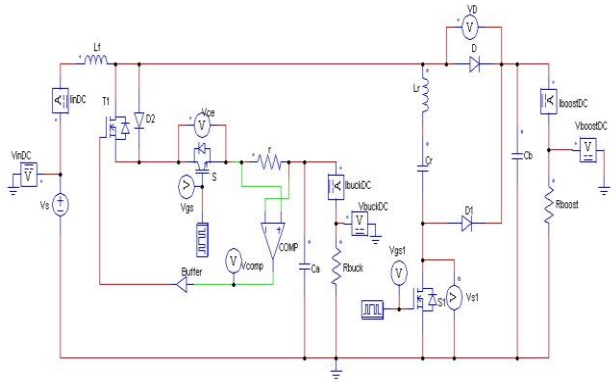

Figure 3. Depicts the architecture of proposed converter.

The circuit consists of two parts: a buck part and a boost part. The boost part consists of a resonant inductor L_r, a resonant capacitor C_r, an auxiliary switch S_1, and an auxiliary diode D_1. This resonant branch is responsible for creating the zero current switching (ZCS) condition for the main switch. The buck part contains an inductor L, a main switch S, a diode D_2, a resistor r, comparator (comp) and a switch T_1.

The proposed circuit works in five operating stages within one switching cycle. The equivalent circuits for five operating stages are shown in the figure 4.

Operating Modes: Prior to stage (a), the switch S is conducting and Cr is negatively charged to a certain voltage. At the stage (a) both the switches are turned on. The auxiliary switch, S1, starts a resonance between C_r and L_r. As a result, the current through the inductor starts increasing. When the current through the inductor reaches at the maximum value, the voltage across C_r becomes zero. For zero current switching to occur, the maximum current through the inductor should be greater than I_i i.e.

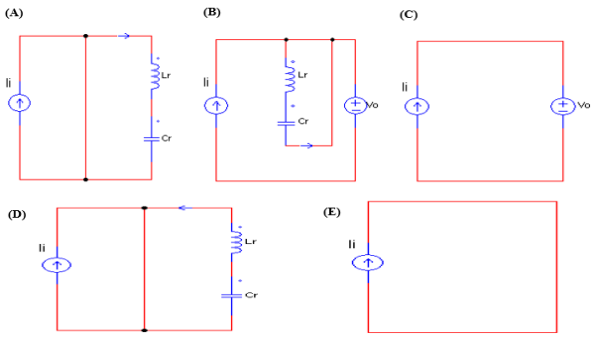

Figure 4. Equivalent circuits with operating stages

$$I_{L_r}^{max} \geq I_i$$

As a result, the current through the transistor, S, becomes zero and the gate-drive signal is disabled at the instant. The time period during which both the switches are conducting in the stage (a) is given by

$$T_{on} = \frac{T_r}{4}$$

Where, $T_r = 2\pi\sqrt{L_r C_r}$ is the resonant period.

The impedance of the resonant tank is given by $Z_r = \sqrt{L_r / C_r}$. The switch S1 is turned OFF in a little while after S is turned OFF. Practically, this time is taken around $0.07T_r$, such that $I_{L_r}^{max}$ is about 10 % higher than I_i. At this instant both the diodes D and D1 start conducting. At the stage (c), the current through the inductor L_r reaches zero i.e., half cycle resonance is complete, and the diode D1 gets turned OFF. In stage (d) the switch S is tuned ON again charging the inductor L by the input voltage and C_r and L_r undergo a half-cycle resonance thereby reversing the polarity of the C_r voltage. During the remaining period of the switching cycle i.e., at stage (e), the switch S is conducting and thus both stage (a) and stage (e) are used to generate the buck voltage. In this way, both the buck and the boost voltages are obtained simultaneously. The varying potential of the comparators input becomes clearly positive, till the I_i show rising voltage (positive) during step (e). As a result, the comparator's response seems to be a positive wave. Until the current through the inductor is positive, the output will continue to be high. The differential voltage at the comparator's input is negative, again when inductor current reaches zero as well as continues to become negative [13]. This negative voltage turns OFF the transistor T2 and the diode D2 comes in series with the switch S. Thus, the diode D2 gets reverse biased, and this restricts the movement of negative I_i inside the network. Hence the proposed circuit automatically shifts from CCM to DCM. The voltage drop due to the diode D2 during the positive inductor current is prevented by the automatic turn ON of the transistor T1. This leads to the shortening of the diode D2.

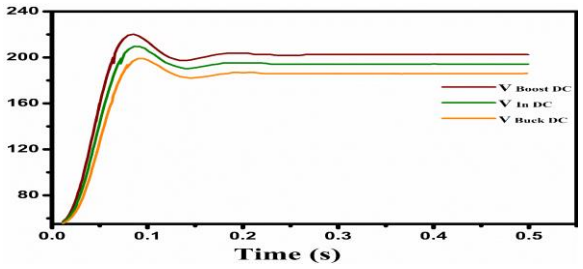

Figure 5. Shows input voltage and output buck and boost voltage waveforms of the proposed converter.

The proposed circuit is simulated at 100 KHz. The simulation of the circuit is done in PSIM simulation software. Fig 5 shows the source voltage, the output buck and boost voltage waveforms of the proposed buck-boost converter at load = 100 ohm.

Figure 6 shows the flow of inductor current with increasing load values, as a function of time, clearly depicting the positive nature of current. Since the inductor current rarely goes negative, power always flows from supply to the load, as seen by the waveform. As a result, our converter's performance is excellent despite extreme loading situations.

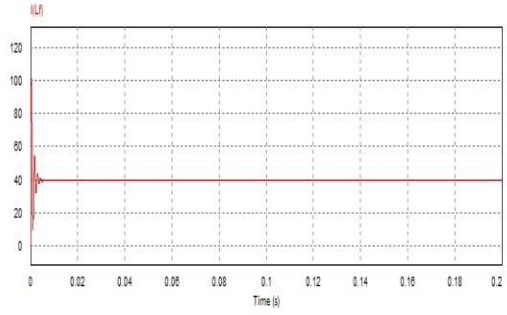

Figure 6. Inductor current I(Lf) under heavy load (R=10 Ω).

Figure 7 shows the I(r), Vcomp and I(D) waveforms under light load conditions. The waveform obtain show clearly matches with the explanation [13]. It's indeed obvious and clear that till the I(r) is positive, differential voltage of comparator's input remain positive. Hence, the comparator shows positive value. Till the current through the inductor is positive, the resultant output depicts previous (same) values. The voltage now at comparator's interface becomes negative when the inductor current value reaches zero and even strives towards negative value. As a result, the comparator (Vcomp) produces a zero output, as seen in Figure 7. As a result, the switch T1 is disabled. When T1 is turned off, thus maintaining inductor current zero & preventing negative current for flowing inside the network. It has been found that the that the efficiency is almost constant and above 99% independent of load resistance.

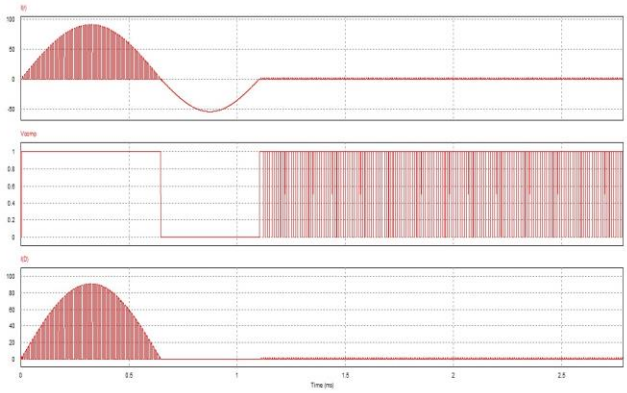

Figure 7. Various waveforms (Ir, Vcomp, and Id) for determining the working mechanism of proposed topology.

The figure 8 shows the comparison curve of efficiency at different output power. The proposed architecture shows higher efficiency than the corresponding literature. The proposed design has efficiency of 99.98%, an increase of 2 and even 3-digit higher value is obtained, which is high and hence the result obtained are desirable.

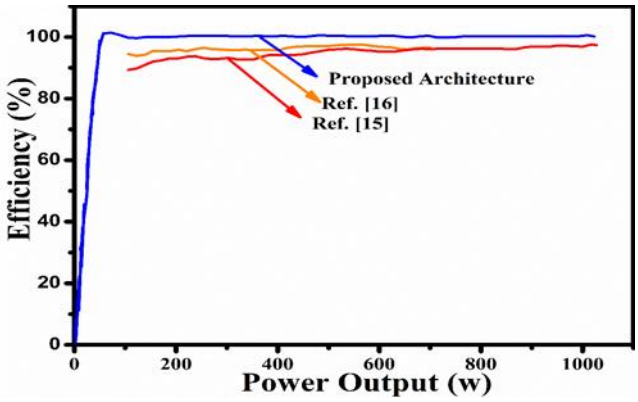

Figure 8. Shows the comparison curve of efficiency at different output power.

Table 1 presents some comparisons of given topologies in the literature with the proposed topology in this paper. It is clear that the proposed converter gives higher efficiency than the other topologies. Also, the number of output pins are two that give simultaneous buck and boost voltages.

TABLE I. SHOWS THE COMPARISON OF VARIOUS PARAMETERS.

Parameter	[15]	[16]	**Proposed**
Input Voltage	100 V	200 V,300 V,400 V	200 V
Output Voltage	200 V	300 V	187 V, 211 V
Switching Frequency	40 KHz	18.7 KHz,	100 KHz

		22.4 KHz, 24.6 KHz	
Maximum Efficiency	96.89	97.11	99.92
Output Pins	1	1	2
Number of components	8	5	14
Sequential	Yes	Yes	No
Simultaneous	No	No	Yes
Load Resistor	100 Ω	120 Ω	100 Ω
PWM	Yes	No	Yes
PFM	No	Yes	No

Table 2 shows that at different resonance frequencies and the different combination of inductors and capacitors, the value of output boost current is almost constant with minute deviation at 50 and 100 KHz.

TABLE II. THE VALUE OF BOOST CURRENT AT DIFFERENT RESONANT FREQUENCIES

5	**L**	**C**	I_{boost}
50 KHz	5.12 µH	5.0 µH	0.416 A
100 KHz	1.53 µH	2.0 µH	0.411 A
175 KHz	0.426 µH	0.40 µH	0.408 A
200 KHz	0.332 µH	0.30 µH	0.408 A
500 KHz	0.0512 µH	0.05 µH	0.408

Thus, the system is stable with respect to the variation of resonance frequency.

IV. ADVANTAGES OF PROPOSED ARCHITECTURE

The proposed design is suitable for the applications that require multiple output voltages simultaneously. The proposed topology also makes automatically switch from CCM to DCM and prevents the flow of inductor current towards negative value. The efficiency of the circuit is very high and thus makes it a better design for various applications.

V. FUTURE PROSPECT

In this paper, we have designed the convertor at higher level i.e., at block level. We keep all the parameters in the power MOSFET's constant i.e., its threshold voltage, aspect ratio (W/L) etc. In future a more work can be done at low abstraction level i.e., device level. We can vary (W/L) ratio and threshold hold and observe their effects on the power loss. Based on the results, we can choose some optimum value of these parameters where the power loss is minimum to get even better efficiency performance. The proposed topology can also be further improved by adding an adaptive controller, which can adapt to different fluctuations and load variations. The hardware size optimization and fixed output voltage depending upon the application are other requirements.

VI. CONCLUSISON

A new topology of buck-boost DC-DC converter has been proposed in this paper having maximum efficiency of 99.98%. The converter is capable of generating both buck and boost voltages simultaneously. The convertor has been simulated at 200 V input voltage with the help of PSIM software at a switching frequency of 100 KHz. In addition, a basic insight into the working of the buck-boost convertor is given. Also, the topology of the buck-boost regulator was studied & the different components present in it were discussed. The various control techniques like PWM and PFM to vary the duty cycle were also discussed. It has also been shown that the power dissipation in case of SMPS is less as compared to the linear regulator which makes it more popular to be used in portable devices than the linear regulator. The converter simultaneously provides voltages more than and less than the magnitude of the source voltage while maintaining high efficiency. Voltage supply to numerous circuits is one of the many applications for such circuits. The two output voltage pins that give simultaneously voltages with high efficiency prove it to be better design.

DECLARATIONS

Ethical Approval: We certify that the manuscript titled "Development of Medium Power High Efficiency Multi-Level Buck-Boost DC-DC Converter" has been entirely our work, and it does not infringe the copyright of any third party. The submission of the paper implies that the paper has not been published previously, and is not under consideration for publication elsewhere.

Competing Interests: The authors declare no competing interests. The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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