2021

Self-Assembly of Electric Circuits

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SELF-ASSEMBLY OF ELECTRIC CIRCUITS

by

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A Dissertation

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

Major: Electrical and Computer Engineering

The University of Memphis

August 2021

ACKNOWLEDGMENTS

Foremost, I would like to express my gratitude towards my advisor Dr. Russell Deaton for his endless patience, motivation, guidance, and support throughout my work; and for always having my back. I want to thank Dr. Max Garzon for his valuable suggestions, informative comments, and guidance on my dissertation. I also want to thank the other members of my dissertation committee: Dr. Hasan Ali and Dr. Madhusudhanan Balasubramanian, for their time, insights, and detailed comments on my research, writings, and presentation. I thankfully remember the contributions of my teachers at the University of Memphis that helped me to flourish my knowledge and vision. I also want to deliver my appreciation to Tyler Moore, who provided knowledgeable suggestions on my works.

A special note of thanks goes to my husband, Md Ashekur Rahman, for his constant support and encouragement throughout the journey. Also, I would like to express my gratitude to my brother Dr. Bashir Morshed whose encouragement helped me to fulfill my dream. Last but not least, I would like to thank my parents, family members, friends, and well-wishers who have always motivated, supported, loved me, and thereby strengthened me up throughout my life.

ABSTRACT

Yasmin, Rojoba. PhD. The University of Memphis. August 2021.
Self-Assembly of Electric Circuits. Major Professor: Dr. Russell Deaton

Inspired by self-assembled biological growth, the circuit tile assembly model (cTAM) is an abstract system that attempts to understand the effects of electricity on growth. The cTAM is based on the DNA tile assembly system with a unit tile that combines chemical glues with basic electrical circuit components. In the cTAM, the growth of resistive tiles is driven by a voltage source until the voltage at the terminus of the circuit is less than a threshold. This simulates a system with a finite resources whose consumption establishes self-control over the extent of its growth. This research has extended the cTAM to develop theoretical models that exhibits specific functionalities, namely replication and logical computation. The first result is a replicating cTAM that exhibits three essential properties of life: self-assembly, self-controlled growth, and self-replication. The second result is a Boolean cTAM model that implements a computationally complete set of Boolean gates that can make decisions about the extent of its growth. The final research goal is to build a sequential logic circuit with memory. This dissertation provides insight into the role of electric phenomena in biological form and function that might be useful for signal propagation in bioelectric networks.

TABLE OF CONTENTS

LIST OF FIGURES

Figures **Pages**

LIST OF TABLES

Tables **Pages**

Chapter 1

Introduction

If humans could make artificial systems with the same capabilities as living systems, then, that could produce more adaptable, sustainable, intelligent, and powerful technologies to confront the challenges of a planet that is significantly impacted by human presence. Self-assembly, self-controlled growth, self-replication, decisions based on self-awareness, and memory of those decisions are capabilities of living systems that we would want to capture in artificial systems. These characteristics can be found in primitive mechanisms in biology, like protein production and folding, as well as in primitive organisms like physarum (slime mold).

Another motivation for this work was to gauge whether electrical mechanisms, in addition to chemicals, could establish another level of control over the assembly of patterns. Bioelectrical effects on somatic cell formation and function are potentially significant and present in primitive organisms. Bioelectric potential distributions influence gene expressionm, and thus, processes like embryogenesis. Therefore, a goal was to determine what sort of advanced capabilities that a self-assembly system augmented with electrical forces could achieve.

Self-assembly is about how biological systems construct and organize themselves into complex structures with powerful functionality, for example, a ribosome factory for producing proteins. Self-assembly is an ubiquitous process in which autonomous components assemble into a target structure by following rules without external control. Numerous examples of self-assembly are prominent in nature and the biological systems around us. Examples range from the formation of crystalline structures, DNA formation, protein folding, tobacco mosaic virus (TMV) to that of social contact networks [2–7]. The initial inspiration for this work was DNA-guided self-assembly of nanostructures [8], in which target structures are programmed through DNA oligonucleotides binding to their complements, and which

is capable of forming complex structures [9] and complex function, such as Turing universal computation [8].

The growth of living systems is controlled by limited resources. Some models of DNA self-assembly have the potential for uncontrolled growth. Motivated by this, the circuit tile assembly model (cTAM) was devised to model a system whose growth was limited by the consumption of a finite resources, in this case, a voltage source. For example, the growth of a bacterial colony on an agar plate is limited by the supply of nutrients. Self-control limits the growth of an open system through local interactions between its own components and the environment. The cTAM [10, 11] intended to capture both self-assembly and self-controlled growth mechanisms. The cTAM model has a voltage source in the seed tile, and the potential decreases with the growing assembly until the potential drops below a threshold voltage. This growth is referred to as self-controlled growth because the size and shape of the final circuit configuration depend on the primary determinants of the system, such as the potential source and parameters, such as resistance, of the component tiles.

Another characteristic of living systems is the ability to reproduce. Self-replication is the process in which an individual senses when it has reached adulthood and starts to construct a similar copy of itself. The replicating circuit tile assembly model (rcTAM) [12] augmented the cTAM model with another capability: Self-replication (Chapter 2). [12] presented a cTAM that has the power of self-replication along with other two features: self-assembly and self-controlled growth. Self-replication has the potential to model a nanomanufacturing system, for example, that consumes resources to construct copies of the desired product.

Living systems sense their environment, and then use that information to respond appropriately. This capability is present in even the most primitive organisms and might be called self-aware. For example, the slime mold physarum can explore a maze to locate nutrient supplies, and then, strengthen those connections to the

nutrient while eliminating unproductive paths [13, 14]. In [15], the Boolean Circuit Tile Assembly Model (bcTAM) implements a complete set of Boolean gates that can make logical decisions based on interactions with the environment (Chapter 3). In the bcTAM, the lengths of simple resistive ladders represent signals that could be interpreted as the response of the system to the environment. These environmental signals could be either a variable set of source voltages representing input from sensors or a spatial distribution of thresholds voltages representing a temperature or chemical gradient in the environment. Thus, the bcTAM represents a self-aware system that possesses all the components necessary to interact with and measure environmental input and compute a response.

By remembering successful responses to environmental factors, organisms increase their chance of survival and gain an evolutionary advantage. This “memory” could be realized in successive generations that evolve according to the demands of external conditions, or physiological change in a single organism that has adapted to a given environment, like physarum and the nutrient supply. To remember responses and act accordingly, the bcTAM was extended to implement a system that can remember its state (Chapter 4). Specifically, a flip-flop, which stores state information, was implemented in a bcTAM system.

This dissertation has introduced cTAM, rcTAM, bcTAM, and bcTAM flip-flop as an attempt to capture aspects of the living system and their constraints in a dynamic growth-based model. These models (cTAM, rcTAM, and bcTAM) consist of basic electric circuits like resistors, diodes, and voltage sources. The models are constrained by source potentials and threshold voltages similar to limited resources and environmental conditions, respectively, and they have achieved powerful properties of life, such as self-assembly, self-controlled growth, self-replication, and computation. Moreover, they demonstrate the powerful capabilities that might arise in electrically influenced biological growth phenomena.

1.1 Motivation for the Study

Self-assembly is prominent in atomic interactions to cellular replication, DNA, RNA, protein folding, snowflakes, crystal formation, and social media. Self-assembly integrates concepts from physics, biology, chemistry, materials science, and nanotechnology [5]. [16–19] have mentioned self-assembly as a prospective approach for nanotechnology. [18] introduced a self-assembly technique that arranges conducting nanoparticles into a long chain. [20] described a process of forming interconnections between electronic devices, where the basic unit is a polyhedron on whose faces electrical circuits are printed. Also, DNA self-assembly, a promising paradigm for nanotechnology, provides a potential platform for generating new types of electric circuits [8, 21–23]. Since the seminal work on the Hamiltonian path problem by Adleman [24], the study of DNA molecules that can perform computation is of high interest in nanotechnology. [25] presented a tile assembly model, where electrically active components are attached to DNA tiles, and it can construct a path between two points. Adleman [24], Winfree [26–28], Seeman [29], Wang [30–33], and Rozenberg [34] have established the connection between self-assembly and DNA computation. Therefore, this background acted as a motivation to study the potential of self-assembly models.

Electric signals influence many artificial growth processes, namely additive manufacturing [35], electrospray technology [36], and nanomanufacturing technologies [37–39]. Electric fields and their associated effects are used in processes like electroplating, electrochemical vapor deposition, and so on. The dependence between electric signaling and the electrochemical growth of materials is prominent. Electrochemical growth is a process where a growing film increases its resistance, reduces surface reactants, and eventually, stops the growth. Thus, a voltage-controlled self-assembly model inspired by the electrochemical growth mechanism is one of the initial motivations for this study.

Electric phenomena play a significant role in biological function, self-organization, and self-assembly systems [40–42]. For instance, galvanotaxis is the directional movement of cells in response to an electric field, which is present in wound healing and embryogenesis [43]. Also, the use of electric pulse signals improves the directionality of galvanotaxis [44]. Endogenous electric fields and their potential distribution changes action potentials across cell membranes which interact with genetic mechanisms for pattern formation during tissue generation and embryonic growth [41, 42, 45–47]. During processes like embryogenesis, networks of somatic cells are dynamic as the network structure changes. An electric circuit model that is dynamic in nature and analogous to bioelectric networks for cellular communication is an interesting idea to explore. Moreover, the formation and stability of many biological molecules, such as lipids, nucleic acids, amino acids, are directly affected by electric phenomena [48].

An organism grows in response to environmental stimuli. For example, Physarum polycephalum, which is a simple acellular, multi-nucleated organism, can find the shortest path towards the destination [49], and reconstruct the transportation maps for major cities [50]. Changing the ambient conditions, temperature, stress, or stimulation, bring changes in the response of Physarum [13, 14]. Electricity and circuits are also important in modeling action potentials in a biological cell, such as Hodgkin-Huxley model [51], and are the basis for neural networks. Thus, the exploration of the computational capabilities of the cTAM was also a goal. Therefore, the cTAM is an attempt to integrate ideas from self-assembly with evidence that bioelectricity is important to biological computation, signaling, and pattern formation.

1.2 Introducing the Circuit Tile Assembly Model (cTAM)

Inspired by the biomolecular growth mechanisms, a new self-assembly model consisting of electrical circuit components was introduced and analyzed in [10–12, 52, 53], denoted as *cTAM (Circuit Tile Assembly Model)*. In this model, larger

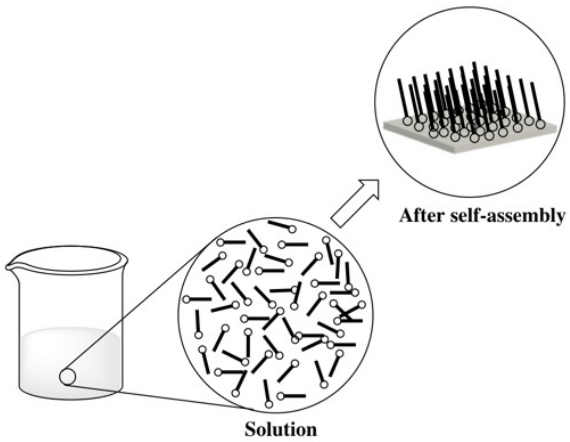


Fig. 1.1: An example of the self-assembly of nanoparticles in a solution. In this diagram, it can be seen that a disordered system formed an organized structure which can be due to specific interactions among the particles [1].

circuits are self-assembled from unit tiles consisting of basic electrical components. This model acts as a generalized model of algorithmic self-assembly since the electric field acts as the driving force of a cTAM until it falls below a predefined threshold value, similar to the nutrient supply of a bacterial colony. Being a nonbiological system but capturing certain aspects of bioelectric networks, the cTAM exhibits important life-like properties, such as self-assembly, self-controlled growth, instant and distant communication [10, 11, 52, 53], self-replication [12], and Boolean computation [15].

The formal definition of a cTAM electric circuit, circuit tile, and the Circuit Tile Assembly Model cTAM are taken from [11].

Definition 1.2.1 (cTAM Electric Circuit)**.** A *circuit* is a tuple $\gamma = (N, E, R, \partial N)$ on a weighted graph (N, E) consisting of nodes N, and weighted edges E, where the weight is a non-negative real number that represents the value of the resistance $R : E \to \mathbb{R}_{\geq 0}$ on that edge $e \in E$ in Ohms (Ω). Moreover, two finite subsets of nodes, $N_{in},\ N_{out} \subseteq N$, identify the inputs and outputs to the circuit, respectively. Inputs and output nodes are points at which other circuits connect to γ or where measurements are made, and are also called the boundary or terminal nodes of the circuit, $\partial N = N_{in} \cup N_{out}$.

(a) (b)

Fig. 1.2: Figure a: Seed Tile (Tile A) for the cTAM consisting of one dc voltage source ν_0 and two resistors, R and αR. It has one pair of output nodes $\{1, 2\}$ across the resistor R. Node 1 has glue a and node 2 has glue b. Figure b: Circuit Tile (Tile B) for the cTAM. It consists of two resistors R and αR in series connection. It has one pair of input nodes at $\{1, 3\}$ and one pair of output nodes $\{1, 2\}$. Node 1 has glues (a, $\overline{a}$), node 2 has glue b, and node 3 has glue $\overline{b}$.

Definition 1.2.2 (Circuit Tile)**.** A *circuit tile* is a cTAM electric circuit in which specific input and output nodes are augmented with glues representing chemical bonds, complementary DNA sequences, *etc*. . ..

Definition 1.2.3 (Circuit Tile Assembly System)**.** A *circuit tile assembly system* is a tuple $\mathcal{C} = (\Gamma, S, \tau, \nu, \zeta)$, where Γ is a finite set of circuit tile types, $S \subseteq \Gamma$ is a set of seed circuit tiles that includes a source and ground, $\tau \in \mathbb{R}$ is the threshold voltage for attachment, $\nu : N \to \mathbb{R}$ is the electric potential energy at a node relative to ground in the circuit, and $\zeta : N_{in} \to N_{out}$ maps input nodes to output nodes.

The growth mechanism of the cTAM is inspired by the DNA tile assembly system, a promising technique for assembling structures. This model consists of tiles which are a square with a glue on each side, and they are complementary DNA sequences. A DNA Tile Assembly system that implements Wang tiles is capable of universal computation. Wang tiles [54], first proposed by Hao Wang, uses square tiles with a color on each side. The attachment is based on the matching colors, without rotation. Our cTAM model is motivated by these attachment rules where every tile has

a set of glues on the input and output nodes. If a glue a matches with its complementary glue $\overline{a}$, they are eligible for attachment, if activated by the electric potential. The attachment depends on two factors: complementary matching glues and the potential across output node pairs that must be greater than the threshold voltage.

The circuit tile assembly model(cTAM) was introduced in [10, 11]. The first and foremost target structure was to build a resistive ladder circuit with cTAM, motivated by Richard Feynman's *Lectures on Physics* [55]. The cTAM ladder requires only two tiles: one seed tile and one circuit tile. Seed tile is a voltage divider circuit with voltage source ν_0 and two resistors (R and αR) connected in series (Figure 1.2(a)). It has one pair of output nodes $\{1, 2\}$ across resistor R. Seed tile has glues $g(1) = a, g(2) = b$. The circuit tile has the same circuit configuration as the seed tile except for the supply voltage (Figure 1.2(b)). It has one pair of input nodes at $\{1, 3\}$ and one pair of output nodes $\{1, 2\}$. It has glues $g(1) = \{a, \overline{a}\}, g(2) = b, g(3) = \overline{b}$. Assembly starts from the seed tile. The input node pair of the circuit tile attaches to the output node pair of the seed tile if the potential across the node pair $\geq \tau$, and they have complementary glue pairs. The growth stops when the output potential voltage falls below the threshold voltage, and the assembly becomes a terminal circuit. Without the control provided by electrical circuit with only DNA glues, the ladder is an example of a system that would have uncontrolled growth increasing in size until tiles ran out.

[10, 11] introduced the cTAM, calculated the size of the assembled circuit, predicted the shape, uniqueness, and symmetry of ladder and grid circuits. [11] also presented two growth models based on whether the node potentials were measured before or after attachment named as *Pre-cTAM* and *Post-cTAM*, which were equivalent in nature. The cTAM in [10, 11] consisted of resistive circuits and voltage sources, and achieved self-assembled and self-controlled growth.

Living cells self-assemble, and understanding life will therefore require

understanding self-assembly [56]. Life can be defined as an open system that interacts with the environment, grows by consuming resources, senses when it has reached its adulthood, and reproduces a copy of itself. The *Replicating Circuit Tile Assembly Model* of [12] has been designed by keeping this in mind. [12] proposed the rcTAM, where a ladder circuit grows until it has reached its limit, and in response, initiates the growth of a new circuit identical to itself. Therefore, [12] augments the cTAM model to achieve another important living system property, self-replication, and hence, the proposed model rcTAM connects more to the bioelectric networks. In rcTAM, an assembly is a sequence of connected ladder circuits but electrically isolated from each other. Some significant results of this paper are self-replicating property, proofs of bounded growth, and possible aging phenomena that produce a stable circuit population.

[15] introduced another family member of cTAM, named as *Boolean Circuit Tile Assembly Model (bcTAM)* in which a computationally complete set of Boolean gates is implemented. Also, a mapping of the growth mechanism to Circuit Satisfiability problem was analyzed in [15]. The bcTAM model achieved Boolean functionality, and the growth approximated axonal growth in the neural network. It provides a new outlook of computation of both bioelectric and neural networks.

Electric signal influences the axonal growth in a neural network. [51] worked on the equivalent circuit model that represents the propagation of action potential. [14] depicted a three-element Windkessel model that is widely used to model coronary blood flow. The three-element Windkessel equivalent circuit is built of an alternating current source, two resistors, and one capacitor. The dc equivalent of that circuit is similar to the cTAM ladder unit tile. This evidence shows that the ladder circuits of cTAM closely resemble the biological signal propagation. The terminal circuits built by the models bcTAM [15] and rcTAM [12] can be converted to a 1D ladder using

equivalent resistance calculation. Thus, an electric ladder is a fundamental circuit configuration for all cTAM models.

In each chapter of this dissertation, different applications of the circuit tile assembly model are investigated. This dissertation is organized as follows: Chapter 2 introduces the replicating cTAM that has the power of self-replication along with self-assembly and self-controlled growth. In chapter 3, the Boolean cTAM is explained to explore Boolean functionality with a circuit tile assembly system. The next chapter attempts to build a memory cell with the cTAM model. Lastly, the significance of the study and future work are described in chapter 5.

1.3 Objectives

Algorithmic self-assembly has emerged as a promising tool for nanoscience, DNA self-assembly, and complex circuits [9, 57]. A self-assembly model (cTAM) that captures the features of biological growth and their connection with bioelectric fields was introduced in [11]. The prime objective is to investigate the capabilities of self-assembly systems augmented by electric phenomena, where growth is driven by an electric potential as long a threshold is exceeded. The circuit tile assembly model, an abstract signal propagation model, is an appropriate candidate for achieving the research goal. The cTAM has already achieved two important features: Self-assembly and self-controlled growth described in section 1.2. The specific objectives of this dissertation are as follows:

1. **Implement self-replication**

   Understanding the properties that govern the life-cycle, such as self-replication, are fundamental scientific questions. The study of artificial self-replicating models has been a topic of interest for a vast range of research areas, ranging from nanoelectronics [9, 57, 58] to space exploration [59]. Von Neumann's universal constructor model [60, 61], John Conway's *Game of Life* [62], or self-reproducing cells in artificial chemistry [63] are some notable works on

finding a simple but cooperative model for a self-replicating system.

Also, [64–67] have conducted a study on the kinetics of self-organization and self-replication. The circuit tile assembly system is an abstraction of a growth process that resembles the living system. Thus, the cTAM model achieves three properties of the living system: self-assembly, self-controlled growth, and self-replication as the first objective of this dissertation. This study will reveal the power inherent in the cTAM to represent biological phenomena that also could be a basis for the manufacturing of nanodevices and nanomaterials.

2. **Implement logical computation**

   The next question is: Can a self-assembly model built with inorganic components perform logical computation? More specifically, can the cTAM system make logical decisions about the extent of its growth, *i.e.* length of ladders? The replicating circuit tile assembly model [12] has shown some capability of decision making. It can sense when the assembly has reached a mature stage and starts producing offspring. The second objective of my dissertation is to extend this idea and build a cTAM model that can take more complicated decisions based on Boolean logic. The cTAM conceptualizes the signal propagation in a biological network, such as axonal growth. Thus, the study intends to investigate the capability to perform Boolean functions in bioelectric networks and use the results of these computations to gather information about the state of growth or non-growth in a family of ladder circuits.

3. **Implement memory of state information**

   This capability forms the basis for a potential memory or more advanced devices, like a counter. The rcTAM [12] produces its clone copy as long as resources are available. From the perspective of nanomanufacturing, producing a finite copy is significant. Thus, having a counter compatible with the circuit tile

assembly system will be helpful. A counter needs to remember its previous state information, and the logic design of a basic counter requires a flip flop, a fundamental block used to store state information. So, the final objective of this study is to build a flip flop with cTAM that can remember its previous state. Therefore, an interesting question might be, can a simple self-assembly system built with basic circuit components exhibit this advanced capability? Also, the ability to remember its previous state is an aspect related to a cTAM reasoning about itself. Thus, would it be called self-aware? These questions are the motivation behind the study of the last objectives and chapter 4.

1.4 Contributions

This research's objective was to develop the cTAM model to be self-replicating, to be capable of doing Boolean computations about its growth and environment, and to implement within the model a device that remembers state information. The cTAM was motivated by DNA self-assembly, electrochemical growth processes, and the influence of bioelectric networks on biological pattern formation. Its basic component is essentially the same circuit that is used to model action potential propagation in axons. These goals have been accomplished, and moreover, they have shown that a simple electric circuit model of growth is capable of a surprising amount of complexity.

The replicating circuit tile assembly model (rcTAM) [12] is a theoretical model that achieves self-replication. The rcTAM generates a dynamic network whose structure changes with each tile attachment, similar to embryogenesis, in which networks of somatic cells are also dynamic. Being a nonbiological system, it attempts to abstract the effect of electric signaling in a bioelectric network with primitive electric circuit components and a threshold mechanism, as in ion channels or gap junctions. This rcTAM has captured three essential properties of life: self-replication, self-controlled growth, and construction through self-assembly. The rcTAM exhibits

such advanced capabilities with very simple circuitry, making the model interesting to study.

The second model bcTAM [15] has achieved a computationally complete set of Boolean gates within the circuit tile assembly system. The bcTAM, a resistive ladder network motivated by biological self-assembly, approximates electrical conduction in axons. It approximates how an organism grows in response to the environment and potential distributions. For example, consider a cTAM system with a set of input voltages that represent sensory inputs in a biological organism. Different sets of these input voltages (high or low) could represent different food sources or potential predators. In bcTAM, the size of the ladders will not be the same because of the difference in input voltages. We might be interested to have a cTAM system that can give signals regarding the size of the ladders, such as when the system is terminal (no growing assembly) or when the system is still growing. With bcTAM, you can recognize these different patterns, and thus, potentially act upon them. Hence, the system is computing information about its own growth. We consider it a form of basic "intelligence" from the perspective of information processing and decision-making.

In addition, this dissertation has found the prospects of sequential logic design with the bcTAM that can remember previous state information, described in chapter 4. A flip flop is designed with the circuit tile assembly system that can stay in the previous logic state, where logic state 1 means node potential is greater than the threshold and logic state 0 indicates less than the threshold voltage. This study explores the scope of the bcTAM as a memory device, which would be a powerful tool for bottom-up fabrication in nanotechnology. Therefore, built with basic circuit components, these models have seemingly advanced capacities, such as self-assembly, self-controlled growth, self-replication, Boolean computation, and storing information.

1.5 List of Publications

1. **Yasmin, R.**, & Deaton, R. (2021). Logical Computation with Self-Assembling Electric Circuits. Under Review.

2. **Yasmin, R.**, Garzon, M., & Deaton, R. (2020). Model for self-replicating, self-assembling electric circuits with self-controlled growth. Physical Review Research, 2(3), 033165.

3. Deaton, R., Garzon, M.,**Yasmin, R.**, & Moore, T. (2020). A model for self-assembling circuits with voltage-controlled growth. International Journal of Circuit Theory and Applications, 48(7), 1017-1031.

4. Deaton, R., **Yasmin, R.**, Moore, T., & Garzon, M. (2017, June). Self-assembled DC resistive circuits with self-controlled voltage-based growth. In International Conference on Unconventional Computation and Natural Computation (pp. 129-143). Springer, Cham.

5. **Yasmin, R.**, & Deaton, R. (2021). A Memory Cell with Self-assembling Electric Circuits. Manuscript in preparation.

6. Garzon, M., Moore, T., Deaton, R., & **Yasmin, R.** (2021). Computational Power and Complexity of Self- Assembling Resistive Electric Ladders. Manuscript in preparation.

7. Deaton, R., Garzon, M., & **Yasmin, R.** (2021). Computation of non-neural bioelectric networks with self-assembling electric circuit. Manuscript in preparation.

Chapter 2

A Model for Self-Replicating, Self-Assembling Electric Circuits with Self-Controlled Growth

2.1 Introduction

Understanding the origin of living systems requires answers to fundamental scientific questions [60, 68, 69], such as the origin and nature of how they employ the mechanism of self-assembled, self-controlled growth to self-replicate themselves. In self-assembly [70], components construct larger, more capable systems through localized interactions. Examples in living systems are amino acids and proteins, lipids and membranes, and cells and higher organisms. As a technology, molecular self-assembly is an ongoing topic of research [71], and has primarily been applied to the growth of nanostructures. Algorithmic assembly controls growth through programmed interactions between component parts, which are represented as matching glues that, for example, have been implemented with complementary DNA oligonucleotides [8, 21]. Self-control limits the growth of living systems with mechanisms contained within the components themselves, as well as interactions with the environment. Biological growth from proteins to higher organisms requires a source of energy to sustain. For example, bacterial colonies are limited by their nutrient supply, and as nutrition has improved, human beings have become larger.

Here, self-replication is defined as a process in which an individual senses a mature stage in its development that triggers the growth of a copy of itself. For example, in eukaryotes, signaling pathways initiate mitosis, which is a process in which two or more daughter cells are produced by cell division from an identical parent. Von Neumann pioneered computational, artificial self-replicating systems in the 1940s, and proposed an abstract machine that has the power of replication in cellular automata [60, 61]. Moreover, a self-replicating molecular assembler has been a dream of nanoscale engineering [72]. In molecular biology, focus has been on

self-replicating systems of RNA, DNA, or proteins, with the most prominent being the RNA world hypothesis [73].

In this chapter, we propose a replicating circuit tile assembly model (rcTAM) that combines self-assembly and self-replication in a nonbiological system, where the self-assembly of ladder circuits from resistive circuit tiles is controlled by a voltage source whose consumption during growth controls the extent and shape of the resulting structures. In rcTAM, a growing circuit senses when growth has reached its limit, and in response, initiates growth of a new circuit identical to itself. Moreover, all of these capabilities are achieved in relatively simple resistive circuits with diodes and voltage sources, without an appeal to molecular biology, or even organic chemistry. On the supposition that living matter self-assembled from non-living components [69, 74] (abiogenesis), many models have focused on the transition from inorganic to organic molecules. Thus, the rcTAM models a system in which many of the basic characteristics of life at the molecular level are captured (self-assembly, self-control, self-replication), and which could be leveraged for enhanced capabilities of man-made technologies and new insights into how self-replicating systems might arise.

Though the rcTAM is not a biological system, it might be a useful abstraction of bioelectric networks among somatic cells that interact with genetic mechanisms to guide pattern and shape formation, including morphogenesis, embryogenesis, tissue regeneration, and regulation of cellular abnormalities [41, 42, 45–47]. Endogenous electric fields and the consequent distribution of electric potentials arise from the distribution of action potentials across cell membranes and gap junctions between cells. These bioelectric networks are ancient mechanisms to control anatomy [41]. Control over pattern and form is established through rapid feedback mechanisms that are characteristic of electrical systems [41, 42, 47]. Likewise, the rcTAM attempts to model ancient mechanisms with primitive electrical components with a threshold

mechanism, as in ion channels or gap junctions. In the preceding circuit tile assembly model (cTAM) [11], the goal was to control pattern formation with the shape of a potential distribution established by a voltage source and boundary conditions. The current state (growing or terminated) of an assembly was communicated instantaneously throughout the circuit by changes in current and voltage. Electric fields in gap junctions transport materials between cells [75], and cTAMs model this type of electrochemical growth phenomenon [11]. The advantage of the cTAM models is that they are amenable to exact analysis and characterization of their properties, and thus, from a theoretical perspective, might produce better understanding of information processing in bioelectric phenomena.

The cTAM in [10, 52, 53] consisted of resistive circuits and voltage sources, and only achieved self-assembled and self-controlled growth. Here, it is augmented with diodes and dependent voltage sources to achieve self-replication. The goal has been to achieve the desired functionality with circuits that are as simple as possible. In Section 2.2, the rcTAM model is defined. In Section 2.3 the self-replicative property of the rcTAM model is demonstrated. In addition, a bound on the maximum length of the assembly is derived, and an aging mechanism is addressed. Finally, some discussion of possible applications and concluding remarks are given in section 2.4.

2.2 A Self-Replicating cTAM (rcTAM)

In the circuit tile assembly model cTAM [10, 52, 53], larger circuits are self-assembled from smaller unit circuits, called circuit tiles. Combining chemically-inspired glues and resistive electrical circuits, circuit tiles attach if the glues match at the attachment points and the voltage drop across the attachment points equals or exceeds a certain threshold τ. As the voltage at attachment points is dissipated by resistive voltage dividers with each new tile addition, growth eventually ceases at a maximum size, and thus, is self-controlled. The rcTAM augments the

capabilities of the cTAM by adding diodes and dependent voltage sources to achieve self-replication.

Definition 2.2.1 (rcTAM Circuit)**.** A rcTAM circuit is a tuple $\Psi = (N, E, C, g, \partial N)$ on a graph (N, E) where N denotes the set of nodes, corresponding to electrical nodes in the circuit, E denotes the set of edges, C is a set of circuit components (chosen from resistors, diodes and voltage sources) assigned to edges $e_{(i,j)} \in E$ where $\{i, j\} \in N$, and g maps some subset of nodes ∂N to some subset of glues labeled from a finite alphabet Σ, *i.e.* $g : \partial N \to \Sigma$. $\partial N = N_{in} \cup N_{out}$ consists of two finite subsets of nodes, input nodes N_{in} and output nodes N_{out} to the circuit, and are the points at which glues bind tiles together on the boundary of the circuit.

The rcTAM tiles (rcTiles) are small rcTAM circuits, and represent the most primitive, singleton circuits from which all others are assembled. Each rcTile contains a voltage divider made of resistors, as well as voltage sources and diodes. A diode is an electrical device that functions as a switch. In an ideal diode, if the voltage across it is greater than or equal to a threshold V_{thr}, then it is *forward biased* and the diode acts as a perfect conductor, or short circuit with zero resistance to current flow. Otherwise, it is *reverse biased* and behaves as a perfect insulator, or open circuit with infinite resistance to current flow.

Definition 2.2.2 (rcTAM Tile Assembly System (rcTAM))**.** A *replicating circuit Tile Assembly system* (rcTAM) is a tuple $\mathcal{C} = (\Gamma, S, \tau, \nu, \zeta)$, where Γ is a finite set of rcTiles, $S \subset \Gamma$ is a set of seed rcTiles, $\tau \in \mathbb{R}_+$ is the threshold voltage that sets one of the criteria for further attachment, and $\nu \in \mathbb{R}_+$ is the electric node potential in the circuit. ζ is a glue indicator function that indicates whether glues on input nodes of rcTiles match or bind to glues on output nodes of rcTAM circuits, or $\zeta : \Gamma(N_{in}) \times \Gamma(N_{out}) \to \{0, 1\}$.

In the rcTAM, an assembly is a sequence of resistive electrical ladders that are

connected, but electrically isolated from each other. Each ladder is obtained from the previous or an initial seed tile by attachment of rcTiles.

A ladder that has finished growth through addition of rcTiles has reached “adulthood," and has a certain number t of tiles. An index $k \in \{1, \ldots, nt, \ldots\}$, indicates a specific tile in the ladder assembly, as well as a time step, where n is the number of adult ladders in the current assembly. The current tile in the ladder that offers a glue for attachment (current last tile added to an assembly) is denoted k_τ, and the voltage drop between its output nodes is the “tip" voltage of the circuit. Once started, the assembly does not stop as long as conditions for attachment are met. Because any replication process that terminates after a finite number of steps would lead to eventual extinction of that species, a prerequisite to a viable self-replication process would be one that is theoretically capable of running forever, as the rcTAM.

Voltages (potential differences between nodes) and currents in the ladder are a function of the location k and tile parameters. Thus, voltages will be denoted as $\mathrm{V}^{\gamma}_{(i,j)}(k)$, where the first node i in an edge refers to the more positive potential for a particular rcTile $\gamma \in \Gamma$. The tip voltage at the current last tile in the ladder, where a new tile attachment is determined, is denoted $\mathrm{V}^{\gamma}_{(i,j)}(k_\tau)$. (The indices γ and k may be omitted when the location of the tile in the ladder is clear.) In general, two nodes $\{i, j\} \in N_{out}$ of an rcTAM circuit ψ_1 can attach to two nodes $\{l, m\} \in N_{in}$ of an rcTile circuit ψ_2 if $\zeta(\psi_1(i), \psi_2(l)) = 1$ and $\zeta(\psi_1(j), \psi_1(m)) = 1$, and either $\mathrm{V}^{\gamma}_{(i,j)}(k_\tau) = \nu(i) - \nu(j) \geq \tau$ or $\mathrm{V}^{\gamma}_{(l,m)} = \nu(l) - \nu(m) \geq \tau$, where $\mathrm{V}_{(l,m)}$ is a voltage across input nodes in a single rcTile (*i.e.* not yet part of a ladder). Ideally, growth is restricted to input nodes of rcTiles attaching to output nodes of a larger, growing rcTAM circuit. Once attached, a given input node and given output node become one node electrically, though the distinct node numbers associated with the attaching rcTiles will be retained.

If life is taken as the prototypical self-replicating system, then, one usually

thinks of a living entity as one that grows by consuming resources from the environment, produces signals indicating that it has reached maturity and is capable of reproduction, and then, engages in processes that result in close facsimiles of itself as offspring. The rcTAM has been designed with this in mind.

Definition 2.2.3 (Self-Replication)**.** A self-replicating rcTAM grows to a maximum size, senses that this specific stage in its growth has occurred, and in response, initiates a new process to grow another identical assembly.

To exhibit self-replication in an rcTAM, three rcTiles will be defined. For clarity, matching glues are denoted like DNA Watson-Crick complementary oligonucleotides, so that a glue a matches its complement $\overline{a}$. In addition, node numbers are referenced to specific, individual rcTiles, and not the entire, growing assembly.

Once the adult ladder has replicated, the tile numbering (k) continues on at the seed for the new, replicated ladder. Tile A is the seed tile for the assembly process. There is only one per assembly at position $k = 1$. It consists of one independent voltage source ($\nu_0 = V^A_{(1,0)}(1)$) on $e_{(1,0)}$, and two resistors with R on $e_{(1,2)}$ and αR on $e_{(2,0)}$ (Figure 2.1). This configuration acts as a voltage divider circuit where the voltage drop across R, $\mathrm{V}^A_{(1,2)}(1) = \nu_0 \frac{R}{R+\alpha R} = \nu_0 \frac{1}{1+\alpha}$. Tile A has output nodes $\{1, 2\}$ across resistor R, whose voltage difference $\mathrm{V}^A_{(1,2)}(1)$ is compared to the threshold τ to determine eligibility for further growth. Tile A has glues $g(1) = a$ and $g(2) = b$.

Tile B serves as the seed for replicated ladders, and is at position $k = nt + 1$ after n rounds of replication. Tile B has the same value for its voltage source $\mathrm{V}^B_{(4,3)}(nt + 1) = \nu_0$ as Tile A, with resistor R on $e_{(1,2)}$, αR on $e_{(1,4)}$, and ideal diode D_6 on $e_{(3,2)}$ with $V_{thr} = 0$. The diode is connected such that it is reverse biased and acts as an open circuit (Figure 2.2). The polarity of the voltage across this open circuit is opposite to that required for attachment to Tile C at nodes $\{3, 4\}$. It has one pair of output nodes $\{1, 2\}$ across the resistor R, and one pair of input nodes $\{3, 2\}$ across the diode D_6. Because D_6 is open circuited, $\mathrm{V}^B_{(1,2)}$ is zero, and hence, it is not eligible

for attachment. Tile B has glues $g(2) = \{b, \overline{d}\}$ (two glues attached), $g(3) = \overline{c}$, and $g(1) = a$.

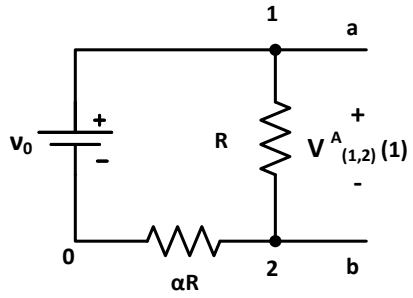


Fig. 2.1: Tile A (Seed Tile) for the rcTAM consisting of one dc voltage source ν_0 and two resistors, R and αR. It has one pair of output nodes $\{1, 2\}$ across the resistor R. Node 1 has glue a and Node 2 has glue b.

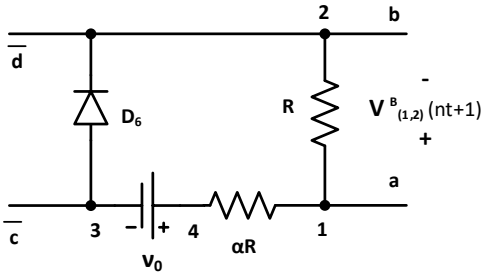


Fig. 2.2: Tile B (Replicating Seed Tile) for the rcTAM. It has a voltage source of ν_0, resistors R and αR, and an ideal diode D_6. It has one output node pair $\{1, 2\}$ across R and one input node pair $\{3, 2\}$ across D_6. Node 1 has glue a, node 2 has glues (b and $\overline{d}$), and node 3 has glue $\overline{c}$.

Tile C is the primary tile that contributes to growth of a ladder and determines whether replication occurs. Tile C consists of one dependent voltage source V_x on $e_{(6,2)}$, three resistors with R on $e_{(1,2)}$, αR on $e_{(2,7)}$, and βR ($\beta >> 0$) on $e_{(1,5)}$, and five diodes (D_3 on $e_{(3,4)}$, D_1 on $e_{(6,5)}$, D_2 on $e_{(1,4)}$, D_4 on $e_{(5,3)}$, and D_5 on $e_{(4,3)}$, parallel to D_3), as shown in Figure 2.3. Here, the dependent voltage source, $V_x = \frac{2\tau\nu_0}{\nu_0} = 2\tau$ is activated only when connected to a circuit with ν_0 (Tile A or B). This tile has two pairs of output nodes $\{1, 2\}$ and $\{3, 4\}$, one pair of input nodes $\{1, 7\}$ and has $g(1) = \{a, \overline{a}\}$, $g(2) = b$, $g(3) = c$, $g(4) = d$, and $g(7) = \overline{b}$. The voltage $\mathrm{V}^C_{(1,2)}(k)$ depends on voltage division between R and αR. Resistor βR has a large value so that V_x has a minimal impact of $V_x \frac{1}{1+\beta}$ on $\mathrm{V}^C_{(1,2)}(k)$, and thus, on growth. Four diodes are connected across resistor βR. Diode D_2 and diode D_4 electrically isolate a replicated assembly from current in resistor βR, and *vice versa*. Diode D_3 and D_5 are connected in parallel with opposite polarity between nodes 3 and node 4. All diodes except D_3 have $V_{thr} = 0$. Diode D_3 has $V_{thr} = 2\tau$, so that it is an open circuit throughout the growth process,

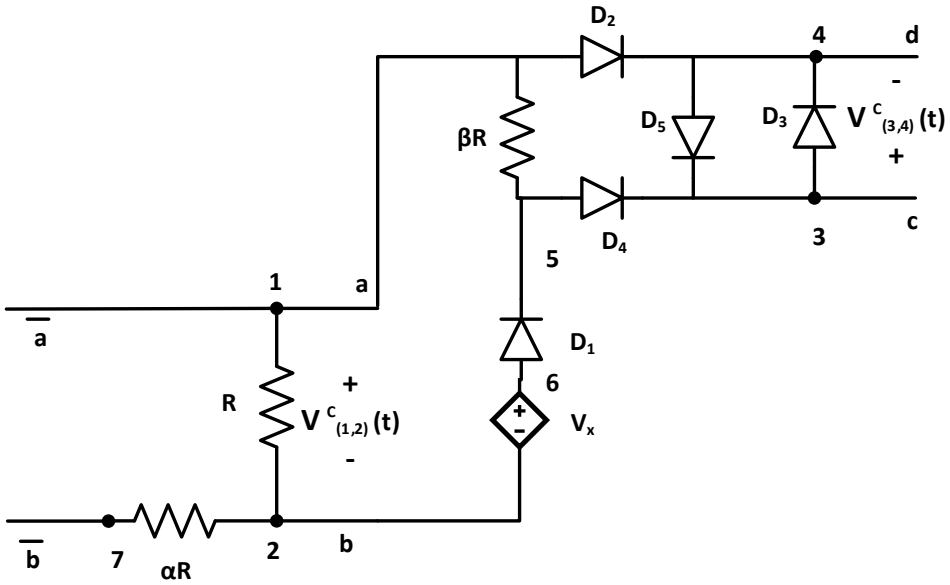


Fig. 2.3: Tile C (Circuit Tile) for the rcTAM consisting of three resistors R, αR, and βR. Diode D_3 has $V_{thr} = 2\tau$, and D_1, D_2, D_4, D_5 have $V_{thr} = 0$. It has two pairs of output nodes at $\{1, 2\}$ and $\{3, 4\}$. The input node pair is $\{1, 7\}$. Node 1 has two glues:(a and $\overline{a}$). Node 2, Node 3, Node 4, and node 7 have glues b, c, d, and $\overline{b}$, respectively.

with a voltage $\mathrm{V}^C_{(3,4)}(k)$ equal to that across resistor βR. When replication occurs, diode D_5 completes the open loop connection across diode D_6 of tile B so that current can flow. $\mathrm{V}^C_{(3,4)}$ thus determines whether replication will occur or not.

2.3 Self-Replication

The rcTAM has two types of tile attachments, one for *regular growth* and another for *replication*. The desired behavior of the assembly process is shown in Figure 2.4. Assume the system has one seed tile A, multiple tiles B, and multiple tiles C.

As will be shown later, unwanted attachments between tiles that are not connected to a seeded ladder assembly do not occur. For regular growth, we must have $\mathrm{V}^A_{(1,2)}(1) \geq \tau$ for tile A.

Tile C attaches to tile A. As long as $\mathrm{V}^C_{(1,2)}(k) \geq \tau$, $k \geq 2$, growth of the ladder proceeds with tile C attaching to tip tile C in the ladder. Eventually, as ν_0 is dissipated by the voltage divider in the ladder, $\mathrm{V}^C_{(1,2)}(k) < \tau$ (for example $k = t = 3$) for the last

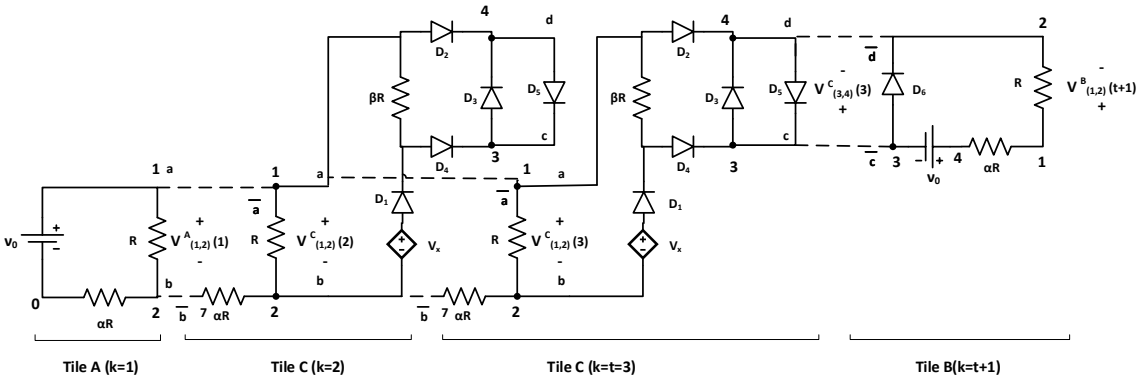


Fig. 2.4: Example of an assembly process. Here, An assembly starts from the seed tile A, and then, two tile C's are attached to the seeded growth. As $\mathrm{V}^C_{(1,2)}(3)$ falls below τ, a tile B is attached to start replication. Attachments between tiles are shown as dashed lines.

tile C in the ladder (Figure 2.4). At this point, as will be shown below, with a proper choice of V_x, α, and β, V_x will forward bias D_1 and drop enough voltage across βR so that $\mathrm{V}^C_{(3,4)}(t = 3) \geq \tau$.

Tile B will then attach at nodes $\{3, 4\}$ of tile C, causing D_5 to become forward biased, providing a conducting path so that current flows through R in tile B and thus growth of a new ladder starts. Diodes D_2 and D_4 are ideal diodes that are used to isolate the parent circuit from the child circuit. Thus, for replication to occur, the circuit needs to undergo a conformation change from an open circuit to a closed circuit. In summary, when $\mathrm{V}^C_{(1,2)}(k_\tau) \geq \tau$, then $\mathrm{V}^C_{(3,4)}(k_\tau) < \tau$ and only regular growth occurs. When $\mathrm{V}^C_{(1,2)}(t) < \tau$, then $\mathrm{V}^C_{(3,4)}(t) \geq \tau$, and replication growth occurs, only once per parent ladder assembly.

The ideal growth regions are depicted in Figure 2.5. To summarize: when $\mathrm{V}^C_{(1,2)}(k_\tau) \geq \tau$, then regular growth occurs where $\mathrm{V}^C_{(3,4)}(k_\tau) < \tau$, when $\mathrm{V}^C_{(1,2)}(k_\tau) < \tau$, $\mathrm{V}^C_{(3,4)}(k_\tau) \geq \tau$ and replication growth occurs, and when $\mathrm{V}^C_{(1,2)}(k_\tau) > 2\tau$, the diode D_1 is reverse biased and in turn, $\mathrm{V}^C_{(3,4)}(k_\tau) = 0$. Moreover, replication occurs only once at the maximum size of the ladder, t.

The goal of this section is to prove the following Theorem in several stages.

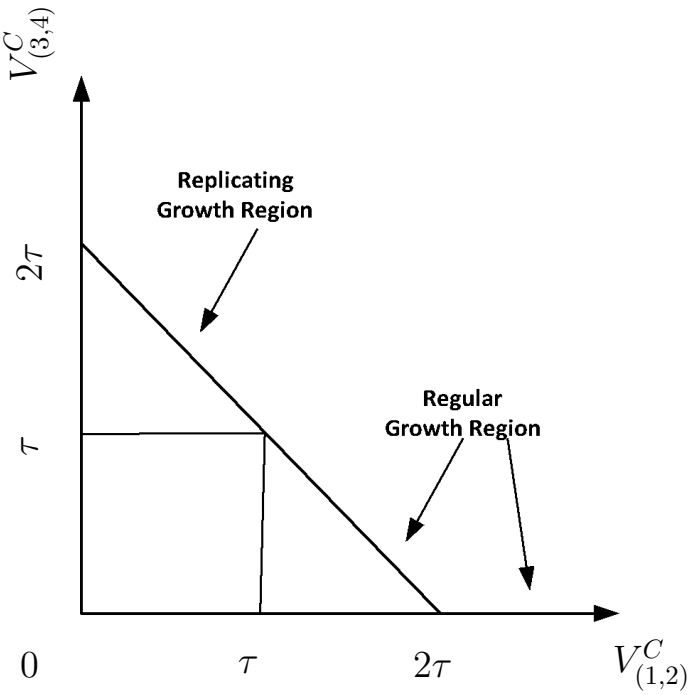


Fig. 2.5: The regions for regular growth and replication. When$\mathrm{V}^C_{(1,2)}(k_\tau) \geq \tau$, regular growth occurs as $\mathrm{V}^C_{(3,4)}(k_\tau) < \tau$. When $\mathrm{V}^C_{(1,2)}(k_\tau) < \tau$, $\mathrm{V}^C_{(3,4)}(k_\tau) \geq \tau$ and self-assembly starts replication.

Theorem 2.3.1. *There exists an infinite number of rcTAM systems exhibiting self-controlled regular growth, followed by replication in which this cycle repeats infinitely often.*

As mentioned above, for the self-replication process to proceed as desired, certain attachments must be prevented, as described next.

Lemma 2.3.1.1. *Only attachments between rcTiles and a seeded ladder assembly (one containing tile A) are possible.*

Proof. If tile C is not attached to a seeded assembly, because V_x is a source dependent on being in a circuit connected to ν_0, $\mathrm{V}^C_{(1,2)}(k) = 0 < \tau$ and $\mathrm{V}^C_{(3,4)}(k) = 0 < \tau$, and no attachments can occur between two unseeded Tile C. Unless tile B is part of a circuit with tile A, D_6 is reverse biased and an open circuit, and no current flows in R. Thus, $\mathrm{V}^B_{(1,2)}(k) = 0 < \tau$, and no attachments occur

between tile B and C. In addition, the polarity of $\mathrm{V}_{(3,2)}$ in tile B is opposite to that required for attachment to nodes $\{3, 4\}$ of tile C. □

Lemma 2.3.1.2. *If $\nu_0/(1+\alpha) \geq \tau$, at least one tile C attaches to tile A.*

Proof. For minimal growth, at least one tile C should attach to seed tile A. Therefore tile A must satisfy $\mathrm{V}^A_{(1,2)}(1) \geq \tau$. According to Kirchoff's Voltage Law (KVL) [76] for the seed tile A ($k = 1$, Figure 2.1),

$$\nu_0 = \mathrm{V}^A_{(1,2)} + \mathrm{V}^A_{(2,0)}. \tag{2.1}$$

Using Ohm's Law $\mathrm{V}^A_{(1,2)} = IR$ [76], where I is the current, in expression (2.1) yields

$$\begin{aligned} \nu_0 &= IR + \alpha IR, \\ \nu_0 &= \mathrm{V}^A_{(1,2)} + \alpha \mathrm{V}^A_{(1,2)}. \end{aligned}$$

Thus, $\mathrm{V}^A_{(1,2)} = \nu_0/(1+\alpha)$ and tile C can attach to the seed. □

To ensure regular growth and replication, a suitable value of V_x needs to be determined.

Lemma 2.3.1.3. *If $V_x = 2\tau$ and $V^C_{(1,2)}(k) < \tau$, then $V^C_{(3,4)}(k) > \tau$.*

Proof. If $\mathrm{V}^C_{(1,2)}(k) < \tau$, then, regular growth has ceased. Since $V_x = 2\tau > \mathrm{V}^C_{(1,2)}(k)$, D_1 is forward biased ($V_{D_1} = 0$.) Applying KVL [76] to the loop $(V_x, D_1, \beta R, R)$ yields

$$\begin{aligned} V_x - V_{D_1} - V_{\beta R} - V_R &= 0, \\ V_x - 0 - \mathrm{V}^C_{(3,4)} - \mathrm{V}^C_{(1,2)} &= 0, \\ \mathrm{V}^C_{(3,4)} &= V_x - \mathrm{V}^C_{(1,2)}. \end{aligned}$$

Since $V_x = 2\tau$, then

$$\mathrm{V}^C_{(3,4)}(k) = 2\tau - \mathrm{V}^C_{(1,2)}(k), \tag{2.2}$$

Now $\mathrm{V}^C_{(1,2)}(k) < \tau$ gives the conclusion $\mathrm{V}^C_{(3,4)}(k) > \tau$. □

Lemma 2.3.1.4. *If $V_x = 2\tau$ and $V^C_{(1,2)}(k) > 2\tau$, then $V^C_{(3,4)}(k) < \tau$.*

Proof. Since $\mathrm{V}^C_{(1,2)}(k) > V_x = 2\tau$, D_1 is reverse biased, no current flows through βR and $\mathrm{V}^C_{(3,4)}(k) = 0 < \tau$. □

Lemma 2.3.1.5. *If $V_x = 2\tau$ and $\tau < V^C_{(1,2)}(k) \leq 2\tau$, then $V^C_{(3,4)}(k) < \tau$.*

Proof. Since $\tau < \mathrm{V}^C_{(1,2)}(k) \leq V_x = 2\tau$, D_1 is forward biased and current flows in βR, hence $\mathrm{V}^C_{(3,4)}(k) \neq 0$. Again, substituting in $\tau < \mathrm{V}^C_{(1,2)}(k) \leq 2\tau$ into equality (2.2) above gives

$$0 \leq \mathrm{V}^C_{(3,4)}(k) < \tau,$$

where $\mathrm{V}^C_{(3,4)}(k) = 0$ when $\mathrm{V}^C_{(1,2)}(k) = 2\tau$. In this case, D_1 is forward biased, but no current flows in βR. □

Lemma 2.3.1.6. *If $V_x = 2\tau$ and $V^C_{(1,2)}(k) = \tau$, then $V^C_{(3,4)}(k) = \tau$.*

Proof. Since $\mathrm{V}^C_{(1,2)}(k) = \tau < V_x$, D_1 is forward biased, current flows through βR and $\mathrm{V}^C_{(3,4)}(k) \neq 0$. Substituting in $\mathrm{V}^C_{(1,2)}(k) = \tau$ into Expression (2.2), gives

$$\mathrm{V}^C_{(3,4)}(k) = \tau.$$

□

Lemmas 2.3.1.3-2.3.1.6 altogther imply that the desired behavior of the rcTAM is obtained, except when $\mathrm{V}^C_{(1,2)}(k) = \tau$ (Lemma 2.3.1.6). In that case, undesirably, both regular growth and replication will occur. Therefore, the model parameters should be chosen such that $\mathrm{V}^C_{(1,2)}(k) \neq \tau$ for all k. Moreover, when $\tau \leq \mathrm{V}^C_{(1,2)}(k) \leq 2\tau$, diode D_1 is forward biased and it creates a closed loop among $V_x, D_1, \beta R$ and R that would inject an additional current $I_d = 2\tau/(R + \beta R)$ into R. Depending on the value of resistor αR, there could be several loops where diode D_1 is forward biased, and these

additional I_d currents could influence the final size of the ladder assembly. Finally, since tiles are added in parallel to previous tiles, the equivalent resistance between nodes $\{1, 2\}$ could decrease according to Rayleigh's Monotonicity Law [77], which could cause $\mathrm{V}_{(1,2)}$ to decrease below τ as more tiles attach. These potential problems, however, can be avoided if we chose α such that the voltage in the last two tiles added, $\mathrm{V}^C_{(1,2)}(nt)$ and $\mathrm{V}^C_{(1,2)}(nt-1)$, go from at least $\geq 2\tau$ to under τ with the attachment of one tile. Therefore, for a ladder assembly of length t, the goal is to find some combination of ν_0, τ, and α such that $\mathrm{V}^C_{(1,2)}(nt) < \tau$ for the last tile, and $\mathrm{V}^C_{(1,2)}(nt-1) \geq 2\tau$ for the next to last tile. In that case, current would only flow in βR, producing a $\mathrm{V}^C_{(3,4)}(k) \neq 0$ for only the last tile at position nt. This also assures that only the last tile in an adult ladder at nt will have $\mathrm{V}^C_{(1,2)}(k) < \tau$.

An exact equation for the potential distribution of a one-dimensional ladder has been derived in [52] as,

$$V^C_{(1,2)}(nt) = \frac{\nu_0(-1)^{nt}}{A_{nt} + A_{nt-1}} = \frac{\nu_0}{|A_{nt} + A_{nt-1}|} \geq 0 \tag{2.3}$$

$$V^C_{(1,2)}(k) = \nu_0(-1)^k A_{k-1} \sum_{j=0}^{nt-k} \frac{1}{A_{k+j-1}A_{k+j}} \geq 0 \tag{2.4}$$

for every node $1 \leq k < nt$, where $A_k = \frac{\rho^{2k+2}-1}{\rho^k(\rho^2-1)}$ and $\rho = \frac{-\left(2+\alpha+\sqrt{\alpha(\alpha+4)}\right)}{2} < -2$ for $\alpha > 0$.

Lemma 2.3.1.7. *For a ladder assembly of size $t > 0$, there exists ν_0, τ and $\alpha > 0$ such that*

$V^C_{(1,2)}(nt-1) \geq 2\tau$ *and* $V^C_{(1,2)}(nt) < \tau$.

Proof. Using expression (2.3) for the last tile, the desired condition is equivalent to

$$\begin{aligned} \mathrm{V}^{C}_{(1,2)}(nt) &< \tau, \\ \frac{\nu_0(-1)^{nt}}{A_{nt} + A_{nt-1}} &< \tau, \\ |A_{nt} + A_{nt-1}| &> \frac{\nu_0}{\tau}. \end{aligned}$$

The value of $|A_{nt} + A_{nt-1}|$ is:

$$\begin{aligned} |A_{nt} + A_{nt-1}| &= \left| \frac{\rho^{2nt+2} - 1}{\rho^{nt}(\rho^2 - 1)} + \frac{\rho^{2nt} - 1}{\rho^{nt-1}(\rho^2 - 1)} \right|, \\ &= \left| \frac{\rho^{2nt+1}(1+\rho) - (1+\rho)}{\rho^{nt}(\rho^2 - 1)} \right|, \\ &= \left| \frac{(\rho^{2nt+1} - 1)(1+\rho)}{\rho^{nt}(1+\rho)(\rho - 1)} \right|, \\ &= \left| \frac{(\rho^{2nt+1} - 1)}{\rho^{nt}(\rho - 1)} \right|, \\ |A_{nt} + A_{nt-1}| &= \left| \frac{\rho^{nt+1}}{\rho - 1} - \frac{1}{\rho^{nt}(\rho - 1)} \right| > \frac{\nu_0}{\tau}. \end{aligned}$$

Therefore, it suffices to ensure that

$$\left| \frac{\rho^{nt+1}}{\rho - 1} \right| > \frac{\nu_0}{\tau}. \tag{2.5}$$

Next, further constraints for the condition $\mathrm{V}^{C}_{(1,2)}(nt-1) \geq 2\tau$ are determined. According to Rayleigh's monotonicity principle, voltages only decrease as the ladder grows, which guarantees that $\mathrm{V}^{C}_{(1,2)}((nt-1)_\tau) \geq 2\tau$. $\mathrm{V}^{C}_{(1,2)}(nt-1)$ can be calculated

using expression (2.4),

$$\begin{aligned} \mathrm{V}^{C}_{(1,2)}(nt-1) &\geq 2\tau, \\ \nu_0(-1)^{nt-1}A_{nt-2}\left[\frac{1}{A_{nt-2}A_{nt-1}}+\frac{1}{A_{nt-1}A_{nt}}\right] &\geq 2\tau, \\ \nu_0(-1)^{nt-1}\left[\frac{A_{nt}+A_{nt-2}}{A_{nt}A_{nt-1}}\right] &\geq 2\tau. \end{aligned}$$

Since

$$\begin{aligned} A_{nt}+A_{nt-2} &= \frac{\rho^{2nt+2}-1}{\rho^{nt}(\rho^2-1)}+\frac{\rho^{2nt-2}-1}{\rho^{nt-2}(\rho^2-1)}, \\ &= \frac{\rho^{2nt+2}-1+\rho^{2nt}-\rho^2}{\rho^{nt}(\rho^2-1)}, \\ &= \frac{(\rho^{2nt}-1)(1+\rho^2)}{\rho^{nt}(\rho^2-1)}, \end{aligned}$$

and

$$A_{nt}.A_{nt-1} = \left[\frac{\rho^{2nt+2}-1}{\rho^{nt}(\rho^2-1)}\right]\times\left[\frac{\rho^{2nt}-1}{\rho^{nt-1}(\rho^2-1)}\right],$$

the bracket in the inequality (2.7) can be reduced to

$$\frac{A_{nt}+A_{nt-2}}{A_{nt}.A_{nt-1}} = \frac{(\rho^4-1)(\rho^{nt-1})}{\rho^{2nt+2}-1},$$

where, $\rho = \frac{-\left(2+\alpha+\sqrt{\alpha(\alpha+4)}\right)}{2}$.

Further, since $\rho^{2nt+2} >> 1$, a sufficient condition for the second inequality can be further simplified (by ignoring the -1 in the denominator) to

$$\nu_0(-1)^{nt-1}\left[\frac{(\rho^4-1)(\rho^{nt-1})}{\rho^{2nt+2}}\right] \geq 2\tau. \tag{2.6}$$

From [52], $\rho < -2$ and ρ^4 is a positive number. The value of nt is odd if and only if both n and t are odd numbers. Otherwise, nt is an even number. Therefore,

there are two cases to consider for the length of the ladder nt: even or odd. If nt is odd, $(-1)^{nt-1} = +1$, ρ^{nt-1} is a positive number, and ρ^{2nt+2} is also positive. So, $\frac{(-1)^{nt-1}(\rho^4-1)(\rho^{nt-1})}{\rho^{2nt+2}}$ is a positive number. On the other hand, if nt is even, $(-1)^{nt-1} = -1$, ρ^{nt-1} is a negative number, and their product in the numerator is positive. Moreover, ρ^{2nt+2} is a positive value. Therefore, $\frac{(-1)^{nt-1}(\rho^4-1)(\rho^{nt-1})}{\rho^{2nt+2}}$ is a positive number.

Therefore, inequality (2.6) is equivalent to the following inequalities:

$$\begin{aligned}
\nu_0(|\rho|^4 - 1)\frac{|\rho^{nt-1}|}{|\rho^{2nt+2}|} &\geq 2\tau, \\
\frac{\nu_0}{2\tau}(|\rho|^4 - 1) &\geq \frac{|\rho^{2nt+2}|}{|\rho^{nt-1}|}, \\
|\rho|^{nt+3} &\leq \frac{\nu_0}{2\tau}(|\rho|^4 - 1),
\end{aligned}$$

and

$$\frac{|\rho|^{nt+3}}{|\rho|^4 - 1} \leq \frac{\nu_0}{2\tau}. \tag{2.7}$$

Combining inequalities (2.5) and (2.7), a sufficient condition for self-replication is thus

$$\frac{2|\rho|^{nt+3}}{|\rho|^4 - 1} \leq \frac{\nu_0}{\tau} < \left|\frac{\rho^{nt+1}}{\rho - 1}\right|. \tag{2.8}$$

Therefore, it suffices to ensure that

$$\frac{2|\rho|^{nt+3}}{|\rho|^4 - 1} < \left|\frac{\rho^{nt+1}}{\rho - 1}\right|, \tag{2.9}$$

so that there will exist a ρ that satisfies both inequalities (2.5) and (2.7) for a given $\frac{\nu_0}{\tau}$. This condition is readily equivalent to

$$0 < |\rho^4| - 2|\rho^3| + 2|\rho^2| - 1, \tag{2.10}$$

which is true for all $|\rho| > 2$, *i.e.*, there is no restriction on ρ. □

This argument completes the proof of Theorem 2.3.1.

The range of parameters afforded by condition 2.9, is illustrated in Figure 2.6 for $\nu_0 = 100$ and $\tau = 1$. Circuit simulations of $\mathrm{V}^C_{(1,2)}(k)$ using MATLAB-Simulink [78] show that for given $\alpha, \tau, \text{ and } \nu_0$ in the feasible region in Figure 2.6, the voltages $\mathrm{V}^C_{(1,2)}(nt-1) \geq 2\tau$ and $\mathrm{V}^C_{(1,2)}(nt) < \tau$. Therefore, appropriate input parameters can always be found so that $\mathrm{V}^C_{(1,2)}(k) \neq \tau$, for example, $\nu_0 = 100V$, $\tau = 1V$, and $\alpha = 4$.

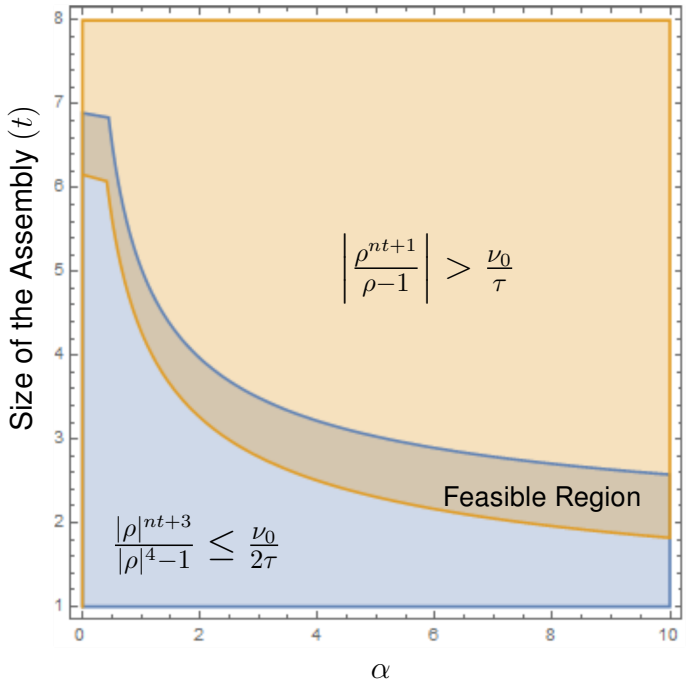


Fig. 2.6: Feasible region for inequalities (2.5) and (2.7) for $\nu_0 = 100$ and $\tau = 1$. The y-axis indicates the size of a terminal assembly and the x-axis indicates the value of α.

2.3.1 Bounded growth for the Ladders

The cTAM model exhibits self-assembly with instant cooperation and control on the size of the assembly [10], [52]. The maximum size depends on the voltage source (ν_0) of the seed tiles A and B, the threshold voltage (τ), and the ratio of the resistor values in the tileset, α. We can derive a similar bound for the rcTAM as shown next. In the rcTAM, because both seeds, Tile A and B, contain identical voltage sources and resistors, and each ladder is isolated from each other by reversed biased diodes, all copies of the ladder are equivalent. Therefore, the bound is proven for a single ladder.

Theorem 2.3.2. *The maximum length of the rcTAM ladder is bounded by*

$$B = \left\lceil \frac{\ln[\frac{\nu_0}{\tau}\frac{\beta}{\alpha+\beta+\alpha\beta}]}{\ln(1+\alpha)} + 1 \right\rceil. \tag{2.11}$$

Proof. The voltage supply ν_0 acts as a finite source of energy that is depleted as the circuit grows. The growth will stop when the $\mathrm{V}^C_{(1,2)}(t)$ drops below a pre-defined threshold value. Using some basic electrical engineering methods, such as Kirchoff's Voltage law [76], the maximum length t of a self-assembled ladder is bounded from above. To calculate the equivalent resistance, each circuit tile has resistor R is in series with another resistor αR and that combined resistance is in parallel with R of previous circuit tile. If diode D_1 is forward biased, then the resistor βR is in parallel with resistor R, whose equivalent resistance is denoted as γR where $\gamma = \frac{\beta}{1+\beta}$.
$\mathrm{V}^C_{(1,2)}(nt)$ can be calculated in terms of $\mathrm{V}^C_{(1,2)}(nt-1)$ as follows:

$$\mathrm{V}^C_{(1,2)}(nt) = \mathrm{V}^C_{(1,2)}(nt-1)\left(\frac{\gamma R}{\gamma R + \alpha R}\right) + \frac{2\tau R_{eq}(nt)}{R_{eq}(nt) + \beta R}, \tag{2.12}$$

where $R_{eq}(nt)$ is the equivalent resistance seen by the dependent source V_x from the rest of the ladder. Since $R > R_{eq}(nt)$, Equation 2.12 can be written as

$$\begin{aligned}
\mathrm{V}^C_{(1,2)}(nt) &< \mathrm{V}^C_{(1,2)}(nt-1)\left(\frac{\gamma R}{\gamma R + \alpha R}\right) + \frac{2\tau R}{(1+\beta)R}, \\
\mathrm{V}^C_{(1,2)}(nt) &< \mathrm{V}^C_{(1,2)}(nt-1)\left(\frac{\gamma}{\gamma + \alpha}\right) + \frac{2\tau}{1+\beta}.
\end{aligned}$$

By Lemma 2.3.1.7, only the last tile will have a forward biased D_1 diode. All other tiles' diodes will be reverse biased. Hence, resistor βR will not effect $\mathrm{V}^C_{(1,2)}(k)$ for

$(n-1)t+1 \leq k \leq (nt-1)$. Thus,

$$\mathrm{V}^{C}_{(1,2)}(nt-1) = \mathrm{V}^{C}_{(1,2)}(nt-2)\left(\frac{R_{eq}(nt-1)}{R_{eq}(nt-1)+\alpha R}\right),$$
$$\mathrm{V}^{C}_{(1,2)}(nt) = (\mathrm{V}^{C}_{(1,2)}(nt-2))\left(\frac{R_{eq}(nt-1)}{R_{eq}(nt-1)+\alpha R}\right)\left(\frac{\gamma}{\gamma+\alpha}\right)+\frac{2\tau}{1+\beta},$$

where $R_{eq}(nt-1)$ indicates the equivalent resistance at tile position $(nt-1)$. Since $R_{eq}(nt-1) < R$ for any tile $k < nt$ because of the parallel combination of resistors, then, substituting $R_{eq} = R$ preserves the bound,

$$\mathrm{V}^{C}_{(1,2)}(nt) < \left(\mathrm{V}^{C}_{(1,2)}(nt-2)\right)\left(\frac{1}{1+\alpha}\right)\left(\frac{\gamma}{\gamma+\alpha}\right)+\frac{2\tau}{1+\beta}. \tag{2.13}$$

Iterating the process recursively up to $k = (n-1)t+1$ yields

$$\mathrm{V}^{C}_{(1,2)}(nt) < \nu_0\left(\frac{1}{1+\alpha}\right)^{t-1}\left(\frac{\gamma}{\gamma+\alpha}\right)+\frac{2\tau}{1+\beta}. \tag{2.14}$$

Thus the growth will stop at a maximum size when $\mathrm{V}^{C}_{(1,2)}(nt) < \tau$, *i.e.* when the following equivalent inequalities hold:

$$\nu_0 \left(\frac{1}{1+\alpha}\right)^{t-1} \left(\frac{\gamma}{\gamma+\alpha}\right) + \frac{2\tau}{1+\beta} < \tau,$$
$$\nu_0 \left(\frac{1}{1+\alpha}\right)^{t-1} \left(\frac{\gamma}{\gamma+\alpha}\right) < \tau - \frac{2\tau}{1+\beta},$$
$$\left(\frac{1}{1+\alpha}\right)^{t-1} < \frac{\tau - \frac{2\tau}{1+\beta}}{\nu_0 \left(\frac{\gamma}{\alpha+\gamma}\right)},$$
$$(1+\alpha)^{t-1} > \frac{\nu_0 \left(\frac{\gamma}{\alpha+\gamma}\right)}{\tau \left(1 - \frac{2}{1+\beta}\right)},$$
$$(t-1)\ln(1+\alpha) > \ln \left[\frac{\nu_0 \left(\frac{\gamma}{\alpha+\gamma}\right)}{\tau \left(1 - \frac{2}{1+\beta}\right)}\right],$$
$$t > \frac{\ln \left[\frac{\nu_0\left(\frac{\gamma}{\alpha+\gamma}\right)}{\tau\left(1-\frac{2}{1+\beta}\right)}\right]}{\ln(1+\alpha)} + 1,$$
$$t > \frac{\ln \left[\frac{\nu_0\left(\frac{\gamma}{\alpha+\gamma}\right)}{\tau\left(\frac{\beta-1}{\beta+1}\right)}\right]}{\ln(1+\alpha)} + 1,$$
$$t > \frac{\ln \left[\left(\frac{\nu_0}{\tau}\right)\left(\frac{\gamma}{\alpha+\gamma}\right)\left(\frac{\beta+1}{\beta-1}\right)\right]}{\ln(1+\alpha)} + 1.$$

Taking $\left(\frac{\beta+1}{\beta-1}\right) \approx 1$, the bound is preserved, and substituting $\frac{\gamma}{\alpha+\gamma} = \frac{\beta}{\alpha+\beta+\alpha\beta}$, then

$$t > \frac{\ln[(\frac{\nu_0}{\tau})(\frac{\beta}{\alpha+\beta+\alpha\beta})]}{\ln(1+\alpha)} + 1. \tag{2.15}$$

□

From Theorem 2.3.2, the effect of the additional circuit components to achieve replication is small (< 1), namely, an additive term $\left[\ln\left(\frac{\beta}{(\alpha+\beta+\alpha\beta}\right)\right]$. Figure 2.7 confirms the soundness of this bound. Here, the maximum size of a circuit tile assembly model is calculated both as the bound B in equation 2.11 and by using a

simulation on MATLAB-Simulink [78]. The same procedure was done for values of α equals to 1 and 2.

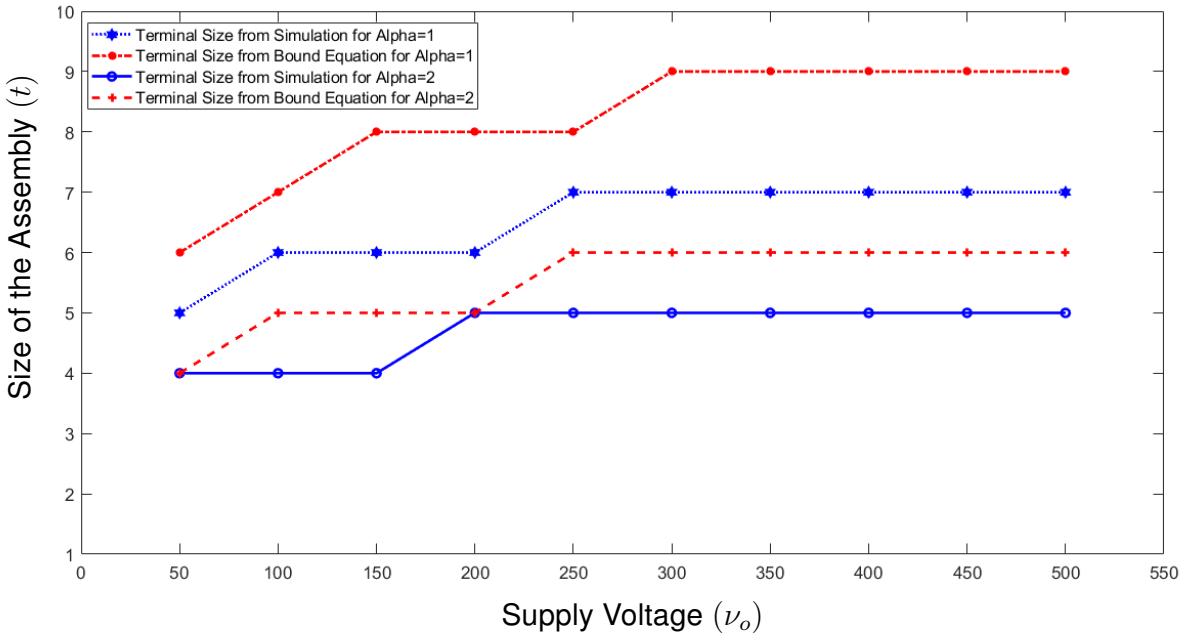


Fig. 2.7: Quality of the bound on ladder size for model parameters $\tau = 1$, $n = 1$, $\beta = 1000$. This plot confirms the validity of the bound and how tight it is for values of $\alpha = 1, 2$. The simulations of the circuits were done with MATLAB-SIMULINK.

Therefore, an rcTAM generates a circuit assembly system that is self-controlled and self-replicated with identical copies. For example, consider a terminal circuit configuration for input parameters $\nu_o = 50$, $\tau = 1$, $\alpha = 1$, and $\beta = 1000$. This circuit ladder grows up to length $t = 5$. Then $\mathrm{V}^C_{(1,2)}(5)$ falls below τ and $\mathrm{V}^C_{(3,4)}(5)$ becomes greater than τ. A tile B is attached to the $\mathrm{V}^C_{(3,4)}(5)$ node terminals and starts to replicate a copy of itself. Fig. 2.8 shows $\mathrm{V}^k_{(1,2)}$ for $1 \leq k \leq t$ and $t = 5$. Four replications are considered, *i.e.* $n = 5$. The pattern of voltages is the same in the original and replicated ladders.

2.3.2 Aging and the Ecology of rcTAMs

Biological individuals do not replicate forever, but age and die. Likewise, electrical components, or wires for that matter, will not function indefinitely. As components age, they will experience performance degradation and eventual failure.

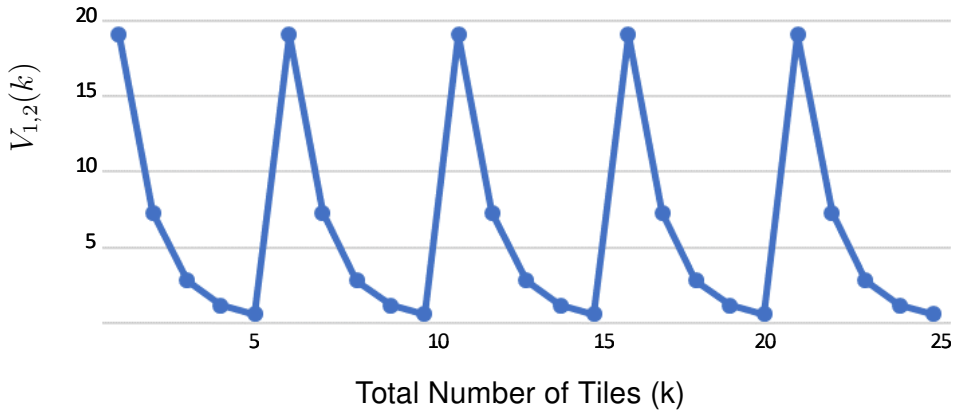


Fig. 2.8: $\mathrm{V}_{(1,2)}(k)$ after tile attachment for model parameters $\nu_0 = 50$, $\tau = 1$, $n = 5$, $\alpha = 1$, and $\beta = 1000$. In this example, replication occurs after $t = 5$ tiles attachment. This figure illustrates that the pattern of $\mathrm{V}_{(1,2)}(k)$ repeats identically after every replication. The y-axis shows the potential drop across R resistor for the terminal assembly. The x-axis indicates the total tile size of the assembly. After 25 steps, four replications have occurred.

For example, electromigration, a process that causes circuit failure by increasing the resistivity of a wire [79], is accelerated by high temperatures [80], [81]. The *time-to-failure* [79] is a common measure of reliability. In rcTAM, the maximum current will flow in resistor αR of either seed tile A or B. Therefore, these resistors are most likely to fail after some time M, the time-to-failure or lifetime of that component. Thus, this age-based failure mechanism ensures that the rcTAM will produce a stable population of ladders.

Theorem 2.3.3. *A rcTAM will produce a stable population of size $\lfloor \frac{M}{t} \rfloor$, where M indicates the lifetime of a resistor, and t is the number of time steps required for a ladder to reach adulthood (maximum size) and start to replicate.*

Proof. Let M be the time-to-failure of resistor αR in Tile A or B. A rcTAM starts its growth from the Tile A, and after a certain amount of time or number of attachments, the growth stops at an adult assembly. After that, the replication process starts and the growth of the child ladder continues according to the replication dynamics of

rcTAM. The number of time steps (tile attachments) for the ladders to become an adult again is t, the size of the adult ladders.

Assuming that a tile attaches at the rate of 1 tile per time unit, for the original ladder to replicate we must have $M > t$. The resistor αR of Tile A or B will fail after M time steps, so the total living population has roughly $\frac{M}{t}$ ladders. When αR fails, that ladder becomes electrically inactive. On the other hand, if a replicated ladder has started growing, it will complete its life cycle and become an adult, replicating in turn. Therefore, the total population of ladders or the size of the assembly remains ultimately constant, with size $\lfloor \frac{M}{t} \rfloor$ complete ladders. □

For example, if $M = 15.5$ and $t = 4$, the assembly has 3 mature ladders and one partial ladder when the first ladder dies. Nevertheless, the last ladder will complete the growth process and initiate another replication. This cycle repeats all over again. Thus the total living population stabilizes at size $\lfloor \frac{15.5}{4} \rfloor = 3$.

2.4 Discussion and Conclusion

We have proposed the rcTAM model of self-assembly consisting of basic circuit components (resistors, diodes and voltage sources) with a self-controlled growth mechanism. Except for the dependent source, the components do not include transistors and are not organic. The model exhibits instant cooperation among components that results in provable properties, such as self-controlled growth and self-replication. In addition, realistic failure mechanisms were used to prove that the system produces a stable population of adult assemblies. Therefore, the rcTAM is a family of models of nonbiological systems that exhibits life-like properties, such as self-assembly, self-controlled growth, and controlled self-replication. Usually, organic chemistry is assumed for life-like systems (though not exclusively). Several researchers have been exploring inorganic chemical systems that have certain properties of biological life, including self-replication, and asking the question whether organic chemistry is a prerequisite to life-like systems [74]. In that spirit, rcTAMs have

something to offer. Given their simplicity, it is somewhat surprising that rcTAMs exhibit such seemingly advanced capabilities. This emphasizes, perhaps, the power of self-assembly. For example, would a static circuit in the rcTAM have the same properties if it did not self-assemble?

An open question is to characterize the computational power of the rcTAM model. Given its parentage in algorithmic self-assembly models where glues provide the computational power, with sufficient number and types of glues, rcTAM would also be Turing universal. The question is really whether the electrical mechanisms present in the model allow computational universality to be achieved with a small glue set. In recent work [82], one-dimensional resistive ladders with annealing schedules of a decreasing sequence of thresholds were found to be capable of super-Turing computation.

Although an abstract, theoretical model intended to explore mechanisms of self-replication, the rcTAM might have application in self-assembly of nanostructures in general. Electric phenomena are useful in a variety of artificial growth processes, such as additive manufacturing [35], electrospray technology [36], and other nanomanufacturing technologies [37–39]. Electrostatic interactions have been reported as a mechanism to control nanoscale assemblies [83–85], and the rcTAM affords a theoretical framework to explore the ability of potential fields to control self-assembly size and shape.

The model also might have relevance to several examples of biological function, self-assembly, and organization. For example, galvanotaxis is the movement of cells under the influence of an electric field, and is a mechanism for both wound healing, as well as embryonic cell migration [86]. The biological molecules that inspire artificial approaches to self-assembly, namely lipids, nucleic acids, and amino acids, are charged molecules, and electric phenomena are directly involved in their formation

and stability [48]. Electric circuits, like the Hodgkin-Huxley model, have been used to describe mechanisms that produce action potentials in cells, particularly neural [51].

As described in section 2.1 endogenous fields from potential distributions in collection of cells interact with genetic mechanisms for pattern formation during tissue regeneration or embryo development [41, 42, 45–47]. There are similarities between the cTAM models and the effects of these bioelectric networks. The cTAM is potentially an abstract model for how electric signals might propagate in bioelectric networks, and the rcTAM for how they might replicate. Both the cTAM models and models of bioelectric networks capture how electric potentials can influence shape, size, and pattern. Except for small frequency-dependent capacitive effects, the electrical connection between cells across the gap junction is primarily Ohmic [87], and thus, the resistive ladder of the rcTAM is an approximate equivalent circuit for bioelectric intercellular communication among cells in a network [88]. The rcTAM and related models describe growing networks of circuit tiles whose properties are dynamic as the network structure changes. During processes like embryogenesis, networks of somatic cells are also dynamic, and thus the methods used to analyze cTAM networks might enable theoretical predictions to be made about them. In addition, in preliminary work [82], the cTAM is shown to be a powerful model of computation, and might elucidate the role of computation in bioelectric networks and information processing in biological systems. Therefore, the rcTAM and related models capture some of the characteristics of bioelectric networks, though abstracted to make analysis simpler, and that connection would be an interesting area for future investigation.

In conclusion, a new tile assembly model, rcTAM, whose components are simple electric circuits, exhibits the lifelike properties of self-assembled and self-controlled growth with self-replication. It accomplishes this without explicit biological components or mechanisms. Nevertheless, there seem to be mechanisms that are necessary that have analogs in biology, namely self-assembly, a source of

energy that is consumed to drive growth, a threshold value for control, and even, when replication occurs, conformational change. Thus, the rcTAM has potential not only to study self-assembly of nanostructure that are driven by an electric field, but also to provide insight into the necessary properties for systems to achieve characteristics similar to living systems.

Chapter 3

Logical Computation with Self-Assembling Electric Circuits

3.1 Introduction

Distributions of electric potentials in bioelectric networks influence gene expression, and thus, development of complex biological patterns [41, 42, 45, 46]. This feedback between bioelectric and biomolecular mechanisms is postulated to be an ancient mechanism and operates in many cellular processes, including embryonic growth and morphological differentiation [89–91]. In this paper, a simple circuit model for growth processes that are influenced by electric potentials, the *circuit tile assembly model (cTAM)* [10, 11], is extended to implement a computationally complete set of Boolean logic gates.

The development of a single cell to a functioning organism is a striking example of a self-assembly process, in which a larger, more capable system is constructed from small components through localized interaction. In the cTAM, larger circuits are self-assembled from unit tiles consisting of basic electrical components. An electric potential drives growth, dissipating as growth proceeds and eventually falling below a predefined threshold value. Thus, the electric potential acts similarly to a finite nutrient supply in a bacterial colony, or for that matter, the electric potential in artificial growth processes, like electroplating [92]. Though a nonbiological system, the cTAM achieves life-like properties, such as self-assembled, self-controlled growth [10, 11, 52, 53], and self-replication [12]. Bioelectricity influences gap junction-coupled transport phenomena [75], and the cTAM models the signal propagation in a bioelectric network. In this work, another cTAM model termed as "Boolean circuit tile assembly model (*bcTAM*)" is presented that implements computational mechanisms through growth processes, demonstrating that a simple model for electrically motivated growth contains powerful information processing capabilities.

Another important property of the living system is self-awareness which means

the system can sense the resources or environment and makes some decisions to respond to it. For example, primitive organisms like physarum can sense the positions of the nutrient supply and find the shortest path towards it [13, 14, 49]. The bcTAM model is a self-aware system that is capable of sensing the changes in the surroundings and processing information regarding its own growth. This is achieved by instrumenting growing resistive ladders with Boolean gates to make decisions about the extent of growth, which is determined by each ladder's input voltage and threshold for growth. Variable voltage inputs and thresholds potentially represent signals from sensors and environmental conditions, respectively. Thus, the bcTAM is a simple, abstract model of a system that can make decisions related to its awareness of its environment.

Electrical signals are potentially important in neural development [93–95], and when coupled with gene expression, have a fundamental role in the growth and organization of neural networks [93]. Electrical stimulation of neurons restrains axonal outgrowth [96]. The quality and quantity of sensory inputs that reached the brain are related to the rules of plasticity within cortical sensory areas [94]. The axon is the information-carrying path in the nervous system, and knowledge of how neurons extend axons and dendrites is critical to understand the nervous system better. The axonal growth dynamics can be modulated using signals, for example, when extracellular signals elongate axons and change the growth dynamics [95]. In 1952, Hodgkin and Huxley described how action potentials are initiated and propagated with an equivalent circuit model [51]. In [88], an equivalent circuit model represents gap-connected cells and their frequency response. The ladder circuits in the cTAM closely resemble those for the propagation of action potentials down axons, though with non-time varying signals. The cTAM conceptualizes the signal propagation across cell membranes by the electric potential distribution through a ladder circuit. The influence of the electrical potentials on the ion channel, analogous to the

threshold potential of the cTAM, is proven experimentally [47]. The cTAM growth generates a dynamic circuit configuration whose structure changes as per the growth mechanism, capturing dynamic biological growth processes, such as embryogenesis. Thus, the cTAM ladder circuit is an approximate equivalent circuit for bioelectric communication. Our previous work [10–12, 52, 53] investigated electric signal propagation and its impact on dynamic circuit configurations, and this work focuses on the capacity for logical decision making in the circuit tile assembly model. The bcTAM model shows the capability of performing Boolean functions in simple, biological mechanisms, such as axon growth. Using different computational models, others have shown the computational power of axons [97], but without growth.

Section 3.2 defines the bcTAM model, its tileset, working principle, and growth mechanism. It also explains how the bcTAM system uses logic about its own growth. Section 3.3 investigates an extension of the bcTAM to more complex boolean decision problems. The final section presents the concluding statements regarding the Boolean computational capability of the circuit tile assembly model.

3.2 Introducing Boolean Circuit Tile Assembly Model (bcTAM)

Biological organisms control molecular self-assembly using biochemical circuits and algorithms [26]. Motivated from these mechanisms, the *Circuit Tile Assembly Model* combines chemically-inspired glues and electric circuitry. The basic cTAM is a self-controlled self-assembly model [10, 11], and achieves self-replication with modified electric circuit components in the *replicating Circuit Tile Assembly Model (rcTAM)* [12]. This work adds an additional capability, *i.e.* molecular computation, with a modified cTAM model, termed the *Boolean Circuit Tile Assembly Model (bcTAM)*.

Definition 3.2.1 (bcTAM circuit)**.** A bcTAM circuit is a tuple $\Psi = (N, E, C, g, \partial N)$ where N and E represent electrical nodes and edges of a circuit respectively. Thus, the circuit is analogous to a graph (N, E). C is a set of circuit components required to build the tile types, and g is the glue set necessary for attachment among input and

output nodes. $\partial N = N_{in} \cup N_{out}$ consists of input nodes and output nodes of the circuit at which glues bind tiles together.

Definition 3.2.2 (Boolean Circuit Tile Assembly Model)**.** A Boolean cTAM assembler is a tuple $\mathcal{C} = (\Gamma, S, G, \tau, \nu, \zeta)$, where Γ is a finite set of circuit tile types built with basic electrical circuit components, $S \subseteq \Gamma$ is a set of seed tile type that are the starting point for the growth of an assembly, $G \subseteq \Gamma$ is a set of gate tile types that is capable of computing Boolean logic functions, $\tau \in \mathbb{R}_+$ is the threshold voltage, the parameter to determine the eligibility of further attachment, $\nu \in \mathbb{R}_+$ is the node potential, *i.e.* electric potential energy at the node relative to the ground node of the circuit, and ζ maps input nodes to output nodes according to the glue rules, *i.e.* $\zeta : \Gamma(N_{in}) \times \Gamma(N_{out}) \to \{0, 1\}$.

3.2.1 Description of the Assembly Process

An assembly describes a complete electrical circuit. It starts growing from the seed tile, and growth continues by attaching tiles based on the glue rules and a predefined threshold voltage. If the differential voltage across a node pair is greater than or equal to the threshold τ, the glues of the nodes are activated. The potential difference between two nodes (p, q) will be denoted as $\mathrm{V}^{\gamma}_{(p,q)}(k)$, where the first node $p \in N$ in an edge refers to the more positive potential, $\gamma \in \Gamma$ is the tile type, and the index $k \in \{1, \ldots, n\}$, denotes a specific tile in the ladder assembly of size n, as well as timestep. Inspired by the DNA tile assembly, the attachment rules of the cTAM is based on DNA Watson-Crick complementary oligonucleotides, where a glue matches with its complement. Each tiles of the bcTAM tileset has a particular set of glues, denoted as g^m_k where g indicates the glue type, m indicates the assembly number, and k denotes the timestep. For example, for the first step of the first ladder will have glues g^1_1 where $g = a, b, \ldots$. A stable attachment may occur if the potential difference between the nodes (either input or output) is greater than the threshold voltage, and the tiles have complementary glues, *i.e.* g attaches to $\overline{g}$. Figure 3.1 shows an example of two ladders with two tile types and four tiles. Tile A, the seed tile, has two glues at

the output nodes and tile B has two glues at input nodes and two glues across the output nodes. For the tile A of ladder 1, $m = 1, k = 1$, for the tile B of ladder 1, $m = 1, k = 2$, for the tile A of ladder 2, $m = 2, k = 1$, and for the tile B of ladder 2, $m = 2, k = 2$. Therefore, tile A of ladder 1 has an output node pair with glues, a_1^1 and b_1^1 that matches with tile B having glues $\overline{a}_1^1$ and $\overline{b}_1^1$ on its input node pair. A tile can attach to a growing ladder if the voltage drop across the output nodes of the ladder is greater than or equal to the threshold voltage. Here, tile A and tile B of the corresponding ladder will attach if the potential across the input or output nodes $\geq \tau$. An attachment requires four complementary glues. Since the each rung of the ladder is instrumented with a gate, the required number of glues is $(n-1) * 4 + 2$, where n is the length of the assembly. For this example case, the connection occurs between $\{a_1^1 - \overline{a}_1^1\}$, $\{b_1^1 - \overline{b}_1^1\}$, $\{a_1^2 - \overline{a}_1^2\}$, and $\{b_1^2 - \overline{b}_1^2\}$, shown in the example case of figure 3.1. Also, tile B has glues $\{c_1^2, d_1^2\}$ for ladder 1, and $\{c_2^2, d_2^2\}$ for ladder 2. As $n = 2$, $(2-1) * 4 + 2 = 6$ glues are required for each of the ladders. Both of the ladders are two tile assembly, making total number of required glues 12, as shown in figure 3.1.

Definition 3.2.3 (Terminal Circuit)**.** A *terminal assembly* is a stable configuration in which no further attachment is possible. A circuit tile assembly model represents a dynamic circuit configuration in which growth continues based on the threshold voltage and matching glues criteria. When growth has stopped, the final circuit configuration is termed as *terminal circuit*. The number of tiles in a terminal assembly is denoted by n.

3.2.2 Logic Gates and Their Truth Tables

In digital logic design, the most common logic gates are AND, OR, NOT, NAND, NOR, and we can build any logic circuitry with these gates. Table 3.1 shows the truth table for the logic gates of AND, OR, NOR, and NAND with two inputs, and table 3.2 shows the truth table of a single input NOT gate. This work aims to build a tile assembly model that has the functionalities of these five gates. The Boolean circuit tile assembly model has one seed tile, one circuit tile, and a set of gate tiles consisting

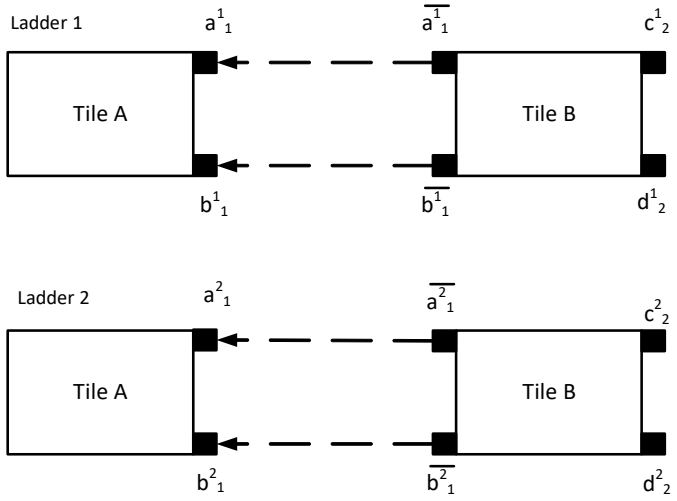


Fig. 3.1: An example representing the matching glue rules. Here, the assembly system has four tiles of two tile types(tile A and tile B). The first tile A has glues $\{a_1^1, b_1^1\}$ and the second tile A has glues $\{a_1^2, b_1^2\}$ at the output nodes. For the tile B, one tile has glues $\{\overline{a}_1^1, \overline{b}_1^1\}$, and the other tile has glues $\{\overline{a}_1^2, \overline{b}_1^2\}$ at the input nodes. According to the glue rules, a stable attachment will occur between the glue pairs $\{a_1^1 - \overline{a}_1^1\}$, $\{b_1^1 - \overline{b}_1^1\}$, $\{a_1^2 - \overline{a}_1^2\}$, and $\{b_1^2 - \overline{b}_1^2\}$ if $\Delta\nu \geq \tau$, shown with dotted arrow in the figure.

Table 3.1: Truth Table of Logic Gates (OR, AND, NOR, NAND)

Input 1	Input 2	OR Output	AND Output	NOR Output	NAND Output
0	0	0	0	1	1
0	1	1	0	0	1
1	0	1	0	0	1
1	1	1	1	0	0

of five tile types. Each gate tile computes one particular Boolean function among the set AND, OR, NOT, NAND, NOR.

3.2.3 Description of Tiles

Seed tile (Tile A) of bcTAM consists of two loops , where the first loop is built with one voltage source ν_0 (at node $\{1, 0\}$), two resistors R (at node $\{1, 2\}$), and αR (at node $\{2, 0\}$) connected as a series circuit (Figure 3.2). The second loop has one

Table 3.2: Truth Table of NOT Gate

Input	Output
0	1
1	0

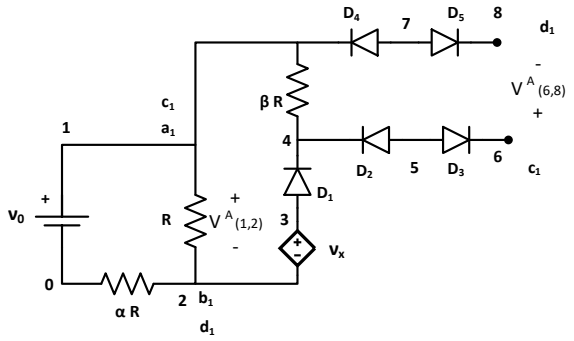


Fig. 3.2: Tile A (Seed Tile) for the bcTAM consisting with one dc voltage source ν_0, one dependent voltage source $V_x = \frac{2\tau\nu_0}{\nu_0}$, five ideal diodes D_1, D_2, D_3, D_4, D_5 with $\tau = 0$, and three resistors (R, αR, and βR where βR is a large value resistor compared to R and αR). It has two output terminals across node $\{1, 2\}$ and node $\{6, 8\}$. Node 1 has glue $\{a_1, c_1\}$, node 2 has glue $\{b_1, d_1\}$, node 6 has glue c_1, and node 8 has glue d_1.

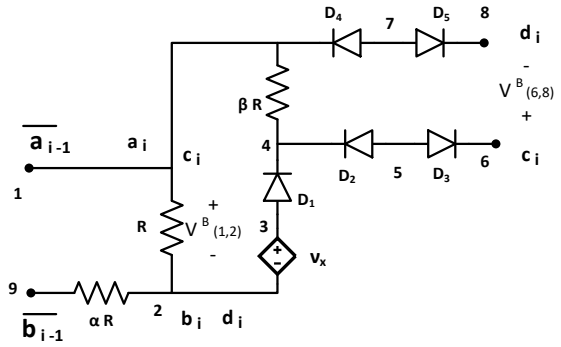


Fig. 3.3: Tile B (Circuit Tile) consists with three resistors (R, αR, and βR), one dependent voltage source $V_x = \frac{2\tau\nu_0}{\nu_0}$, five ideal diodes D_1, D_2, D_3, D_4, D_5 with $\tau = 0$. It has one input node terminal at node $\{1, 9\}$ and two output node terminals at node $\{1, 2\}$ and node $\{6, 8\}$. Glues: $g(1) = \{a_i, c_i, \overline{a}_{i-1}\}$, $g(2) = \{b_i, d_i\}$, $g(6) = c_i$, $g(8) = d_i$, and $g(9) = \overline{b}_{i-1}$, where $i = 2, 3$.....

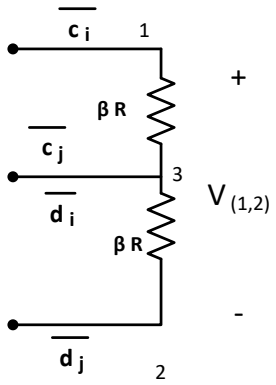


Fig. 3.4: OR tile consists of two βR resistors connected in series. It has two input nodes across $\{1, 3\}$ and $\{3, 2\}$ and one output node at $\{1, 2\}$. Glues: $g(1) = \{\overline{c}_i\}, g(2) = \{\overline{d}_j\}$, and $g(3) = \{\overline{c}_j, \overline{d}_i\}$, where $i = 1, 2, ...$ and $j = 1, 2.....$ indicate the location of the assembly.

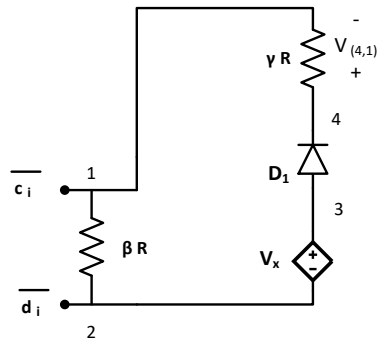


Fig. 3.5: NOT tile consists of two large value resistors (βR and γR, where $\gamma >> \beta$), one ideal diode D_1 with $V_{thr} = 0$, and one dependent voltage source $V_x = \frac{2\tau\nu_0}{\nu_0}$ in series connection. It has input node across node $\{1, 2\}$ and output node at $\{4, 1\}$. Glues: $g(1) = \{\overline{c}_i\}, g(2) = \{\overline{d}_i\}$.

large value resistor βR (at node $\{1, 4\}$), one dependent voltage source $V_x = \frac{\nu_0 2\tau}{\nu_0}$ (at node $\{3, 2\}$), and one ideal diode D_1 (at node $\{3, 4\}$) with threshold voltage $\tau = 0$. The dependent source V_x equals to dc voltage source of 2τ if connected with ν_0; otherwise it is not activated. Four ideal diodes with zero threshold voltage are connected across the βR resistor: D_2 at node $\{5, 4\}$, D_3 at node $\{5, 6\}$, D_4 at node $\{7, 1\}$, and D_5 at node $\{7, 8\}$. This diode bridge prevents current flow from next tile to

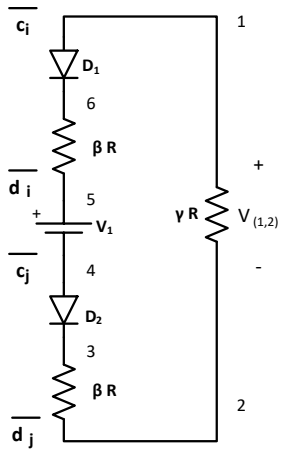


Fig. 3.6: AND tile consists of two ideal diodes D_1 and D_2 with $V_{thr} = \tau$, two large value βR resistors, one large value γR resistor, and one dc voltage source $V_1 = \tau$. It has input nodes across node pair $\{1, 5\}$ and $\{4, 2\}$, and output node at $\{1, 2\}$. Glues: $g(1) = \{\overline{c}_i\}, g(2) = \{\overline{d}_j\}, g(4) = \{\overline{c}_j\}, g(5) = \{\overline{d}_i\}$.

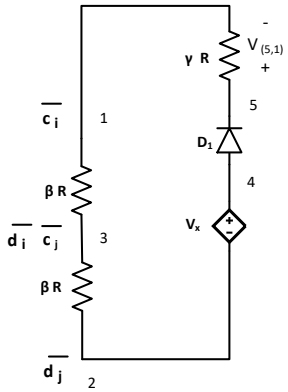


Fig. 3.7: NOR tile has three resistors (two βR resistors, and γR resistors where $\gamma >> \beta >> R$), one ideal diode D_1 with zero threshold voltage, and one dependent voltage source $V_x = \frac{2\tau\nu_0}{\nu_0}$. It has two input node pairs across node $\{1, 3\}$ and $\{3, 2\}$. This tile has output node at $\{5, 1\}$. Glues: $g(1) = \{\overline{c}_i\}, g(2) = \{\overline{d}_j\}$, and $g(3) = \{\overline{c}_j, \overline{d}_i\}$.

the seed tile, *i.e.* they act as an isolator between two adjoining tiles. The tile has two pairs of output nodes at $\{1, 2\}$ and $\{6, 8\}$ with glues $g(1) = \{a_1, c_1\}$, $g(2) = \{b_1, d_1\}$, $g(6) = \{c_1\}$, and $g(8) = \{d_1\}$. The first loop of seed tile A acts as a voltage divider circuit where ν_0 is divided between the resistors R and αR. The second loop has a

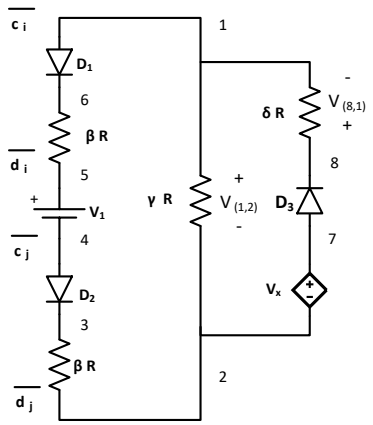


Fig. 3.8: NAND tile consists of three ideal diodes (Diode D_1, D_2 have $V_{thr} = \tau$, and diode D_3 has $V_{thr} = 0$), four resistors (Two βR resistors, one γR resistor, and one δR resistor, where $\delta >> \gamma >> \beta >> R$), and two voltage sources (One dc voltage source $V_1 = \tau$, and one dependent voltage source of $V_x = \frac{2\tau\nu_0}{\nu_0}$). It has two input terminals across node pairs $\{1, 5\}$ and $\{4, 2\}$, and output terminal at $\{8, 1\}$. Glues: $g(1) = \{\overline{c}_i\}, g(2) = \{\overline{d}_j\}, g(4) = \{\overline{c}_j\}$, and $g(5) = \{\overline{d}_i\}$.

dependent voltage source that provides a 2τ dc voltage source if activated. Using KVL along nodes $\{1, 2, 3, 4, 1\}$ at tile A:

$$
\begin{aligned}
&V_x - V_{D_1} - \mathrm{V}^A_{(4,1)}(1) - \mathrm{V}^A_{(1,2)}(1) = 0, \\
&2\tau - 0 - \mathrm{V}^A_{(4,1)}(1) - \mathrm{V}^A_{(1,2)}(1) = 0, \\
&\mathrm{V}^A_{(4,1)}(1) = 2\tau - \mathrm{V}^A_{(1,2)}(1).
\end{aligned} \tag{3.1}
$$

If $\mathrm{V}^A_{(1,2)}(1) > \tau$, then $\mathrm{V}^A_{(4,1)}(1) < \tau$ and if $\mathrm{V}^A_{(1,2)}(1) < \tau$, then $\mathrm{V}^A_{(4,1)}(1) > \tau$. From equation 3.1, $\mathrm{V}^A_{(1,2)} = \tau$, $\mathrm{V}^A_{(4,1)} = \tau$ creates an unwanted condition of activation for both outputs $\mathrm{V}^A_{(1,2)}$ and $\mathrm{V}^A_{(6,8)}$. This condition can be avoided by choosing appropriate values of the input parameters ($\nu_0,\ \tau,\ \alpha$) such that the tip voltage goes from $\mathrm{V}_{(1,2)}(n-1) > 2\tau$ for a ladder of length $(n-1)$ to $\mathrm{V}_{(1,2)}(n) < \tau$ for a ladder of length n, at which point the assembly terminates. To prove that there exists values of the input parameters that will reduce the tip voltage from $> 2\tau$ to $< \tau$ with the addition of a

single tile, the values of the voltage will be bound, and the existence of a gap between the bound voltages shows that the condition is possible to achieve. For a ladder of length $(n-1)$, the desired condition is that $\mathrm{V}_{(1,2)}(n-1) > 2\tau$. Since R is greater than the equivalent resistance for a given length ladder, a voltage divider between R and αR is used to upper bound the voltage,

$$2\tau < V_{n-1} < (\frac{1}{1+\alpha})^{n-1}\nu_0. \tag{3.2}$$

Solving for n, produces

$$1 + \frac{\log(2\tau/\nu_0)}{\log(\frac{1}{1+\alpha})} < n. \tag{3.3}$$

For a ladder of length n, the equivalent resistance for an infinite length ladder, R_{eq}^{∞}, is used in the bound since it is less than the actual equivalent resistance. It's value

$$R_{eq}^{\infty} = R\left[\frac{-\alpha + \sqrt{\alpha^2 + 4\alpha}}{2}\right] = R\chi. \tag{3.4}$$

was derived in [11]. Therefore, the bound on the tip voltage for a ladder of length n is

$$\left[\frac{R_{eq}^{\infty}}{R_{eq}^{\infty} + \alpha R}\right]^n \nu_0 < V_n < \tau. \tag{3.5}$$

Solving for n results in

$$n < \frac{\log(\tau/\nu_0)}{\log(\frac{\chi}{\chi+\alpha})}. \tag{3.6}$$

Combining Equations 3.3 and 3.6, requiring that Equation 3.6 be at least one tile larger than Equation 3.3, and setting $\alpha = 1$, produces

$$\frac{\log(2\tau/\nu_0)}{\log(1/2)} < \frac{\log(\tau/\nu_0)}{\log(\frac{1}{1+\phi})}, \tag{3.7}$$

where ϕ is the golden ratio [10]. Solving gives

$$0.0839\nu_0 < \tau, \tag{3.8}$$

which can be satisfied for any ν_0 by an appropriate choice of τ, proving that the condition of the tip voltage identically equal to τ can be avoided. Therefore, in this work, we will consider Logic 1=HIGH ($> \tau$), Logic 0=LOW ($< \tau$) and exclude the condition of tip potential is exactly equal to τ.

Now, from equation 3.1, when $\mathrm{V}^A_{(4,1)}(1) > \tau$, the output nodes $\mathrm{V}^A_{(6,8)}(1) > \tau$ due to the open loop condition at node $\{6, 8\}$. So, before any attachment, the glues of the output nodes $\{6, 8\}$ are activated and ready to attach with other tiles of matching glues. However, after the attachment, it will contribute LOW ($< \tau$) potential for the next tile as the diode bridge acts as an open circuit. To sum up, when the growth is continuing, output $\{1, 2\}$ activates, and it provides HIGH ($> \tau$) potential to attach a tile to these nodes. In contrast, when $\mathrm{V}^A_{(1,2)} < \tau$, $\mathrm{V}^A_{(6,8)} > \tau$, output $\{6, 8\}$ activates, and it provides LOW ($< \tau$) potential to the next tile attached to these nodes.

Circuit tile (Tile B) has the same circuit configuration as the seed tile except for the supply voltage (Figure 3.3). It has one pair of input nodes at $\{1, 9\}$ and two pairs of output nodes $\{1, 2\}$ and $\{6, 8\}$ same as the seed tile. It has glues: $g(1) = \{a_i, c_i, \overline{a}_{i-1}\}, g(2) = \{b_i, d_i\}, g(6) = \{c_i\}, g(8) = \{d_i\}$, and $g(9) = \overline{b}_{i-1}$, where $i = 2, 3...$ It provides HIGH input when $\mathrm{V}^B_{(1,2)}(k) > \tau$, and provides LOW input when $\mathrm{V}^B_{(1,2)}(k) < \tau$.

The bcTAM has a set of gate tiles: OR gate, AND gate, NOT gate, NOR gate, and NAND gate. The OR tile consists of two large value βR resistors (at node $\{1, 3\}$ and $\{3, 2\}$) connected in series. It has two input node pairs across each βR resistors, *i.e.* at $\{1, 3\}$ and $\{3, 2\}$ and one output node pair at $\{1, 2\}$. It has glues: $g(1) = \{\overline{c}_i\}$, $g(2) = \{\overline{d}_j\}$, and $g(3) = \{\overline{c}_j, \overline{d}_i\}$, where $i = 1, 2, \ldots$ and $j = 1, 2, \ldots$ indicate the

location of the assembly (Figure 3.4). For all of the two input gate tiles, i and j will indicate the location for the attachment at different assemblies. Also, the glue set will be unique for each ladder at each step. The output of OR tile is the potential across node $\{1, 2\}$, which equals to:

$$\mathrm{V}^{OR}_{(1,3)} + \mathrm{V}^{OR}_{(3,2)} = \mathrm{V}^{OR}_{(1,2)}. \tag{3.9}$$

If any or both input nodes are connected with the assembly location $\{1, 2\}$, the tip potential is HIGH ($> \tau$), then the output potential is also HIGH.

If any input nodes (such as $\{1, 3\}$) of the OR gate connects with the location $\{6, 8\}$ of the assembly at step k, according to the KVL,

$$\mathrm{V}_{(4,1)}(k) + \mathrm{V}_{(1,7)}(k) + \mathrm{V}_{(7,8)}(k) + \mathrm{V}^{OR}_{(1,3)}(k) + \mathrm{V}_{(6,5)}(k) + \mathrm{V}_{(5,4)}(k) = 0. \tag{3.10}$$

As the diode D_2 and D_4 are reverse biased, no current can flow in this loop, and $\mathrm{V}^{OR}_{(1,3)}(k) = 0$, indicating LOW potential. From the equation 3.9, if any of the inputs or both inputs ($\mathrm{V}^{OR}_{(1,3)}$ or $\mathrm{V}^{OR}_{(3,2)}$) are HIGH, output $\mathrm{V}^{OR}_{(1,2)}$ is HIGH ($> \tau$). If both input is LOW (*i.e.* Zero), then the output $\mathrm{V}^{OR}_{(1,2)}$ is LOW. Therefore, it matches with the truth table of an OR gate. The two-input OR gate can be modified for an m input OR gate by adding m number of βR resistors and unique glues.

The NOT tile is a single loop circuit with two large value resistors (βR at node $\{1, 2\}$ and γR at node $\{4, 1\}$ and $\gamma >> \beta$), one ideal diode D_1 at node $\{3, 4\}$, and one dependent voltage source of $V_x = \frac{\nu_0 2\tau}{\nu_0}$ at $\{3, 2\}$. The threshold voltage of the diode, $V_{thr} = 0$. It has one input node at $\{1, 2\}$ and one output node at $\{4, 1\}$. Input node $\{1, 2\}$ has glues $\overline{c}_i$ and $\overline{d}_i$ respectively (Figure 3.5). The working mechanism of the

NOT tile is similar to NOT gate. Using KVL along the tile:

$$
\begin{aligned}
V_x - V_{D_1} - \mathrm{V}^{NOT}_{(4,1)} - \mathrm{V}^{NOT}_{(1,2)} &= 0, \\
2\tau - 0 - \mathrm{V}^{NOT}_{(4,1)} - \mathrm{V}^{NOT}_{(1,2)} &= 0, \\
\mathrm{V}^{NOT}_{(4,1)} &= 2\tau - \mathrm{V}^{NOT}_{(1,2)}.
\end{aligned} \tag{3.11}
$$

If the NOT tile has logic HIGH as input *i.e.* $\mathrm{V}^{NOT}_{(1,2)}(k) > \tau$, using equation 3.11, $\mathrm{V}^{NOT}_{(4,1)} < \tau$. In contrast, if the tile is connected with a terminal circuit at node $\{6, 8\}$, it gets a LOW input across resistor βR. Then, $\mathrm{V}^{NOT}_{(1,2)}(k) < \tau$ and from the equation 3.11, $\mathrm{V}^{NOT}_{(4,1)} > \tau$. Thus, the NOT tile's output potential is inverted with respect to its input potential, acting like a NOT gate (Table 3.2).

The AND tile consists of a series connection among two diodes D_1, D_2(Ideal diodes with threshold τ), one dc voltage source $V_1 = \tau$, and three resistors (Two βR resistors and one γR resistor where $\gamma >> \beta >> R$) (Figure 3.6). It has two input nodes at $\{1, 5\}$ and $\{4, 2\}$. The output nodes are across γR resistor at node $\{1, 2\}$. It has glues: $g(1) = \overline{c}_i$, $g(5) = \overline{d}_i$, $g(4) = \overline{c}_j$, $g(2) = \overline{d}_j$. When an AND tile is floating (not connected with the seeded assembly), both diodes are reverse-biased, and no current flows through the γR resistor. If any input nodes ($\mathrm{V}^{AND}_{(1,5)}$ or $\mathrm{V}^{AND}_{(4,2)}$) connects with the LOW potential output terminal, *i.e.* node $\{6, 8\}$ of the assembly, the corresponding diode of AND tile is still in reverse bias condition, acts as an open circuit, no current flows through the tile, and hence $\mathrm{V}^{AND}_{(1,2)} = 0 < \tau$. If both of the input nodes are connected with node pair $\{1, 2\}$ of the growing assembly, they get HIGH potential ($> \tau$). So, both diodes become forward bias, current flows through the loop $\{5, 6, 1, 2, 3, 4, 5\}$. Using KVL at the loop:

$$
\begin{aligned}
V_1 + \mathrm{V}^{AND}_{(5,1)} - \mathrm{V}^{AND}_{(1,2)} + \mathrm{V}^{AND}_{(2,4)} &= 0, \\
\mathrm{V}^{AND}_{(1,2)} &= \tau + \mathrm{V}^{AND}_{(5,1)} + \mathrm{V}^{AND}_{(2,4)}.
\end{aligned} \tag{3.12}
$$

If both diodes D_1 and D_2 are forward biased, $\mathrm{V}_{(5,1)}^{AND}$ and $\mathrm{V}_{(2,4)}^{AND}$ are greater than τ. Using equation 3.12, $\mathrm{V}_{(1,2)}^{AND} > \tau$ =HIGH output. These properties match with a two-input AND gate. Same as the OR tile, it can be modified to make it an m input AND gate by adding m number of diode-resistor pairs on the input side with a new glue pairs.

Figure 3.7 shows a NOR tile with *bcTAM*. It has one loop consisting of three resistors in series (βR resistor at node $\{1,3\}$, βR resistor at $\{3,2\}$, and γR resistor at node $\{5,1\}$ where $\gamma >> \beta$), an ideal diode D_1 at node $\{4,5\}$ with $V_{thr} = 0$, and one dependent voltage source $V_x = \frac{\nu_0 2\tau}{\nu_0}$ at node $\{4,2\}$. It has two input nodes across two βR resistors and output nodes across γR resistor. The glues are:$g(1) = \{\overline{c}_i\}$, $g(2) = \overline{d}_j$, and $g(3) = \{\overline{c}_j, \overline{d}_i\}$. The NOR tile can attach to two assemblies with a complementary glues $\{c_i - d_i\}$ or $\{c_j - d_j\}$. Applying KVL to the loop:

$$\begin{aligned} V_x - V_{D_1} - \mathrm{V}_{(5,1)}^{NOR} - \mathrm{V}_{(1,3)}^{NOR} - \mathrm{V}_{(3,2)}^{NOR} &= 0, \\ 2\tau - 0 - \mathrm{V}_{(5,1)}^{NOR} - \mathrm{V}_{(1,3)}^{NOR} - \mathrm{V}_{(3,2)}^{NOR} &= 0, \\ \mathrm{V}_{(5,1)}^{NOR} &= 2\tau - \mathrm{V}_{(1,3)}^{NOR} - \mathrm{V}_{(3,2)}^{NOR}. \end{aligned} \tag{3.13}$$

If both inputs ($\mathrm{V}_{(1,3)}^{NOR}$ and $\mathrm{V}_{(3,2)}^{NOR}$) are LOW, the potential is approximately zero as per our previous discussion. From equation 3.13, $\mathrm{V}_{(5,1)}^{NOR} = 2\tau - 0 = 2\tau$, which indicates HIGH output. But if both or either of the inputs are HIGH, $\mathrm{V}_{(5,1)}^{NOR} < \tau$, indicating LOW output. So, the output is HIGH iff both inputs are LOW, and output is LOW otherwise, representing the NOR operation.

The last tile for the logic gate set is NAND tile. This tile has two loops. The first loop has one voltage source $V_1 = \tau$ (at node $\{5,4\}$), three resistors: Two βR resistors (at node $\{5,6\}$ and $\{2,3\}$), one γR resistor (at node $\{1,2\}$), two ideal diodes D_1 (at node $\{1,6\}$) and D_2 (at node $\{4,3\}$) with $V_{thr} = \tau$. The second loop is similar to the NOT tile with one dependent voltage source V_x (at node $\{7,2\}$), one ideal diode D_3 (at

node $\{7, 8\}$) with $\tau = 0$, and one δR resistor at $\{8, 1\}$. Among the resistor values, $\delta >> \gamma >> \beta >> R$. It has input nodes across node pair $\{1, 5\}$ and $\{4, 2\}$, and output node at $\{8, 1\}$ (Figure 3.8). The glues are: $g(1) = \{\overline{c}_i\}$,$g(2) = \{\overline{d}_j\}$, $g(4) = \{\overline{c}_j\}$, $g(5) = \{\overline{d}_i\}$. The tile acts as a two-input NAND gate for the Boolean circuit tile assembly model. The first loop is the same as AND tile, and the second loop is the same as NOT Tile. Using KVL for the second loop:

$$\mathrm{V}_{(8,1)}^{NAND} = 2\tau - \mathrm{V}_{(1,2)}^{NAND}. \tag{3.14}$$

From the working principle of AND tile, it is proven that if both of the diodes D_1 and D_2 are forward biased due to the HIGH input node potential, then $\mathrm{V}_{(1,2)}^{NAND} > \tau$. From equation 3.14, $\mathrm{V}_{(8,1)}^{NAND} < \tau$. In contrast, if any or both input diodes are reverse biased due to the LOW input node potential, $\mathrm{V}_{(1,2)}^{NAND} < \tau$ and $\mathrm{V}_{(8,1)}^{NAND} > \tau$. Thus, all the input conditions for the NAND truth table are satisfied with the NAND tile.

3.2.4 Implementation of the bcTAM

In this section, we will discuss an example problem and its solution using bcTAM. The problem is to instrument a set of growing ladders with variable input voltages to determine when all the ladders have stopped growing. In order to do this, each tile of each ladder must be connected to a logic gate tile. To demonstrate, the case of two growing ladders is highlighted. We can design it with two seed tiles (tile A), multiple circuit tiles (tile B), and multiple NOR tiles (tile C). We annotated the tileset based on the number of seed tiles, as the number of seed tiles decides the number of ladders. As the system has two seed tiles, two ladders will grow, and hence, there will be two distinct glue sets: i and j. The glues are denoted as g_k^m where g indicates the glue types (such as a, b, c, d), m indicates the assembly number, and k denotes the timestep. For example, the first assembly ($m = 1$) will have a glues as a_1^1, a_2^1, a_3^1 and the second assembly will have glues a_1^2, a_2^2, a_3^2 for $k = 1, 2, 3$, respectively. The same

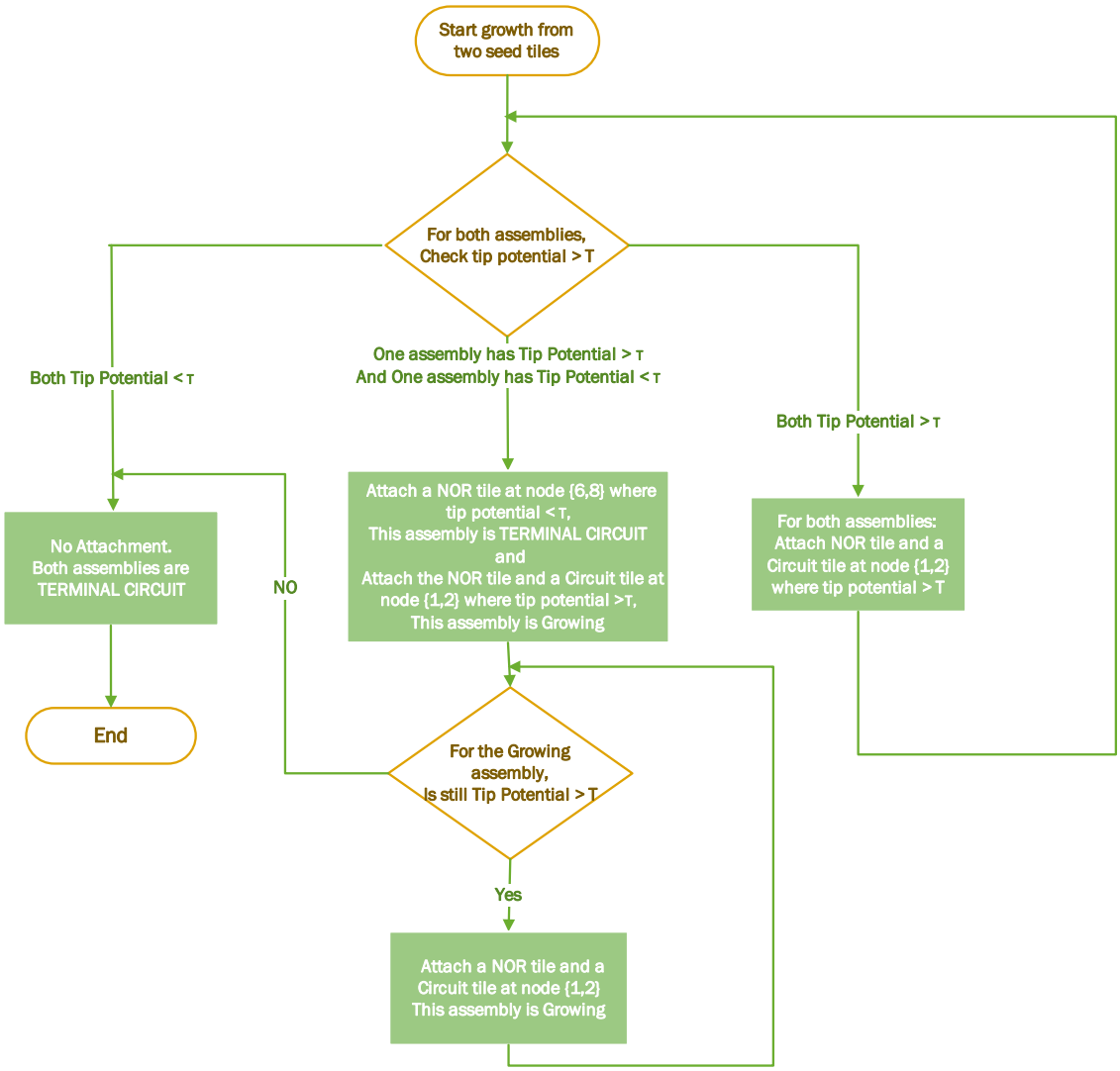


Fig. 3.9: The figure shows the assembly process of the example case of section 3.2.4.

glue notations will be used for other glues: b, c, d. Except for the seed tile, there is no independent voltage source in other tiles. Therefore, all output node potentials will be less than the threshold as the dependent source is not activated until it is attached to the ν_0.

The growth starts from the seed tiles and compares the tip potential to the threshold voltage. If tip potential is higher than the threshold τ, another tile will attach based on the glue rules. Figure 3.9 shows the flowchart of the assembly process. The assembly starts with seed tile (tile A). Let's assume both tile A has source potential

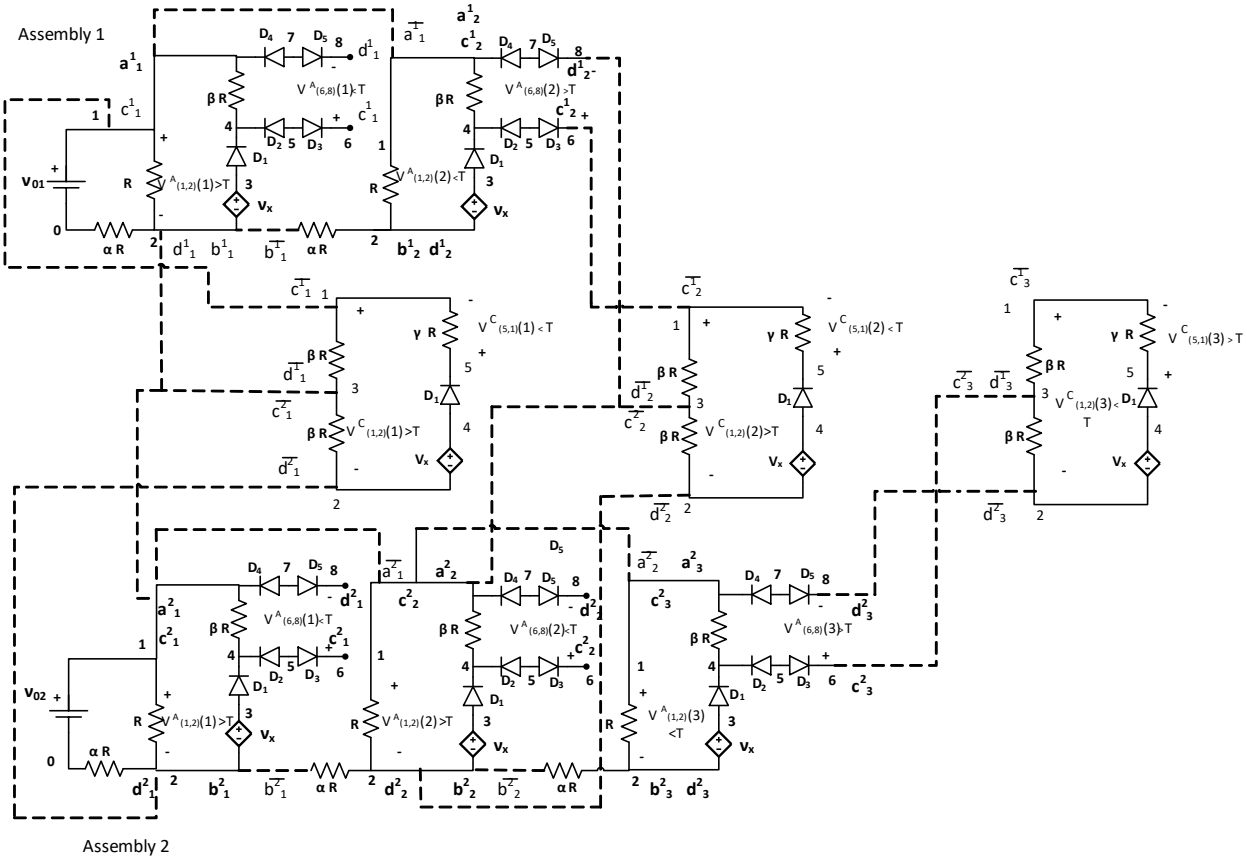


Fig. 3.10: The figure shows an example assembly that represents the working mechanism of a NOR gate. Here, two assemblies are growing simultaneously. The dotted lines are showing attachment with glues. The first assembly has a length of two, and the second assembly has a length of three. As long as both of the assembly, or any one of them is growing, the output potential of NOR tile (middle tier), $\mathrm{V}^{C}_{(5,1)}(k) < \tau = LOW$. When both assemblies are terminals, $\mathrm{V}^{C}_{(5,1)}(t) > \tau = HIGH$.

$> \tau$ as well as $\mathrm{V}^{A}_{(1,2)} > \tau$. Also, assume, the source potentials for the first and second assemblies are ν_{01} and ν_{02} respectively where $\nu_{0_1} < \nu_{0_2}$. For both of the assemblies, $\mathrm{V}^{A}_{(1,2)}(1) > \tau$, it activates the attached glues *i.e.* $\{a^1_1 - b^1_1\}$, $\{c^1_1 - d^1_1\}$, $\{a^2_1 - b^2_1\}$, and $\{c^2_1 - d^2_1\}$. A circuit tile with complementary glues $\{\overline{a}^1_1 - \overline{b}^1_1\}$ attaches to the first assembly at node $\{1 - 2\}$. Similarly, the second assembly attaches with the circuit tile having matching glues. A NOR tile (tile C) with input glues $\{\overline{c}^1_1, \overline{d}^1_1\}, \{\overline{c}^2_1, \overline{d}^2_1\}$ also attaches to node pair $\{1 - 2\}$. Since $\mathrm{V}^{C}_{(1,2)}(1) > \tau$ in NOR tile 1, $\mathrm{V}^{C}_{(5,1)}(1) < \tau$ that indicates a LOW state [Figure 3.10].

For the next step, in tile B, input potential $\mathrm{V}^{B}_{(1,9)}(2)$ is further distributed in circuit components. Lets assume, $\mathrm{V}^{B}_{(1,2)}(2) < \tau$ in assembly 1, and $\mathrm{V}^{B}_{(1,2)}(2) > \tau$ in assembly 2. For the first assembly, according to the Kirchoff's Voltage Law across the loop $\{1, 2, 3, 4, 1\}$, $\mathrm{V}^{B}_{(4,1)}(2) = \mathrm{V}^{B}_{(6,8)}(2) > \tau$. It activates glue $\{c^1_2 - d^1_2\}$ only and a NOR tile C with glue $\{\overline{c}^1_2, \overline{d}^1_2\}$ will attach to the node $\{6, 8\}$, and no further circuit tiles can attach to the assembly. But in case of the second assembly, $\mathrm{V}^{B}_{(1,2)}(2) > \tau$ and it activates both the glues $\{a^2_2 - b^2_2\}$ and $\{c^2_2 - d^2_2\}$. A circuit tile and a NOR tile with complementary glues will attach to the assembly at node $\{1, 2\}$. As the tile C is still having input greater than τ, $\mathrm{V}^{C}_{(5,1)}(2) < \tau$, that means LOW output.

In the third timestep, assume, second assembly also has less than τ tip potential *i.e.* $\mathrm{V}^{B}_{(1,2)}(3) < \tau$ and $\mathrm{V}^{B}_{(6,8)}(3) > \tau$. It activates only $\{c^2_3 - d^2_3\}$ glues. Hence, only a NOR tile attaches with glues $\{\overline{c}^2_3, \overline{d}^2_3\}$. As per the mechanism described in the earlier section, the input potential of tile C is LOW. In tile C, $\mathrm{V}^{C}_{(1,2)}(3) < \tau$ resulting in $\mathrm{V}^{C}_{(5,1)}(3) > \tau$, a HIGH state of output [Figure 3.10]. Thus, the output terminal of NOR tile, $\mathrm{V}^{C}_{(5,1)}(k)$ is HIGH($> \tau$) iff both assemblies are terminal configuration and acts as an indicator of the moment when the system has no growing assembly.

3.3 Why Significant

The bcTAM, a model of biological growth in which electric potential is the driving force, is capable of implementing a complete set of Boolean gates with which

all Boolean functions can be realized. The example of the last section can be generalized to ask more complicated Boolean questions about the growth of a set of ladders. The computational complexity and power of the bcTAM to make boolean-based decisions, without outside intervention, about complex problems related to the growth of a set of ladders is motivated by the following decision problem:

Definition 3.3.1. bcTAM SATISFIABILITY
INSTANCE: A bcTAM in which the set of seed tiles $S = \{s_1, s_2, \ldots, s_m\}$ are assigned arbitrary input voltages $\nu = \{\nu_0^1, \nu_0^2, \ldots, \nu_0^m\}$.
QUESTION: Does the bcTAM assemble a satisfiable circuit, *i.e.* one whose output is true?

This problem of bcTAM satisfiability is thus a subproblem of the well known SATisfiability problem [98, 99] in Computer Science since bcTAM models are built of AND, OR and NOT logical gates and can thus be described by a Boolean formula. SAT is an NP-complete problem and bcTAM models are fairly complex already, so the interesting question remains whether bcTAM SAT is still NP-complete.

Variable input voltages (ν_0's) could have biological relevance as well. They could represent variable sources of energy that produce growth. They could arise as output voltages from sensors, which is common whether the sensor is a neuron or some nonbiological sensor. As the input voltages vary, bcTAM produces different Boolean circuits, and thus, different electric potential distributions at the terminus, as well as throughout the circuit itself. This represents an abstraction of endogenous electric potential distributions, which are produced by membrane potentials. There is increasing evidence that these bioelectric networks influence gene expression, and thus, have an important role in embryonic development, including morphogenesis, tissue regeneration, and general biological pattern formation [41, 42, 45, 46, 89–91]. Boolean networks have long been models for genetic regulatory networks [100], and the bcTAM provides an electric analog. Thus, the bcTAM is a system that is self-aware

in the sense that it can decide for itself when target potential distribution have been achieved through growth by sensing the outputs of logic gates. This feature is similar to primitive biological mechanisms or organisms, such as physarum. For example, the physarum can explore the paths in a maze, and find the shortest path to the nutrient supplies [49]. A system that can sense its environment, process information about itself is an interesting property of the living system, and bcTAM intends to achieve it.

Moreover, the bcTAM is implemented with relatively simple circuit components that approximate the DC electric functionality of axons, showing the power inherent in axonal growth. Finally, the relationship between the length of the ladders and the electric potential is known [52], and thus, the input voltages can be determined to a given range based on the length of the ladder. Therefore, the bcTAM provides a new model for biological growth with powerful computational capabilities that might further understanding of the role of electric phenomena in biological form and function.

3.4 Conclusion

Biological systems have long inspired models of computation, from genetic algorithms to artificial neural networks. Logic gates are a widely accepted model of computation and decision-making [40]. In addition, self-assembly is a core mechanism for biological development and structure formation. In this work, by implementing a computationally complete set of Boolean gates through voltage-controlled self-assembled growth, the bcTAM connects these important ideas. The bcTAM explores how an organism responds in dynamic environment, *i.e.* variable inputs and threshold. Being able to sense the environment, respond to it, and make a decision, whether conscious or not, is one characteristic of living systems. Thus, the bcTAM is a self-aware system that can make decisions about its growth as represented by a potential distribution.

The bcTAM is a resistive network model inspired by biological growth mechanisms, *i.e.* self-assembly, and with a circuit components that approximate

electrical conduction in axons. The model performs logical computation with a tile assembly system that is driven by an electric potential. Thus, it provides a new perspective for computation in growing networks of axons, and by extension, the influence of distributions of electric potentials on the development of biological form and function. In the bcTAM, because of its abstraction of electric potential effects on biological growth mechanisms, the resulting networks are amenable to detailed analysis. For example, the range of input potentials to produce given lengths and how the potential changes for each step can be calculated. Thus, from a theoretical perspective, it might produce a better understanding of Boolean decision making in bioelectric phenomena. This model is a unique self-assembly model with the power of self-controlled growth and logical computation. These features make the model an attractive candidate for further research from the perspective of both bioelectric networks and neural computation.

Chapter 4

A Memory Cell with Self-assembling Electric Circuits

4.1 Introduction

In the quest for new semiconductor materials or processes, researchers have focused on self-assembly, an ubiquitous process by which components assemble into larger structures through local interactions only. In December 1959, Richard Feynman gave his famous talk, “There is plenty of room at the bottom” that hinted at the importance of scaling in manufacturing [101]. Self-assembly and self-organization promise an alternative vision for the future of nanofabrication [7, 102]. For example, DNA-guided self-assembly is one of the most promising techniques for nanomanufacturing to generate new types of electric circuits [8, 21, 22, 103]. This approach has interesting applications in a sequential logic detection system [104]. The sequential logic gate with DNA in functional nanosystems was reported in [104, 105]. For instance, [104] presents a model based on sequential logic DNA gate that is capable of recognizing "before" and "after" triggering sequences of DNA signals. Self-assembled monolayers (SAMs) on silicon are also an excellent candidate for a memory element [106]. This study investigates the scope of self-assembly as a memory device using the circuit tile assembly model (cTAM).

Inspired by biomolecular growth mechanisms, a novel algorithmic model consisting of electrical circuit components was introduced and analyzed in [10–12, 52, 53]. Denoted as *cTAM (circuit tile assembly model)*, larger circuits are self-assembled from unit tiles consists of basic electrical components. Though the cTAM is a nonbiological family of circuits, it attempts to abstract a bioelectric network [15]. The influence of the electrical potentials on the ion channel, analogous to the threshold potential of the cTAM, is proven experimentally [47]. The cTAM growth generates a dynamic circuit configuration whose structure changes as per the growth mechanism, capturing dynamic biological growth properties, such as embryogenesis.

Thus, the cTAM ladder circuit is an approximate equivalent circuit for a bioelectric model for cellular communication. Also, the cTAM exhibits important properties, such as self-assembly, self-controlled growth, instant and distance communication [10, 11, 52, 53], self-replication [12], and logical computation [15]. [10, 11] introduced the model, calculated the upper bounds of the assembled circuits, and proved the uniqueness and symmetry of the grid circuits' final shape. [52] derived the exact values for the potential distribution of the cTAM ladder, which is representative of a dynamic circuit configuration, and [53] extended the analysis to two-dimensional resistive grid circuits to explore the size, shape, and energy distribution of the assembled cTAM circuit. [12] augmented the model to achieve another important living system property, self-replication, and hence, the proposed model connects more to the bioelectric networks. [15] proposed a model termed *bcTAM* that has power of logical computation. The *bcTAM* achieved a computationally complete set of Boolean gates through voltage controlled self-assembled growth. [15] contains an example of combinational logic design. This work is a part of series of research works [10–12, 15, 52, 53] investigating the scope of the circuit tile assembly model to design a sequential logic circuit and hence, the ability to store the state information like a memory device.

Living systems interact with the environment, grow by consumption of resources, react to the ambient changes, and evolve to survive by remembering successful responses to environmental factors. The power of adaptation is a prerequisite for the advancement of life. Without some sort of memory of what responses worked, adaption appears impossible. For example, acellular organism, physarum, can find the shortest of path to the nutrient supply in a maze, indicating that it explores all the paths and chooses the shortest one by remembering the responses [49]. The bcTAM [15] is a self-assembled, self-controlled growth, and self-aware system that can sense environmental changes and respond to them. This

chapter aims to use this capability to build a system that can remember its previous state. Also, rcTAM [12] produces copies of itself as long as resources are available. The model is expected to have applications in self-assembly of nanostructures, and thus, having a system that can generate finite number of copies is also a research interest. The general approach to building a counter requires a flip flop, the most common example of sequential logic design. A Flip Flop is a fundamental building block of digital electronic systems used to store state information. D flip flop is the most commonly used one and it follows the truth table 4.1. Building a flip flop using the proposed bcTAM model is the primary goal of this chapter. Section 4.2 defines the Boolean circuit tile assembly model, its terminologies, and assembly process. The following section 4.3 contains tile description and the working principle of bcTAM as a sequential circuit. Finally, the significance of this study and concluding remarks are mentioned in the last section.

4.2 Boolean Circuit Tile Assembly Model

The Circuit Tile Assembly Model (cTAM) was introduced in [10, 11]. This model consists of a finite set of template tiles, built with basic circuit components, capable of *gluing* to each other upon fulfillment of the defined criteria and assembling to larger structures. The basic cTAM [10, 11] possesses self-controlled self-assembled growth mechanisms with instant and distant communication. This model is augmented to achieve self-replication in [12] in the *replicating circuit Tile Assembly Model (rcTAM)*. Another family member of cTAM, *Boolean circuit Tile Assembly Model (bcTAM)* was introduced in [15] and is capable of performing Boolean operations. This work focuses on investigating the capability of *bcTAM* to construct a flip flop that is an implementation of sequential logic design. This chapter will use the *bcTAM* model of [15] which is formally defined as follows.

Definition 4.2.1 (Boolean Circuit Tile Assembly Model)**.** A Boolean cTAM assembler is a tuple $\mathcal{C} = (\Gamma, S, G, \tau, \nu, \zeta)$, where Γ is the set of circuit tile types, S is the set of

seed tile type where the assembly starts growing, G is the set of gate tile types that act as Boolean logic gates, $\tau \in \mathbb{R}_+$ is the threshold voltage for attachment, $\nu \in \mathbb{R}_+$ is the node potential, and ζ maps input nodes to output nodes according to the glue rules *i.e.* $\zeta : \Gamma(N_{in}) \times \Gamma(N_{out}) \rightarrow \{0, 1\}$.

Assembly Process:

A circuit tile assembly model starts growing from the seed tile. A *cTAM* model has a finite number of tiles where each tile has a number of glues on input and output terminals. When the differential voltage across a node pair is greater than or equal to the threshold τ, the glues of the nodes get activated, and the attachment of additional tiles is enabled. The potential difference between two nodes (p, q) will be denoted as $\mathrm{V}^{\gamma}_{(p,q)}(k)$, where the first node $p \in N$ refers to the more positive potential, and $\gamma \in \Gamma$ is the tile type. An index $k \in \{1, \ldots, n\}$, denotes a specific tile in the ladder assembly as well as the timestep and the number of tiles in a terminal assembly, denoted by n. An attachment of a new tile automatically changes the potential values at every node in the circuit as the circuit configuration is changed. The tileset will have differences in glues, and glues are denoted as g^m_k where g indicates the glue types, m indicates the assembly number, and k denotes the timestep. A stable attachment may occur if glues are matched based on DNA Watson-Crick complementary oligonucleotides, where a glue matches with its complement. The growth process continues as long as the attachment criteria are fulfilled. When no growth is possible, the final assembly is denoted as a *terminal circuit*. Some definitions of this model are as follows.

Definition 4.2.2 (Attachment)**.** An attachment can occur between input and output node pairs of the two tiles if two conditions are fulfilled: 1) The potential difference between input terminals or output terminals is greater than or equal to a predefined threshold voltage (τ) and 2) Glue rules are satisfied. Glues are denoted like DNA Watson-Crick complementary oligonucleotides, so that a glue $\{a\}$ matches its

complement $\{\overline{a}\}$. If the potential difference across node pairs $\geq \tau$, it activates glues, and an attachment can happen between complementary glues.

Definition 4.2.3 (Terminal Circuit)**.** A *terminal circuit* is the final configuration in which no tiles can be attached to the assembly. A circuit tile assembly model starts its growth from the seed tile and continues until the attachment conditions are fulfilled. When the assembly has grown to the final configuration in which growth has stopped, the final structure is denoted as *terminal Circuit*.

4.3 A sequential logic design(Flip Flop) using bcTAM

4.3.1 Description of Tiles

A flip-flop serves as the primary block of a memory device and counter. There are different kinds of flip-flops, the most common of which is the D flip-flop. It has an output state according to the given input D, and output remains in the same state until the input changes. The *bcTAM* model can implement a D flip flop circuit using five tile types, where one of them will produce a clock signal termed the “clock tile", and the other four will work as basic blocks of a D flip flop. Tile A of the model consists of a series circuit with two dc voltage sources, one large value resistor, and one ideal diode with zero threshold voltage. The tile has four nodes where V_0 is at $\{1, 2\}$, $V_1 = 2\tau$ is at $\{3, 2\}$, diode D_1 is at $\{3, 4\}$, and Resistor βR is at $\{4, 1\}$ (Figure 4.1). V_0 is the input of flip-flop circuit: $V_0 < \tau$ is considered as logic zero, and $V_0 > \tau$ indicates logic one. $V_0 = \tau$ condition is excluded as like as the bcTAM [15]. It has glues: $g(1) = \{a, d\}$, $g(2) = \{b\}$, and $g(4) = \{c\}$.

Tile B (Figure 4.2(a)) and tile C (figure 4.2(b)) are identical to two-input AND gate in accordance with Boolean circuit tile assembly model (*bcTAM*) [15]. It consists of a series circuit with three resistors (two βR resistor and one γR resistor where $\gamma >> \beta$), one dc voltage source ($V_2 = \tau$), and two ideal diodes D_1, D_2 with $V_{thr} = \tau$. Among the resistors, two resistors are of βR values (at node $\{5, 6\}$, and node $\{3, 2\}$), and one resistor has larger value of γR (at node $\{1, 2\}$). It has two ideal diodes with

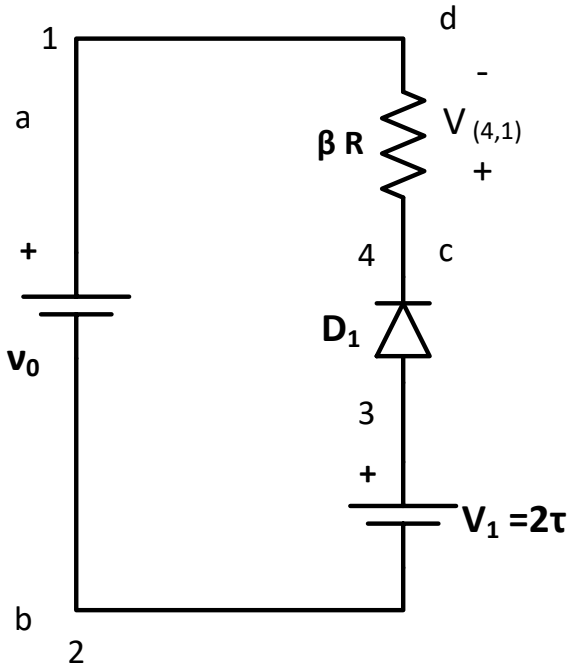


Fig. 4.1: Tile A has two dc source voltage V_0 and $V_1 = 2\tau$, one large value resistor βR, and one ideal diode with $V_{th} = 0$. It has two output node pairs $\{1, 2\}$, and $\{4, 1\}$. Glues: $g(1) = a, d$, $g(2) = b$, and $g(4) = c$.

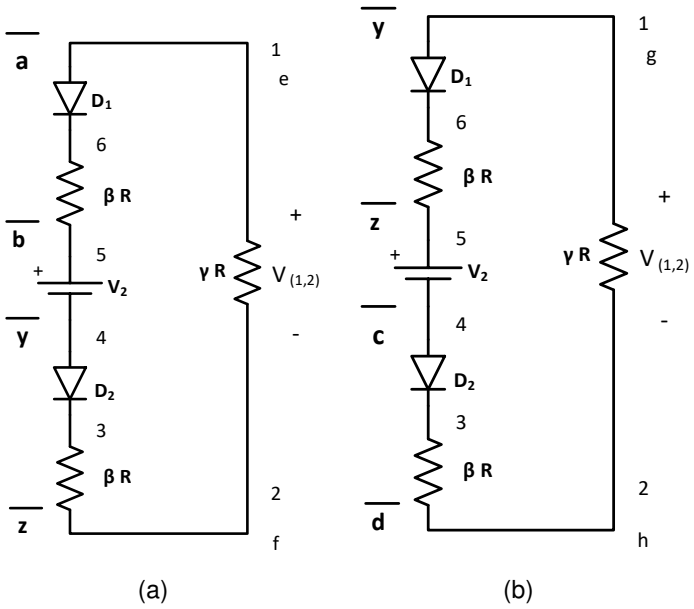


Fig. 4.2: Tile B and tile C has a voltage source of $V_2 = \tau$, two βR resistors, one γR resistor, and two ideal diodes D_1 and D_2 with threshold value τ. Glues for tile B: $g(1) = \{\overline{a}, e\}$,$g(2) = \{\overline{z}, f\}$, $g(4) = \{\overline{y}\}$, $g(5) = \{\overline{b}\}$. Glues for tile C: $g(1) = \{\overline{y}, g\}$,$g(2) = \{\overline{d}, h\}$, $g(4) = \{\overline{c}\}$, $g(5) = \{\overline{z}\}$.

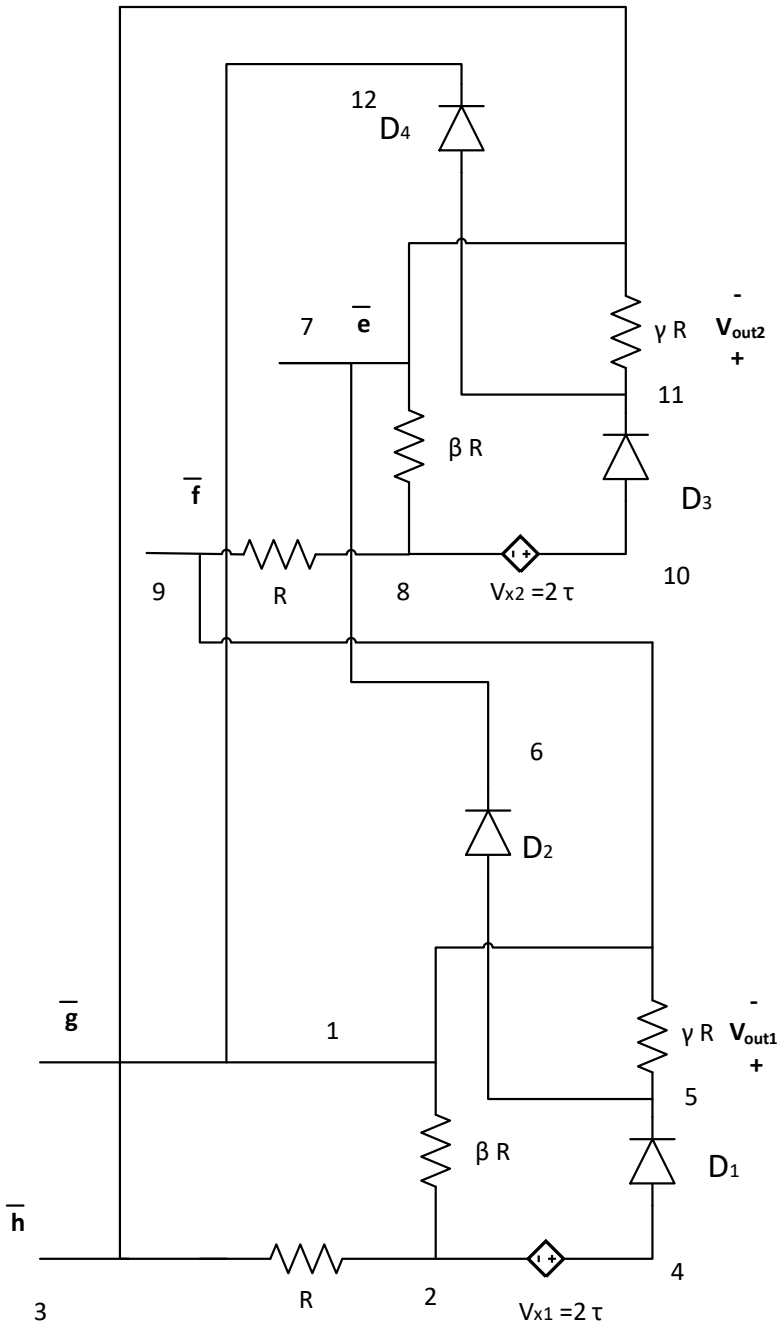


Fig. 4.3: Tile D has total six resistors (two R resistors, two βR resistors, and two γR resistors where $\gamma >> \beta >> R$), two dependent voltage sources ($V_{x_1} = V_{x_2} = 2\tau$), four ideal diodes $D_1 - D_4$ with threshold $V_{thr} = 0$. It has two input node pairs at $\{1, 3\}$ and $\{7, 9\}$, and two output node pairs at $\{5, 1\}$ and $\{11, 7\}$. Glues are: $g(1) = \{\overline{g}\}$, $g(3) = \{\overline{h}\}$, $g(7) = \{\overline{e}\}$, $g(9) = \{\overline{f}\}$.

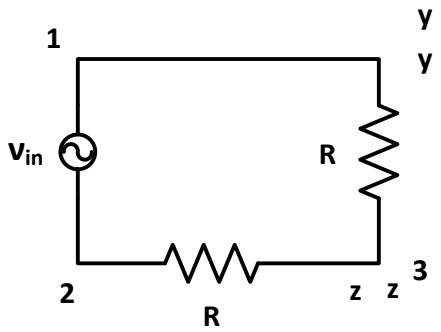


Fig. 4.4: Tile E consisting of one ac voltage source V_{in}, and two R resistors is series. It has pulse train as input signal. Node 1 has glue $\{y, y\}$, and node 3 has glue $\{z, z\}$.

predefined threshold τ (at node $\{1, 6\}$ and $\{4, 3\}$). The voltage source is of τ value that is located at node $\{5, 4\}$. The only difference between tile B and tile C is the glues at nodes. Glues of tile B are: $g(1) = \{\overline{a}, e\}$, $g(2) = \{\overline{z}, f\}$, $g(4) = \{\overline{y}\}$, $g(5) = \{\overline{b}\}$ and glues of tile C are: $g(1) = \{\overline{y}, g\}$, $g(2) = \{\overline{d}, h\}$, $g(4) = \{\overline{c}\}$, $g(5) = \{\overline{z}\}$.

Tile D works similar to two NOR gates connected to each other via feedback, *i.e.* output of one NOR gate acts as an input of other NOR gate. It has total six resistors (two R resistors at node $\{2, 3\}$ and $\{8, 9\}$, two βR resistors at node $\{1, 2\}$ and $\{7, 8\}$, and two γR resistors at node $\{1, 5\}$ and $\{7, 11\}$, and $\gamma >> \beta >> R$), two dependent voltage sources ($V_{x_1} = V_{x_2} = 2\tau$) at nodes $\{4, 2\}$ and $\{10, 8\}$ respectively, and four ideal diodes with threshold $V_{thr} = 0$ (D_1 at $\{4, 5\}$, D_2 at $\{5, 6\}$, D_3 at $\{10, 11\}$, and D_4 at $\{11, 12\}$). It has two input node pairs at $\{1, 3\}$ and $\{7, 9\}$, and two output node pairs: $V_{out_1} = Q$ at $\{5, 1\}$ and $V_{out_2} = \overline{Q}$ at $\{11, 7\}$. Glues are: $g(1) = \{\overline{g}\}$, $g(3) = \{\overline{h}\}$, $g(7) = \{\overline{e}\}$, $g(9) = \{\overline{f}\}$.

Tile E acts as a clock tile that gives a clock signal to tile B and tile C. Tile E consists of one ac voltage source (V_{in}) at node $\{1, 2\}$, and two R resistors at $\{1, 3\}$ and $\{3, 2\}$(Figure 4.4). Pulse train is given as ac voltage source. It has one output node pair at $\{1, 3\}$ with glues $g(1) = \{y, y\}$, and $g(3) = \{z, z\}$.

Table 4.1: Truth Table of D Flip Flop

Clock	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

4.3.2 How it works

Figure 4.5 shows a D flip flop logic diagram where D is the data input, and Q is the output value. Table 4.1 shows the truth table of D Flip Flop. Let's check with an example assembly built with *bcTAM* to see if it has achieved the functionality of D Flip Flop.

In our model, tile A, B, C, and D will build an assembly similar to figure 4.5, based on the *bcTAM*. Tile E acts as a clock signal for the flip flop assembly. Tile A is a series circuit with following KVL equation:

$$\begin{aligned}
&\mathrm{V}^{A}_{(1,2)}(1) + \mathrm{V}^{A}_{(4,1)}(1) + V_{D_1} - V_1 = 0,\\
&\mathrm{V}^{A}_{(1,2)}(1) + \mathrm{V}^{A}_{(4,1)}(1) + 0 - 2\tau = 0,\\
&\mathrm{V}^{A}_{(4,1)}(1) = 2\tau - \mathrm{V}^{A}_{(1,2)}(1).
\end{aligned}$$

When $\mathrm{V}^{A}_{(1,2)}(1) > \tau$, then $\mathrm{V}^{A}_{(4,1)}(1) < \tau$, and if $\mathrm{V}^{A}_{(1,2)}(1) < \tau$, then $\mathrm{V}^{A}_{(4,1)}(1) > \tau$. $V_0 = \mathrm{V}^{A}_{(1,2)}(1)$ is the D input of flip flop, hence, $\mathrm{V}^{A}_{(4,1)}(1)$ functions like NOT(D) *i.e.* $\overline{D}$. Both the node pairs of $\{1, 2\}$ and $\{4, 1\}$ have glues that activate when the differential voltage across the node pair is $> \tau$. So, the tile is designed such that only one glue pair, either $\{a - b\}$ or $\{c - d\}$, is activated at once and available for additional attachment with a complementary glue pair.

Tile E has a pulse train as input and the output at $\{1, 3\}$ is also an ac signal. When $\mathrm{V}^{E}_{(1,3)}(1) > \tau$, the glues are activated, and they can attach to the

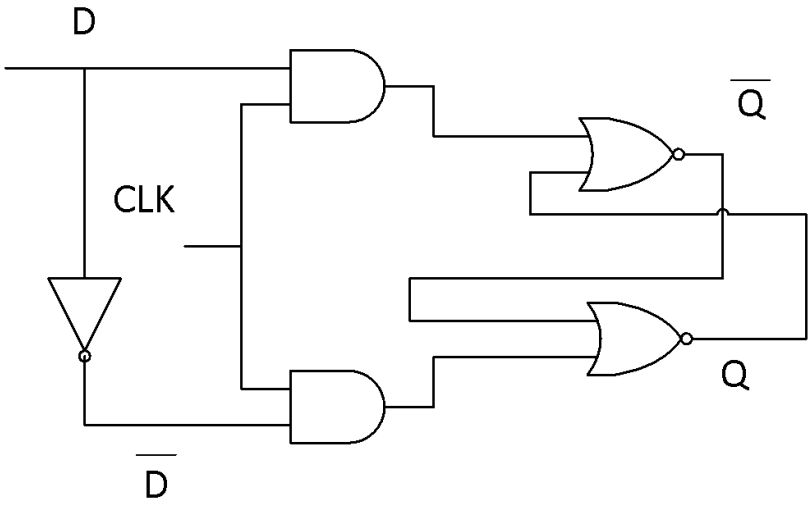


Fig. 4.5: D flip flop logic design

complementary glues. Therefore, tile E works as a clock tile as it produces a signal that is ON($> \tau$) and OFF($< \tau$) repeatedly.

Tile B has one input node pairs $\{1, 5\}$ with glue $\{\overline{a} - \overline{b}\}$. So, tile B will attach to the tile A if $\{a - b\}$ is activated. The input nodes $\{4, 2\}$ has glues $\{\overline{y} - \overline{z}\}$ that connects with $\{y - z\}$ glues of clock assembly. Therefore, if tile B connects to tile A as well as clock assembly, both diodes D_1, D_2 will forward bias, and the potential drop across γR resistor $\mathrm{V}^{B}_{(1,2)}(2) > \tau$, that in turn activates glue pair $\{e - f\}$ to continue further growth. Tile C acts the same way as tile B, and it activates glue pair $\{g - h\}$, if both of the diodes are forward biased. According to the glue rules, tile D will attach to tile B or tile C in location $\{7, 9\}$ or $\{1, 3\}$, respectively. Based on the input potential, KVL, and diode condition, we have the output potentials $\mathrm{V}^{D}_{(5,1)}$ and $\mathrm{V}^{D}_{(11,7)}$, which is considered as Q and $\overline{Q}$, respectively.

4.3.3 An Example Assembly

D flip flop is used as a part of a memory storage element that can store one-bit data. The output Q follows the D input if the clock signal is HIGH. The other output $\overline{Q}$ represents the opposite state of the Q output (Table 4.1). If the clock signal is LOW, the outputs are not affected by input D, which stays in the previous state.

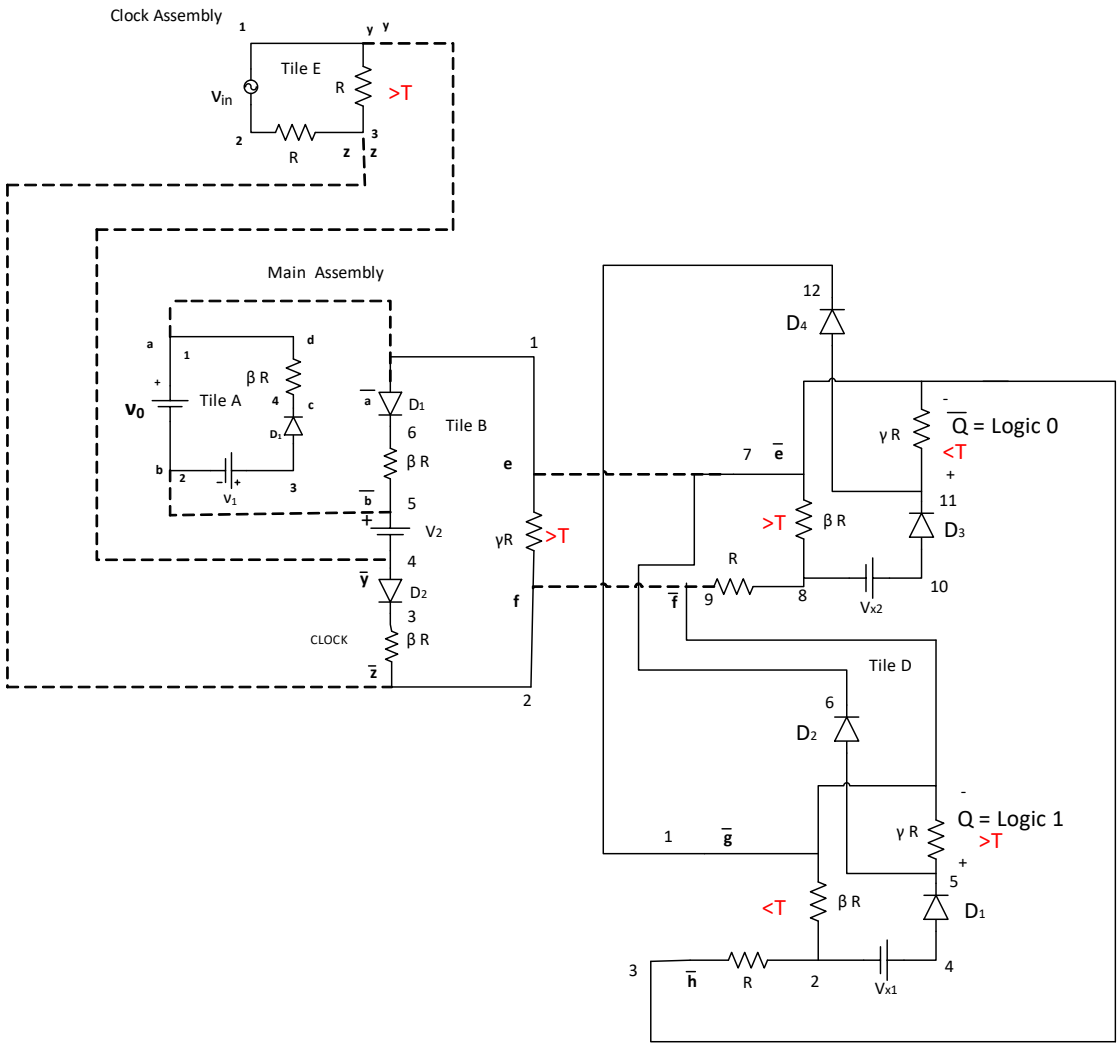


Fig. 4.6: An example of bcTAM flip flop mechanism for input= Logic 1. Assembly starts with seed tile A. Tile B and tile D are attached to the seeded assembly due to the matching glues. Tile C is connected with tile E, but it is not connected with the seed tile. There is no other attachment to the output of tile C, hence tile C is not drawn in the figure. Here, Output $Q = 1(HIGH)$, and $\overline{Q} = 0(LOW)$, that matches with flip flop functionality.

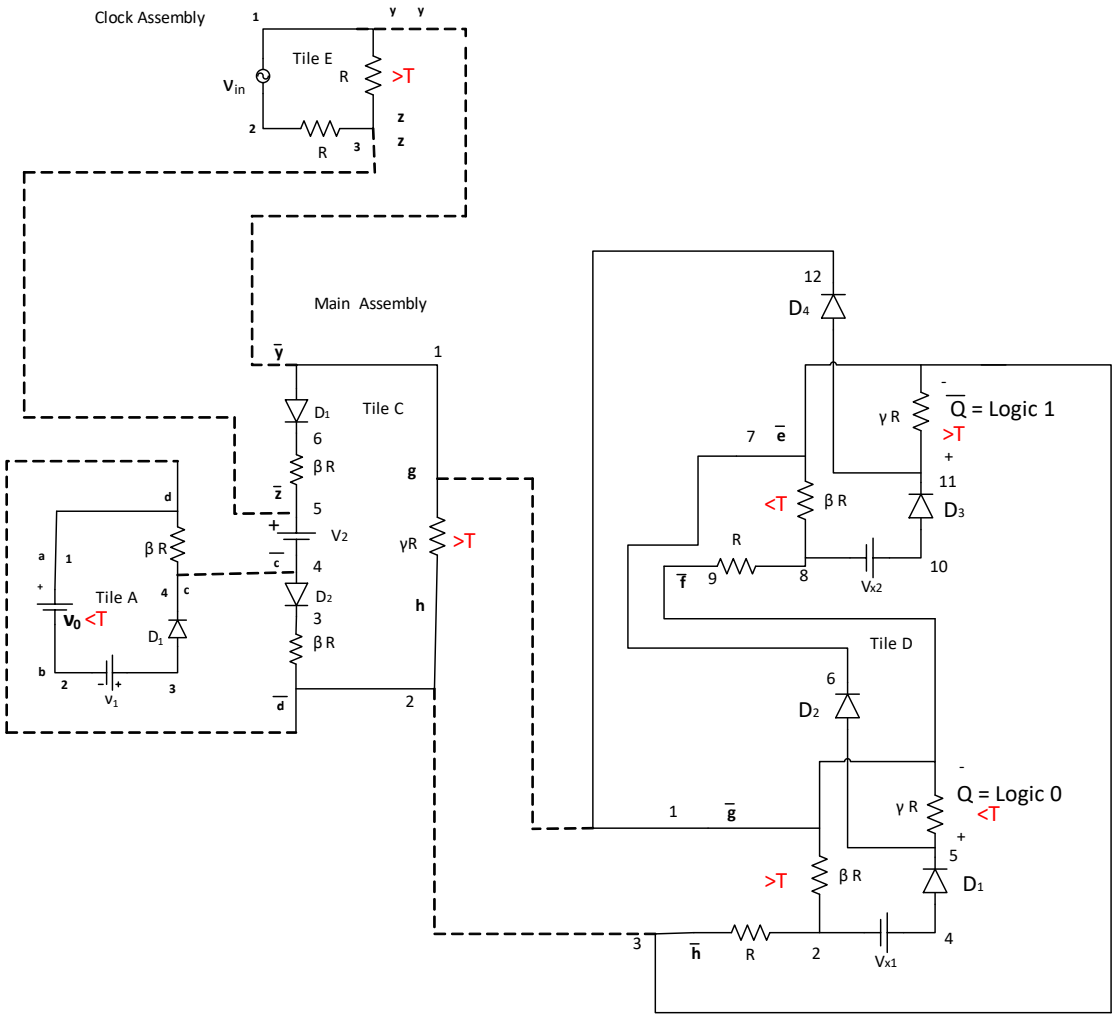


Fig. 4.7: An example of bcTAM flip flop mechanism for input= Logic 0. Assembly starts with seed tile A. Then, tile C and tile D are attached due to the matching glues. Tile B is connected with tile E, but it is not connected with the seed tile. There is no further attachment to the output of tile B, hence tile B is not drawn in the figure. and Here, Output $Q = 0(LOW)$, and $\overline{Q} = 1(HIGH)$, that matches with flip flop principle of operation.

Assume the DC input voltage V_0, Max value of clock input V_{in}, and Max value of clock output $\mathrm{V}^{E}_{(1,3)}(1)$ greater than the threshold τ. $V_0 = \mathrm{V}^{A}_{(1,2)}(1) > \tau$ *i.e.* D =HIGH $=$ Logic 1 results in $\mathrm{V}^{A}_{(4,1)}(1) < \tau$. Glues $\{a - b\}$ activate, tile B attaches to tile A, and diode D_1 is forward biased. The output of tile E gives an alternating signal where the peak amplitude is greater than τ. When $\mathrm{V}^{E}_{(1,3)}(1) > \tau$, glue pair $\{y - z\}$ activates and attaches to its complementary pair $\{\overline{y} - \overline{z}\}$ of tile B and tile C. Tile B gets both clock signal and D input signals, whereas tile C gets clock signal only. Tile C has forward biased diode D_1, but D_2 is reverse biased. Hence, no current flows through it and $\mathrm{V}^{C}_{(1,2)}(2) < \tau$ and unavailable for growth. In tile B, both of the diodes D_1 and D_2 are ON, current flows through it, and the output node voltage $\mathrm{V}^{B}_{(1,2)}(2) > \tau$. It activates glue pair $\{e, f\}$. Hence, tile D attaches to tile B at node location $\{7, 9\}$. Due to the large resistor βR, $\mathrm{V}^{D}_{(7,9)}(3) \approx \mathrm{V}^{D}_{(7,8)}(3) > \tau$. According to KVL:

$$V_{x_2} - V_{D_1} - \mathrm{V}^{D}_{(11,7)}(3) - \mathrm{V}^{D}_{(7,8)}(3) = 0,$$
$$\mathrm{V}^{D}_{(11,7)}(3) = 2\tau - \mathrm{V}^{D}_{(7,8)}(3).$$

As $\mathrm{V}^{D}_{(7,8)}(3) > \tau$, $\mathrm{V}^{D}_{(11,7)}(3) = \overline{Q} < \tau$ (LOW). This $\mathrm{V}^{D}_{(11,7)}(3)$ is connected to node $\{1, 3\}$ of tile D. So, $\mathrm{V}^{D}_{(1,3)}(3) < \tau$ and $\mathrm{V}^{D}_{(5,1)}(3) = Q > \tau$ indicating HIGH output. Therefore, when D input is logic 1 ($> \tau$), Q is also equals to logic 1 ($> \tau$) (Figure 4.6).

Similarly, when input of tile A is logic 0 *i.e.* $\mathrm{V}^{A}_{(1,2)}(1) < \tau$, $\mathrm{V}^{A}_{(4,1)}(1) > \tau$. It activates glues $\{c - d\}$ and tile C attaches to tile A. Both diodes of tile C are forward biased, $\mathrm{V}^{C}_{(1,2)}(2) > \tau$, glue pair $\{g, h\}$ activates, and tile D attaches to the assembly at the node pair $\{1, 3\}$. It results to $\mathrm{V}^{D}_{(1,3)}(3) > \tau$, $\mathrm{V}^{D}_{(1,2)}(3) > \tau$, $\mathrm{V}^{D}_{(5,1)}(3) < \tau$ means $Q =$LOW. Also, $\mathrm{V}^{D}_{(7,9)}(3) < \tau$, $\mathrm{V}^{D}_{(7,8)}(3) < \tau$, and $\mathrm{V}^{D}_{(11,7)}(3) > \tau$, indicating $\overline{Q} = HIGH$. Thus, when D input is logic 0, the output Q is LOW and $\overline{Q}$=HIGH (Figure 4.7).

The circuit tile assembly model does not allow detachment *i.e.* once a tile is attached, it will not be detached even if the input falls below the threshold. Due to this

property, though the clock signal is alternating, it will not change the state of Q and $\overline{Q}$ output.

There are two more conditions to analyze:

1. Case I: When $D = V_0 = HIGH(> \tau)$, following steps occur:
   - Tile B attaches to Tile A, $\mathrm{V}^B_{(1,2)}(2) > \tau$,
   - Tile D attaches to tile B at node pair $\{7, 9\}$, $\mathrm{V}^D_{(7,8)}(3) > \tau$, $\mathrm{V}^D_{(11,7)}(3) < \tau$ ($\overline{Q} = 0$)
   - $\mathrm{V}^D_{(1,2)}(3) < \tau$, $\mathrm{V}^D_{(5,1)}(3) > \tau$ ($Q = 1$).
   - Now change the D input to logic zero ($< \tau$)
   - As the model do not allow detachment, the circuit configuration will not change. Still, $\mathrm{V}^B_{(1,2)}(2) > \tau$ due to the clock pulse which is $> \tau$ and dc source $V_2 = \tau$. Hence, the output still remains above τ, maintaining the previous potential condition, and $Q = 1$.
2. Case II: When $D = V_0 = LOW(< \tau)$, following steps occur:
   - Tile C attaches to Tile A, $\mathrm{V}^C_{(1,2)}(2) > \tau$,
   - Tile D attaches to tile C at node pair $\{1, 3\}$, $\mathrm{V}^D_{(1,2)}(3) > \tau$, $\mathrm{V}^D_{(5,1)}(3) < \tau$ ($Q = 0$)
   - $\mathrm{V}^D_{(7,9)}(3) < \tau$, $\mathrm{V}^D_{(11,7)}(3) > \tau$ ($\overline{Q} = 1$).
   - Now change the D input to logic one ($> \tau$)
   - $\mathrm{V}^A_{(4,1)}(1) < \tau$. But as detachment is not allowed, tile C still has a closed path for current flow. Clock pulse is giving positive signal and dc source $V_2 = \tau$ act as voltage supply. The voltage will drop across node pair $\{1, 2\}$ (across resistor R) and nodes $\{2, 4\}$ (across diode D_2 and βR). But as current path exists, $\mathrm{V}^C_{(1,2)}(2)$ remains positive (> 0).

- Due to the feedback connection, $\mathrm{V}^{C}_{(1,2)}(2) = \mathrm{V}^{D}_{(11,7)}(3) > 0$. It makes $\mathrm{V}^{D}_{(7,8)}(3) = 2\tau - \mathrm{V}^{D}_{(11,7)}(3) > 0$. This nodes $\{7, 9\}$ is connected to nodes $\{5, 1\}$ via feedback, making $\mathrm{V}^{D}_{(5,1)}(3) < \tau$ ($Q = 0$).

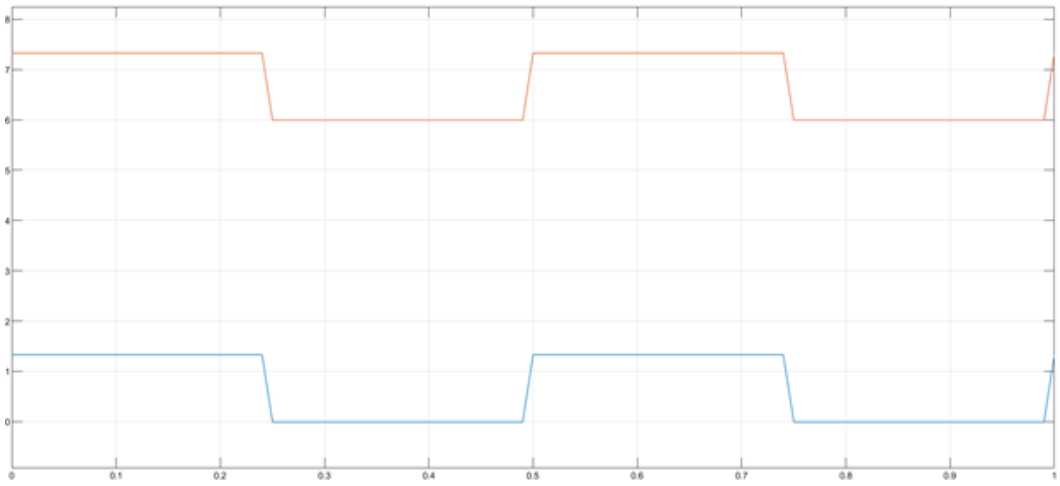
Figure 4.8 shows an example simulation for Case I and figure 4.6. Here $V_0 = 5$, $V_{in} = 3$V pulse train, $R = 1$, $\beta = 1000$, $\gamma = 1000000$, and $\tau = 1$. As D input is HIGH, Q output is HIGH as per figure 4.8(a). Then change the V_0 to 0.5 *i.e.* LOW. Still, the output Q is above τ (Figure 4.8(b)), indicating the Output Q remembers the previous logic state. Also, Figure 4.9 shows an example simulation for Case II and figure 4.7. Here, initial input is $< \tau$ resulted to $Q < \tau$. Then, input is raised to $> \tau$, still Q remains $< \tau$, showing the capability to remember the previous logic state.

These functionalities satisfy all the characteristics of a D flip flop and its truth table 4.1, and hence, the *bcTAM* model has the potential to build a sequential logic design.

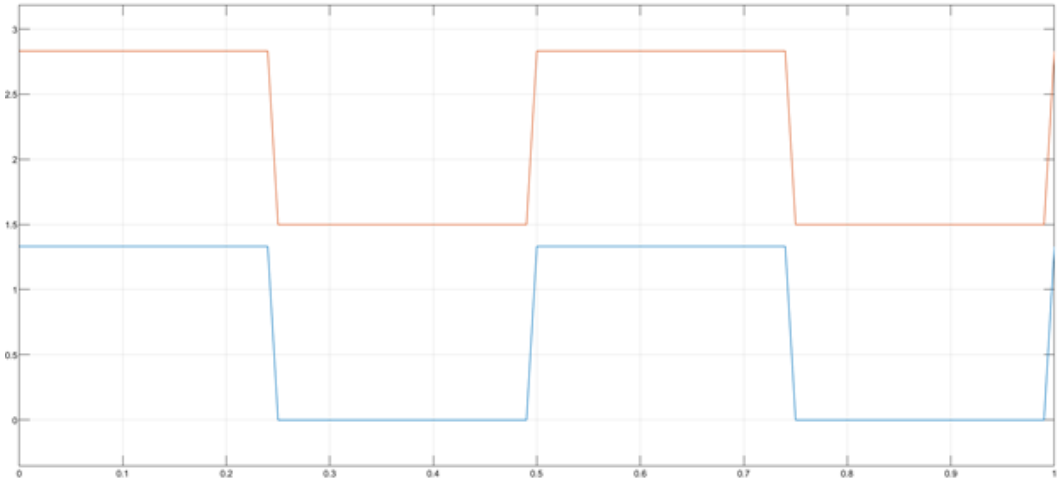
4.4 Conclusion and Future Work

Inspired by living systems, the circuit tile assembly model is built to achieve some interesting properties of life, such as self-assembly, self-controlled growth [10, 11], self-replication [12], and self-awareness [15]. This chapter focuses on another important property of life, *i.e.* memory. The evolution of any organism requires adjusting itself to the environmental changes, and thus, it needs to remember its previous responses. Our model focuses on capturing this quality. The bcTAM abstracts biological growth phenomenon, and having a memory will be a desirable addition. Thus, to achieve such interesting features of life with an inorganic system makes the cTAM a powerful model of computation.

In this chapter, a flip-flop is designed with the cTAM, the most common example of a sequential logic design. Thus, it can be considered as an initial step towards building a counter. The next problem of interest might be to build a counter with bcTAM and incorporating it to the rcTAM to generate a predefined number of

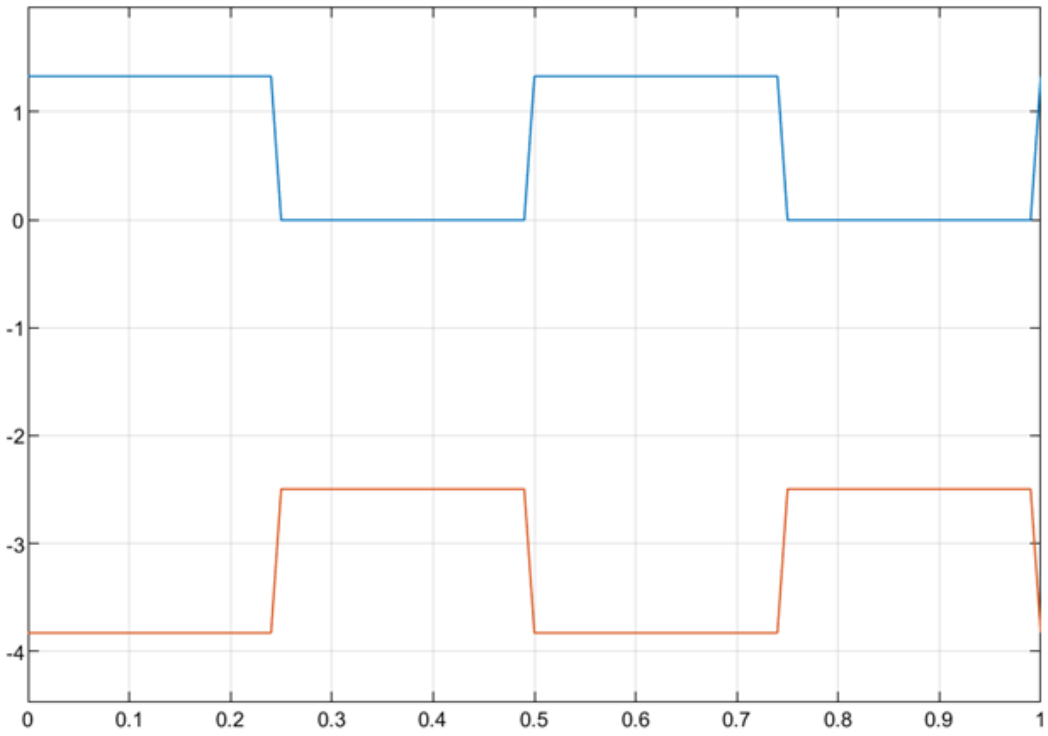


(a)

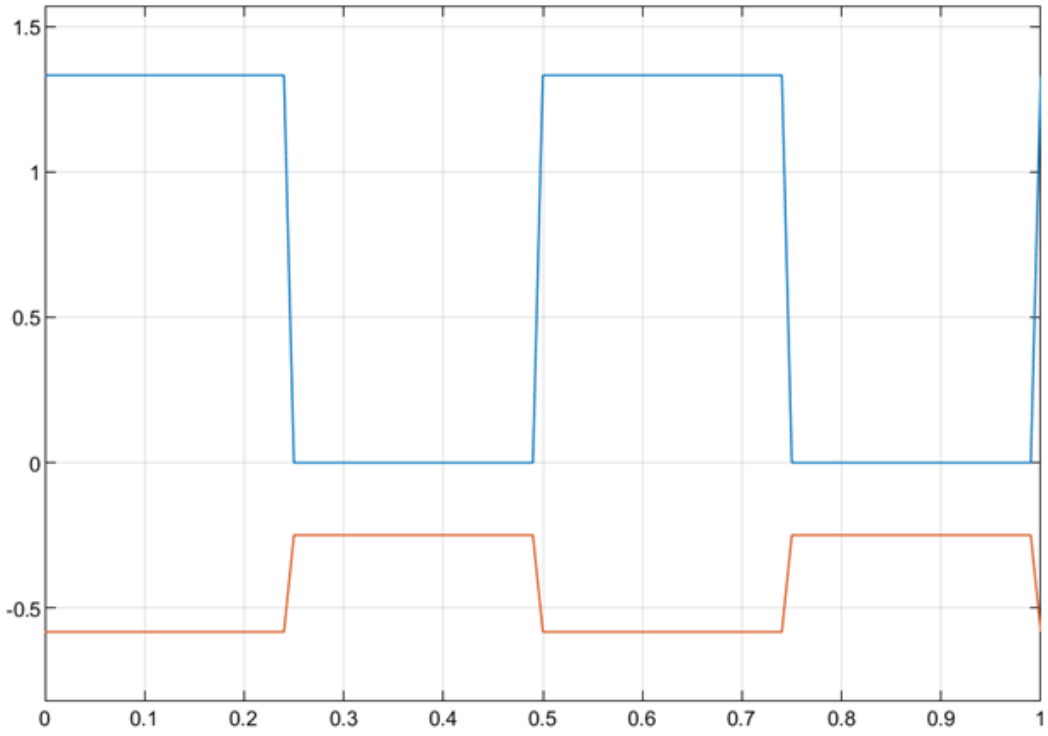


(b)

Fig. 4.8: The red line indicates Q output, and the blue line indicates clock signal. Figure (a) shows the Q output when the assembly grows for $V_0 = 5$ (HIGH). After the growth has completed, change the input to $V_0 = 0.5$ (LOW). Figure (b) shows that changing the input to logic zero, do not change the output Q to logic zero; Output still remains HIGH.



(a)



(b)

Fig. 4.9: The red line indicates Q output and the blue line indicates clock signal. Figure (a) shows the Q output when the assembly grows for $V_0 = 0.5$ (LOW). After the growth has completed, change the input to $V_0 = 5$ (HIGH). Figure (b) shows, changing the input to logic one, do not change the output Q to logic one; Output still remains LOW.

replications. A controlled-replicating model or finite replicating circuitry has the potential in nanomanufacturing to produce a finite number of products. Thus, the bcTAM model has prospects to study the self-assembly of nanostructures along with the analogs to a biological growth model that is dynamic and adaptive to the environment.

Chapter 5

Conclusion

5.1 Contributions of the Research

The living cell contains chemicals for energy and communication, is instrumented with environmental sensors, grows by consuming energy, self-replicates, and adapts to changes in its environment. Self-assembly systems attempt to capture the properties of living cells, which is the primary motivation behind the *cTAM*. All living organisms share some key characteristics, such as order, energy processing, response to the environment, homeostasis, development, reproduction, etc... These characteristics altogether serve to define life. Thus, to build a prototype model that captures some of the properties of life is a primary inspiration behind the development of the Circuit Tile Assembly Model.

Inspired by self-assembled biological growth, the cTAM is a powerful computational model that potentially contributes to understanding of bioelectric networks and information processing in biological systems. This dissertation investigates a family of *Circuit Tile Assembly Model's* with a focus on achieving advanced capabilities like computation or self-replication. To achieve the target, this work investigates two models of the cTAM: replicating cTAM(*rcTAM*) and Boolean cTAM(*bcTAM*). The cTAM investigates how electric signals propagate in the bioelectric cellular system and the impact of distributed signal strength [11]. The rcTAM achieves self-replication [12], and the bcTAM focuses on the capacity of logical decision-making [15]. The beauty of these models is their simplicity. Built with basic circuit components, they offer many interesting properties like replication, logical computation, and instant and distant communication. Therefore, this research has some potential to make a significant impact on bioelectric networks and nanotechnology.

Replication is a fundamental property of life and the basis of genetic integrity.

The study of the artificial self-assembly model that exhibits self-replication is a topic of long interest [60, 61, 63, 64, 107–110]. Much research is ongoing to find a prototype model that has certain properties of the living system, including self-replication [8, 21, 111–116]. To have self-replication with a self-assembly system is the prime focus of the rcTAM, presented in chapter 2. With simple electric circuitry, the rcTAM has achieved three important features of living organisms: self-assembly, bounded growth, and replication. On the supposition that living matter is self-assembled from nonliving components [69, 74](abiogenesis), the rcTAM is an interesting model that has some basic characteristics of life built with inorganic materials. Also, as described in chapter 2, the rcTAM provides an equivalent circuit for bioelectric intercellular communication. The cTAM abstracts signal propagation in a bioelectric network and the rcTAM focuses on how they replicate. Thus, the replicating circuit tile assembly model has applications to electrochemical growth processes at the nanoscale, and provides insight into self-replicating systems that are not necessarily composed of organic materials.

The next chapter presented another cTAM model, the *Boolean Circuit Tile Assembly Model (bcTAM)*, which is capable of Boolean computation. The chapter details a computationally complete set of Boolean gates implemented with the bcTAM. The bcTAM approximates axonal growth in neural networks, and thus, this model investigates the computational capability of a dynamic biological networks, for example, in growing networks of axons. Also, the model captures another significant property of life: self-awareness through sensing and responding to environmental conditions. The lengths of self-assembled ladders depend upon the input voltage and the voltage threshold for growth, which could represent sensory input and environmental conditions, like chemical or temperature gradients, respectively. Thus, the bcTAM can recognize environmental changes through those mechanisms, as well

as make Boolean decisions about its own growth. Therefore, the bcTAM exhibits a kind of self-awareness of its own growth.

Self-adaptation is a powerful skill for an organism to survive. Memory of its previous responses is required to have self-adaptation, whether that is encoded in evolutionary adaptation or biological networks. Chapter 4 focuses on having a system capable of remembering its state information within the family of cTAM. Also, the model advances toward building a counter with circuit self-assembly. A Flip flop is the building block of a memory device that is capable of saving its state. This chapter has built a system that can store its own information, like a flip flop, and represents the first steps toward a self-assembled memory within the cTAM models.

5.2 Future Work

This work can be extended to perform the following research tasks:

1. The rcTAM model is replicating in nature, and the growth continues as long as a supply of raw material exists. Having a finite number of replications is interesting from the perspective of manufacturing. It requires the ability to count. Thus, building a counter will be an important application of bcTAM.

2. In current models, once an attachment is made, detachment is not allowed. Detachment can be introduced so that when the differential voltage across output nodes is less than the threshold voltage, the tile will be detached. This behavior will make the cTAM model more dynamic and interesting, but also harder to analyze.

3. Incorporating the cTAM model into the smart grid by focusing on the self-healing property could be a potential research area. From the information of a grid monitored by line sensors, the fault location can be identified as the location with the worst impact. Adding a combination of resistors can minimize the impact of failure preventing the risk of propagating it to a blackout. The Circuit Tile

Assembly Model comes into the picture here, as the important feature of the cTAM is dynamic behavior. The cTAM model has self-controlled growth so that when the fault location is identified, it allows the grid to change the network, such as adding more resistors in the system. Therefore, the cTAM model might have prospects for a self-healing smart grid system.

4. Introducing reactive components, such as inductors or capacitors, is another interesting research area. Also, using a time-varying alternating source instead of DC will make the cTAM model closer to the bioelectric networks. Therefore, transient and ac analysis of the cTAM model are also future scopes of this study.

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