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ABSTRACT

The effect of the native silicon oxide layer on the passivation properties of Al_2O_3 on p-type Si surfaces has been investigated. This was done by comparing effective carrier lifetime, surface saturation current density, fixed charge, and density of interface states of samples, where the native oxide was not removed prior to Al_2O_3 passivation, with samples subjected to a 3 min HF-dip. The sample with the native oxide exhibits excellent surface passivation post-annealing, with a surface saturation current density of 13 fA/cm^2 and significantly longer effective lifetime compared to the sample, where the native oxide was removed. Capacitance–voltage measurements of a sample with the native oxide revealed a remarkably low density of interface states (10^{10} eV^{-1} cm^{-2}), almost three times lower than a sample where the native oxide was removed prior to Al_2O_3 deposition. The results indicate that a thin layer of native oxide improves the Al_2O_3 surface passivation of silicon.

I. INTRODUCTION

As microelectronic devices are continuously scaled down in size, the surface becomes an increasingly larger part of the device. For applications relying on the collection of excited charge carriers, minimizing surface recombination losses associated with the dangling bonds at the surface has become critical for device performance, particularly in the silicon-based photovoltaics, where cost reductions in recent years have been achieved by continuously reducing wafer thickness down to the current gold standard of 160 μm,[1] development made possible due to excellent passivation of the dangling bonds associated with the silicon surface.

Historically, two strategies have been employed to reduce surface recombination: reducing the number of electronically active defect states at the surface and/or reducing the presence of one type of charge carrier from the surface by creating an internal electric field.[2–8] Reducing the number of electrically active defects at the surface is assumed to be achieved by hydrogen or halide ions attaching to the dangling Si bonds at the surface, a process referred to as chemical passivation. Creating an internal electrical field is achieved by coating the surface with a material containing fixed charges, Q_{fix}, that repels charges of the same polarity and thus reduces the possibility for electron–hole recombination.

Surface passivation of p-type Si using ultrathin layers of Al_2O_3 by atomic layer deposition (ALD) has been employed in the state of the art PERC (passivated emitter rear contact) solar cells,[9] due to their high level of field-effect passivation by fixed negative charges ($Q_{fix} > 10^{12}$ cm^{-2}) and low interface defect density ($D_{it} \leq 10^{11}$ eV^{-1} cm^{-2}).[2,3,7,10]

The origin of the high Q_{fix} in Al_2O_3 was recently identified as Al-induced acceptor states at the interface between the deposited Al_2O_3 and the 1–2 nm thick SiO_2 that is unintentionally formed before and during the first cycles of Al_2O_3 deposition.[11–14] The states have been predicted to have an energy level 0.5–0.8 eV below the Si valence band edge that captures electrons from the Si substrate and that act as hopping sites for holes.[14] The Al-induced acceptor states have also been shown to reduce the electrically active D_{it} at the Si/SiO_2 interface, attributed to an interface defect *deactivation* mechanism that involves the discharge of the singly occupied dangling bonds (P_{b0} defects) into the acceptor states, without any need for passivation with H_2.[15]

The SiO_2 layer is thus required for the negative Q_{fix} in Al_2O_3, and the thickness, oxygen content, impurities, and structure of this layer should affect the surface passivation properties. Indeed, it has previously been demonstrated that thermally grown SiO_2 has a significantly reduced positive field-effect passivation compared to deposited SiO_2.[16,17] It has also been shown that the thickness of the layer can be used to tune the effective charge, Q_{eff}, enabling Al_2O_3 to also passivate n-type Si by still reducing D_{it}, while avoiding a negative inversion layer to form that causes minority carriers to be transported to poorly passivated or damaged areas.[18,19]

As it has become evident that the interfacial SiO_2 layer plays a crucial part in the Al_2O_3 passivation, it is of interest to investigate how the conditions under which the layer is formed have impact on the passivation properties. With a very few exceptions,[10] studies performed on the passivation properties of Al_2O_3 generally use some sort of pretreatment in order to achieve an H-terminated surface prior to deposition. In most cases, a standard or modified RCA procedure or a simple HF-dip has been employed. A study comparing HF-dip and a modified RCA pretreatment before Al_2O_3 deposition revealed minor differences in the minority carrier lifetime post-annealing;[20] however, an HF-dipped sample stored in a cleanroom for one week prior to deposition exhibited significantly improved lifetime, indicating that the native oxide may result in superior passivation properties. A completely untreated sample was not included in the study.

In the present study, the minority carrier lifetime, Q_{fix}, and D_{it} of Al_2O_3 deposited at 150 °C on p-type Si substrates and dipped in diluted HF for 3 min, is compared with untreated versions of the same wafer, i.e., the native oxide is still present. Al_2O_3 was carried out using H_2O and O_3 as oxidants, as this has previously been shown to result in the lowest surface recombination velocities.[21,22]

Comparing samples with SiO_2 formed under different conditions could provide more information on how SiO_2 affects the passivation properties of Al_2O_3 and whether it is beneficial to wait for the native oxide to regrow following an HF-dip, or even omit the HF-dip entirely for processes where that is an option, thus reducing processing steps and the use of HF. Improved surface passivation at a reduced cost would make Al_2O_3 more attractive for silicon passivation for any application relying on the collection of mobile charge carriers.

II. EXPERIMENTAL

The substrates that were used for the fabrication of the MOS capacitors in this study were cut from single side polished (SSP) p-type $525 \pm 20\,\mu m$ ⟨100⟩ oriented silicon wafers with a doping of $1.8–2.0 \times 10^{16}\,cm^{-3}$ from Siegert Wafer. The wafers were cut into $\sim 3\,cm^2$ pieces with a diamond pen. Two of the substrates were submerged in 2% HF solution for 3 min, followed by a ~1 min bubble rinse in DI water, labeled as "HF-dipped" from here on, while another two substrates received no further pretreatment, labeled as "no-HF" from here on. The unpolished side (back side) of all the substrates were contacted with ~180 nm Al by thermal evaporation.

The substrates were loaded into a Beneq TFS-200 ALD reactor preheated at approximately 125 °C. The reactor was evacuated and heated up to the deposition temperature of 150 °C. The time from the DI-H_2O rinse and until the samples were inside the reactor and evacuated is estimated to be 1–2 min. ALD deposition was carried out at a background pressure of 2 mbar. The deposition was preceded by an *in situ* 5 min O_3 pretreatment (30 cycles of 1 s O_3/9 s N_2) at the deposition temperature to remove potential organic contaminants and flush the O_3 line while the reactor temperature stabilized.

Al_2O_3 deposition was carried out using trimethyl-aluminum (TMA) (99.999%) from Strem chemicals, H_2O and O_3, with a pulse duration of 0.4/2/0.4/2/1/2.5 s for 145 cycles of TMA/N_2/H_2O/N_2/O_3/N_2, respectively. Native SiO_2 and deposited Al_2O_3 film thicknesses were determined with a J. A. Woollam ellipsometer in the 380–890 nm range. The Cauchy-model was used to parameterize the ellipsometry experimental data. Three measurements were performed at different locations on the surfaces of samples. The uncertainty provided in the reported thicknesses reflect the different thicknesses measured across the surface and includes the uncertainties in the fitted values. The SiO_2 thicknesses were fitted using the native silicon oxide model provided by the CompleteEASE software, which uses optical constants determined by Herzinger *et al.*[23]

Post-deposition, one HF-dipped and one no-HF sample were annealed in a tube furnace at 435 °C for 10 min in a forming gas. The temperature at the sample position was monitored with an external thermocouple.

Approximately 180 nm thick circular Al gate electrodes were deposited using shadow masks with holes diameters of ~1 mm by thermal evaporation. Optical microscopy and the resulting *CV* measurements revealed that the effective contact area is somewhat smaller than the hole diameter of the shadow mask. A contact area of $0.709\,mm^2$ was deduced and this value is used for the calculations performed in this study.

The impedance was measured at various probe frequencies in the range of 500 Hz–250 kHz, with an oscillation voltage of 30 mV using a Precision Impedance LCR Analyzer (4284 A, Agilent Technologies) in a parallel conductance mode. The samples were briefly illuminated prior to the voltage sweep, which were performed in darkness. The gate voltage was swept in ambient conditions from depletion (−5 V) to accumulation (3 V) and back again at a rate of 0.02 V/s.

The substrates that were used for lifetime measurements were $\sim 12\,cm^2$ double side polished p-type $500\,\mu m$ ⟨100⟩ oriented silicon wafers with a nominal resistivity of >5 kΩ cm from Topsil. Different substrates than the ones used for CV measurements had to be used as the 1–5 Ω cm substrates required for low series resistance in the bulk and back contact for the CV measurements exhibited too low bulk lifetime to observe surface recombination. Samples were prepared using the same pretreatment as for the CV measurement (HF-dip and no-HF) and Al_2O_3 was deposited on each side of the wafers simultaneously using the same deposition parameters. The effective minority carrier lifetimes were recorded by quasi-static photo conductance (QSSPC) using a Sinton Instruments WCT-120 post-deposition, and once again post-annealing in a tube furnace at 435 °C for 10 min in the forming gas (90% N_2/10% H_2).

III. RESULTS

The samples used for the *CV* measurements deposited on single-side polished (SSP) wafers were characterized by spectroscopic ellipsometry (SE) before and after back side contacting and

before and after the deposition. The measured thickness of the two HF-dipped samples less than 1 min after the bubble rinse was 0.6 ± 0.04 nm, and 0.7 ± 0.06 nm after back side contacting, similar to previously observed values.[24–27] The thickness of no-HF samples was 1.8 ± 0.2 nm before back side contacting and 1.9 ± 0.2 nm after. While the fit to the SE data was excellent using the optical constants for native SiO_2,[23] accurate thickness determination of such thin layers is considered unreliable below 1 nm due to the gradual change in the oxidation state of Si close to the interface. The chemical composition of this layer and the reactions that occur during the HF-dip, the DI-H_2O rinse, and the exposure to air has been extensively discussed previously.[24–31] Comparison of the native oxide thickness by SE and x-ray photoelectron spectroscopy generally suggest a small overestimation of the thickness by SE, and the error is considered to be on the fraction of a monolayer and thus acceptable.[32] The optical thickness obtained by SE is also highly reproducible and the value should thus be comparable with others using a similar model and differences in the measured SE thickness may be useful for understanding changes in lifetime, D_{it} and Q_{fix}.

After Al_2O_3 deposition, the extracted $Al_2O_3 + SiO_2$ thickness was 20.7 ± 0.05 nm for the HF-dipped samples and 21.3 ± 0.2 nm for no-HF samples. The actual Al_2O_3 thickness is not possible to determine precisely without knowing how much SiO_2 was grown during the deposition; however, for HF-dipped samples, previous studies observe SiO_2 thicknesses in the range of 1.0–1.4 nm post-Al_2O_3 depositions by ALD.[12,33–35] The Al_2O_3 thickness of the samples deposited on SSP substrates is thus likely to be ∼19.5 nm, indicating that there is little or no SiO_2 growth during the deposition for the no-HF samples. The film thicknesses post-annealing in the forming gas for 10 min at 435 °C were within the measured ranges before annealing for both samples. The thicknesses for the samples prepared on the DSP wafers are provided in Table S1 in the supplementary material.

Note that another set of samples were also prepared on CZ DSP wafers with a similar resistivity and from the same producer as the SSP wafers for lifetime determination by QSSPC. However, due to the low bulk lifetime of these wafers, both pretreatments resulted in the same lifetime of 600 μs over a wide injection level range post-annealing (Fig. S1 in the supplementary material), and FZ wafers with quoted bulk lifetimes of ∼20 ms were used instead in order to observe the effect of the pretreatments post-annealing (Fig. 1). The no-HF samples exhibit lifetimes approximately an order of magnitude longer both as deposited and post-annealing, reaching the bulk lifetime at low injection levels post-annealing.

The surface saturation current density, J_{0s}, used to quantify the passivation of the films, was extracted by the relation proposed by Kane and Swanson,[36]

$$\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{Auger}}} = \frac{1}{\tau_{\text{SRH}}} + 2\frac{J_{0s}(N_a + \Delta n)}{q n_i^2 W}, \tag{1}$$

where τ_{eff} is the measured effective excess carrier lifetime, τ_{Auger} is the intrinsic Auger lifetime,[37] τ_{SRH} is the defect-related bulk lifetime, N_a is the base doping level, Δn is the excess carrier density, q is the elementary charge, n_i is the intrinsic carrier concentration, and W is the wafer thickness. J_{0s} can be extracted from the slope of the linear fit of the inverse lifetime data in the high-injection region, provided that Shockley–Read–Hall and Auger recombination is negligible, available for these samples in Fig. S2 in the supplementary material. J_{0s} was determined to be 13 fA/cm^2 and 20 fA/cm^2 for the no-HF sample and HF-dipped sample, respectively. Note that J_{0s} is analogous to the more commonly reported emitter saturation current density, J_{0e}.[38] J_{0s} provides a better comparison of dielectric passivation quality than J_{0e} for samples without an emitter and with significant field-effect passivation.[8] The implied 1 sun open-circuit voltage, V_{oc}, was 712 mV for the no-HF sample and 657 mV for the HF-dipped sample. Previously reported values for Al_2O_3 passivation that resulted in a solar cell efficiency of 23.3% was J_{0e} = 29 fA/cm^2 and V_{oc} = 703.6 mV,[39] implying that the no-HF sample exhibits an excellent level of surface passivation.

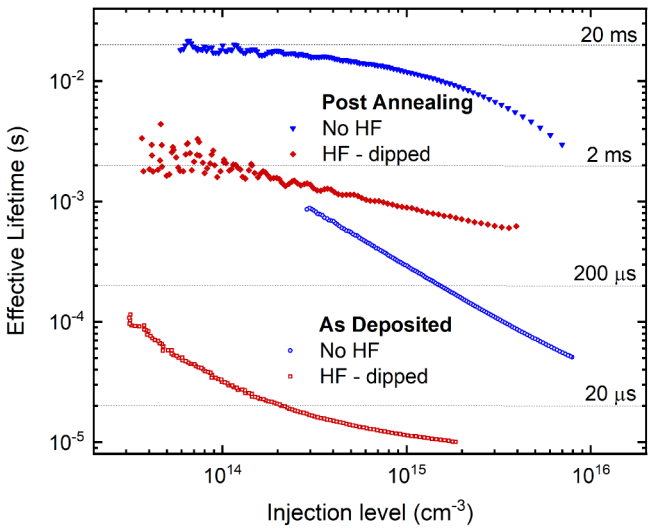

FIG. 1. Injection level-dependent effective lifetime of HF-dipped (red) and no-HF (blue) samples as deposited (open) and post-annealing (filled).

A bare no-HF reference wafer was annealed at the same conditions, with negligible improvement in the lifetime (Fig. S3 in the supplementary material), demonstrating that the annealed native SiO_2 by itself does not passivate the surface.

Capacitance–voltage measurements were performed to determine how the pretreatments affect Q_{fix} and D_{it}, and how these correlate to the observed lifetimes. The measured capacitance and conductance obtained from the parallel conductance mode, C_m and G_m, respectively, are not compensated for series resistance, R_s. The effect of series resistance on capacitance–voltage measurements is well established in the literature[40] and needs to be corrected for before any parameters can be extracted. R_s was determined by[41]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2}, \tag{2}$$

where C_{ma} and G_{ma} are the measured capacitance and conductance in accumulation, respectively, and ω is the angular frequency, $2\pi f$. The series corrected capacitance, C and G was then

determined by[41]

$$C = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2}, \tag{3}$$

$$G = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2}, \tag{4}$$

where

$$a = G_m - (G_m^2 + \omega^2 C_m^2)R_s. \tag{5}$$

The corrected CV and G/ω vs V data of an as-deposited, HF-dipped sample is presented in Fig. 2. The raw parallel conductance CV and G/ω vs V data are available in Fig. S4 in the supplementary material. The effective charge, Q_{eff}, was determined by first calculating the flatband capacitance, C_{FB}, given by

$$C_{FB} = \frac{C_{ox}\varepsilon_{Si}A/\lambda}{C_{ox} + \varepsilon_{Si}A/\lambda}, \tag{6}$$

where C_{ox} is the Al_2O_3 capacitance given by the corrected capacitance in strong accumulation, ε_{Si} is the relative dielectric constant of silicon assumed to be 1.03 F/cm,[42] A is the area of the gate electrode, and λ is the Debye length given by

$$\lambda = \frac{\varepsilon_{Si}k_BT}{q^2N_a}, \tag{7}$$

where k_B is the Boltzmann constant and T is the measurement temperature. The flatband voltage, V_{FB}, was then extracted by reading out the voltage at C_{FB}. Q_{eff} was finally calculated from[40]

$$Q_{eff} = \frac{C_{ox}(\varphi_{ms} - V_{FB})}{q}, \tag{8}$$

where φ_{ms} is given by

$$\varphi_{ms} = F_m - \chi_{Si} - \frac{E_g}{2} - \frac{k_BT}{q}\ln\left(\frac{N_A}{n_i}\right), \tag{9}$$

where $F_m = 4.08$ eV[43] is the work function of Al, and χ_{Si}, E_g, and n_i are the electron affinity (4.05 eV),[44] bandgap (1.12 eV), and intrinsic doping (9.65×10^9 cm^{-3})[45] of silicon, respectively. φ_{ms} was determined to be ≈−0.9 V for the samples used in this study.

The calculated Q_{eff} is the sum of all charges, including the fixed, mobile, and interfacial charges. To find the fixed oxide charge, Q_{fix}, which quantifies the contribution of Al_2O_3 to the field-effect passivation of Si, it is necessary to use CV data where only contributions from the fixed charge significantly affect V_{FB}. For this, a high frequency (hf) measurement is required as the filling and emptying of interfacial traps is too slow to follow the frequency and will eventually no longer contribute to the CV signal, as can be observed by the gradual shift in the capacitance with increased frequency in Fig. 2. The highest frequency used in this study, 250 kHz, was not high enough to completely avoid contributions from interfacial states, however, by calculating Q_{eff} for each frequency and fitting it to a double exponential (Fig. 3), it is possible to estimate what Q_{eff} would be at a given frequency. Letting f approach infinity for the as-deposited HF-dipped sample, $Q_{eff}(hf) \approx -4 \times 10^{12}$ cm^{-2} is obtained.

The contribution from mobile charges can be roughly estimated from the hysteresis that arises by first sweeping the voltage from inversion to accumulation and then back again to inversion

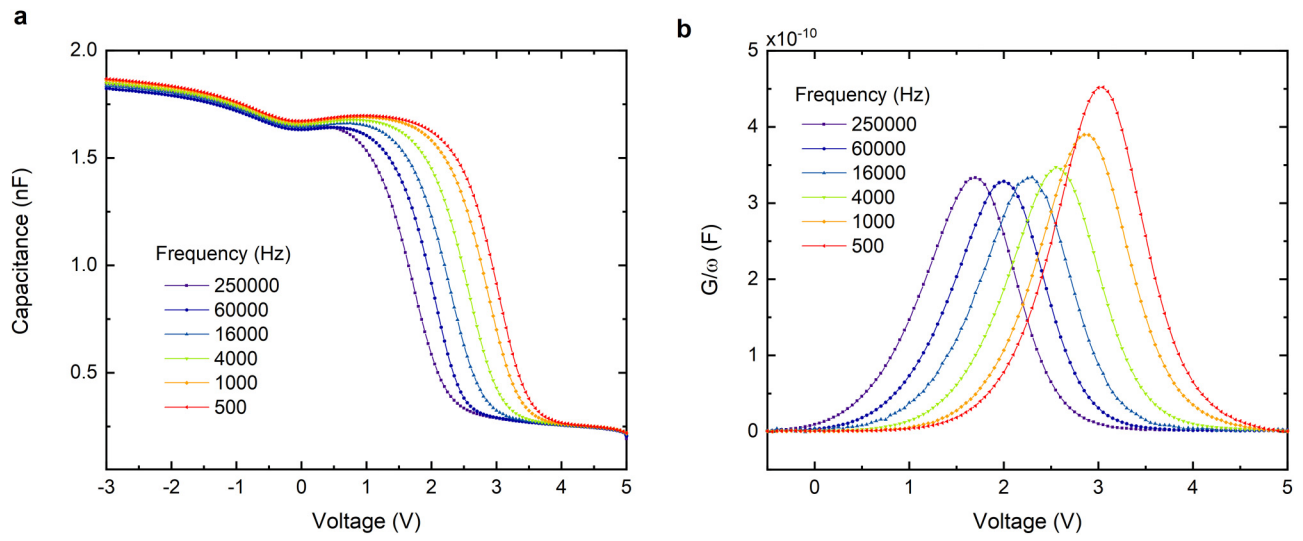

FIG. 2. CV (a) and G/ω vs V (b) of an HF-dipped as-deposited sample.

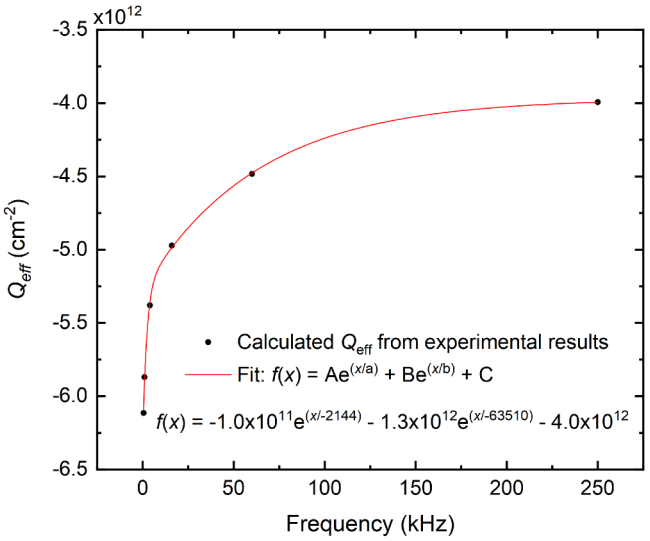

FIG. 3. Calculated Q_{eff} for each frequency in Fig. 2 and fitted to a double exponential in order to estimate Q_{eff} at high frequencies.

(Fig. S5 in the supplementary material). The hysteresis for the 250 kHz sweep was ~50 mV at V_{FB}, indicating that the contribution from mobile charges is negligible so that the approximation $Q_{eff}(hf) \approx Q_{fix}$ is valid, where Q_{fix} is the sum of positive fixed charges in SiO_2 and the negative fixed charges in Al_2O_3. The obtained value is in line with previously reported values of Q_{fix} for Al_2O_3 (-10^{11-13} cm^{-2}).[3,10,12]

There are several methods to determine D_{it}, but given the lack of real high and low frequency measurements, the optimal method was considered to be the conductance method devised by Hill and Coleman,[46]

$$D_{it} = \frac{2}{qA}\frac{\max\left(\frac{G}{\omega}\right)}{\left(\max\left(\frac{G}{\omega}\right)\frac{1}{C_{ox}}\right)^2 + \left(1 - \frac{C}{C_{ox}}\right)^2}, \quad (10)$$

where $\max(G/\omega)$ is the peak value of the largest peak in Fig. 2(b) and C is the corresponding capacitance at that voltage. D_{it} was determined to be 2.7×10^{12} ev^{-1} cm^{-2}, which is similar to previously reported values for as-deposited Al_2O_3.[47,48] Note that with $\max(G/\omega)$ occurring at the lowest frequency used, i.e., 500 Hz, it is probable that the actual maximum is at a lower frequency, so the value obtained is likely to be a small underestimation of the actual D_{it}.

The as-deposited no-HF sample exhibits similar behavior (Fig. 4), with the fit to Q_{eff} available in Fig. S6 in the supplementary material, and the values should thus be comparable. The estimated Q_{fix} and D_{it} for the as-deposited no no-HF samples was determined to be -4.7×10^{12} cm^{-2} and 2.0×10^{12} eV^{-1} cm^{-2}, respectively.

The no-HF sample exhibits both higher Q_{fix} and lower D_{it}, indicating that it will have a higher effective carrier lifetime than the HF-dipped sample, in agreement with the lifetime measurements presented in Fig. 1.

The *CV* and G/ω vs *V* measurements of the annealed samples are presented in Fig. 5. Post-annealing, there is no frequency dispersion in the depletion of the *CV* measurement for either of the samples, and the magnitude of the G/ω peaks have been reduced by approximately two orders of magnitude. Q_{fix} and D_{it} of the HF-dipped sample is calculated to be -3.6×10^{12} cm^{-2} and 2.7×10^{10} eV^{-1} cm^{-2}, respectively, while for the no-HF sample,

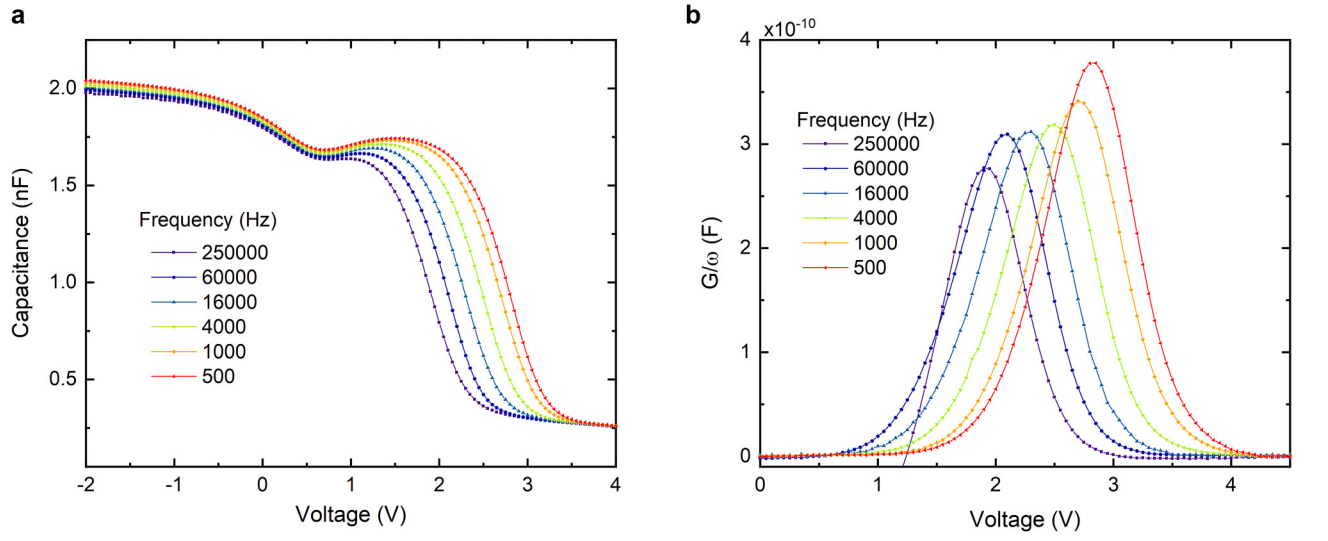

FIG. 4. *CV* (a) and G/ω vs *V* (b) of a no-HF sample as deposited.

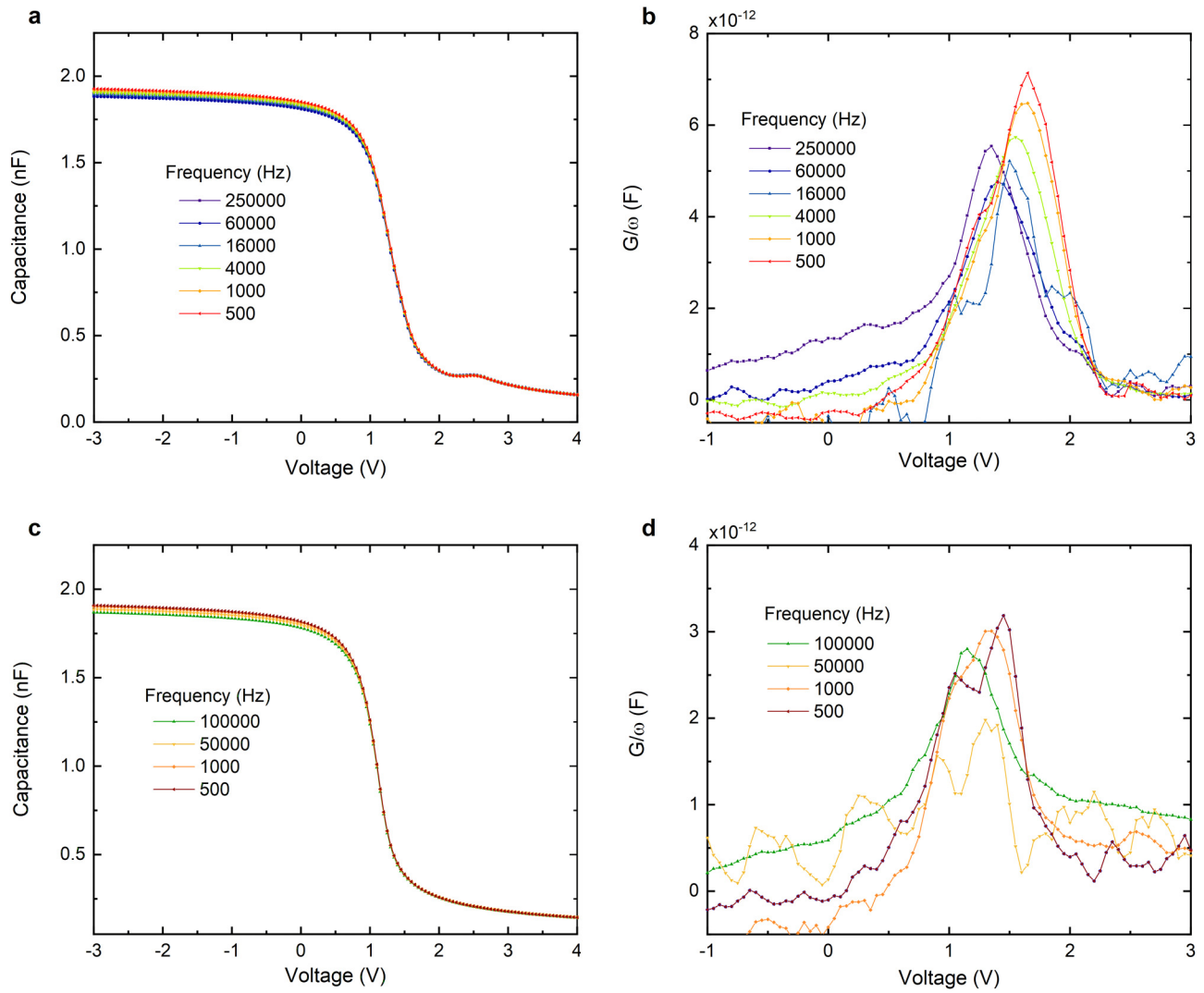

FIG. 5. *CV* (a) and *G*/ω vs *V* (b) of an annealed HF-dipped sample, and *CV* (c) and *G*/ω vs *V* (d) of an annealed no-HF sample. The 250 kHz *G*/ω vs *V* data for the HF-dipped sample are affected by an instrument error occurring at high frequencies that are not accounted for by the parallel conductance model.

$Q_{fix} = -3.3 \times 10^{12}\,cm^{-2}$ and $D_{it} = 1 \times 10^{10}\,ev^{-1}\,cm^{-2}$. A summary of the results obtained in this study is presented in Table I.

Q_{fix} has been reduced post-annealing for both pretreatments, particularly for the no-HF sample, while D_{it} is reduced by around two orders of magnitude for both samples. As the lifetime increases dramatically post-annealing, it indicates that a Q_{fix} of $\sim -3 \times 10^{12}\,cm^{-2}$ provides sufficient field effect passivation, and that the reduction in interface states is the main factor for the

TABLE I. Summary of results—fitted thicknesses before and after deposition, and estimated Q_{fix} and D_{it} for as-deposited and annealed samples deposited on SSP substrates for both pretreatments.

Pretreatment	Thickness before deposition (nm)	Thickness post-deposition (nm)	Annealing	Q_{fix} (cm^{-2})	D_{it} ($eV^{-1}\,cm^{-2}$)
3 min HF dip	0.7 ± 0.06	20.7 ± 0.05	⋯	-4.0×10^{12}	2.7×10^{12}
⋯	1.9 ± 0.2	21.3 ± 0.2	⋯	-4.7×10^{12}	2.0×10^{12}
3 min HF dip	0.7 ± 0.06	20.7 ± 0.05	10 min FG 435 °C	-3.6×10^{12}	2.7×10^{10}
⋯	1.9 ± 0.2	21.3 ± 0.2	10 min FG 435 °C	-3.3×10^{12}	1.0×10^{10}

improvement in lifetime. The no-HF sample has a D_{it} 2.7 times lower than the HF-dipped sample, in agreement with the improved lifetime observed for the no-HF sample used for the QSSPC measurements.

IV. DISCUSSION

The QSSPC data show that the lifetime for HF-dipped sample is approximately an order of magnitude less than the no-HF sample both as-deposited and post-annealing, while J_{0e} is significantly increased. With the pretreatment being the only difference between the samples, it is evident that it has a significant effect on the performance of the passivation layer.

The purpose of the HF-dip and similar pretreatments, like the standard RCA procedure, is to achieve a clean hydrophobic H-terminated silicon surface and remove impurities present in the native SiO_2; however, the exact state of the surface following an HF-dip depends on several variables. For example, it has previously been determined that the surface is primarily H-terminated after an HF-dip, with 10%–50% F-termination.[28,30] During the DI-H_2O rinse, any F bonded to the surface is replaced by OH, and condensation of OH in air results in Si–O–Si formation, which leads to SiO_x growth.[27] There are numerous studies on native oxide growth and surface analysis following an HF-dip or DI-H_2O rinse, indicating or demonstrating that the ratio of OH- and H-terminated Si, and hence the SiO_x growth rate, depends on the Si surface orientation,[27] doping concentration,[24] dissolved oxygen concentration in the HF solution,[49,50] HF-concentration and pH,[31] dip duration, rinse-duration,[27] illumination,[31] and dissolved oxygen content in the rinsing water.[24] Achieving an exclusively H-terminated surface while using a DI-H_2O rinse and allowing for air exposure prior to Al_2O_3 deposition, is unrealistic without, e.g., H_2S treatment to exchange the adsorbed OH with H. TMA is also known to react poorly with H-terminated Si, resulting in low deposition rates during initial ALD-cycles and island growth formation,[51,52] indicating that the TMA primarily reacts with OH-terminated Si. Any H-terminated Si likely needs to be oxidized before the reaction with TMA will take place, which is why 1–2 nm of SiO_x at the interface between Si and Al_2O_3 is unavoidable, even for H-terminated Si regardless of Al_2O_3 thickness, as observed by transmission electron microscopy.[10,33,34,53] *In situ* ellipsometry has shown increased growth rates during the first cycles of an ALD-Al_2O_3 deposition,[12] despite the reduced Al_2O_3 growth rate during the initial ALD-cycle, indicating that the majority of the SiO_2 growth occurs during this process step. As some amount of the surface will be OH-terminated for an HF-dipped sample, some TMA will chemisorb and Si–O–Al–CH_2 bonds will form, while the H-terminated Si will be less reactive toward TMA. During the H_2O and O_3 pulse, a mixed oxide phase will form, containing both SiO_x and AlO_x, in agreement with previous secondary ion mass spectrometry results.[54] The SiO_x layer should thus contain more Al than the native oxide layer formed in air and will possibly also contain more carbon impurities stemming from the TMA precursor.[55]

The SE results indicated that the total film thickness post-deposition was only slightly less for the HF-dipped sample compared to the no-HF sample. This indicates that the SiO_2 growth previously observed during the first ALD-cycles is significantly reduced if there already is a >1.9 nm SiO_2 layer present on top of the silicon substrate. The likely reason being that the native SiO_2 present on the no-HF sample is impeding further oxidation of the underlying Si.

As the SiO_2 thickness is similar for both pretreatments, while the QSSPC and CV measurements show significant differences in lifetime and D_{it}, the results suggest that the SiO_x grown at the start of the deposition forms a poorer interface with Si and/or Al_2O_3 than the native oxide formed at ambient conditions. The reason could be that the mixed SiO_x-AlO_x interface reduces H-diffusion through the layer, resulting in more P_{b0} defects.

The differences in oxidizing agent and temperature, i.e., 20 °C in air vs 150 °C in H_2O and O_3 for the HF-dipped one, may also affect the oxygen content in SiO_x and positive fixed oxide charge formation. This is probable considering thermally grown SiO_2 has a significantly reduced positive field-effect passivation compared to deposited SiO_2,[16,17] so it is also reasonable to assume that there will be a difference in the field-effect of the native SiO_2 and the one grown during deposition, which could also explain small differences observed in Q_{fix} in the as-deposited samples. Finally, dissolved oxygen content in the HF-solution has been shown to have a significant impact on defect formation at a low pH due to oxidation of Si, resulting in small amounts of Si dissolving and increased surface roughness.[49] It is possible that a 3 min 2% HF dip may not only etch the oxide, but also etch a small amount of Si, resulting in increased surface roughness.

Post-annealing, Q_{fix} is slightly reduced for both pretreatments. This has been observed previously,[4] but more commonly, an increase in Q_{fix} is observed. Hoex *et al.* previously observed significantly smaller increases in Q_{fix} post-annealing for Al_2O_3 layers with a thickness of 32 nm, compared to samples with 6 and 11 nm thickness, and proposed that this could be due to the longer deposition time causing an effect similar to that of annealing.[56] In this study, the use of O_3 increases the deposition time by ~40% relative to the standard process that only uses H_2O as an oxidant. This could thus be one of the reasons for the large Q_{fix} in the as-deposited samples, as the use of O_3 has previously been shown to have a beneficial effect on the minority carrier lifetime,[21,22] and that the use of O_3 increases the amount of Q_{fix} in the as-deposited sample.

As the Q_{fix} is reduced post-annealing and not simply unchanged, it indicates the SiO_2 thickness increases slightly during annealing. Previous studies on similar samples show that the SiO_2 thickness increased by ~0.2 nm when annealed in the forming gas,[33] and as SiO_2 has a slight positive fixed charge, this would result in an overall decrease in Q_{fix}. However, the total film thickness did not change during annealing for the samples investigated in this study. If the SiO_2 thickness has increased without the total film thickness changing, it implies that the density of the Al_2O_3 film has increased during annealing, which previous results also seem to indicate,[35] and which is consistent with the observed increase in capacitance and the reduced negative Q_{fix} observed post-annealing.

As the differences in Q_{fix} are minor, both between the two pretreatments and between the as-deposited and annealed samples, while the changes in lifetime are large, it is our interpretation that the differences in D_{it} between the HF-dipped and no-HF sample and the sharp reduction in D_{it} observed post-annealing has a larger significance for the lifetime.

It is evident that obtaining a Si–Al_2O_3 interface without a SiO_x interface layer in between is not readily achieved by performing the usual pretreatments, and the effect of the pretreatments using HF is thus primarily replacing the native oxide with an oxide formed under different conditions and that contains significant amounts of Al. The results obtained in this study indicate that the process used for the HF-dipped samples result in more electrically active interface states. The native oxide and the deposited Al_2O_3 used in this study yields excellent surface passivation in line with the lowest D_{it} values reported for Al_2O_3,[3] and with similar J_{0s} as that of high-efficiency solar cells.[57] So while excellent surface passivation has been achieved using HF pretreatments before, the results in this study indicate that using any type of pretreatment that removes the native SiO_2 should thus be performed with care, and may not only be unnecessary, but is likely to have a negative impact on device performance. For processes where a thick surface layer has to be removed prior to the surface passivation process, e.g., $POCl_3$ diffusion, it may be beneficial to wait for a thin native oxide layer to grow before the Al_2O_3 deposition is performed.

V. CONCLUSION

The minority carrier lifetime, Q_{fix}, and D_{it} of samples subjected to an HF-dip prior to Al_2O_3 passivation, has been compared with samples where the native oxide was not removed. An excellent surface saturation current density of 13 fA/cm^2 was observed post-annealing in the forming gas at 435 °C for the sample with a native silicon oxide layer, while the sample where this layer was removed prior to Al_2O_3 deposition exhibited lower lifetime, both as deposited and post-annealing and exhibited a higher J_{0s}.

CV measurements on highly doped wafers receiving similar pretreatments revealed lower D_{it} in samples with the native oxide compared to samples where the native oxide was removed, both as deposited and post-annealing, which could explain the observed differences in lifetime.

The results indicate that D_{it} has a larger impact on the carrier lifetime than Q_{fix}, and that the SiO_x that is formed during deposition results in a higher D_{it} compared to the native oxide. The standard procedure of removing the native oxide prior to Al_2O_3 passivation may, based on these results, reduce the lifetime of excited charge carriers and increase D_{it} and thus reduce device performance.

SUPPLEMENTARY MATERIAL

See the supplementary material for additional sample information, measurements on reference samples, raw measurement data, and measurement data that support findings in the article without being critical to the drawn conclusions.

AUTHORS' CONTRIBUTIONS

M.N.G. contributed to the investigation, data curation, writing—original draft, visualization. M.P. contributed to the funding acquisition, resources, supervision, writing—review and editing. E.M. contributed to the resources, supervision, writing—review and editing.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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