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MODELING AND CONTROL OF DIRECT-CONVERSION HYBRID SWITCHED-CAPACITOR DC-DC CONVERTERS

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MODELING AND CONTROL OF DIRECT-CONVERSION HYBRID SWITCHED-CAPACITOR DC-DC CONVERTERS

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ABSTRACT

Efficient power delivery is increasingly important in modern computing, communications, consumer and other electronic systems, due to the high power demand and thermal concerns accompanied by performance advancements and tight packaging. In pursuit of high efficiency, small physical volume, and flexible regulation, hybrid switched-capacitor topologies have emerged as promising candidates for such applications. By incorporating both capacitors and inductors as energy storage elements, hybrid topologies achieve high power density while still maintaining soft charging and efficient regulation characteristics. However, challenges exist in the hybrid approach. In terms of reliability, each flying capacitor should be maintained at a nominal 'balanced' voltage for robust operation (especially during transients and startup), complicating the control system design. In terms of implementation, switching devices in hybrid converters often need complex gate driving circuits which add cost, area, and power consumption.

This dissertation explores techniques that help to mitigate the aforementioned challenges. A discrete-time state space model is derived by treating the hybrid converter as two subsystems, the switched-capacitor stage and the output filter stage. This model is then used to design an estimator that extracts all flying capacitor voltages from the measurement of a single node. The controllability and observability of the switched-capacitor stage reveal the fundamental cause of imbalance at certain conversion ratios. A new switching sequence, the modified phase-shifted pulse width modulation, is developed to enable natural balance in originally imbalanced scenarios. Based on the model, a novel control algorithm, constant switch stress control, is proposed to achieve both output voltage regulation and active balance with fast dynamics. Finally, the design technique and test result of an integrated hybrid switched-capacitor converter are reported. A proposed gate driving strategy eliminates the need for external driving supplies and reduces the bootstrap capacitor area. On-chip mixed signal control ensures fast balancing dynamics and makes hard startup tolerable. This prototype achieves 96.9% peak efficiency at 5V:1.2V conversion and a startup

time of $12\mu s$, which is over 100 times faster than the closest prior art.

With the modeling, control, and design techniques introduced in this dissertation, the application of hybrid switched-capacitor converters may be extended to scenarios that were previously challenging for them, allowing enhanced performance compared to using traditional topologies. For problems that may require future attention, this dissertation also points to possible directions for further improvements.

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Chapter 1

Introduction

The use of electric energy has enabled various innovations that have shaped modern society: from light bulbs, to computing and communications, consumer, industrial, and automotive electronics. Since generation and consumption of electricity usually does not happen at the same location, at the same voltage, or even with the same form of electric power (AC or DC), there is a near-universal need for power conversion electronics.

This work focuses on power converters that interface between two DC voltages. The necessity for power conversion arises from different characteristics of the source end (input) and the load end (output). In data centers, for example, a high bus voltage (usually 48V) helps reduce supply current and thus the ohmic loss [1], whereas the processor load may require a voltage as low as 1V to minimize power consumption, maximize performance, or simply maintain a voltage suitable for modern deep-submicron semiconductor technologies. DC-DC converters alter the supply voltage level to another that is suitable for the load, ideally without dissipating energy, and may provide other functions such as regulation of voltage, current, or power.

Defined as the ratio of the output power to the input power, efficiency is one of the most important metrics of DC-DC converters. A higher efficiency indicates that more of the input power is delivered to the load while less is dissipated, often in the form of heat. This

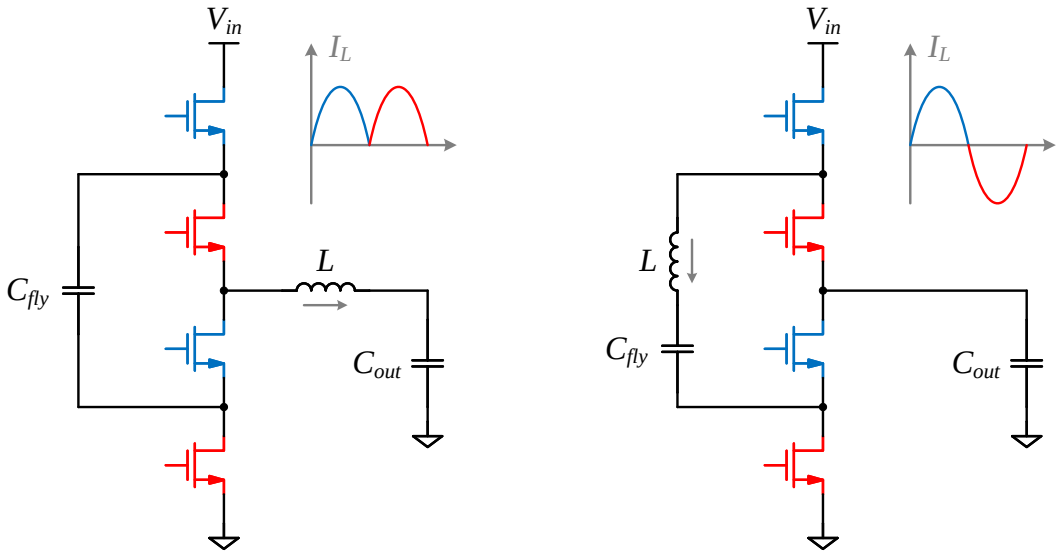
helps conserve energy and limit temperature increase. Power density is another important metric that describes the power handling capability per unit area or volume of the converter. It is especially emphasized in applications where the physical size is minimized, such as in portable electronic devices. Regulation characteristics also need attention if the converter is designed to maintain a desired output despite disturbances or changes in input or output conditions. In some cases, a wide range of input or output conditions must be tolerated with minimal effect on efficiency or power dissipation.

Among various DC-DC conversion architectures, the buck topology is probably the most basic and prolific [2]. It uses two semiconductor switches to generate a pulse-width modulated (PWM) waveform, which is then passed through an inductive low-pass filter to arrive at a DC output voltage. However, the achievable energy density of inductors is relatively low, specifically, it is 3 to 6 orders of magnitude lower than that of capacitors [3]. This disadvantage impacts magnetic-based converter class, including buck, leading to challenges on converter design. Using low-energy-density inductors to process a certain amount of energy requires either large physical size or high switching frequency, penalizing power density and efficiency, respectively.

Another DC-DC converer class, comprising switched-capacitor (SC) topologies, uses capacitors as energy storage components and therefore show better performance in size-constrained applications [4, 5, 6]. However, SC topologies suffer from the intrinsic hard charging loss [7], which happens when capacitors with different voltages are connected. In addition, though SC converters have high performance when the conversion ratio is close to one or several nominal points, flexible output voltage regulation is usually achieved at the cost of increased output impedance, similar to a linear regulator, which hurts the efficiency [8]. An alternative approach is to adopt multi-ratio (gear box) architectures, however, the implementation also requires additional space, degrading the power density [9].

1.1 Hybrid Switch-Capacitor Converters

The hybrid switched-capacitor converter class involves the addition of inductor(s) or inductive impedance(s) to SC topologies [10, 11, 12, 13, 14], or from another perspective, the addition of flying capacitor(s) to inductor-based topologies [15, 16], leading to combined advantages of both conventional classes. The inductor(s) achieve soft charging of flying capacitors and enable efficient regulation characteristics; the capacitor(s) boost the average energy density of passive components thus reducing the overall volume [17].



(a) direct type. (b) indirect type.

Figure 1.1: Example of the two types of 2:1 hybrid SC topologies.

While many hybrid SC topologies are explored in the literature [18, 19, 20, 21, 22, 23, 24], they can generally be segmented into either 'direct-conversion' or 'indirect-conversion' architectures [25]. Illustrated in Figure 1.1 for the simplest nominal 2:1 step-down cases, direct type architectures have a defining characteristic that one terminal of the inductor is directly coupled to an input or output terminal; indirect type topologies have inductor(s) in a permanent series configuration with flying capacitors. In resonant mode, inductor current of both architectures exhibit sinusoidal trajectory (full wave for indirect type and rectified

for direct type), and the voltage conversion ratio (VCR) is nominally determined by the SC network. Regulation of direct type topologies can be achieved by pulse width modulating the voltage seen by the inductor, similar to the case of magnetics-based topologies. However, regulation of indirect type topologies needs more complicated approaches such as off-time modulation [26, 27, 28], quasi-resonant operation [29], and phase-shift control [30]. This work primarily discusses the direct-conversion hybrid SC topologies.

Many benefits of hybrid (resonant) switched capacitor converters have been discussed and demonstrated in the literature. Compared to pure SC topologies, resonant and hybrid topologies can achieve lower effective output resistance (R_{eff}) at resonant frequency, reducing the conduction loss [31]. Alternatively speaking, when approaching the minimum R_{eff}, the switching frequency of hybrid SC converters is lower than the SC counterparts, reducing the switching loss [32, 33]. Compared to conventional buck converters, even with a conservative estimation of energy density ratio between capacitors and inductors, hybrid SC topologies have significantly smaller passive component volume [34]. Additionally, a multi-objective optimization and comparison showed that hybrid SC converters outperform buck converters in terms of losses and total volume in many realistic scenarios [35].

While showing promising performance, hybrid SC topologies face challenges in practical implementation, one of which being flying capacitor voltage imbalance [36, 37, 38]. In pure SC converters, flying capacitor voltages are rigidly constrained by Kirchhoff's Voltage Law (KVL): charge is transferred through pure capacitive loops (including flying capacitors and bypass capacitors), which show simple dynamics and lead to a unique (balanced) voltage on each flying capacitor. However, in hybrid topologies, the charge transfer path typically links an inductor, which breaks the pure capacitive loops and increases the order of dynamics. Flying capacitors become independent energy storage elements and their unique (balanced) voltages are no longer guaranteed. Due to either external disturbances or intrinsic mechanisms, flying capacitor voltages may deviate from their balanced level [39, 40, 41, 42, 43]. This imbalance can cause increased ripple quantities and switch

voltage stress, penalizing efficiency and reliability. Hence, modeling the flying capacitor voltage dynamics and developing active balancing control algorithms have been appealing research topics to enable wider application of hybrid SC converters.

Another challenge associated with the hybrid SC topology is the complexity of gate driving. Since most transistors in hybrid SC converters have a floating reference, each of them requires its own bootstrap capacitor or even voltage source to supply the gate driver [27, 44]. The large number of switches further complicates the design, especially for integrated converters, because this translates to either increased number of off-chip components or reduced on-chip power density.

1.2 Review of Related Work

Examples of innovations that have inspired hybrid SC architectures date back to at least 1984, when a large conversion ratio topology without transformer was proposed in [45]. Based on a Ćuk converter, multiple flying capacitors were incorporated to scale down the voltage across the inductors and to provide part of the conversion ratio. In 1992, Meynard introduced the multilevel buck or flying capacitor multilevel (FCML) converter [46]. While originally targeted at high-voltage multilevel conversion, the hybrid SC topology started to show potential in low-voltage applications as the volume of passive components became a bottleneck of high-density power delivery.

The series-capacitor buck topology was developed in 2005 to achieve high conversion ratio: a peak efficiency of 94.1% was obtained at 12V:1.2V [47]. An early implementation of monolithic hybrid SC converter in 2008 adopted 3-level buck architecture, achieving 69.7% peak efficiency with 5.01 mm^2 area [48]. Another fully-integrated 3-level converter improves the peak efficiency to 77% and peak power density to 0.2W/mm^2 [49]. Hybrid SC topologies also found application in photovoltaic power management [11] and energy harvesting [50] with over 95% efficiency. Switching at 10MHz, a merged two-stage hybrid

SC converter reached 81% peak efficiency at 5V:1V conversion [19]. A highly integrated hybrid series-parallel converter achieved 87% peak efficiency at 12V:3.7V [29].

More recent studies have demonstrated state-of-the-art performance in computing as well as point of load (PoL) applications. For discrete designs, a 48V:12V cascaded hybrid SC converter with resonant operation achieved 99.0% peak efficiency and 4kW/in^3 power density [51]; a 48V:1V hybrid SC converter with vertically stacked architecture achieved 91.1% peak efficiency and 1kW/in^3 power density [52]. For integrated designs, a 12V:1V hybrid SC converter with double step-down architecture reached 92.1% peak efficiency and 0.48W/mm^2 power density [53]; a monolithic 2:1 hybrid SC converter using on-chip merged LC resonator obtained 85.5% peak efficiency and 0.1W/mm^2 power density [27].

Modeling techniques for hybrid SC converters are almost as old as the converter class itself. Soon after FCML converters were invented, a frequency domain model based on harmonic analysis was proposed in 1997 to investigate the steady state voltage on flying capacitors [54]. Still in the frequency domain, [55] extended the scope to transient analysis by decomposing the topology into two-port switching circuits, showing the convergence speed of flying capacitor voltages. Later, approaches involving time-domain averaging were used to simplify calculations and provide more insights on oscillation in the balancing process [56]. Discrete-time state space modeling proved to be powerful tools to analyze switching-mode converters [57, 58]. More specifically for hybrid SC converters, a state-space model was used to investigate the influence of input impedance on flying capacitor voltage dynamics [39]. An augmented state-space approach that assumed piecewise linear inductor current was derived in [40] to explore the impact of more complex nonidealities. A phase-transition state space model was proposed for FCML converters in [43], showing accurate estimation of both steady state and startup characteristics.

The challenge of maintaining flying capacitor voltage balance also motivated various explorations. In the early history of hybrid SC converters, safe operation primarily relied on natural balance. It was first proved in [54] that natural balance in FCML converters has

the potential to automatically regulate flying capacitor voltages. However, [42] found that natural balance does not work at certain duty cycles, and conditions which guarantee natural balance were analytically derived. Natural balance was also found to be highly sensitive to circuit operating conditions and parasitic resistances, therefore, it may not be sufficiently reliable in many practical applications. In 2002, active balance was first described in [59] to control flying capacitor voltages in the presence of rapid input voltage transients. Later, a practical current-limit balancing control algorithm was implemented in [60] to balance a 3-level hybrid converter. An improved analytical treatment of current-limit balancing control with mathematical proof was developed in [61] and [62], which also extended this method to FCML converters with multiple switching cells. Proposed in [63], the constant effective duty cycle control overcome the challenge of balancing flying capacitors at light load. Other variations on current limit control were also explored to improve the stability and transient response, [64, 65, 66, 67]. Recently, a novel voltage-mode algorithm, modified ripple injection control, was proposed to achieve both flying capacitor balance and output voltage regulation for FCML converters, and it can be potentially applied to other direct hybrid SC topologies [68].

1.3 Dissertation Outline

The rest of this dissertation is organized as follows. In Chapter 2, a discrete-time state space model is derived by treating direct hybrid SC converters as two sub-systems, the switched capacitor stage and the output filter stage. The model for the two subsystems are first individually derived then merged. Investigation of the controllability and observability of the SC stage provides intuitive explanation for many characteristics of direct hybrid SC converters, such as natural balancing. This model also serves as the foundation of various explorations in the following chapters.

In Chapter 3, the state-space model is averaged then applied to the design of a state

estimator, which extracts all flying capacitor voltages from the measurement of a single node. Furthermore, it is proved that in scenarios where the SC stage is uncontrollable and unobservable, all balancing mechanisms (including natural balance and active balance) would fail. A straightforward method to rectify this issue, which requires modifying the sequence of switching states of the converter, is also proposed and implemented.

In Chapter 4, based on the state-space model, a new control algorithm for direct hybrid SC converters, the constant switch stress (CSS) control, is presented. It achieves both active balancing and output voltage regulation, featuring fast transient response and simple implementation. Not requiring complicated current-sensing or signal processing circuit, the basic function of CSS control can be realized with only 2 comparators and a digital logic circuit. Experimental results show robust operation and fast response to both load and line transients.

Chapter 5 presents an integrated hybrid SC converter prototype for universal serial bus (USB) powered computing applications. This design uses cascaded architecture to achieve high step-down ratio but does not require intermediate bypass capacitors. Advanced gate driving strategy eliminates the need for external driving supplies and reduces the area of bootstrap capacitors. The on-chip non-linear control maintains flying capacitor voltage balance and ensures fast transient response. Experiments show 96.9% peak efficiency at 5V:1.2V conversion and a startup time of 12μs.

Finally, Chapter 6 concludes the dissertation and summarizes the main contributions. Promising future research directions are also highlighted.

Chapter 2

Discrete-Time State Space Model

In this chapter, a discrete-time state space model is developed to analyze direct-conversion hybrid SC converters, with a focus on the flying capacitor multilevel (FCML) topology. The primary purpose of this model is to explore fundamental principles that govern flying capacitor voltage dynamics. The model can also serve as a fast simulator for both transient and steady state characteristics of direct hybrid SC converters.

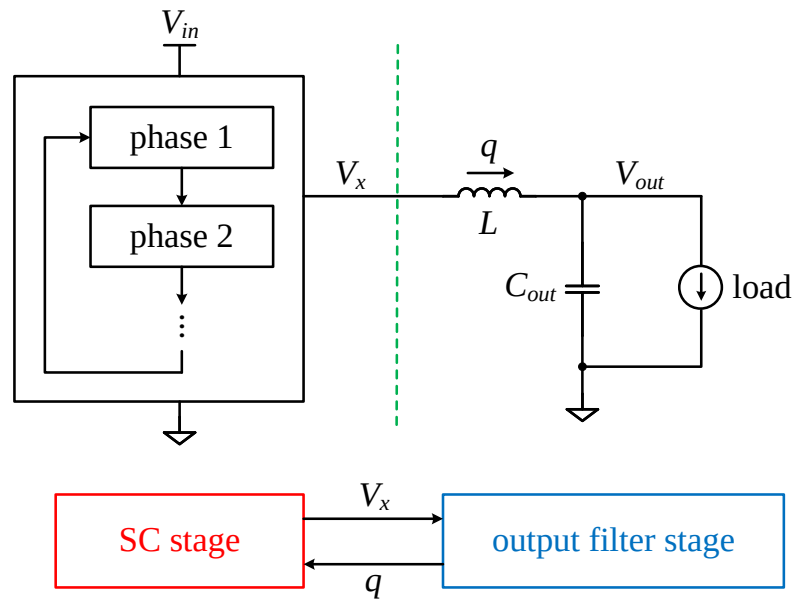


Figure 2.1: A direct hybrid switched-capacitor converter treated as two subsystems.

As shown in Figure 2.1, the general form of a step-down, direct hybrid SC converter

comprises a switched capacitor stage, where semiconductor switches are used to reconfigure a network of flying capacitors, and a single inductor, which connects the SC stage to the output terminal. This architecture can be intuitively treated as two subsystems: the SC stage and the output filter stage. The former constantly alters configuration during a switching period, resulting in multiple switching phases, while the latter does not change structure over time. The switching node voltage, V_x, is the output signal of SC stage and the input signal of output filter stage; the charge transferred through the inductor, q, is the output signal of output filter stage and the input signal of SC stage[1]. The derivation will be based on two simple assumptions:

1. During each phase, the circuit is linear, and the final condition can be expressed as linear combinations of the initial condition given a known or fixed time duration.

2. At switching events, capacitor voltage and inductor current are continuous. In other words, the final condition of previous phase is the initial condition of present phase.

The rest of this chapter will use the FCML topology as an example to derive the state space model. Part of the content was previously presented in IEEE Applied Power Electronics Conference and Exposition (APEC) in 2019 [69].

2.1 Flying Capacitor Multilevel Converters

The flying capacitor multilevel (FCML) topology belongs to the direct hybrid SC family and features no parallel-connected flying capacitor networks in any switching phase. This eliminates charge sharing even with mismatched flying capacitance but also makes balance notoriously challenging.

Figure 2.2 shows the general schematic of an FCML converter with N commutation cells, each of which includes two complementary switches. While many naming systems exist in the literature, an N-cell FCML converter is equivalent to an (N+1)-level FCML

[1]The V_x and q quantities are only for illustration purpose here. There will be more formal and accurate definitions for them later in the chapter.

converter, and has N-1 flying capacitors between adjacent cells. In each phase, the states of switching cells configure flying capacitors to be charged, discharged or remain idle, leading to one of the N+1 possible voltage levels at the switching node: $i/N \times V_{in}$ ($i = 0, 1, 2, \cdots, N$). The switching node voltage, V_x, is averaged by the output filter to produce a DC output voltage, V_{out}.

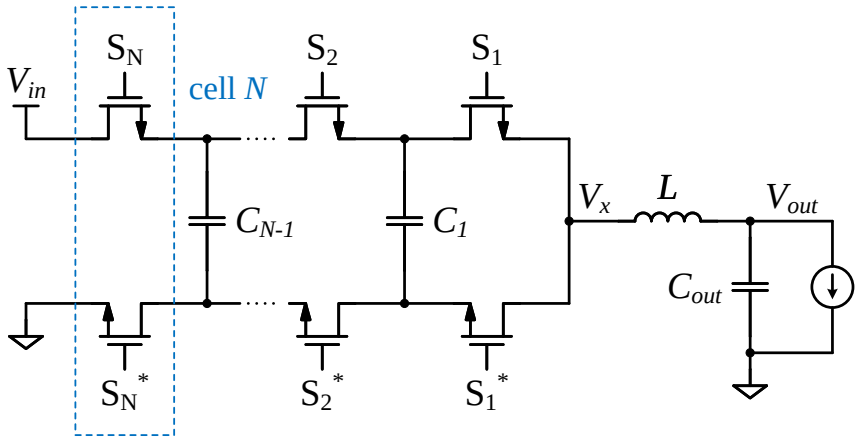


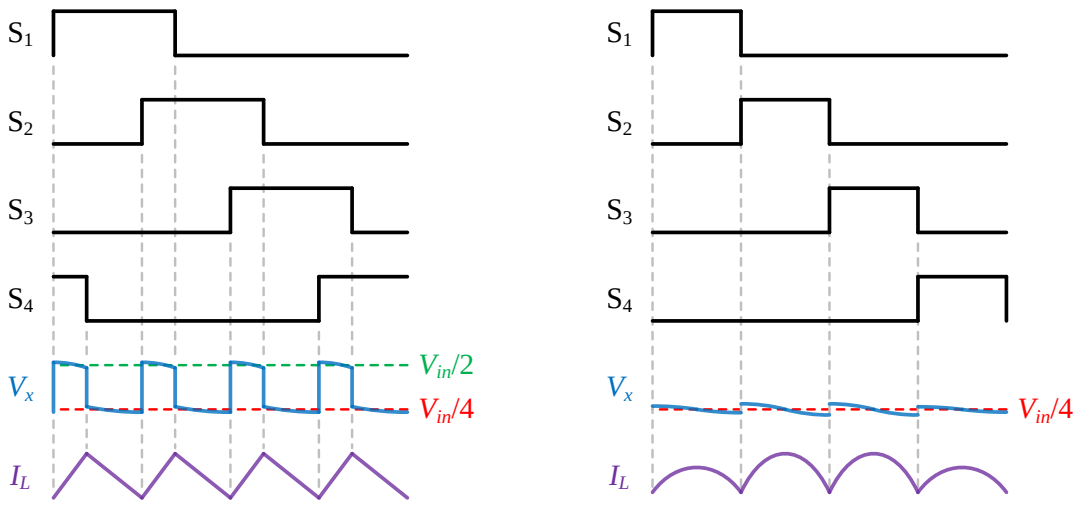
Figure 2.2: The general schematic of an N-cell FCML converter.

A common way to operate the switching cells is phase-shifted pulse width modulation (PSPWM) [46], where all cells share the same duty cycle[2], D, but cell i ($i = 1, 2, \cdots, N$) is phase shifted by (i-1)/N×360°. The output voltage is given by the product of the duty cycle and the input voltage, DV_{in}. While D may be any value between 0 and 1, it can be normalized to the following form:

$$D = \frac{m}{N}, \tag{2.1}$$

where the denominator equals the number of cells, N; the numerator obtained from this normalization is denoted as m. If m is not an integer, V_x will be alternating between two adjacent voltage levels, resembling a square wave; this scenario is hereby referred to as the inductive mode operation. In the special cases where m is an integer, V_x remains at one voltage level through the whole period, leading to sinusoidal characteristics of the

[2]Since the two switches are always complementary, the duty cycle is defined as the ratio of top switch turn on time to the whole period, similar to that of buck converters.



(a) inductive mode.

(b) resonant mode.

Figure 2.3: Two operation modes for a 4-cell FCML converter.

inductor current; this scenario is hereby referred to as the resonant mode operation[3]. The two operating modes are illustrated in Figure 2.3 using a 4-cell example.

However, the above operating principles put specific requirements on flying capacitors: for capacitor C_i ($i = 1, 2, \cdots, N$-1), its 'average' voltage should be $i/N \times V_{in}$, which is defined as the balanced voltage. The term 'average' may have more than one possible interpretation, but for the switches to have minimum voltage stress, it should be 'the algebraic average of the initial and final voltage during a switching phase that the capacitor is either being charged or discharged'. This point will be further explained in later chapters. If flying capacitors become imbalanced, both ripple quantities and switch voltage stress will increase, harming the efficiency and reliability of the converter.

Given balanced flying capacitors, the operation of FCML converters is fairly similar to that of buck converters, especially in the inductive mode. One major difference is that, referring to Figure 2.3a, V_x in FCML converters has reduced amplitude and multiplied effective frequency, both by a factor of N. Therefore, compared to buck converters, the

[3]This classification generally follows [9, 61], however, the 'quasi-resonant' mode is included in the inductive mode here, due to similarities in modeling. The resonant mode also includes the cases where phase durations are less than half resonant period and the inductor current is in continuous conduction.

inductance in FCML converters can be reduced by a factor of N^2 while maintaining the same ripple, showing the potential to achieve higher power density [22, 62].

In terms of active components, the FCML topology does have more switches in the current conduction path than the buck topology, but they can be rated at a lower voltage (V_{in}/N). Depending on how the switch on-state resistance scales with voltage rating[4], the increased number of switches does not necessarily lead to higher conduction loss. Furthermore, the ability to use low voltage rated switches is beneficial in applications where high voltage rated devices have poor performance or are not available [70].

2.2 Modeling the Switched-Capacitor Stage

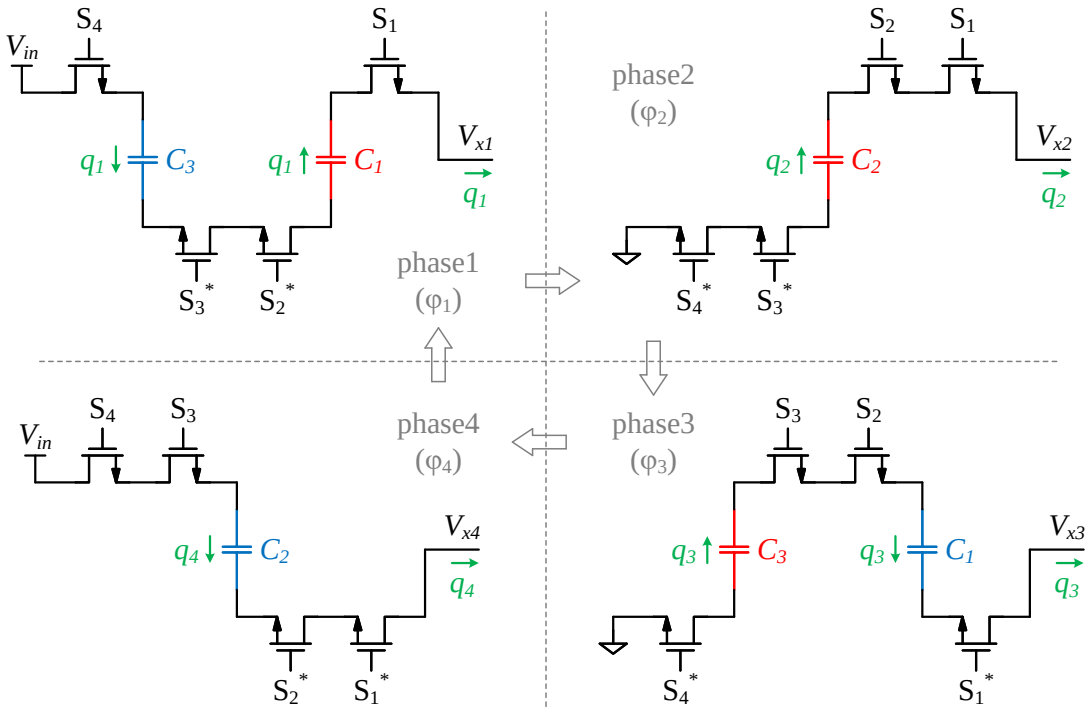


Figure 2.4: Equivalent circuits of the SC stage for a 4-cell FCML converter at $D = 2/4$.

In the SC stage, voltage on flying capacitors are affected by the charge transfer; they also determine the switching node voltage. Derivation of the state-space model is essen-

[4] more directly the specific parameters of the semiconductor technology $R_{on,sp}$, defined in [70]

tially the process of quantifying this relationship. As an example, Figure 2.4 shows the SC stage equivalent circuits for a 4-cell FCML converter at $D = 2/4$. The charge transferred to the output during phase j is denoted as q_j. The flying capacitors being discharged and charged are marked with red and blue, respectively. In one switching period, each flying capacitor is charged and discharged both once.

For capacitor C_1, the initial voltage in period k is defined as $V_{C1,0}(k)$. It is discharged in phase 1 and charged in phase 3, therefore, the net charge flow during period k is $q_3(k) - q_1(k)$. Since the voltage increment equals charge divided by capacitance, its final voltage in period k, which is also the initial voltage in period k+1, can be expressed as:

$$V_{C1,0}(k+1) = V_{C1,0}(k) + \frac{q_3(k) - q_1(k)}{C_1}. \tag{2.2}$$

Similar relationships for other flying capacitors can be obtained:

$$V_{C2,0}(k+1) = V_{C2,0}(k) + \frac{q_4(k) - q_2(k)}{C_2}, \tag{2.3}$$

$$V_{C3,0}(k+1) = V_{C3,0}(k) + \frac{q_1(k) - q_3(k)}{C_3}. \tag{2.4}$$

Assuming all flying capacitors share the same capacitance[5], C_f, the above equations can be packed into a matrix form:

$$\begin{bmatrix} V_{C1,0}(k+1) \\ V_{C2,0}(k+1) \\ V_{C3,0}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{C1,0}(k) \\ V_{C2,0}(k) \\ V_{C3,0}(k) \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \\ 1 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} q_1(k) \\ q_2(k) \\ q_3(k) \\ q_4(k) \end{bmatrix}, \tag{2.5}$$

or simply denoted as

$$\boldsymbol{V_C}(k+1) = \boldsymbol{A} \cdot \boldsymbol{V_C}(k) + \boldsymbol{B} \cdot \boldsymbol{q}(k), \tag{2.6}$$

[5]The primary results developed here still hold true even if this assumption is violated. Scenarios where flying capacitor values are different will be discussed in Chapter 3.

where $\boldsymbol{V_C}$ contains the initial values of voltage on flying capacitors; $\boldsymbol{q}$ contains the charge transfer during each phase. Equation (2.6) is hereby defined as the state equation of the SC stage; it describes how the input signal, $\boldsymbol{q}$, affects the state variable of the system, $\boldsymbol{V_C}$.

There is another relationship in the SC stage: the switching node voltage is determined by voltage on flying capacitors. In phase 1, for example, the initial value of the switching node voltage in period k is denoted as $V_{x1,0}(k)$. Neglecting switch on-state resistance, it can be calculated from KVL:

$$V_{x1,0}(k) = V_{in} - V_{C3,0}(k) + V_{C1,0}(k). \tag{2.7}$$

The relationship in later phases may be slightly more complicated. In phase 3, C_1 and C_3 are involved again:

$$V_{x3,0}(k) = V_{C3,\varphi3}(k) - V_{C1,\varphi3}(k), \tag{2.8}$$

where $V_{C1,\varphi3}(k)$ and $V_{C3,\varphi3}(k)$ are their initial voltage in phase 3, respectively. These new initial voltage can be obtained by accounting for the previous charge transfer in phase 1:

$$V_{C1,\varphi3}(k) = V_{C1,0}(k) - \frac{q_1(k)}{C_f}, \tag{2.9}$$

$$V_{C3,\varphi3}(k) = V_{C3,0}(k) + \frac{q_1(k)}{C_f}. \tag{2.10}$$

Substituting (2.9) and (2.10) into (2.8) gives

$$V_{x3,0}(k) = V_{C3,0}(k) - V_{C1,0}(k) + \frac{2q_1(k)}{C_f}. \tag{2.11}$$

Following similar process, in phase 2 and phase 4:

$$V_{x2,0}(k) = V_{C2,0}(k), \tag{2.12}$$

$$V_{x4,0}(k) = V_{in} - V_{C2,0}(k) + \frac{q_2(k)}{C_f}. \tag{2.13}$$

Packing the equations in all 4 phases gives

$$\begin{bmatrix} V_{x1,0}(k) \\ V_{x2,0}(k) \\ V_{x3,0}(k) \\ V_{x4,0}(k) \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_{C1,0}(k) \\ V_{C2,0}(k) \\ V_{C3,0}(k) \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 2 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} q_1(k) \\ q_2(k) \\ q_3(k) \\ q_4(k) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 1 \end{bmatrix} V_{in},$$

or simply denoted as

$$\boldsymbol{V_x}(k) = \boldsymbol{C} \cdot \boldsymbol{V_C}(k) + \boldsymbol{D} \cdot \boldsymbol{q}(k) + \boldsymbol{W_1} \cdot V_{in}, \tag{2.14}$$

where $\boldsymbol{V_x}$ contains the initial switching node voltage during each phase. Equation (2.14) is hereby defined as the output equation of the SC stage; it describes how the state variable, $\boldsymbol{V_C}$, determines the output signal of the system, $\boldsymbol{V_x}$. Here the input voltage, V_{in}, is treated as a constant, however, it can also be treated similar to a state variable. This becomes useful in applications where V_{in} is unknown, which will be discussed in Chapter 3.

Equation (2.6) and (2.14) forms the full state space model for the SC stage, which is rewritten here for convenience of observation:

$$\begin{aligned} \boldsymbol{V_C}(k+1) &= \boldsymbol{A} \cdot \boldsymbol{V_C}(k) + \boldsymbol{B} \cdot \boldsymbol{q}(k), \\ \boldsymbol{V_x}(k) &= \boldsymbol{C} \cdot \boldsymbol{V_C}(k) + \boldsymbol{D} \cdot \boldsymbol{q}(k) + \boldsymbol{W_1} \cdot V_{in}. \end{aligned}$$

There are two important features that result from the nature of switched-capacitors[6]:

1. Matrix $\boldsymbol{A}$ is the (N-1)$^{\text{th}}$ order identity matrix. Neglecting non-idealities such as self leakage, the voltage on flying capacitors can only be changed by the charge transfer. When $\boldsymbol{q} = \boldsymbol{0}$, $\boldsymbol{V_C}$ has to remain the same, leading to $\boldsymbol{A}$ being the identity matrix.

[6]These features may not hold true for direct hybrid SC topologies where charge sharing is present, such as the hybrid Dickson, because charge transfer can happen among capacitors and not necessarily through the inductor. However, with split phase control [71], complete soft charging is achieved and these features can be enabled.

2. Matrices $\boldsymbol{B}$ and $\boldsymbol{C}$ have a transpose relationship:

$$C_f \cdot \boldsymbol{B} = -\boldsymbol{C}^T. \tag{2.15}$$

This is because both $\boldsymbol{B}$ and $\boldsymbol{C}$ are determined by the flying capacitor connection in each phase. Specifically, if a flying capacitor is being charged, its voltage must show a negative sign in the KVL equation, and vice versa.

2.3 Controllability and Observability of the SC Stage

Controllability and observability are important characteristics for a system modeled in the state space. For the SC stage, controllability describes whether the state variable (voltage on flying capacitors) can be arbitrarily adjusted by the input signal (charge transferred through the inductor); observability describes whether the state variable can be identified from measurement of the output signal (switching node voltage in each phase).

The system being controllable is equivalent to its controllability matrix,

$$\boldsymbol{\mathcal{C}} = \begin{bmatrix} \boldsymbol{B} & \boldsymbol{AB} & \cdots & \boldsymbol{A}^{N-2}\boldsymbol{B} \end{bmatrix}, \tag{2.16}$$

being full-rank. Noticing that $\boldsymbol{A}$ is the identity matrix, it simplifies to:

$$\boldsymbol{\mathcal{C}} = \begin{bmatrix} \boldsymbol{B} & \boldsymbol{B} & \cdots & \boldsymbol{B} \end{bmatrix}, \tag{2.17}$$

showing that $\boldsymbol{\mathcal{C}}$ is the horizontal expansion of $\boldsymbol{B}$. Since $\boldsymbol{B}$ has more columns than rows, this expansion does not affect the rank. Therefore, the controllability criteria for the SC stage is $\boldsymbol{B}$ being full-rank, or

$$\text{rank}(\boldsymbol{B}) = N - 1. \tag{2.18}$$

It can be seen that the controllability of the SC stage is solely dependent on the rank of

matrix $\boldsymbol{B}$, which will be referred to as the charge transfer matrix. This dependency can be understood in an informal but intuitive way: if the charge transfer matrix is not full rank (i.e. there are linearly dependent rows), the effect of the input signal (charge transferred through the inductor) always applies to a subset of flying capacitors in the same manner, therefore, individual control within this subset is not possible.

Similarly, the system being observable is equivalent to its observability matrix[7],

$$\boldsymbol{\mathcal{O}} = \begin{bmatrix} \boldsymbol{C} \\ \boldsymbol{CA} \\ \vdots \\ \boldsymbol{CA}^{N-2} \end{bmatrix}, \tag{2.19}$$

being full-rank. Since $\boldsymbol{A}$ is the identity matrix, it reduces to

$$\boldsymbol{\mathcal{O}} = \begin{bmatrix} \boldsymbol{C} \\ \boldsymbol{C} \\ \vdots \\ \boldsymbol{C} \end{bmatrix}. \tag{2.20}$$

This vertical expansion does not affect the rank either, as $\boldsymbol{C}$ always has more rows than columns. Consequently, the observability criteria for the SC stage is $\boldsymbol{C}$ being full-rank, or

$$\text{rank}(\boldsymbol{C}) = N - 1. \tag{2.21}$$

The observability of the SC stage is dependent on matrix $\boldsymbol{C}$, which will be referred to as the connection matrix. Another intuitive explanation can be formed: if the connection matrix is not full-rank, certain flying capacitors are always connected in a group, so that individual identification within this group is not possible.

[7] In the output equation, (2.14), the term $\boldsymbol{W} \cdot V_{in}$ is treated as a constant therefore does not affect the observability.

Since matrices $\boldsymbol{B}$ and $\boldsymbol{C}$ have a transpose relationship, (2.15), they also share the same rank, which means, interestingly, the controllability and observability of the SC stage are equivalent. It can be summarized as: *the SC stage is controllable and observable if and only if $\boldsymbol{C}$ is full-rank*[8]. Additionally, $\boldsymbol{C}$ can be conveniently obtained without the need of writing KVL equations. Its j^{th} row and i^{th} column element, c_{ji}, has the following pattern:

$$c_{ji} = \begin{cases} -1 & \text{capacitor } C_i \text{ is charged in phase } j, \\ 0 & \text{capacitor } C_i \text{ is idling in phase } j, \\ 1 & \text{capacitor } C_i \text{ is discharged in phase } j. \end{cases} \tag{2.22}$$

This allows writing the connection matrix directly from the equivalent circuits of a hybrid SC converter. Then the controllability and observability of its SC stage can be determined.

Specifically for an N-cell FCML converter with $D = m/N$, Appendix A proves that the connection matrix is full-rank (the SC stage is controllable and observable) except the case where m and N are integers whose greatest common factor is larger than one (i.e., m and N are not coprime). The result is summarized in Table 2.1.

	resonant mode		inductive mode
	m and N coprime	m and N not coprime	
controllability	✓	×	✓
observability	✓	×	✓

Table 2.1: Controllability and observability of the SC stage for an N-cell FCML converter with $D = m/N$.

This conclusion has a strong correlation with some findings in the previous literature:

[8]Here $\boldsymbol{B}$ and $\boldsymbol{C}$ are equivalent, but $\boldsymbol{C}$ is used due to convenience of investigation, as it is independent of the flying capacitance.

natural balance of FCML converters does not function in resonant mode where m and N are not coprime [42, 43]. Here this section showed that in the same cases, active balance also fails, because the voltage on flying capacitors are not controllable. This may not seem like a major problem, since the 'bad' cases are only several discrete points in a continuous range. However, in practice, due to limitations of hardware, the 'bad' points expand into their vicinity, making the influence much greater than the ideal scenario. Some approaches to alleviate this problem include:

1. Let N be a prime number, such that the SC stage is controllable and observable at any duty cycle, since a prime number is coprime with any integer.

2. Adjust the switching sequence to make the SC stage controllable and observable. This method will be introduced in Chapter 3.

2.4 Modeling the Output Filter Stage

For the output filter stage, the inductor current and the output voltage are affected by the switching node voltage; they also determine the charge transferred through the inductor. To quantify this relationship, the per-phase equivalent circuit of a direct hybrid SC converter is constructed in Figure 2.5. The SC stage is represented by its Thevenin equivalent capacitance, C_x. All equivalent series resistance (ESR), including on-state resistance of switches and winding resistance of the inductor, are lumped into R.

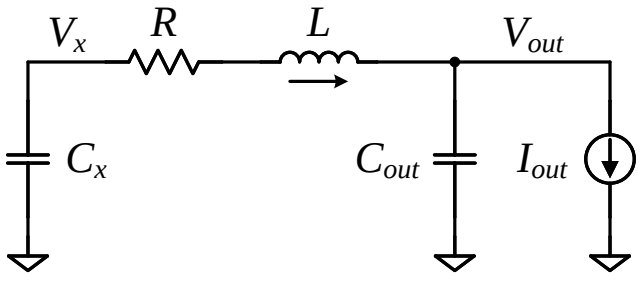


Figure 2.5: Equivalent circuit of a direct hybrid SC converter in each phase.

The following equations can be obtained from circuit analysis:

$$I_L = -C_x \frac{dV_x}{dt} = C_{out} \frac{dV_{out}}{dt} + I_{out}, \tag{2.23}$$

$$V_x = V_{out} + I_L R + L \frac{dI_L}{dt}. \tag{2.24}$$

They can be packed into a matrix form:

$$\begin{bmatrix} \frac{dI_L}{dt} \\ \frac{dV_{out}}{dt} \\ \frac{dV_x}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} & \frac{1}{L} \\ \frac{1}{C_{out}} & 0 & 0 \\ -\frac{1}{C_x} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_L \\ V_{out} \\ V_x \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C_{out}} \\ 0 \end{bmatrix} I_{out}, \tag{2.25}$$

or compactly denoted as:

$$\frac{d\boldsymbol{z}}{dt} = \boldsymbol{M_1} \cdot \boldsymbol{z} + \boldsymbol{M_2} \cdot I_{out}. \tag{2.26}$$

Solving (2.26) yields:

$$\boldsymbol{z}(t) = e^{\boldsymbol{M_1} t} \boldsymbol{z}(0) + \int_0^t e^{\boldsymbol{M_1} \tau} \boldsymbol{M_2} \, d\tau \cdot I_{out}, \tag{2.27}$$

or simply denoted as:

$$\boldsymbol{z}(t) = \boldsymbol{U}(t) \cdot \boldsymbol{z}(0) + \boldsymbol{V}(t) \cdot I_{out}. \tag{2.28}$$

Equation (2.28) gives the time-domain expression of the inductor current, output voltage, and switching node voltage. It is worth noticing that, in the case where C_x is different in certain phases, matrices $\boldsymbol{U}$ and $\boldsymbol{V}$ also need to be recalculated.

Returning to the example of a 4-cell FCML converter with $D = 2/4$, during period k, the initial condition of the inductor current and output voltage are denoted as $I_{L,0}(k)$ and $V_{out,0}(k)$, respectively. Referring to (2.28), their final condition in phase 1, which are also

their initial condition in phase 2, can be expressed as

$$\begin{bmatrix} I_{L,\varphi 1}(k) \\ V_{out,\varphi 1}(k) \end{bmatrix} = \begin{bmatrix} u_{11} & u_{12} \\ u_{21} & u_{22} \end{bmatrix}\Bigg|_{t=t_1} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + \begin{bmatrix} u_{13} \\ u_{23} \end{bmatrix}\Bigg|_{t=t_1} V_{x1,0}(k) + \begin{bmatrix} v_{11} \\ v_{21} \end{bmatrix}\Bigg|_{t=t_1} I_{out},$$

where u_{ij} and v_{ij} are the i^{th} row and j^{th} column element of matrices $\boldsymbol{U}$ and $\boldsymbol{V}$, respectively; t_1 is the time duration of phase 1. It can be denoted in a simpler form by symbolizing the coefficient matrices as $\boldsymbol{f_1}$, $\boldsymbol{g_1}$, and $\boldsymbol{h_1}$:

$$\begin{bmatrix} I_{L,\varphi 1}(k) \\ V_{out,\varphi 1}(k) \end{bmatrix} = \boldsymbol{f_1} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + \boldsymbol{g_1} V_{x1,0}(k) + \boldsymbol{h_1} I_{out}. \tag{2.29}$$

Similar relationships can be derived from the initial moment to the final moment of phase j ($j = 2, 3, 4$):

$$\begin{bmatrix} I_{L,\varphi j}(k) \\ V_{out,\varphi j}(k) \end{bmatrix} = \boldsymbol{f_j} \begin{bmatrix} I_{L,\varphi(j-1)}(k) \\ V_{out,\varphi(j-1)}(k) \end{bmatrix} + \boldsymbol{g_j} V_{xj,0}(k) + \boldsymbol{h_j} I_{out}. \tag{2.30}$$

The final condition of phase 4 in period k is also the initial condition in period (k+1):

$$\begin{bmatrix} I_{L,0}(k+1) \\ V_{out,0}(k+1) \end{bmatrix} = \begin{bmatrix} I_{L,\varphi 4}(k) \\ V_{out,\varphi 4}(k) \end{bmatrix}. \tag{2.31}$$

Solving the equations during each phase gives:

$$\begin{bmatrix} I_{L,0}(k+1) \\ V_{out,0}(k+1) \end{bmatrix} = \boldsymbol{f_4 f_3 f_2 f_1} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + \begin{bmatrix} \boldsymbol{f_4 f_3 f_2 g_1} & \boldsymbol{f_4 f_3 g_2} & \boldsymbol{f_4 g_3} & \boldsymbol{g_4} \end{bmatrix} \begin{bmatrix} V_{x1,0}(k) \\ V_{x2,0}(k) \\ V_{x3,0}(k) \\ V_{x4,0}(k) \end{bmatrix}$$

$$+ (\boldsymbol{f_4 f_3 f_2 h_1} + \boldsymbol{f_4 f_3 h_2} + \boldsymbol{f_4 h_3} + \boldsymbol{h_4}) I_{out}, \tag{2.32}$$

or compactly denoted as

$$\boldsymbol{x}(k+1) = \boldsymbol{P} \cdot \boldsymbol{x}(k) + \boldsymbol{Q} \cdot \boldsymbol{V_x}(k) + \boldsymbol{W_2} \cdot I_{out}, \tag{2.33}$$

where $\boldsymbol{x}$ contains initial values of the inductor current and output voltage. Equation (2.33) is the state equation of the output filter stage, since it describes how the input signal, $\boldsymbol{V_x}$, affects the state variable, $\boldsymbol{x}$. Here the load current, I_{out}, is treated as a constant.

The output signal, charge transferred through the inductor, also depends on the state variable. It may be intuitive to calculate charge by integral of current, however, analyzing the voltage drop on C_x gives a simpler solution. Referring to (2.28), the final condition of V_x in phase 1 can be obtained:

$$V_{x,\varphi 1}(k) = \begin{bmatrix} u_{31} & u_{32} \end{bmatrix}\Big|_{t=t_1} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + u_{33}|_{t=t_1} V_{x1,0}(k) + v_{31}|_{t=t_1} I_{out}. \tag{2.34}$$

The charge transferred through the inductor equals the charge lost on C_x:

$$\begin{aligned} q_1(k) &= C_x(V_{x1,0} - V_{x,\varphi 1}) \\ &= -C_x \begin{bmatrix} u_{31} & u_{32} \end{bmatrix}\Big|_{t=t_1} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + C_x(1 - u_{33}|_{t=t_1}) V_{x1,0}(k) - C_x v_{31}|_{t=t_1} I_{out}. \end{aligned}$$

which can be denoted as:

$$q_1(k) = \boldsymbol{F_1} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + G_1 V_{x1,0}(k) + H_1 I_{out}, \tag{2.35}$$

where $\boldsymbol{F_1}$, G_1, and H_1 represent the corresponding coefficients.

Similarly, the charge transferred through the inductor in phase j ($j = 2, 3, 4$) can be

obtained by evaluating the voltage drop of V_x during that phase:

$$q_j(k) = \boldsymbol{F_j} \begin{bmatrix} I_{L,\varphi(j-1)}(k) \\ V_{out,\varphi(j-1)}(k) \end{bmatrix} + G_j V_{xj,0}(k) + H_j I_{out}. \tag{2.36}$$

Solving the equations in each phase yields

$$\begin{bmatrix} q_1(k) \\ q_2(k) \\ q_3(k) \\ q_4(k) \end{bmatrix} = \begin{bmatrix} \boldsymbol{F_1} \\ \boldsymbol{F_2 f_1} \\ \boldsymbol{F_3 f_2 f_1} \\ \boldsymbol{F_4 f_3 f_2 f_1} \end{bmatrix} \begin{bmatrix} I_{L,0}(k) \\ V_{out,0}(k) \end{bmatrix} + \begin{bmatrix} G_1 & 0 & 0 & 0 \\ \boldsymbol{F_2 g_1} & G_2 & 0 & 0 \\ \boldsymbol{F_3 f_2 g_1} & \boldsymbol{F_3 g_2} & G_3 & 0 \\ \boldsymbol{F_4 f_3 f_2 g_1} & \boldsymbol{F_4 f_3 g_2} & \boldsymbol{F_4 g_3} & G_4 \end{bmatrix} \begin{bmatrix} V_{x1,0}(k) \\ V_{x2,0}(k) \\ V_{x3,0}(k) \\ V_{x4,0}(k) \end{bmatrix}$$
$$+ \begin{bmatrix} H_1 \\ \boldsymbol{F_2 h_1} + H_2 \\ \boldsymbol{F_3 f_2 h_1} + \boldsymbol{F_3 h_2} + H_3 \\ \boldsymbol{F_4 f_3 f_2 h_1} + \boldsymbol{F_4 f_3 h_2} + \boldsymbol{F_4 h_3} + H_4 \end{bmatrix} I_{out}, \tag{2.37}$$

or compactly denoted as

$$\boldsymbol{q}(k) = \boldsymbol{R} \cdot \boldsymbol{x}(k) + \boldsymbol{S} \cdot \boldsymbol{V_x}(k) + \boldsymbol{W_3} I_{out}. \tag{2.38}$$

This is the output equation of the output filter stage, as it describes how the state variable, $\boldsymbol{x}$, determines the output signal of the system, $\boldsymbol{q}$. Equation (2.33) and (2.38) make up the state space model of the output filter stage.

2.5 The Complete Model

With the two subsystems, the SC stage and the output filter stage, both modeled in state space, the complete model can be obtained by combining them. As shown in Figure 2.6, the input signal of one subsystem is provided by the output signal of the other. When the

two subsystems are seen as an entity, their input and output signals become internal signals and are not externally visible, leading to the complete model of the converter.

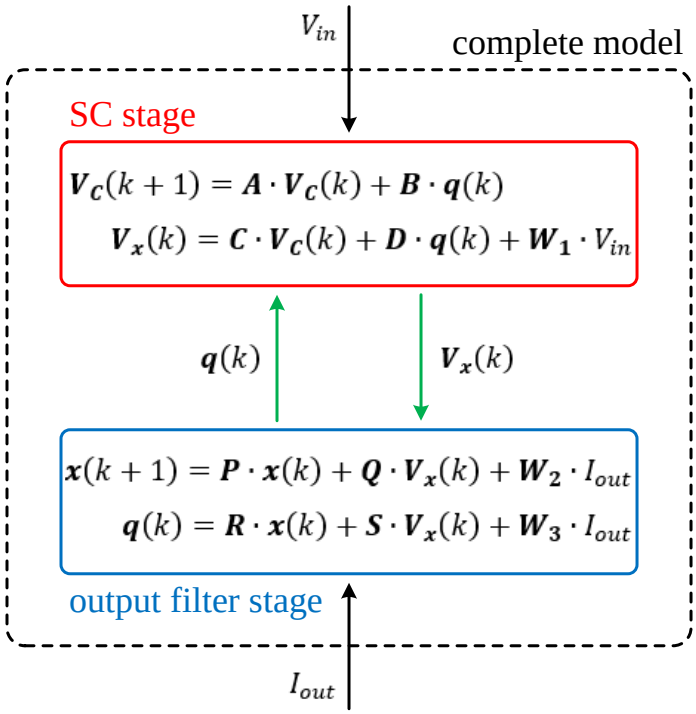


Figure 2.6: The relationship of the SC stage, the output filter stage, and the complete model.

Directly solving models of the subsystems, (2.6), (2.14), (2.33), (2.38), gives

$$\begin{bmatrix} \boldsymbol{V_C}(k+1) \\ \boldsymbol{x}(k+1) \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} + \boldsymbol{B}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{SC} & \boldsymbol{B}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{R} \\ \boldsymbol{QC} + \boldsymbol{QD}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{SC} & \boldsymbol{P} + \boldsymbol{QD}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{R} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_C}(k) \\ \boldsymbol{x}(k) \end{bmatrix} + \begin{bmatrix} \boldsymbol{B}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{SW_1} & \boldsymbol{B}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{W_3} \\ \boldsymbol{QW_1} + \boldsymbol{QD}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{SW_1} & \boldsymbol{W_2} + \boldsymbol{QD}(\boldsymbol{I} - \boldsymbol{SD})^{-1}\boldsymbol{W_3} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix}, \tag{2.39}$$

where $\boldsymbol{I}$ is the identity matrix. Equation (2.39) can be simply denoted as

$$\boldsymbol{x_{cl}}(k+1) = \boldsymbol{A_{cl}} \cdot \boldsymbol{x_{cl}}(k) + \boldsymbol{E} \cdot \boldsymbol{e}, \tag{2.40}$$

where $\boldsymbol{x_{cl}}$ includes the state variables of both subsystems; $\boldsymbol{A_{cl}}$ characterizes the intrinsic

nature of the complete system; $\boldsymbol{e}$ represents the external excitation and $\boldsymbol{E}$ is its coefficient matrix. Equation (2.40) describes the behavior of the whole converter: the dynamics are determined by its own characteristics (circuit parameters and phase duration) and external excitation (input voltage and load current).

The complete model is helpful in many aspects. As an example, simply by substituting $\boldsymbol{x_{cl}}(k+1) = \boldsymbol{x_{cl}}(k)$, the steady state of the converter can be solved:

$$\boldsymbol{x_{cl}}(k) = (\boldsymbol{I} - \boldsymbol{A_{cl}})^{-1}\boldsymbol{E}\boldsymbol{e}. \tag{2.41}$$

The dynamic response can also be conveniently explored by investigating eigenvalues of $\boldsymbol{A_{cl}}$. More applications of the subsystem models and the complete model will be gradually revealed in following chapters.

Chapter 3

Estimation and Balance of Flying Capacitor Voltage

For hybrid SC converters, knowledge of voltage on flying capacitors is useful for converter lifetime estimation, fault detection, and active balance [59, 72, 73]. However, direct measurement is challenging due to the large common mode voltage variation and is expensive in terms of hardware when the topology has many flying capacitors. Therefore, simple and effective estimation approaches can be beneficial.

To ensure safe operation of hybrid SC converters, flying capacitors need to be balanced (either through natural balance or active balance). But the condition to do so is that the SC stage is controllable. According to the conclusion in section 2.3, there are certain scenarios where FCML converters have uncontrollable SC stage, so that flying capacitors cannot be balanced. This problem needs to be further investigated to arrive at a solution.

With the help of the state space model, this chapter explores ways to estimate voltage on flying capacitors effectively and to balance flying capacitors in conventionally uncontrollable cases. Part of the content was previosuly presented in IEEE 20th workshop on Control and Modeling for Power Electronics (COMPEL) in 2019 [74].

3.1 Averaged Model of the SC Stage

According to state-space theory, state variables (flying capacitor voltages) can be estimated from input and output signals if the system is observable. As discussed in Chapter 2, the switching node voltage, V_x, is treated as the output of the SC stage; this is convenient to measure since it is generally accessible and is referenced to ground. However, the input signal, charge transferred through the inductor, is difficult to quantify without complex instrumentation. To keep the implementation simple and effective, an averaging technique will be applied to the output equation of the SC stage, eliminating the need of input signals for estimation. For consistency, the example of 4-cell FCML converter with $D = 2/4$ will continue to be used to illustrate this treatment. Figure 3.1 shows the equivalent circuit and representative voltage waveform in phase 1.

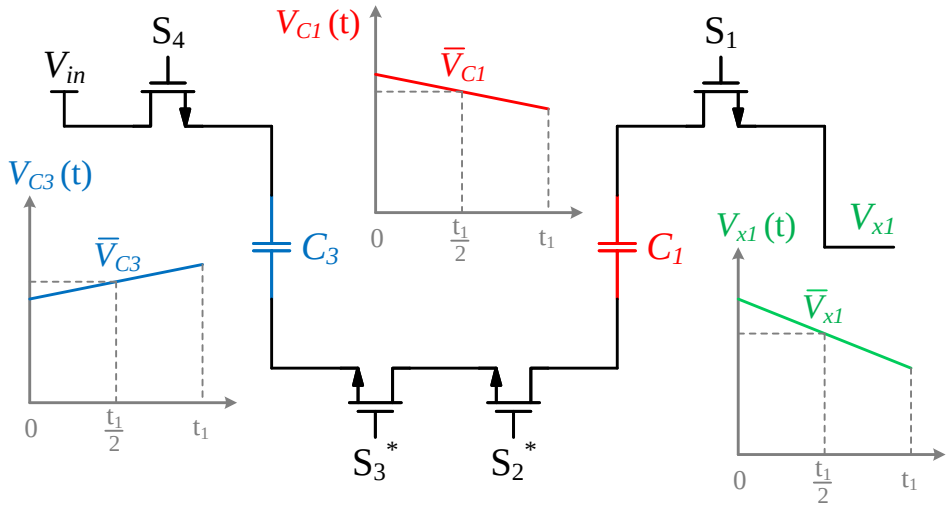


Figure 3.1: Equivalent circuit and linearized voltage waveform in phase 1.

Assuming positive inductor current, C_3 is being charged and C_1 is being discharged, causing voltage swing on both flying capacitors and at the switching node. The voltage waveform should be damped sinusoidal, but can be approximated as linear if the ripple is small compared to the DC value. With this assumption, the average voltage (the algebraic average of initial and final value) can be represented by the instantaneous voltage at $t_1/2$.

Take V_{C1} as an example:

$$\overline{V}_{C1} = V_{C1}(\frac{t_1}{2}) = \frac{V_{C1}(0) + V_{C1}(t_1)}{2}. \tag{3.1}$$

The average voltage $\overline{V}_{C3}$ and $\overline{V}_{x1}$ can also be defined accordingly. In period k, applying KVL at the middel moment of phase 1 gives:

$$\overline{V}_{x1}(k) = V_{in} - \overline{V}_{C1}(k) + \overline{V}_{C3}(k). \tag{3.2}$$

Similar relationships can be obtained in other phases:

$$\overline{V}_{x2}(k) = \overline{V}_{C2}(k), \tag{3.3}$$

$$\overline{V}_{x3}(k) = \overline{V}_{C3}(k) - \overline{V}_{C1}(k), \tag{3.4}$$

$$\overline{V}_{x4}(k) = V_{in} - \overline{V}_{C2}(k). \tag{3.5}$$

The above equations can be packed into a matrix form that describes the relationship between average values of the switching node voltage, flying capacitor voltages and the input voltage:

$$\begin{bmatrix} \overline{V}_{x1}(k) \\ \overline{V}_{x2}(k) \\ \overline{V}_{x3}(k) \\ \overline{V}_{x4}(k) \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} \overline{V}_{C1}(k) \\ \overline{V}_{C2}(k) \\ \overline{V}_{C3}(k) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 1 \end{bmatrix} V_{in}, \tag{3.6}$$

or compactly denoted as

$$\overline{\boldsymbol{V}}_{\boldsymbol{x}}(k) = \boldsymbol{C} \cdot \overline{\boldsymbol{V}}_{\boldsymbol{C}}(k) + \boldsymbol{W_1} \cdot V_{in}. \tag{3.7}$$

This is the averaged output equation of the SC stage. Compared to the original output

equation, (2.14), the state variable and output signal are averaged and the dependency on input signal (charge transfer through the inductor) disappears. Notice that the connection matrix, $\boldsymbol{C}$, remains the same, as it only depends on the capacitor connections in each phase. If $\boldsymbol{C}$ is full-rank, the SC stage is observable and flying capacitor voltages can be solved from the output signal:

$$\overline{\boldsymbol{V}}_{\boldsymbol{C}}(k) = \boldsymbol{C}^{\dagger}(\overline{\boldsymbol{V}}_{\boldsymbol{x}}(k) - \boldsymbol{W_1}{\cdot}V_{in}), \tag{3.8}$$

where $\boldsymbol{C}^{\dagger}$ is the pseudoinverse of the connection matrix, $\boldsymbol{C}$ (it is not a square matrix thus simple inverse cannot be applied).

The connection matrix always has more rows than columns, so the averaged output equation, (3.7), is an equation set that has more constraints than variables. This is not a problem because a physical system does not give conflicting equations. Furthermore, it leads to an alternative estimation scheme: rather than being treated as a constant, V_{in} can be estimated as well, because the system has sufficient information to do so. Knowledge of V_{in} can be valuable in applications where it is unknown. The ability of estimating V_{in} simplifies instrumentation since direct measurement is no longer necessary. Transforming (3.8) yields the corresponding algorithm:

$$\begin{bmatrix} \overline{\boldsymbol{V}}_{\boldsymbol{C}}(k) \\ V_{in} \end{bmatrix} = \begin{bmatrix} \boldsymbol{C} & \boldsymbol{W_1} \end{bmatrix}^{-1} \cdot \overline{\boldsymbol{V}}_{\boldsymbol{x}}(k). \tag{3.9}$$

The coefficient matrix, $[\boldsymbol{C}\ \boldsymbol{W_1}]$, is a square matrix, so simple inverse can be applied. The hardware implementation and test result of both estimation algorithms, (3.8) and (3.9), are described in the next section.

3.2 Flying Capacitor Voltage Estimator

The previous analysis indicated that flying capacitor voltages can be estimated from the switching node voltage in each phase, if the SC stage is observable. In the example of the

4-cell FCML converter, $D = 2/4$ is the only duty cycle that leads to unoberservable SC stage. However, the situation is worse in practical scenarios.

When the duty cycle is very close but not equal to $2/4$, for example, $D = 2.1/4$, the converter is in inductive mode. Assuming balanced flying capacitors, the switching node voltage, V_x, resembles a square wave between $V_{in}/2$ and $3V_{in}/4$, as shown in Figure 3.2. Due to parasitic inductance, there will be overshoot and ringing after a phase transition. The switching node voltage stablizes after a settling time, t_s. In addition, the interfacing hardware, usually a sample and hold circuit, requires V_x to remain stable for a certain duration, t_h, to make reliable measurement.

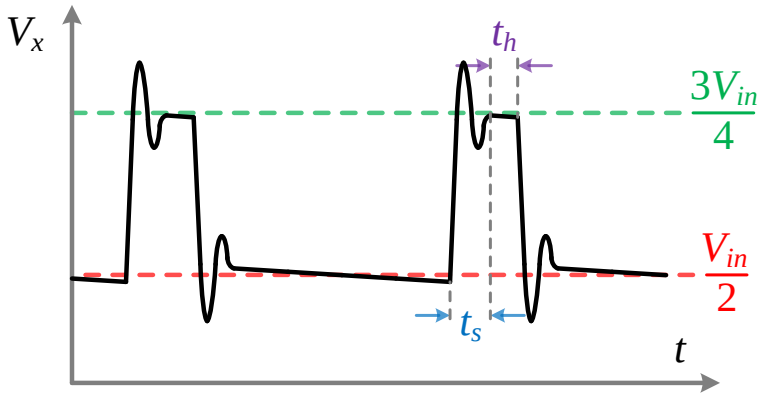


Figure 3.2: Switching node voltage waveform at $D = 2.1/4$ in practical scenario.

If the duration of any phase is shorter than $t_s + t_h$, V_x in that phases cannot be reliably measured. With a duty cycle close to $2/4$, V_x is only accessible in the phases where it is around $V_{in}/2$, as if the converter is operating exactly at $D = 2/4$, leading to unobservable SC stage. The duty cycle that avoids this situation has to satisfy:

$$|D - \frac{2}{4}| \cdot \frac{1}{f_{sw}} > t_s + t_h, \tag{3.10}$$

where f_{sw} is the switching frequency of the converter.

Similar challenge occurs at duty cycles close to 0 or 1. In these scenarios, V_x is only

accessible when it is at ground or V_{in}, thus no information of flying capacitor voltages can be obtained. This impact is summarized in Figure 3.3. One possible way to mitigate the unobservable challenge is to let the number of switching cells, N, be a prime number. As long as the duty cycle is not close to 0 or 1, the SC stage is always observable.

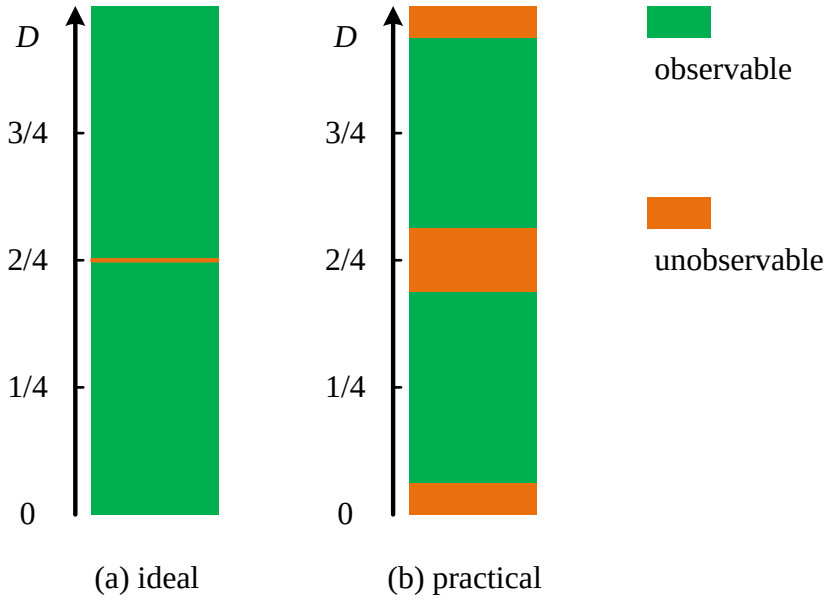


Figure 3.3: The impact of hardware limitations on the observability.

A flying capacitor voltage estimator was designed and evaluated for a 5-cell FCML converter. The top-level system block diagram is shown in Figure 3.4. The switching node voltage, V_x, is divided down and pre-processed by the differential amplifier. At the rising edge of the sampling clock, an analog to digital converter (ADC) takes a measurement of V_x and transfers the result to a field programmable gate array (FPGA) device through a serial peripheral interface (SPI). Based on the measurement of V_x and the known switch states, the FPGA calculates the estimated flying capacitor voltages and store them in the random access memory (RAM). Finally, results are moved to MATLAB by an universal asynchronous receiver-transmitter (UART) to be visualized.

Equation (3.8) and (3.9) provide the algorithms of estimating flying capacitor voltages (and the input voltage, V_{in}), however, the computational cost of matrix inversion is high. In

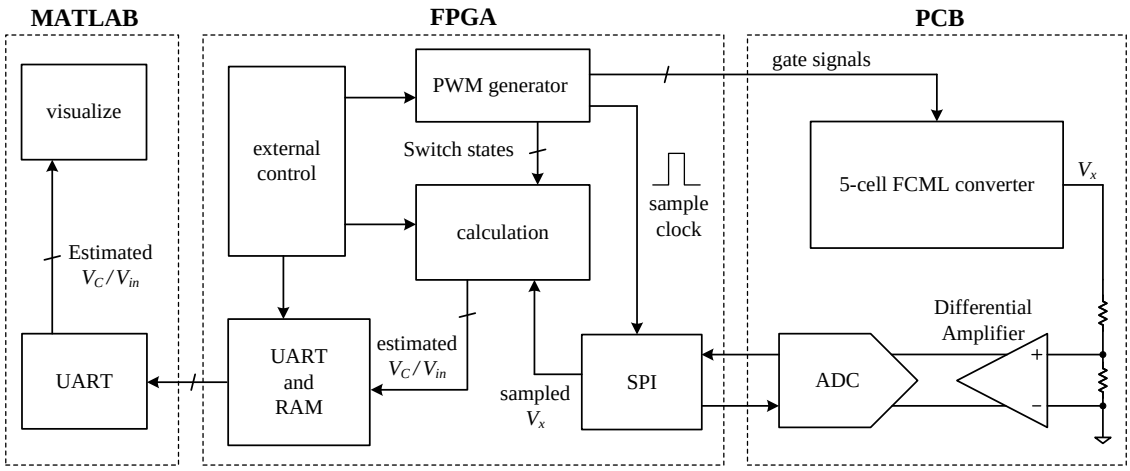


Figure 3.4: Block diagram of the flying capacitor voltage estimator.

the actual implementation, an iterative algorithm is adopted to avoid matrix inversion. The result converges to that of (3.8) and (3.9) in steady state.

During phase j of period k, the switching node voltage can be expressed as a linear combination of flying capacitor voltages and the input voltage:

$$\overline{V}_{xj}(k) = bV_{in} + \sum_{i=1}^{N-1} a_i \overline{V}_{Ci}(k), \tag{3.11}$$

where a_i ($i = 1, 2, \cdots, N$-1), b are coefficients determined by switch states. If capacitor C_i is being charged or discharged ($a_i \neq 0$), its new estimation can be solved:

$$\overline{V}_{Ci,new}(k) = \frac{1}{a_i}(\overline{V}_{xj}(k) - bV_{in} - \sum_{n \neq i}^{N-1} a_n \overline{V}_{Cn,est}(k-1)), \tag{3.12}$$

where $\overline{V}_{Cn,est}(k-1)$ is the estimation of $\overline{V}_{Cn}$ in period k-1. To reduce the impact of noise and quantization error, the updated estimation is obtained by averaging:

$$\overline{V}_{Ci,est}(k) = \frac{1}{2}(\overline{V}_{Ci,est}(k-1) + \overline{V}_{Ci,new}(k)). \tag{3.13}$$

The detailed algorithm and implementation were contributed by collaborating researcher Dobbins, and are described in [69].

In steady state, a total number of 3000 consecutive estimations were collected for each flying capacitor. They are compared against DC voltages measured by oscilloscope. The estimation error is normalized to V_{in} and the histogram is shown in Figure 3.5. It can be seen that the maximum steady state estimation error does not exceed 0.25% of V_{in} for all flying capacitors, proving accuracy of the estimation algorithm.

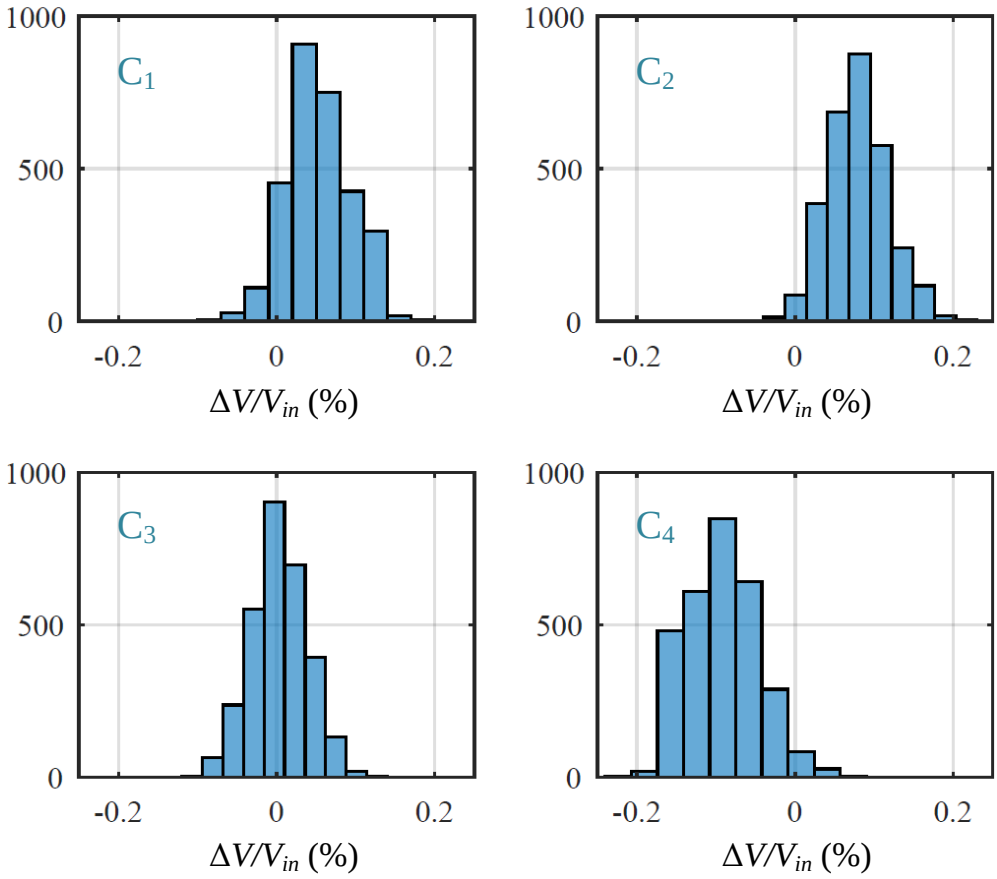


Figure 3.5: Histogram of normalized steady state estimation error.

Transient behavior of the estimator was also tested. The converter operates in steady state when the estimator is activated with initial estimations being set to zero. The output result of the estimator is recorded over time and shown in Figure 3.6. Partly due to the averaging process in (3.13), it takes some time for the estimations to converge to the correct

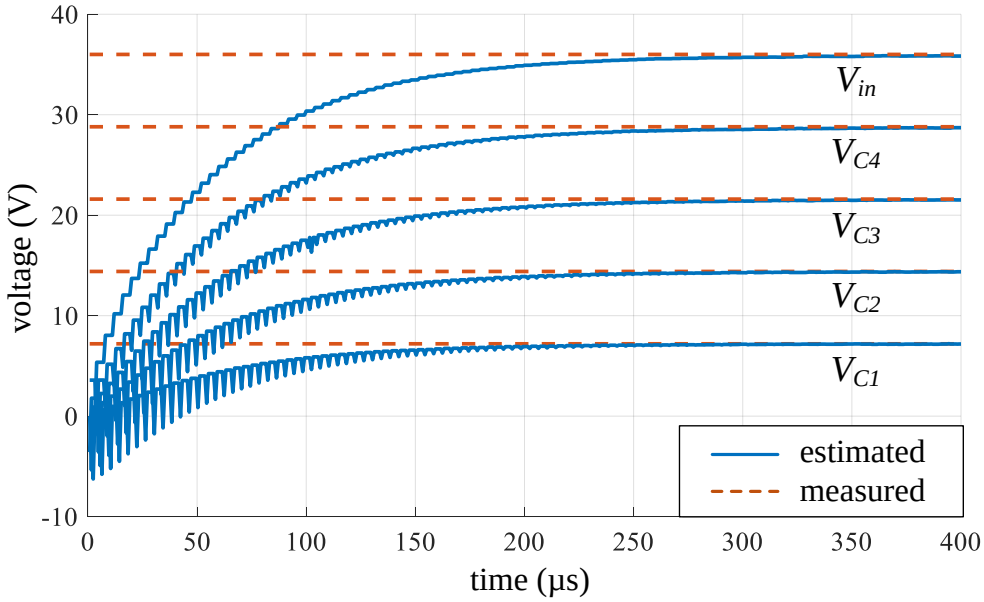


Figure 3.6: Transient response of the estimator with zero initial estimation.

values. In this case, the 5% settling time is 214μs (9 periods). The averaging weight can also be adjusted to trade signal to noise ratio for convergence speed.

3.3 Natural Balancing of Hybrid SC Converters

For hybrid SC converters, especially FCML converters, it was observed that flying capacitor voltages are automatically regulated to balance by harmonic feedback of the inductor [54, 55], which is called natural balance. However, natural balance does not work at some duty cycles even when the powertrain is ideal [42, 43], and interestingly, these duty cycles happen to make the SC stage not controllable, identified in section 2.3. This coincidence implies a fundamental relationship between natural balance and controllability of the SC stage, which had not been previously explored. To understand the link between these two concepts, the following analysis starts with simplification of the state space model.

In a linear circuit, the time-domain response, y, can be decomposed as the sum of the

zero-state response, y_{zs}, and the zero-input response, y_{zi}:

$$y = y_{zs} + y_{zi}. \tag{3.14}$$

The zero-state response is excited merely by the active sources; the zero-input response is excited merely by initial condition of energy-storage components. In open-loop operation, a naturally balanced hybrid SC converter should arrive at the balanced state regardless of the initial condition. Alternatively speaking, it should satisfy:

1. The steady state of zero-state response is the balanced state.

2. The steady state of zero-input response is zero.

Either of the above statements alone is a necessary condition for natural balance. The following analysis will focus on the second statement because it leads to a more intuitive explanation. Since the zero-input response is analyzed, active sources, $\boldsymbol{e}$, in the complete model, (2.40), can be set to zero, leading to the reduced model:

$$\boldsymbol{x_{zi}}(k+1) = \boldsymbol{A_{cl}} \cdot \boldsymbol{x_{zi}}(k), \tag{3.15}$$

where $\boldsymbol{x_{zi}}$ is the zero-input portion of state variables. Its must decay to zero in steady state for natural balance to hold:

$$\lim_{k\to\infty} \boldsymbol{x_{zi}}(k) = \boldsymbol{0}. \tag{3.16}$$

In discrete-time state space, this is equivalent to the condition that all eigenvalues of $\boldsymbol{A_{cl}}$ are within the unit circle. Interestingly, there is always an eigenvalue on the unit circle if the SC stage is uncontrollable (the connection matrix, $\boldsymbol{C}$, is not full-rank). In this case, the system is 'marginally stable' and the steady state is finite but non-zero.

Eigenvalues of $\boldsymbol{A_{cl}}$ are values of λ that satisfy equation

$$|\boldsymbol{A_{cl}} - \lambda \boldsymbol{I}| = 0. \tag{3.17}$$

Substituting $\lambda = 1$, the matrix on the left hand side of (3.17) becomes:

$$\begin{aligned}\boldsymbol{A_{cl} - I} &= \begin{bmatrix} \boldsymbol{B(I - SD)^{-1}SC} & \boldsymbol{B(I - SD)^{-1}R} \\ \boldsymbol{QC + QD(I - SD)^{-1}SC} & \boldsymbol{P + QD(I - SD)^{-1}R - I} \end{bmatrix} \\ &= \begin{bmatrix} \boldsymbol{B} & \mathbf{0} \\ \mathbf{0} & \boldsymbol{I} \end{bmatrix} \begin{bmatrix} \boldsymbol{(I - SD)^{-1}S} & \boldsymbol{(I - SD)^{-1}R} \\ \boldsymbol{QC + QD(I - SD)^{-1}S} & \boldsymbol{P + QD(I - SD)^{-1}R - I} \end{bmatrix} \begin{bmatrix} \boldsymbol{C} & \mathbf{0} \\ \mathbf{0} & \boldsymbol{I} \end{bmatrix},\end{aligned}$$

or abbreviated as

$$\boldsymbol{A_{cl} - I = B' \cdot T \cdot C'}. \tag{3.18}$$

Due to the property of matrix multiplication,

$$\text{rank}(\boldsymbol{A_{cl} - I}) \leq \min\{\text{rank}(\boldsymbol{B' \cdot T}), \text{rank}(\boldsymbol{C'})\} \leq \text{rank}(\boldsymbol{C'}). \tag{3.19}$$

When $\boldsymbol{C}$ is not full-rank, neither is $\boldsymbol{C'}$, therefore, according to (3.19), matrix $\boldsymbol{A_{cl} - I}$ is not full-rank, indicating:

$$|\boldsymbol{A_{cl} - I}| = 0, \tag{3.20}$$

meaning one is an eigenvalue of $\boldsymbol{A_{cl}}$. This eigenvalue is on the unit circle: the steady state of zero-input response is non-zero, and natural balance fails. To summarize, the SC stage being controllable is a necessary condition for natural balance.

This conclusion can be intuitively understood by recognizing the connection between the two subsystems. The harmonic feedback of inductor current, described in [42], can be regarded as an intrinsic control effort of the output filter stage on the SC stage, regulating flying capacitor voltages to balance. However, with a uncontrollable SC stage, the control effort cannot effectively regulate all flying capacitor voltages, causing natural balance to fail. It is worth noticing that in this case, some flying capacitors are still under the effect of natural balance. To identify which flying capacitors can be balanced, the example of 4-cell FCML converter with $D = 2/4$ is revisited. Its equivalent circuit in phase 1 and phase 3

are presented again in Figure 3.7.

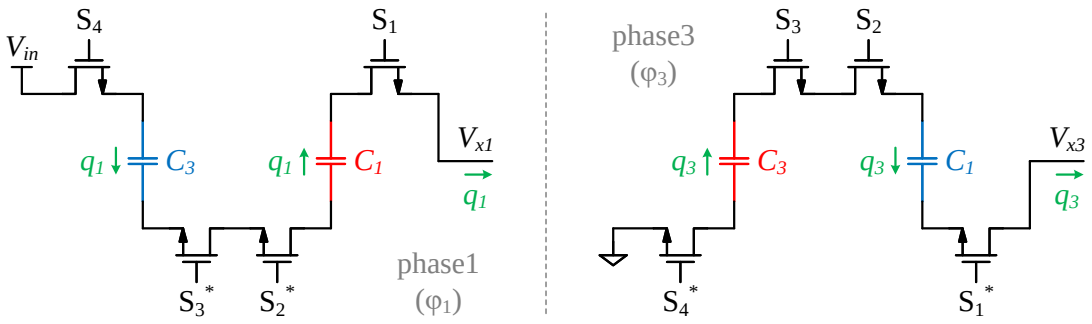


Figure 3.7: Equivalent circuits of the SC stage during phase 1 and phase 3.

It can be observed that the charge transfer of C_1 and C_3 are directly correlated: if C_1 is charged by a certain amount, C_3 has to be discharged by the same amount, and vice versa. Due to this correlation, individual control is not possible. The state equations that govern their voltage dynamics are reproduced here:

$$V_{C1,0}(k+1) = V_{C1,0}(k) + \frac{q_3(k) - q_1(k)}{C_f}, \tag{3.21}$$

$$V_{C3,0}(k+1) = V_{C3,0}(k) + \frac{q_1(k) - q_3(k)}{C_f}. \tag{3.22}$$

Directly adding them yields

$$V_{C1,0}(k+1) + V_{C3,0}(k+1) = V_{C1,0}(k) + V_{C3,0}(k), \tag{3.23}$$

pointing out that the sum of $V_{C1,0}$ and $V_{C3,0}$ is a constant regardless of the charging and discharging process. Furthermore, performing (3.23) recursively gives

$$V_{C1,0}(\infty) + V_{C3,0}(\infty) = V_{C1,0}(0) + V_{C3,0}(0). \tag{3.24}$$

The steady state of $V_{C1,0}$ and $V_{C3,0}$ depend on the initial condition, but natural balance requires the steady state to be balanced regardless of the initial condition. Therefore, C_1

and C_3 are not naturally balanced. Capacitor C_2 does not have this issue, as its charging and discharging process is not correlated with other capacitors.

This conclusion can be generalized: if the i^{th} column of the connection matrix, $\boldsymbol{C}$, is linearly independent from all other columns, capacitor C_i is naturally balanced. In the 4-cell FCML converter with $D = 2/4$,

$$\boldsymbol{C} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \end{bmatrix}. \tag{3.25}$$

The 1st and 3rd columns are linearly dependent with each other; the 2nd column is linearly independent from them. Therefore, C_2 is naturally balanced but C_1 and C_3 are not. When a converter is naturally balanced, obviously all flying capacitors are naturally balanced, as $\boldsymbol{C}$ is full-rank and each of its columns must be linearly independent from others.

To verify the theory, a 4-cell FCML converter is simulated in Cadence at both $D = 1/4$ and $D = 2/4$. The corresponding state space model is also simulated in MATLAB under the same condition. Both results are shown in Figure 3.8. Circuit simulation in Cadence contains ripple, so the result is presented by shaded area within the envelope; state space simulation in MATLAB only contains the initial condition in each period, so there is no ripple and the result is presented by solid curves. The initial condition of C_1, C_2, C_3 are set to 0, 0, 0.2V, respectively.

At $D = 1/4$, the converter can be naturally balanced as the zero-input response decays to zero in steady state. At $D = 2/4$, however, the zero-input response has non-zero steady state thus the converter is not naturally balanced. Specifically, voltage on C_1 and C_3 indeed sum up to a constant, leading to their imbalance, but C_2 can still be balanced. The matching of Cadence and MATLAB simulations also verifies accuracy of the state space model.

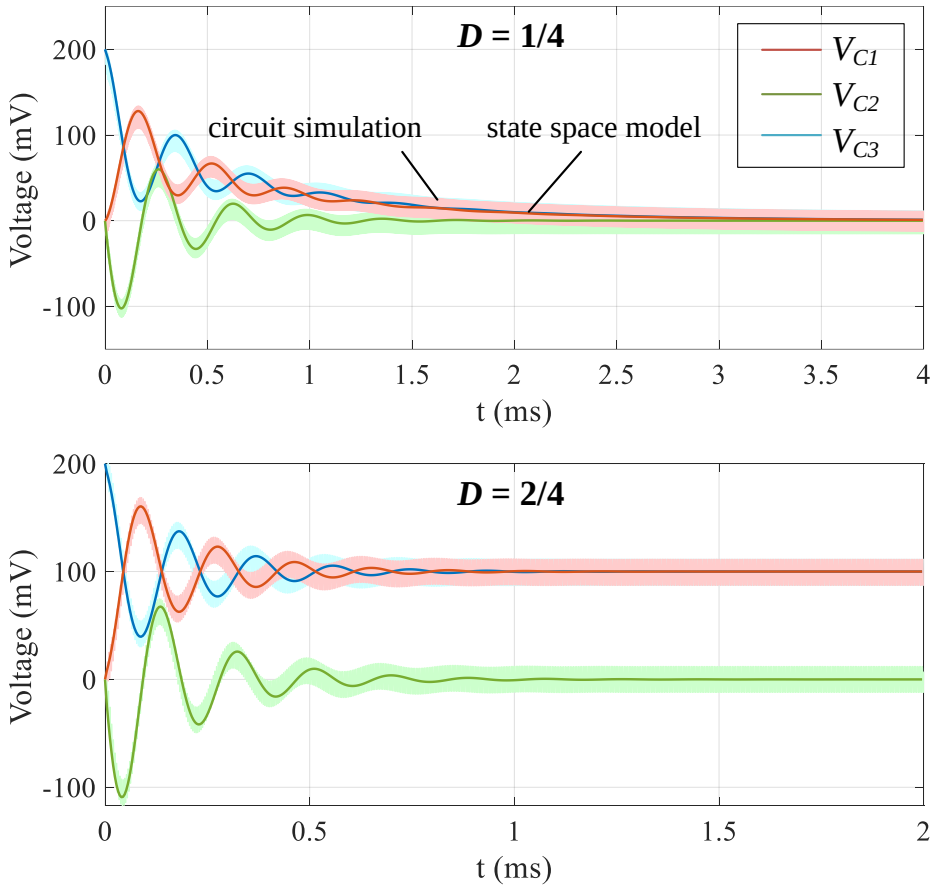


Figure 3.8: Simulated zero-input response of a 4-cell FCML converter.

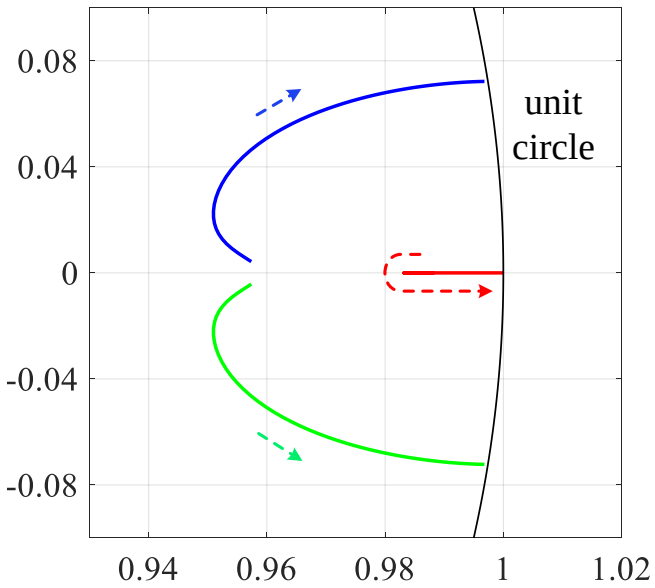


Figure 3.9: Trajectory of some eigenvalues when Q ranges from 0.1 to 100.

In naturally balanced cases, the balancing dynamics (speed) is indicated by location of the eigenvalues of $\boldsymbol{A}_{cl}$, which depends on parameters of the powertrain (ESR, inductance, flying capacitance, etc.). It is slower when the dominant eigenvalue (the one with largest amplitude) is closer to the unit circle. In the 4-cell FCML converter with $D = 1/4$, ESR is scaled such that quality factor (Q) of the equivalent circuit ranges from 0.1 to 100. The trajectory of some eigenvalues under this sweep is plotted in Figure 3.9. Other eigenvalues are out of the scope and close to the origin.

As Q increases, the dominant eigenvalue (marked by red) moves first away from then towards the unit circle, meaning the balancing dynamics is first accelerated then slowed down. In the extreme case where Q approaches infinity (the system has no damping), the dominant eigenvalue arrives at the unit circle and natural balance also fails. Additionally, even with a low Q, amplitude of the dominant eigenvalue is still close to 1 ($>$0.98 in this example), indicating that natural balance is a 'weak' process and is generally slow.

Duty cycle also affects the balancing dynamics. If the 4-cell FCML converter operates at a duty cycle between $1/4$ and $2/4$, it is effectively multiplexing between the $D = 1/4$ and $D = 2/4$ modes. When the duty cycle is close to $2/4$, the converter spend majority of the period in $D = 2/4$ mode (the effective duty cycle is close to one [63]). In this case, although the SC stage is controllable, the effectiveness of any control effort (either natural balance or active balance) is degraded, as will be seen in the next section.

Lastly, it should be emphasized that in practical implementation, natural balance does not guarantee the perfect balance of flying capacitor voltages. The analysis in this section is based on ideal powertrain parameters, however, non-idealities (input impedance, timing mismatch, etc.) may cause additional disturbances [39, 40, 41]. Although natural balance provides a compensation mechanism [54], it does not ensure immunity to disturbances.

3.4 Modified Phase-Shifted Pulse Width Modulation

For FCML converters, both natural balance and active balance fail at certain duty cycles, because the SC stage is not controllable. If the operation space includes these problematic duty cycles (or their vicinity), reliability of the converter can be severely compromised. In practical implementation, it is useful to investigate the impact of non-idealities on the controllability of the SC stage.

In discrete designs, ceramic capacitors are commonly used as flying capacitors. While providing high capacitance density and low ESR, some ceramic capacitors suffer from DC voltage derating[1]: the actual capacitance becomes lower when the applied DC voltage goes higher. In the previous example of a 4-cell FCML converter with $D = 2/4$, the DC voltage of each flying capacitor is different, leading to unequal capacitance. In this case, the charge transfer matrix becomes:

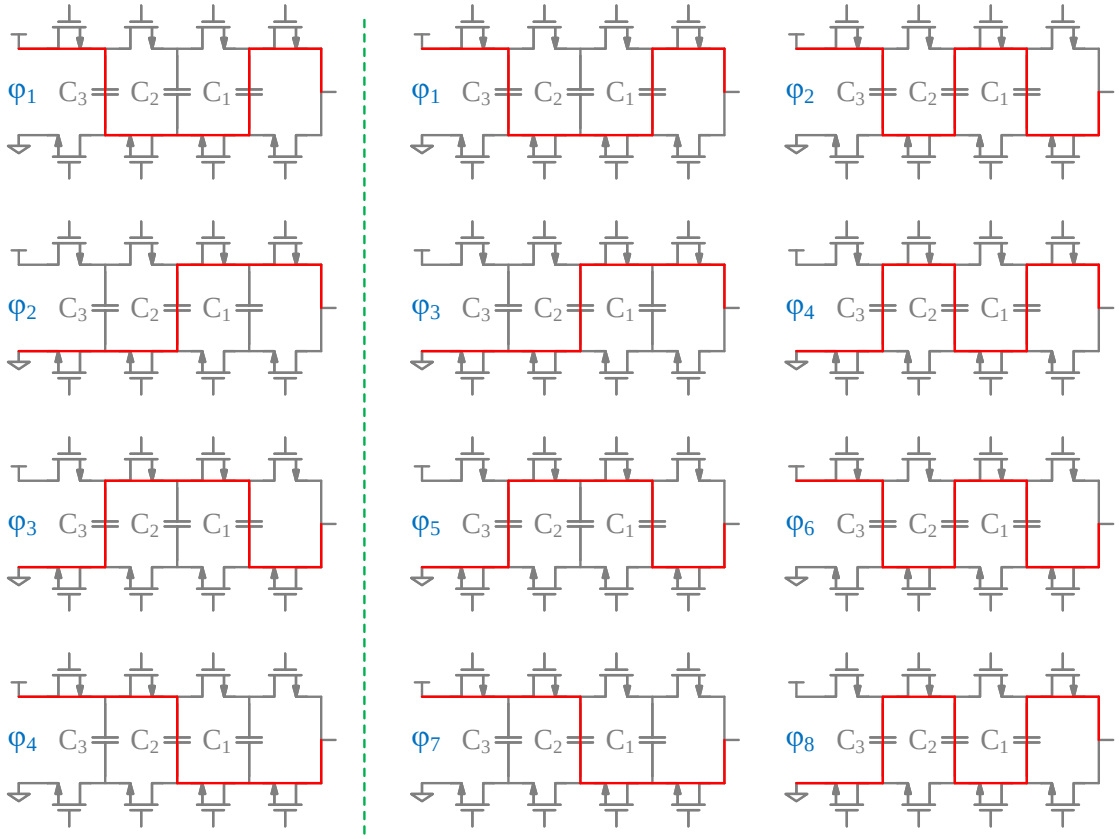
$$\boldsymbol{B_1} = \begin{bmatrix} -\frac{1}{C_1} & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{C_2} & 0 & \frac{1}{C_2} \\ \frac{1}{C_3} & 0 & -\frac{1}{C_3} & 0 \end{bmatrix}. \tag{3.26}$$

Compared to the original charge transfer matrix, each row of $\boldsymbol{B_1}$ is scaled by a factor of C_f/C_i ($i = 1, 2, 3$), or the 'derating ratio'. Since scaling the entire row of a matrix does not change its rank, the rank of $\boldsymbol{B_1}$ and $\boldsymbol{C}$ are still the same. Therefore, the conclusion on controllability is not affected by having unequal flying capacitance, either due to derating or design choice.

To overcome the challenge of uncontrollable SC stage at certain duty cycles, the analysis in the previous section motivates a simple and direct approach. It is possible to modify

[1]This is usually a problem for class II ceramic capacitors using high-permittivity dielectric materials, such as X7R. It can be mitigated by using class I (e.g., C0G) ceramic capacitors, which do not have the derating problem, but at the cost of significantly reduced capacitance density.

the switching sequence to make the connection matrix, $\boldsymbol{C}$, full-rank, so that the SC stage becomes controllable, thus both natural balance and active balance are achieved. The new switching sequence, modified phase-shifted pulse width modulation (PSPWM), introduces additional switching phases to extend the dimension of $\boldsymbol{C}$. The switching diagram of both conventional and modified PSPWM are shown in Figure 3.10. The current conduction path in each phase is highlighted; the corresponding connection matrix is also shown.



(a) PSPWM (b) modified PSPWM

Figure 3.10: Comparison between conventional and modified PSPWM for a 4-cell FCML converter with $D = 2/4$. Note that the connection matrix, $\boldsymbol{C}$, is transposed.

Theoretically, one additional phase is already enough to make $\boldsymbol{C}$ full-rank, however, modified PSPWM introduces 4 additional phases ($\varphi_2, \varphi_4, \varphi_6, \varphi_8$) to keep capacitor charge

balance and to maintain symmetry. The output voltage is not affected, since the additional phases give the same switching node voltage as the conventional phases. The gate driving loss is also not changed: in conventional PSPWM, each switch turns on and off once every 4 phases; in modified PSPWM, each switch turns on and off twice every 8 phases.

The state-space zero-input response is also compared for conventional and modified PSPWM in Figure 3.11. It was already discussed that at $D = 2/4$, the SC stage is not controllable in conventional PSPWM; the zero-input response has non-zero steady state and natural balance fails. But with modified PSPWM, the SC stage becomes controllable because $\boldsymbol{C}$ is full-rank. The zero-input response decays to zero in steady state and natural balance may function.

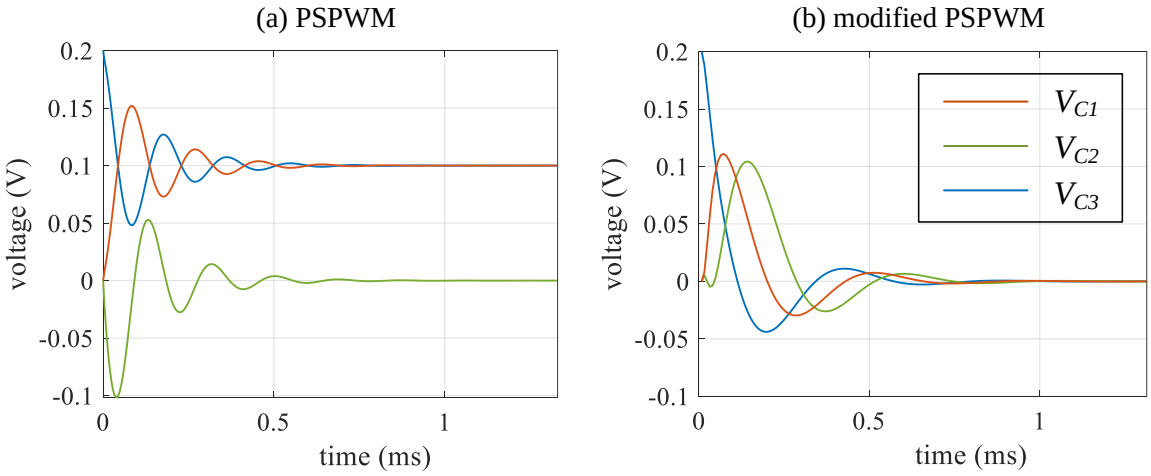


Figure 3.11: Simulated zero-input response of a 4-cell FCML converter with $D = 2/4$, under conventional and modified PSPWM operation.

Modified PSPWM can be extended to inductive mode. As discussed earlier, an FCML converter operating in inductive mode is effectvely multiplexing between two neighboring resonant modes. If the converter spends majority of the time in an uncontrollable resonant mode, the effectiveness of natural balance deteriorates, causing larger imbalance quantity in the presence of external disturbances. In this case, modified PSPWM should be applied to the uncontrollable resonant mode, so that the FCML converter multiplexes between two controllable modes, which improves balance.

V_{in} = 24V

C_{in} = 13.2uF

C_{out} = 9.9uF

C_{fly} = 3.3uF

L = 1uH

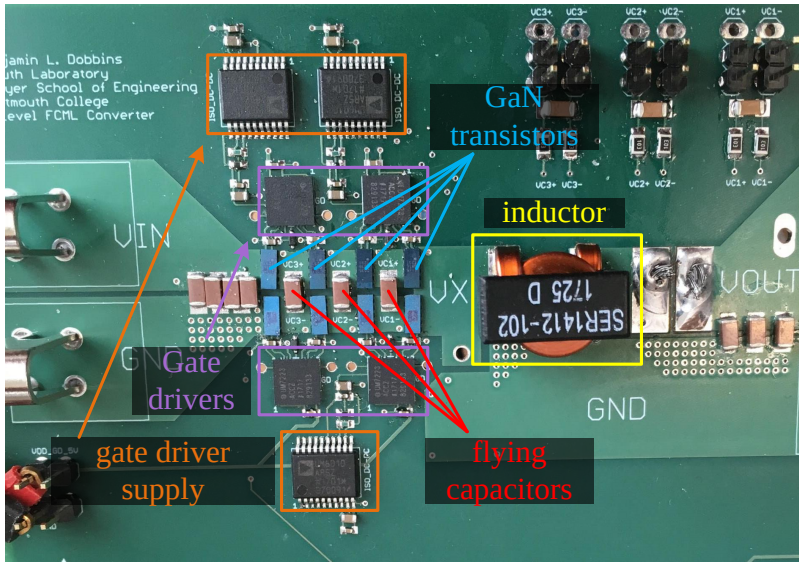


Figure 3.12: Annotated photo of the 4-cell FCML converter PCB.

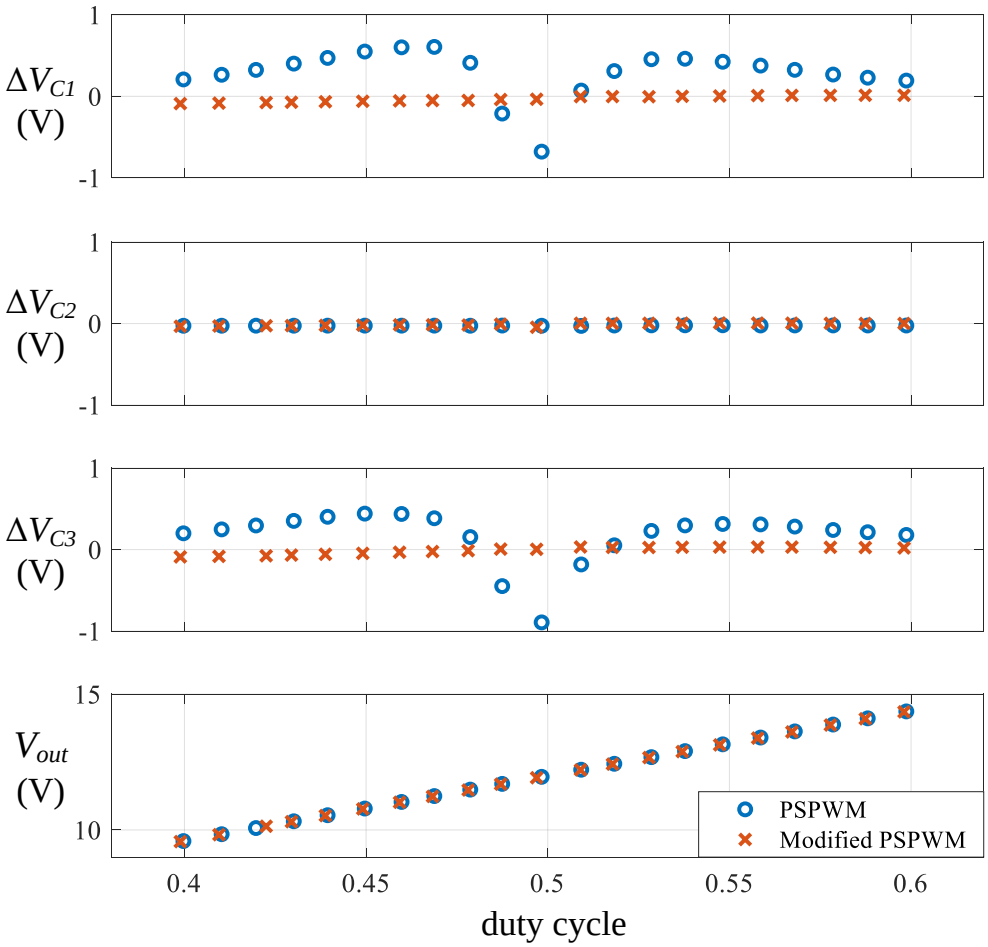


Figure 3.13: Steady state voltage measurements in conventional and modified PSPWM.

A 4-cell FCML converter was built to test the performance of modified PSPWM. The annotated photo of the printed circuit board (PCB) is pictured in Figure 3.12. In steady state, the flying capacitor voltages and output voltage are measured at $0.4 < D < 0.6$, where imbalance is most problematic. The imbalance quantities, ΔV_{Ci}, which represent the difference between the measured values to the balanced values, as well as the output voltage are plotted in Figure 3.13. The results show that modified PSPWM significantly reduces imbalance quantities (strengthens natural balance) in the vicinity of uncontrollable duty cycles, while the output voltage remains unaffected. Furthermore, it is verified that C_1 and C_3 are subject to imbalance, but C_2 is not.

However, this improvement is achieved at the cost of higher conduction loss. Shown in Figure 3.10, compared to conventional scheme, modified PSPWM (on average) has more flying capacitors in the current conduction path, leading to increased ESR. Additioanlly, the smaller effective flying capacitance increases the resonant frequency, causing larger root mean square (RMS) current. On the other hand, modified PSPWM improves balance, thus the ripple and associated loss is reduced. Therefore, the overall impact on efficiency depends on whether the penalty or the benefit has a larger effect.

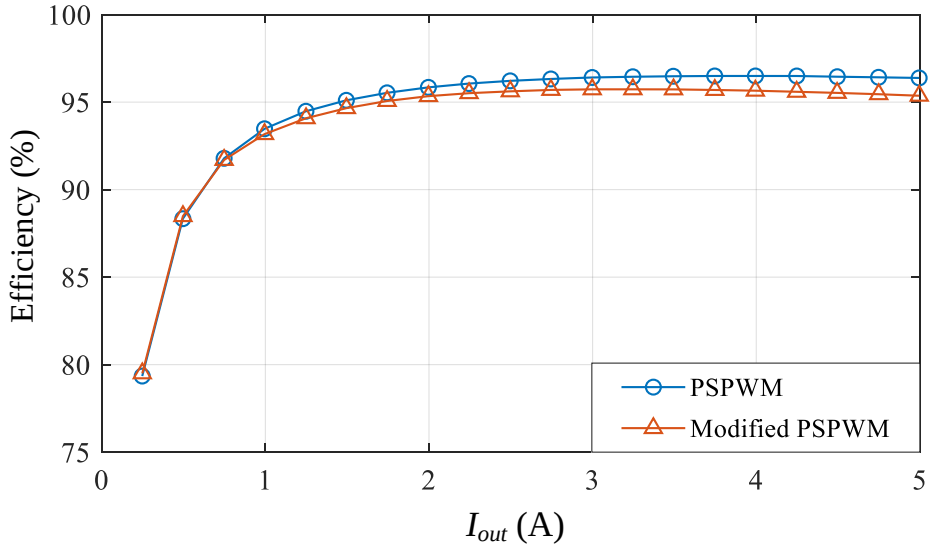


Figure 3.14: Efficiency of conventional and modified PSPWM at 24V:12V.

For this prototype, the efficiency in both conventional and modified PSPWM is shown in Figure 3.14. At light load where switching loss dominates, the two schemes have similar efficiency. But modified PSPWM is less efficient at heavy load, where the conduction loss dominates, meaning that the penalty wins in this example.

Modified PSPWM not only allows natural balance but also enables controllability at duty cycles that are conventionally uncontrollable. In applications where natural balance is too weak to ensure robust operation, active balance techniques can be applied to enforce balance and accelerate the dynamics, which will be discussed in the next chapter.

Chapter 4

Constant Switch Stress Control

Various control algorithms have been developed to regulate flying capacitor voltages in hybrid SC converters. Current mode control achieves balance by aligning the inductor valley or peak current [60], with its variations further improving the light-load stability and transient response [63, 64]. However, high-bandwidth current sensing is often difficult due to challenges in instrumentation. Although it was shown in [75] that balance can be achieved by only sensing the inductor current ripple, it still requires accurate zero crossing detection and valley current matching. Voltage mode algorithms were explored to eliminate the need for current sensing. Phase-shift control balances flying capacitors by adjusting the phase of PWM signals [76], but it requires digital proportional-integral-derivative (PID) compensation and has only been demonstrated on a 3-level buck converter. Modified ripple injection control can potentially be used in multiple hybrid SC topologies [68, 77], but it leads to variable switching frequency and is only applicable to integrated designs due to complexity of signal processing.

Motivated by the need for a balancing algorithm with both fast transient response and simple implementation, this chapter presents the constant switch stress (CSS) algorithm that achieves active balance as well as output voltage regulation for direct type hybrid SC converters. CSS control regulates the final V_x in each phase to achieve balance, therefore,

neither current sensing nor complicated signal processing is required. Based on hysteretic algorithms, CSS control also has the advantage of fast transient response. Certain parts of the chapter was previously presented in IEEE Applied Power Electronics Conference and Exposition (APEC) in 2022 [78].

4.1 Control Principle

Pure SC converters are automatically balanced since flying capacitor voltages are rigidly constrained by KVL. In hybrid SC converters, the same constraints can be duplicated by regulating the switching node voltage, V_x, in certain phases. This concept will be illustrated by a 4-cell FCML converter with $0 < D < 1/4$. Its schematic is shown in Figure 4.1.

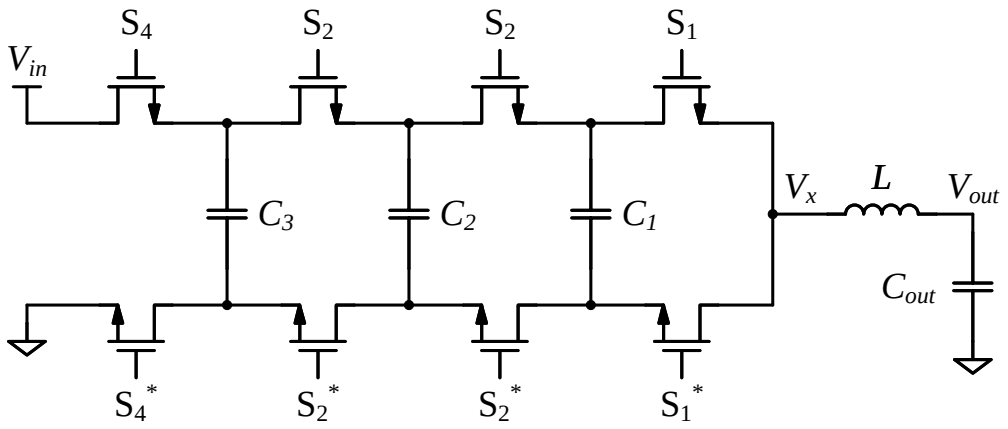


Figure 4.1: Schematic of a 4-cell FCML converter.

During each phase, the SC network is configured into a certain connection, leading to the equivalent circuits shown in Figure 4.2. These phases are classified into two categories: the *high* phases ($H_1 - H_4$) where the switching node is connected to one or more flying capacitors, and the *ground* phase (G) where the switching node is connected to ground. Figure 4.2 also shows the phase transition diagram of the converter: the high phases are circulated sequentially and the ground phase is inserted between adjacent high phases to

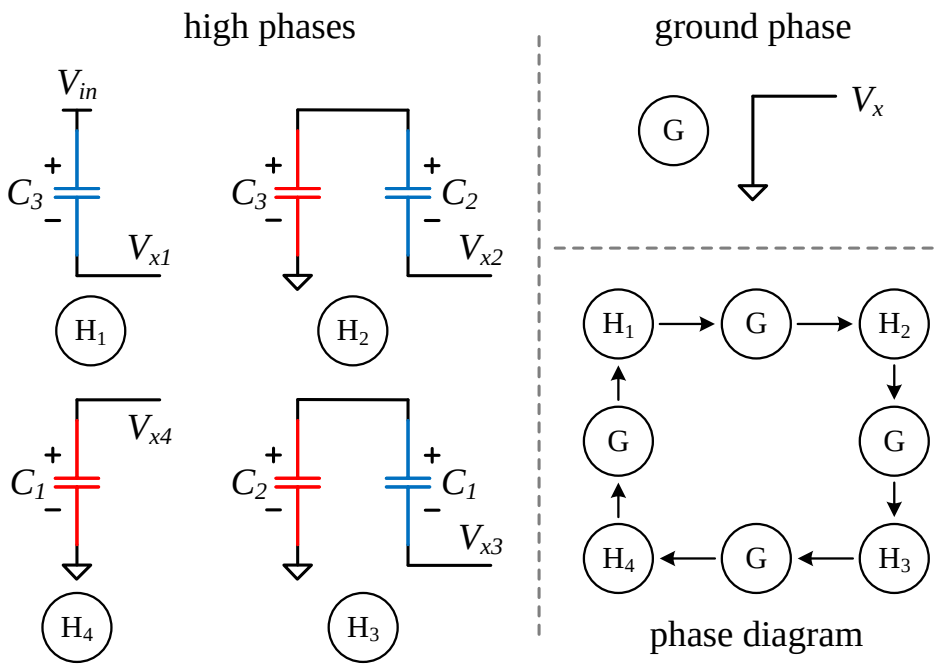


Figure 4.2: Equivalent circuits of the SC stage and phase transition diagram.

enable output voltage adjustment.

For high state H_j $(j = 1, 2, 3, 4)$, the initial and final time are defined as t_{ij} and t_{fj}, respectively; the switching node voltage is denoted as V_{xj}. In high state H_1 for example, KVL equations can be written at t_{i1} and t_{f1}:

$$V_{x1}(t_{i1}) = V_{in} - V_{C3}(t_{i1}), \tag{4.1}$$

$$V_{x1}(t_{f1}) = V_{in} - V_{C3}(t_{f1}). \tag{4.2}$$

Averaging (4.1) and (4.2) yields

$$\frac{V_{x1}(t_{i1}) + V_{x1}(t_{f1})}{2} = V_{in} - \frac{V_{C3}(t_{i1}) + V_{C3}(t_{f1})}{2}. \tag{4.3}$$

For simplicity of notation, the algebraic average of initial and final value is introduced:

$$\widetilde{X} = \frac{X(t_{ij}) + X(t_{fj})}{2}, \tag{4.4}$$

where X is a general quantity which can represent the flying capacitor voltage, switching node voltage, etc. Hence, (4.3) can be written as

$$\widetilde{V}_{x1} = V_{in} - \widetilde{V}_{C3}. \tag{4.5}$$

Similar relationships can be derived for other high phases:

$$\widetilde{V}_{x2} = \widetilde{V}_{C3} - \widetilde{V}_{C2}, \tag{4.6}$$

$$\widetilde{V}_{x3} = \widetilde{V}_{C2} - \widetilde{V}_{C1}, \tag{4.7}$$

$$\widetilde{V}_{x4} = \widetilde{V}_{C1}. \tag{4.8}$$

Equations (4.5)-(4.8) can be packed into matrix form:

$$\begin{bmatrix} \widetilde{V}_{x1} \\ \widetilde{V}_{x2} \\ \widetilde{V}_{x3} \\ \widetilde{V}_{x4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & -1 & 1 \\ -1 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \widetilde{V}_{C1} \\ \widetilde{V}_{C2} \\ \widetilde{V}_{C3} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in}, \tag{4.9}$$

or simply denoted as

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{x}} = \boldsymbol{C} \cdot \widetilde{\boldsymbol{V}}_{\boldsymbol{C}} + \boldsymbol{W} \cdot V_{in}, \tag{4.10}$$

where $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$ and $\widetilde{\boldsymbol{V}}_{\boldsymbol{C}}$ are vectors of the switching node voltage and flying capacitor voltages, respectively; $\boldsymbol{C}$ is the connection matrix. Note that (4.10) has the same form as averaged output equation of the SC stage, (3.7). However, here no assumption has been made on the trajectory of V_x waveform.

According to the analysis in Chapter 2, if the SC stage is controllable (active balance is possible), the connection matrix, $\boldsymbol{C}$, must be full-rank. Under this circumstance, $\widetilde{\boldsymbol{V}}_{\boldsymbol{C}}$ can

be uniquely determined by solving (4.10):

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{C}} = \boldsymbol{C}^{\dagger} \cdot (\widetilde{\boldsymbol{V}}_{\boldsymbol{x}} - \boldsymbol{W} \cdot V_{in}), \tag{4.11}$$

where $\boldsymbol{C}^{\dagger}$ is the pseudoinverse of $\boldsymbol{C}$. If the switching node voltage during high phases are regulated to

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{x}} = \begin{bmatrix} \frac{1}{4} \\ \frac{1}{4} \\ \frac{1}{4} \\ \frac{1}{4} \end{bmatrix} \cdot V_{in}, \tag{4.12}$$

the solution given by (4.11) is

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{C}} = \begin{bmatrix} \frac{1}{4} \\ \frac{2}{4} \\ \frac{3}{4} \end{bmatrix} \cdot V_{in}, \tag{4.13}$$

which is the balanced voltage. Alternatively speaking, regulating $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$ to the correct value will force flying capacitors to balance. For a N-cell FCML converter with $0 < D < 1/N$, this correct value is V_{in}/N. For other direct hybrid topologies (Dickson, series-parallel, Fibonacci, etc.), this value is given by the ideal output voltage of their pure SC version. This important conclusion serves as the foundation of CSS control.

4.2 Control Implementation

Although the previous conclusion provides a simple approach to achieve active balance, regulation of $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$ is not straightforward, as it depends on both initial and final values. This

section explains the practical implementation of CSS control: it will be shown that only the final value needs to be regulated.

The first constraint on $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$ is obtained by adding up (4.5)-(4.8):

$$\widetilde{V}_{x1} + \widetilde{V}_{x2} + \widetilde{V}_{x3} + \widetilde{V}_{x4} = V_{in}, \tag{4.14}$$

which also helps explain why the output voltage of hybrid SC converters is not affected by imbalance: the time-domain average of V_x, which determines the DC level of V_{out}, is independent from flying capacitor voltages.

During high phase H_j, the charge transferred to the output is denoted as q_j. As an example, flying capacitor C_3 is charged by q_1 and discharged by q_2. Across a steady-state period, the net charge flow of a capacitor has to be zero, indicating $q_1 = q_2$. Eventually, the charge balance of all flying capacitors require:

$$q_1 = q_2 = q_3 = q_4. \tag{4.15}$$

Charge q_j can be expressed as the voltage drop from initial to final moment on the switching node multiplies the Thevenin equivalent flying capacitance, $C_{x,j}$:

$$q_j = (V_{xj}(t_{ij}) - V_{xj}(t_{fj})) \cdot C_{x,j}. \tag{4.16}$$

During H_1 and H_4, only one flying capacitor is connected to the switching node; in H_2 and H_3, two flying capacitors are connected in series between V_x and ground. Assuming all flying capacitors have equal capacitance[1], C_f, the equivalent capacitance is given by

$$C_{x,j} = \begin{cases} C_f, & j = 1, 4 \\ \dfrac{C_f}{2}. & j = 2, 3 \end{cases} \tag{4.17}$$

[1] error caused by unequal flying capacitance will be analyzed later

Substituting (4.16) and (4.17) into (4.15) yields

$$V_{xm}(t_{im}) - V_{xm}(t_{fm}) = 2[V_{xn}(t_{in}) - V_{xn}(t_{fn})], \tag{4.18}$$

where $m = 2, 3$ and $n = 1, 4$, indicating that voltage drop on the switching node during H_2 and H_3 are twice larger than in H_1 and H_4 because the equivalent flying capacitance is halved. Equation (4.18) sets the second constraint on $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$.

Pictured in Figure 4.3(a), in CSS control, a design variable ΔV is chosen and the final value of V_{xj} is regulated as below:

$$V_{xj}(t_{fj}) = \begin{cases} \dfrac{V_{in}}{4} - \Delta V, & j = 1, 4 \\ \dfrac{V_{in}}{4} - 2\Delta V. & j = 2, 3 \end{cases} \tag{4.19}$$

It sets the third constraint, which is also an artificial one, on $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$. Solving three constraints, (4.14), (4.18), (4.19), yields

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{x}} = \begin{bmatrix} \frac{1}{4} \\ \frac{1}{4} \\ \frac{1}{4} \\ \frac{1}{4} \end{bmatrix} \cdot V_{in}, \tag{4.20}$$

which forces the flying capacitors to balance, according to the previous conclusion. Since (4.14) and (4.18) are inherent to the topology, the controller only needs to realize (4.19) to achieve active balance. This can be implemented with a comparator that monitors the real-time V_x: once it reaches the desired final value in high phases, a transition to ground phase is triggered such that the final value is enforced. A similar concept was introduced in reference [19].

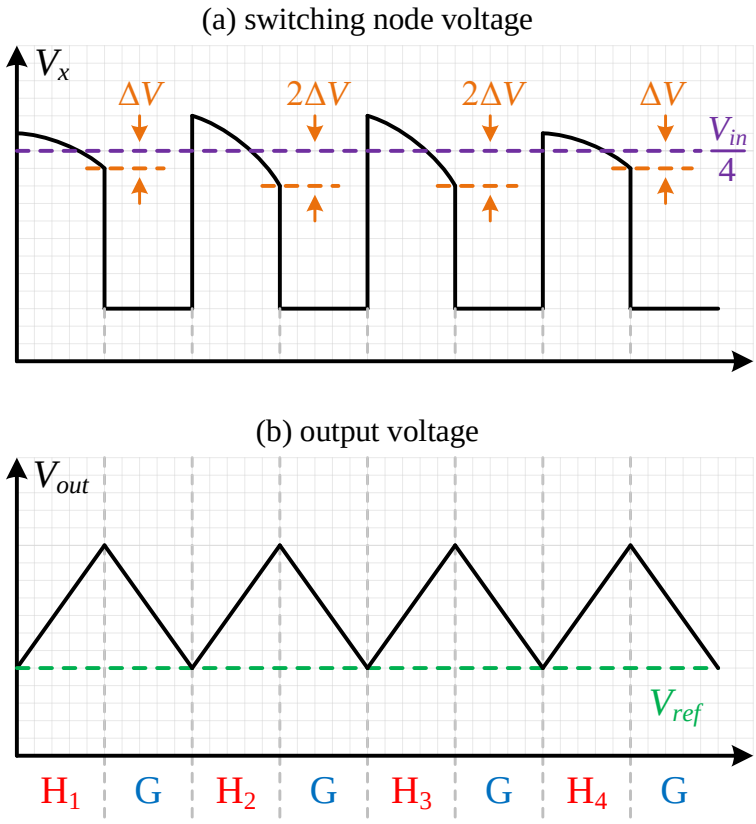


Figure 4.3: Waveform in CSS control: (a) switching node voltage, (b) output voltage.

The balancing control, (4.19), defines the transition from high phases to ground phase, or determines the duration of high phases. As no flying capacitor is charged or discharged in the ground phase, its duration may be freely adjusted, to some extent, without impacting the balance. This additional degree of freedom can be used to achieve output voltage regulation, where multiple 'off time' based algorithms are compatible, such as pulse frequency modulation (PFM), adaptive off time control [79]. The general principle is that *duration of high phases ensures balance, and duration of the ground phase is adjusted accordingly to maintain output regulation.*

In this work, V_{out} is regulated by a single-bounded hysteresis loop, due to its simplicity of implementation. Hysteresis-based methods often require a portion of indutcor current ripple, $I_{L,AC}$, in the feedback loop to prevent overshoot in dynamic response [80]. While

multiple ways exist, one convenient and widely used approach is to leverage an existing or introduced resistance, R_o, in series with the output bypass capacitor, C_{out}, such that the actual V_{out} is given by

$$V_{out} = V_{Cout} + R_o \cdot I_{L,AC}. \tag{4.21}$$

With a proper R_o, V_{out} can be almost 'in-phase' with $I_{L,AC}$: it rises when V_x is high and falls when V_x is grounded, as illustrated in Figure 4.3(b). Hence, transition from the ground phase to high phases can be trigger when V_{out} falls to the reference voltage, V_{ref}.

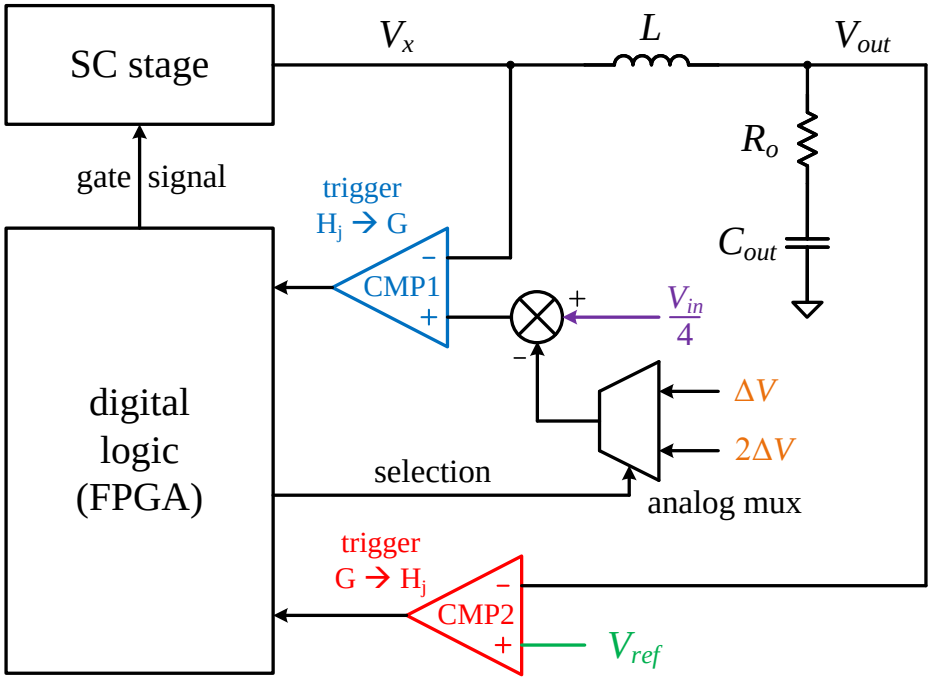


Figure 4.4: Simplified diagram of constant switch stress control.

With both balancing loop and output regulation loop explored, the conceptual diagram of CSS control is illustrated in Figure 4.4. The analog multiplexer selects either ΔV or $2\Delta V$ depending on the current switching phase. This result is subtracted from $V_{in}/4$ to generate the desired final value of V_x, which is compared to the real-time V_x to trigger the transition from high phases to the ground phase. The output voltage is also compared to the reference voltage to trigger the other transition edge ($G \rightarrow H_j$). Based on the output of

the two comparators, the digital logic (implemented with an FPGA) advances through the phase diagram and generates gate signals for indivudual transisitors in the SC stage.

CSS control can also be viewed in the state plane, as illustrated in Figure 4.5 with a 3-level example for convenience of observation. In the active balancing loop, the high phases are terminated when the flying capacitor voltage, V_{Cfly}, reaches $V_{in}/2 \pm \Delta V$, where the corresponding $I_{L,AC}$ limit is obtained (marked by orange). In the output regulation loop, the hyesteresis boundary is defined by the $I_{L,AC}$ limit and the line $V_{Cout} + R_o I_{L,AC} = V_{ref}$ (marked by green).

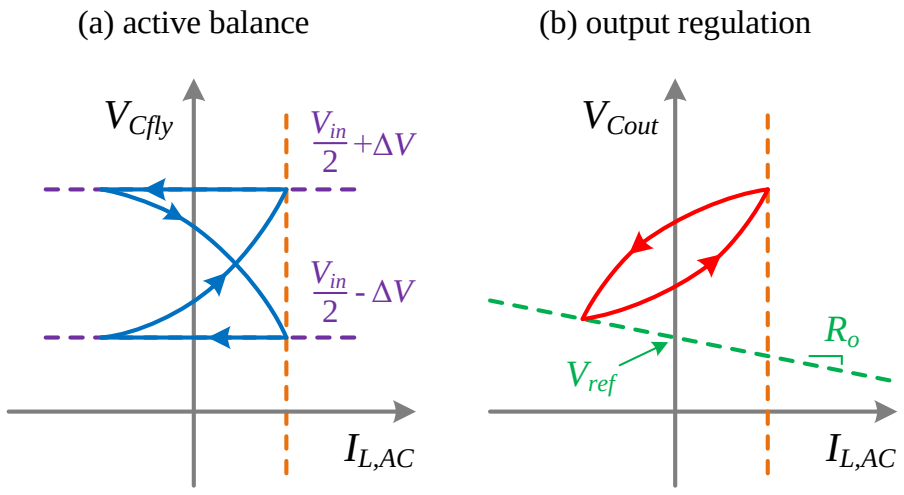


Figure 4.5: State plane view of CSS control for a 3-level hybrid SC converter.

The diagram in Figure 4.4 only demonstrates the basic function of CSS control with minimum hardware requirement. More features can be added to further improve the performance, leading to multi-mode operation under different loading conditions, which will be discussed in the next section.

4.3 Multi-Mode Operation

At light load, the discontinuous conduction mode (DCM) can be implemented with a zero crossing detector (ZCD) to prevent negative inductor current and to reduce the switching frequency as well as associated losses. As shown in Figure 4.6, during the ground phase G, the ZCD senses the inductor current polarity by measuring the voltage drop across the switch on resistance, R_{on}. This configuration is only an example as many other ZCD schemes can be implemented in practice. Once the inductor current falls to zero, the converter transitions to the DCM phase D, where the SC stage presents high impedance and keeps the inductor current at zero. Similar to the basic operation, the next high phase H_j is triggered when V_{out} reaches V_{ref} and the converter exits the DCM phase.

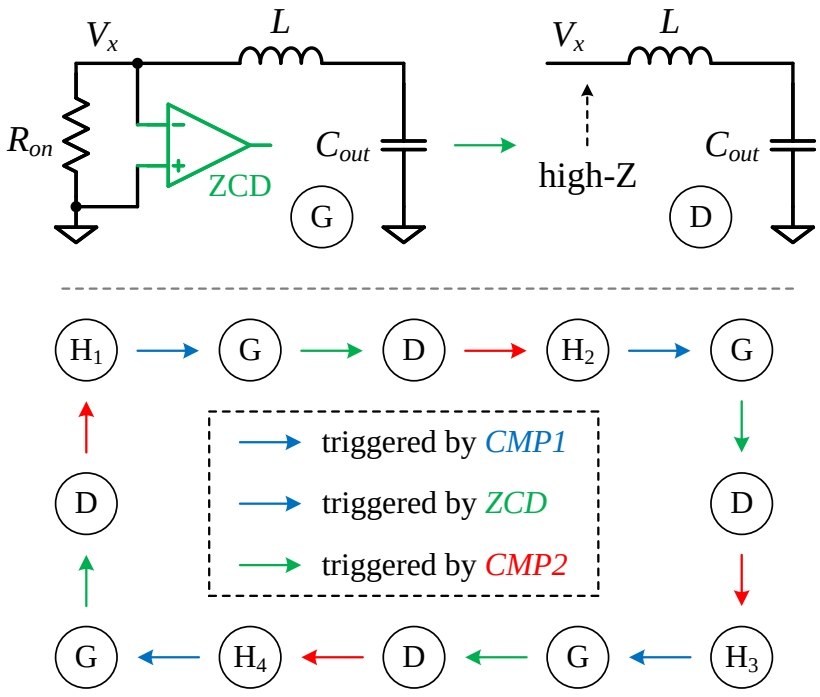


Figure 4.6: Illustration of the DCM operation.

It should be emphasized that the ZCD used in DCM is fundamentally different from the high-bandwidth current sensor required in typical current-mode control. The ZCD can be slow because the DCM phase transition is not necessarily determined in real-time: with

'sub-sampling' strategy, the accurate zero-crossing point may be obtained after a certain number of periods. However, the current sensor in current-mode control has to be fast to ensure good transient response. Therefore, the ZCD in CSS control does not necessarily mean that it is a current-mode algorithm. It is only one approach to realise DCM.

As the load current increases to where the inductor current does not reach zero, the converter enters continuous conduction mode (CCM). Under this circumstance, it is useful to investigate the switching frequency. In steady state, the charge transfer during each high phase can be obtained from (4.16):

$$q_j = (V_{xj}(t_{ij}) - V_{xj}(t_{fj})) \cdot C_{x,j} = 2\Delta V \cdot C_f. \tag{4.22}$$

It can also be expressed in terms of the switching frequency, f_{sw}:

$$q_j = \frac{I_{out} V_{out}}{f_{sw} V_{in}}. \tag{4.23}$$

Equating (4.22) and (4.23) yields

$$f_{sw} = \frac{I_{out} V_{out}}{2 C_f V_{in} \Delta V}, \tag{4.24}$$

indicating that the switching frequency varies with operating conditions of the converter (V_{in}, V_{out}, I_{out}). In certain applications, a variable switching frequency may cause concerns on electromagnetic interference (EMI), ripple, etc. However, (4.24) also shows that ΔV can be tuned to adjust f_{sw}, or specifically, to maintain constant f_{sw} with varying operating conditions. Figure 4.7 illustrates an example of such algorithm, which may be interpreted as a form of adaptive on-time (AOT) control.

The voltage $V_{in}/4$ is produced by a resistor divider followed by an analog buffer. The current-sinking digital to analog converter (DAC) draws a current from the buffer output through resistor R, generating a voltage drop that serves as either the ΔV or $2\Delta V$ term,

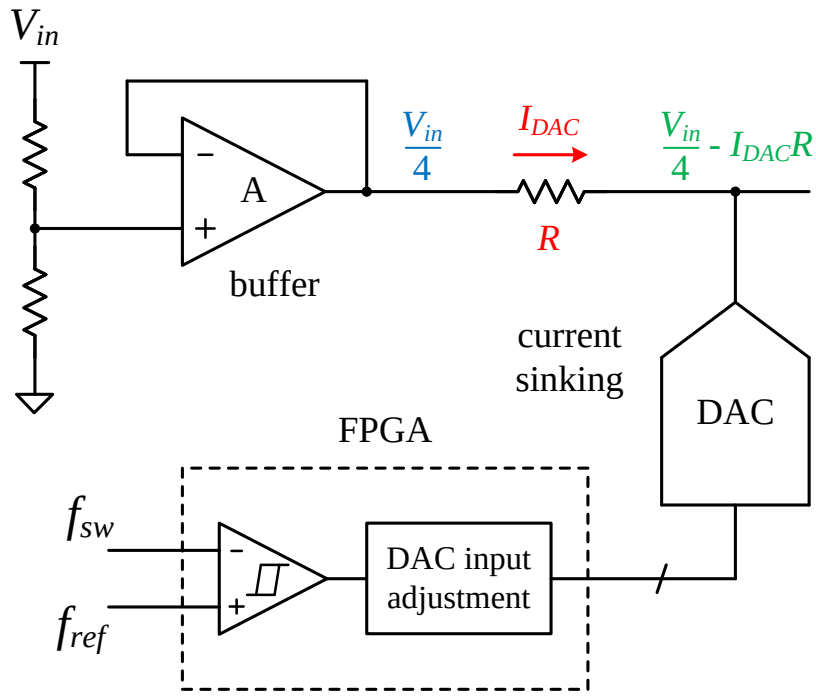


Figure 4.7: Implementation of ΔV dynamic scaling.

depending on the current switching phase:

$$I_{DAC}R = \begin{cases} \Delta V, & \text{in } H_1, H_4 \\ 2\Delta V. & \text{in } H_2, H_3 \end{cases} \tag{4.25}$$

Input of the DAC is controlled by the FPGA, where f_{sw} is compared against a reference frequency, f_{ref}. If f_{sw} is too high, the current I_{DAC} is increased, providing a larger ΔV. This action brings f_{sw} down according to (4.24). Similar negative feedback also applies when f_{sw} is too low, and f_{sw} is kept relatively constant around f_{ref}. The operating mode where ΔV is dynamically adjusted is called constant switching frequency (CSF) mode.

Substituting $f_{sw} = f_{ref}$ into (4.24) gives the ΔV in ideal scenario:

$$\Delta V = \frac{I_{out}V_{out}}{2C_f V_{in} f_{ref}}. \tag{4.26}$$

In practice, it is quantized due to limited resolution of the DAC. Equation (4.26) indicates that ΔV increases with higher load current, however, it cannot be adjusted arbitrarily. Its lower bound, ΔV_{min}, determines when the converter enters DCM, and the upper bound, ΔV_{max}, is limited by the drain-to-source voltage rating of semiconductor switches.

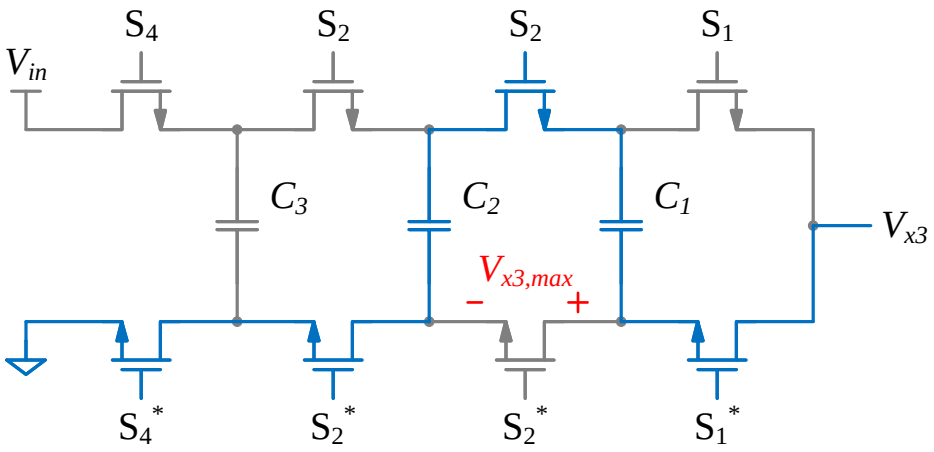


Figure 4.8: Current conduction path in high phase H_3.

Figure 4.8 shows the current conduction path during high phase H_3. Neglecting switch on-state resistance, the voltage stress on S_2^* is equal to the switching node voltage, V_{x3}. Referring to Figure 4.3, the maximum of this value is

$$V_{x3,max} = \frac{V_{in}}{4} + 2\Delta V. \tag{4.27}$$

Therefore, upper limit of ΔV is given by:

$$\Delta V_{max} = \frac{V_{rate}}{2} - \frac{V_{in}}{8}, \tag{4.28}$$

where V_{rate} represents switch voltage rating (with some margin in practice). When ΔV is already at ΔV_{max}, even if f_{sw} is higher than f_{ref}, ΔV cannot be increased to bring down f_{sw} due to reliability concerns. From another perspective, when the load current becomes too high, f_{sw} is allowed to exceed f_{ref}, since it is the only way to deliver the required

current to the output without overstressing the switches. The operating mode where ΔV is kept at maximum is called constant switch stress (CSS) mode.

Figure 4.9 summarizes multi-mode operation of the 4-cell FCML converter under CSS control. At light load, DCM operation eliminates negative inductor current, reducing the switching frequency as well as the associated losses. At medium load, ΔV is dynamically adjusted to maintain relatively constant switching frequency. At heavy load, the switching frequency is allowed to exceed f_{ref} to prevent switch overstress.

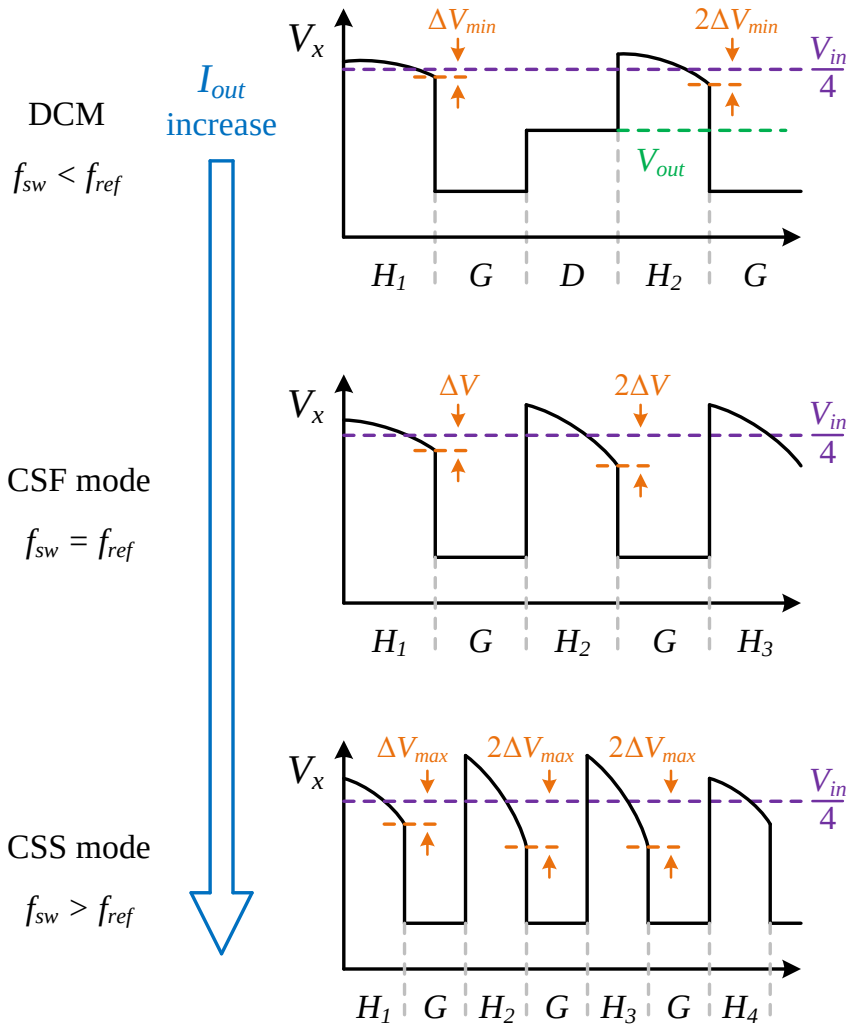


Figure 4.9: Summary of multi-mode operation of CSS control.

4.4 Error Analysis

The accuracy of the balancing loop is mainly affected by the following random errors:

1. Flying capacitance may not be the exact nominal value of choice, either due to DC derating or manufacturing variation. Therefore, the final value of V_x calculated from flying capacitance ratios may not be the value that leads to perfect balance.

2. Transition from high phases to the ground phase is triggered by a comparator; any offset or delay makes the actual final value of V_x different from desired.

3. Other factors that may shift the actual final value of V_x, such as quantization noise of the DAC, ringing caused by parasitics.

The effect of above random errors can be lumped into a difference between the actual switching node voltage in the implemented converter, $\widetilde{\boldsymbol{V}}_{\boldsymbol{x}}$, and the switching node voltage that leads to perfect balance, $\widetilde{\boldsymbol{V}}_{\boldsymbol{x,b}}$:

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{x,e}} = \widetilde{\boldsymbol{V}}_{\boldsymbol{x}} - \widetilde{\boldsymbol{V}}_{\boldsymbol{x,b}}. \tag{4.29}$$

The subsequent imbalance quantity of flying capacitor voltages, $\widetilde{\boldsymbol{V}}_{\boldsymbol{C,e}}$, can be obtained by differentiating (4.11):

$$\widetilde{\boldsymbol{V}}_{\boldsymbol{C,e}} = \frac{\partial \widetilde{\boldsymbol{V}}_{\boldsymbol{C}}}{\partial \widetilde{\boldsymbol{V}}_{\boldsymbol{x}}} \cdot \widetilde{\boldsymbol{V}}_{\boldsymbol{x,e}} = \boldsymbol{C}^{\dagger} \widetilde{\boldsymbol{V}}_{\boldsymbol{x,e}}. \tag{4.30}$$

The *Euclidean norm* can be used to quantify the magnitude of a vector:

$$||\widetilde{\boldsymbol{V}}_{\boldsymbol{x,e}}||_2 = \sqrt{\widetilde{V}_{x1,e}^2 + \widetilde{V}_{x2,e}^2 + \widetilde{V}_{x3,e}^2 + \widetilde{V}_{x4,e}^2}, \tag{4.31}$$

$$||\widetilde{\boldsymbol{V}}_{\boldsymbol{C,e}}||_2 = \sqrt{\widetilde{V}_{C1,e}^2 + \widetilde{V}_{C2,e}^2 + \widetilde{V}_{C3,e}^2}. \tag{4.32}$$

The corresponding metric for a matrix is the *spectral norm*, representing the maximum of its singular values[2]:

$$||\boldsymbol{C}^{\dagger}||_2 = \sigma_{max}(\boldsymbol{C}^{\dagger}). \tag{4.33}$$

[2]obtained from the singular value decomposition (SVD); refer to [81].

The relationship in (4.30) determines the upper bound of imbalance quantity:

$$||\widetilde{\boldsymbol{V}}_{\boldsymbol{C,e}}||_2 \leq ||\boldsymbol{C}^{\dagger}||_2 \cdot ||\widetilde{\boldsymbol{V}}_{\boldsymbol{x,e}}||_2. \tag{4.34}$$

In this example of 4-cell FCML converter, the numerical value of $||\boldsymbol{C}^{\dagger}||_2$ is 1.31, indicating that for a small random error, $||\widetilde{\boldsymbol{V}}_{\boldsymbol{x,e}}||$, the resulting balancing error, $||\widetilde{\boldsymbol{V}}_{\boldsymbol{C,e}}||$, is comparably small. It should be noticed that $||\boldsymbol{C}^{\dagger}||_2$ is only a ratio between two steady-state quantities; the fact that it is larger than one has no implication on stability or steady state response.

Different from active balance, the regulation loop mainly suffers from systematic error. It results from the fact that V_{out} is controlled by a single-bounded hysteretic loop. Its DC value is defined by the lower bound, V_{ref}, and the ripple, ΔV_{out}:

$$V_{out,DC} = V_{ref} + \frac{\Delta V_{out}}{2}. \tag{4.35}$$

If the output capacitor, C_{out}, is sufficiently large, the ripple is given by

$$\Delta V_{out} \approx \frac{R_o C_f (V_{in} - 4V_{out})\Delta V}{2LI_{out}}, \tag{4.36}$$

where R_o is the series resistance of the output capacitor. The DC error can be compensated by setting V_{ref} 'half a ripple' lower, however, during transients, excessive V_{out} overshoot may occur because it does not have a well-defined upper bound.

To mitigate this issue, another comparator, *CMP3*, is needed to detect such overshoot and override *CMP1* to trigger the ground phase, but it should not interfere with the steady state operation, as illustrated in Figure 4.10. Assuming the converter first operates in steady state. During the ground phase, a line transient occurs and V_{in} rapidly reduces to a lower level. Without *CMP3*, high phase H_2 is not terminated until V_x is $2\Delta V$ below the new $V_{in}/4$, leading to an excessively long duration where V_{out} keeps rising. However, with *CMP3*, high phase H_2 is terminated once V_{out} reaches the maximum tolerable overshoot,

$V_{out,max}$, setting an upper bound during transients.

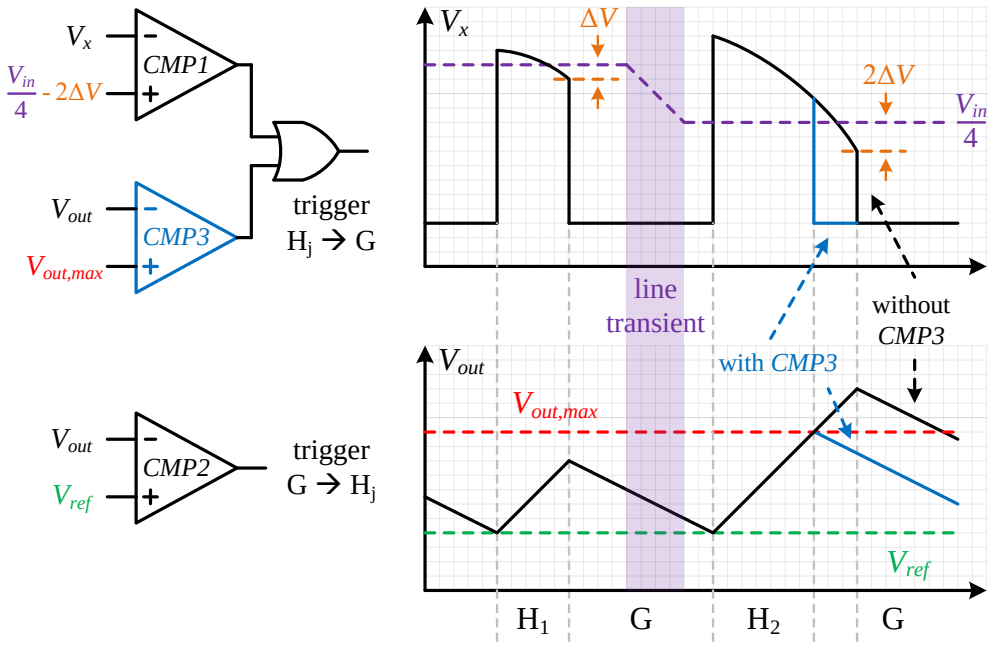


Figure 4.10: Introducing *CMP3* to limit V_{out} overshoot during transients.

Figure 4.10 also indicates that there is a trade-off between active balancing and output regulation. The addition of *CMP3* aims to improve the accuracy of output regulation in transients, but it inevitably compromises the speed of active balance, because it stops V_x from reaching the desired final value in H_2.

Although adding *CMP3* is only an example of limiting V_{out} overshoot[3], this trade-off is universal to voltage mode control of direct hybrid SC converters. To balance the flying capacitors, the duration of a high phase should be extended if its V_x is too high and be shortened if its V_x is too low. As an example, for a line step-up transient, extending a high phase fights against V_{out} regulation. The fundamental cause is the contradicting goals on charge transfer: active balance requires more charge transfer in some high phases and less in some other high phases; output regulation tries to either increase or reduce the charge transfer in all high phases.

[3]Other possible approaches include setting a maximum phase duration: any phase will be forced to terminate once its duration reaches the maximum value.

4.5 Experimental Results

A 4-cell FCML converter was designed to validate the performance of CSS control. Figure 4.11 shows the annotated picture of the PCB with testing structures. The corresponding high-level schematic is also shown in Figure 4.12. Line and load transients are generated with on-board power transistors.

V_{in}: 8 - 12V

C_{in} = 14.1uF

C_{out} = 14.1uF

C_{fly} = 4.7uF

L = 0.47uH

R_o = 50mΩ

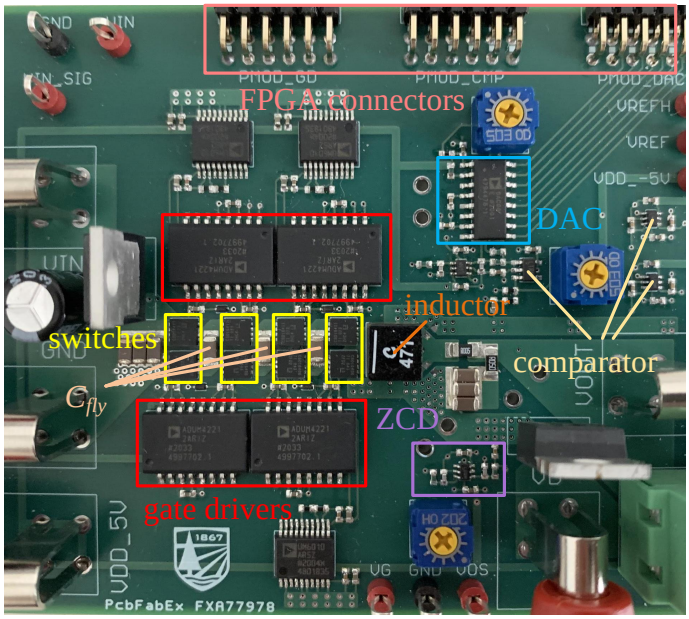


Figure 4.11: The 4-cell FCML converter PCB with test structures.

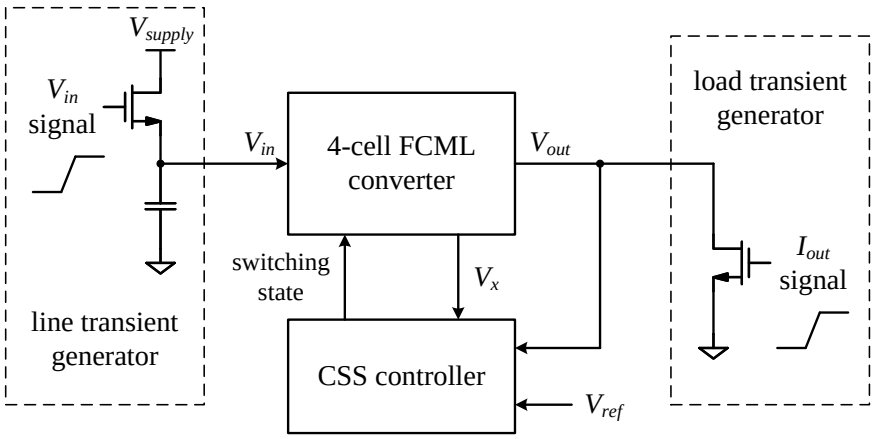


Figure 4.12: Simplified schematic of the testing board.

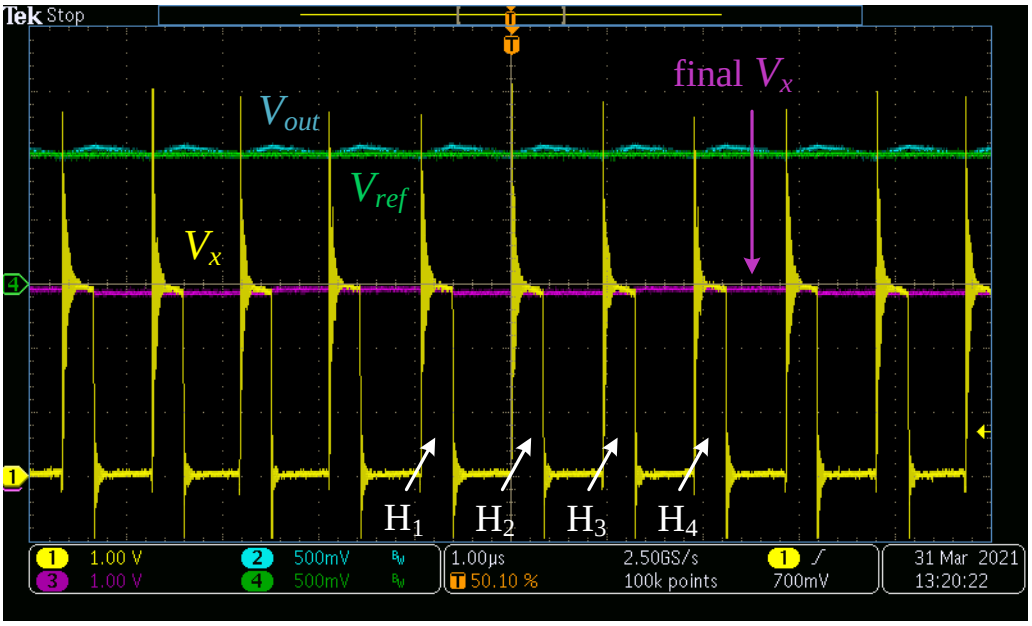


Figure 4.13: Steady state waveform in CCM operation (12V:1V).

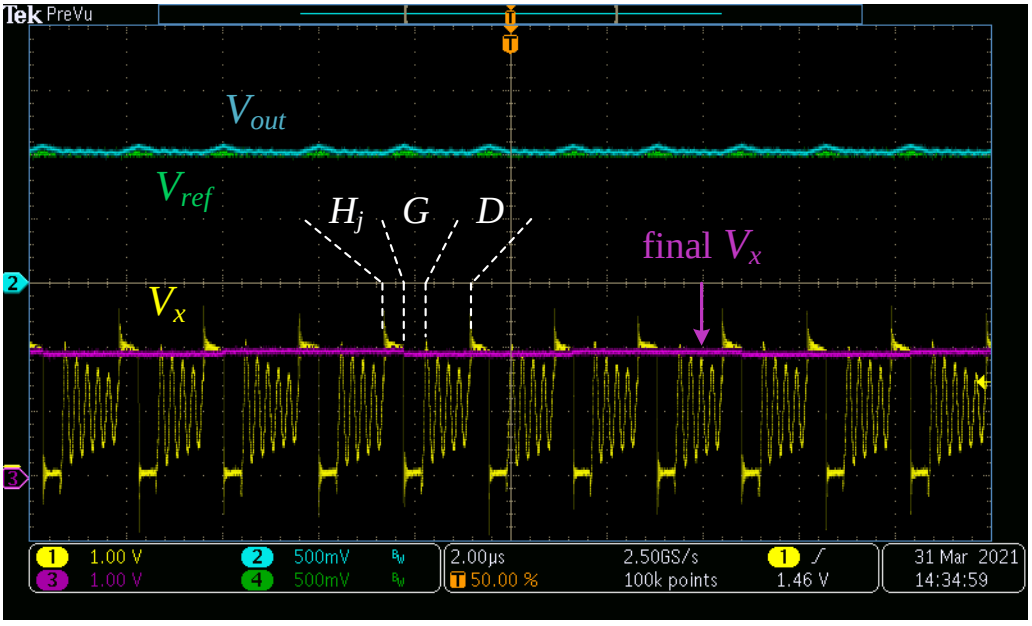


Figure 4.14: Steady state waveform in DCM operation (8V:1V).

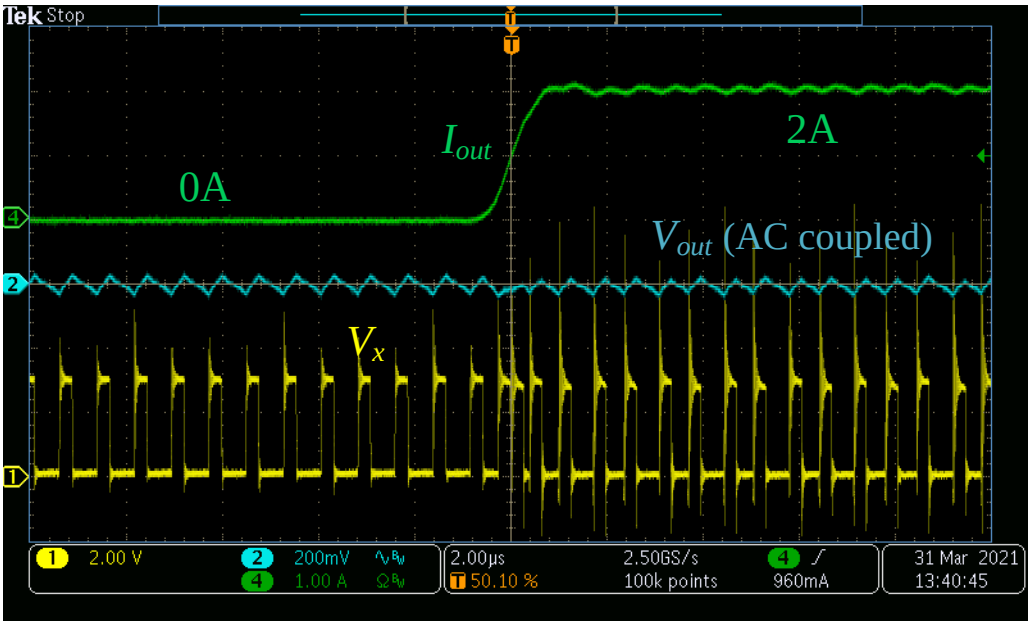


Figure 4.15: Response to load transient (I_{out}: 0→2A).

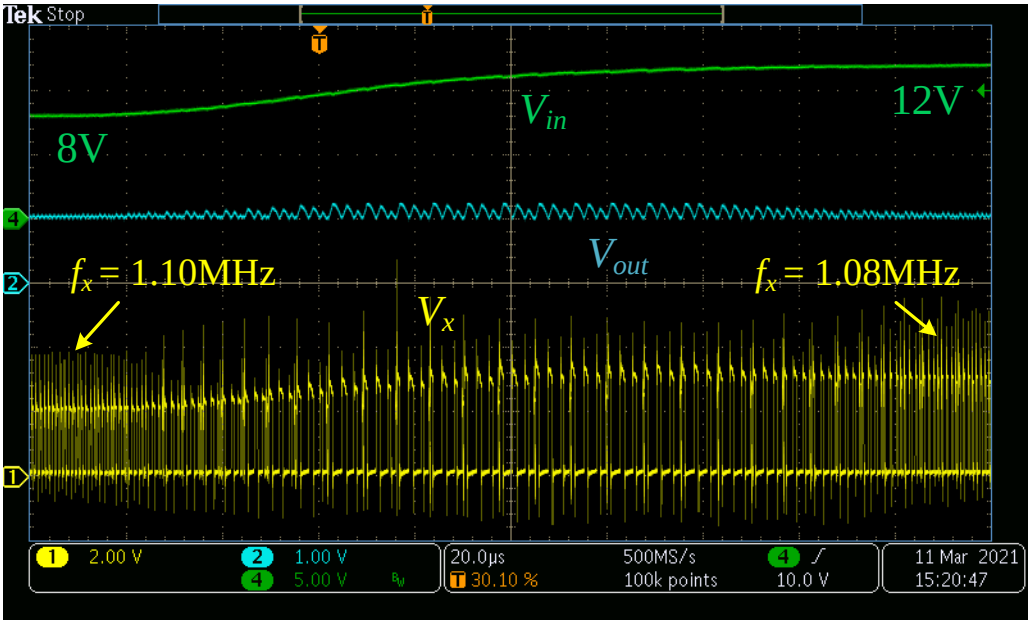


Figure 4.16: Response to line transient (V_{in}: 8V→12V).

Figure 4.13 shows the oscilloscope measured steady state waveform in CCM (including CSF and CSS) operation. The waveform and the control diagram (Figure 4.4) are consistent: the transition from a high phase to the ground phase is triggered by V_x reaching its desired final value given by (4.19); the transition from the ground phase to the next high phase is triggered by V_{out} falling to V_{ref}.

Figure 4.14 shows the measured steady state waveform in DCM operation. The high phases H_j, ground phase G, and DCM phase D can be obviously distinguished from the behavior of switching node voltage. Ideally, in the DCM phase, both current and voltage of the inductor are at zero and the switching node voltage is at V_{out}. However, in practice, the residual current at phase transition ($G \rightarrow D$) may cause the inductor to oscillate with parasitic capacitance of the switching node, which is commonly found in literature [82].

Figure 4.15 shows the converter response to a load transient where I_{out} rises from 0 to 2A within 2μs (1A/μs). During the transient, ground phase G is shortened significantly to quickly ramp up the inductor current, which can be seen from the 3 consecutive pulses of V_x. Balance is maintained by regulating the final value of V_x, while no obvious undershoot of V_{out} is observed.

Figure 4.16 shows the converter response to a line transient, where V_{in} changes from 8V to 12V within 100μs (40V/ms). Balance is maintained during the transient since the pulse height of V_x tracks the trend of V_{in}. However, as explained in the previous section, fast balancing dynamics is achieved at the cost of large V_{out} overshoot, which is limited to 200mV by *CMP3* in this test. Lower tolerance of V_{out} overshoot slows down the active balancing loop. It is also worth noticing that due to dynamic scaling of ΔV, the switching frequency remains roughly the same before and after the transient.

Chapter 5

A Cascaded Hybrid Switched-Capacitor Converter

As advances in CMOS technology push low-voltage digital power supplies down to the sub-volt range, there is growing pressure on DC-DC converters to operate efficiently with ever smaller size and at larger step-down ratios ($V_{in} \gg V_{out}$), while also providing fast transient response [53]. Although hybrid SC converters show favorable performance in this design space, their transient response is limited by the bandwidth of active balancing control, especially during startup. Since flying capacitor voltages should track the trend of input voltage to avoid switch over-stress, the startup speed is restrained by how fast flying capacitors can be charged. Explored methods to accelerate startup of hybrid SC converters include flying capacitor pre-charging [83, 84, 85, 86] and fast balancing control [68], both reporting millisecond-level startup time.

Gate driving of floating switches is also challenging. In integrated designs, bootstrap capacitors often serve as local power supplies for gate drivers to eliminate the need for any external driving supply. However, they occupy a significant amount of die area (on-chip) or require additional discrete components (off-chip), both reducing the power density.

This chapter presents an integrated hybrid SC converter capable of fast self startup for

USB power delivery (5V: 0.4-1.2V). The large step-down ratio is obtained by the cascaded architecture. Fast active balance and output regulation are achieved by the modified ripple injection control (MRIC) [68], with a phase skipping technique further accelerating startup. Gate driving in this design uses synchronous bootstrap operation and shows significantly reduced bootstrap capacitor area compared to traditional bootstrap. Fabricated in 0.18μm CMOS technology, this converter prototype has a peak efficiency of 96.9% for 5V:1.2V conversion and a startup time of 12μs.

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5.1 Cascaded Hybrid SC Architecture

There are a wide range of possible direct-conversion hybrid SC topologies, each derived loosely from a basis set of known switched-capacitor network spanning Dickson, ladder, series-parallel, Fibonacci, and doubler[1]. The hybrid multi-phase doubler has the distinction of achieving largest nominal step-down ratio per flying capacitor, or alternatively, requiring the fewest flying capacitors for a certain nominal step-down ratio [70]. As illustrated in Figure 5.1, the two-stage hybrid doubler achieves 4:1 nominal step-down ratio with only 2 flying capacitors, as compared to 3 for most of other direct hybrid topologies.

From another perspective, the two-stage doubler can be regarded as two 2:1 hybrid SC converters cascaded. But due to synchronous operation of the two stages, the output filter of the first converter is no longer necessary. With this analogy, it is obvious that the balanced flying capacitor voltage and switch voltage stress are $V_{in}/2$ for the first stage and $V_{in}/4$ for the second stage. Another beneficial feature is that the higher voltage rated devices in the first stage switch at half the frequency of the second stage, reducing their switching losses.

[1]Here step-down power conversion is discussed but the term 'doubler' is still used due to convention.

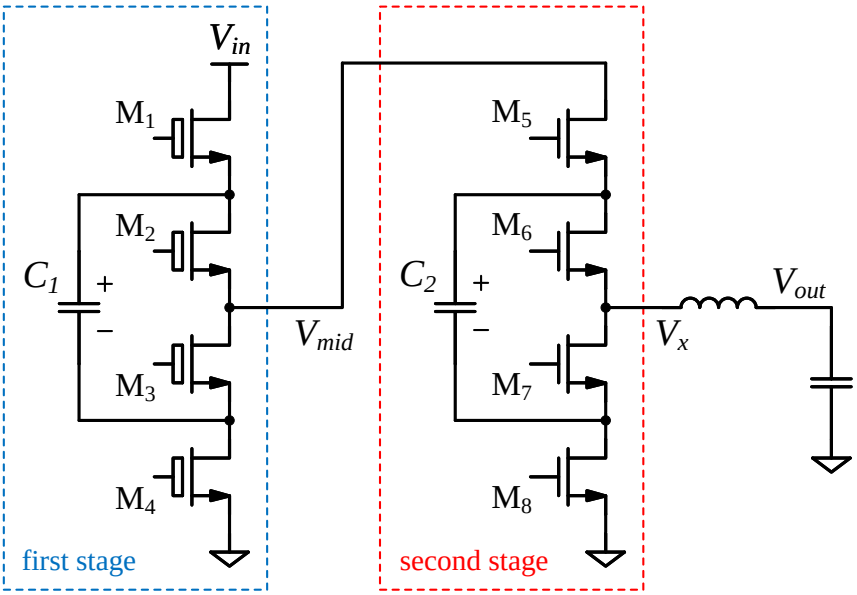

Figure 5.1: Schematic of a two-stage hybrid doubler.

Closer observation shows that switch M_5 can be removed, because the effect of turning it off can be replicated by turning off both M_2 and M_3, decoupling the two power stages. This is similar to the tri-state operation discussed in [53]. Removing M_5 reduces power loss and simplifies the circuit design, but also causes V_{mid} to switch between $V_{in}/4$ and $V_{in}/2$. Due to parasitic capacitance at V_{mid}, including the drain-to-source capacitance of switches and the metal overlap capacitance, the switching behavior induces CV^2 loss. However, in this low frequency application, the power loss caused by such mechanism is insignificant compared to the power saved by removing switch M_5.

Another potential improvement on the two-stage hybrid doubler is interleaving the first stage, as shown in Figure 5.2. In one switching phase, the red switches in Φ_α and the blue switches in Φ_β are turned on, connecting the two flying capacitors, C_α and C_β, in series between V_{in} and ground. In another phase, the black switches are turned on, forming the same equivalent circuit except that the two flying capacitors exchange position.

Interleaving the first stage indeed adds another flying capacitor, which seems to defeat the purpose of adopting the hybrid doubler architecture. However, the required input bypass

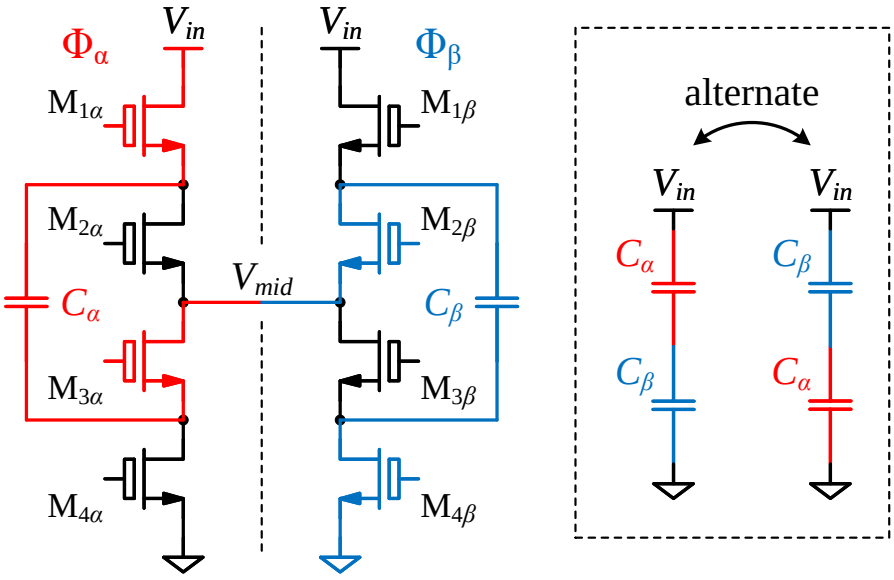

Figure 5.2: Schematic and equivalent circuits of the interleaved first stage.

capacitance can also be reduced, because C_α and C_β already provides a low-impedance path from V_{in} to ground. The main benefit of interleaving is the dramatic acceleration of first stage balancing dynamics, especially during line transients and startup. Given that Φ_α and Φ_β are symmetric, any change of V_{in} will equally distribute between V_{C_α} and V_{C_β} rapidly through charge-sharing. Alternatively speaking, C_α and C_β resemble a capacitor divider such that their voltages automatically track $V_{in}/2$ from AC perspective. It should be noticed that in steady state where V_{in} is constant, charge sharing does not happen and complete soft charging is still achieved by the inductor. In addition, the interleaving also makes design of gate drivers more flexible, as will be discussed later.

Figure 5.3 shows the proposed converter architecture after incorporating the previous improvements. For an input voltage of 4-6V (nominally 5V), the voltage rating of the first stage power switches should be at least 3V, therefore, 5V switches were used due to their availability in the process technology. In the second stage, the minimum switch voltage rating is 1.5V, and 1.8V devices were used.

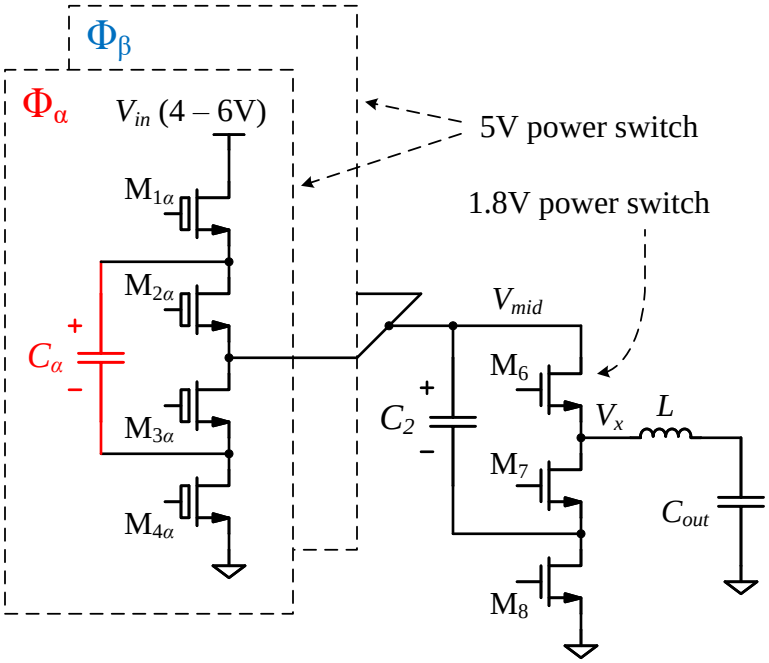

Figure 5.3: The proposed two-stage cascaded hybrid SC architecture.

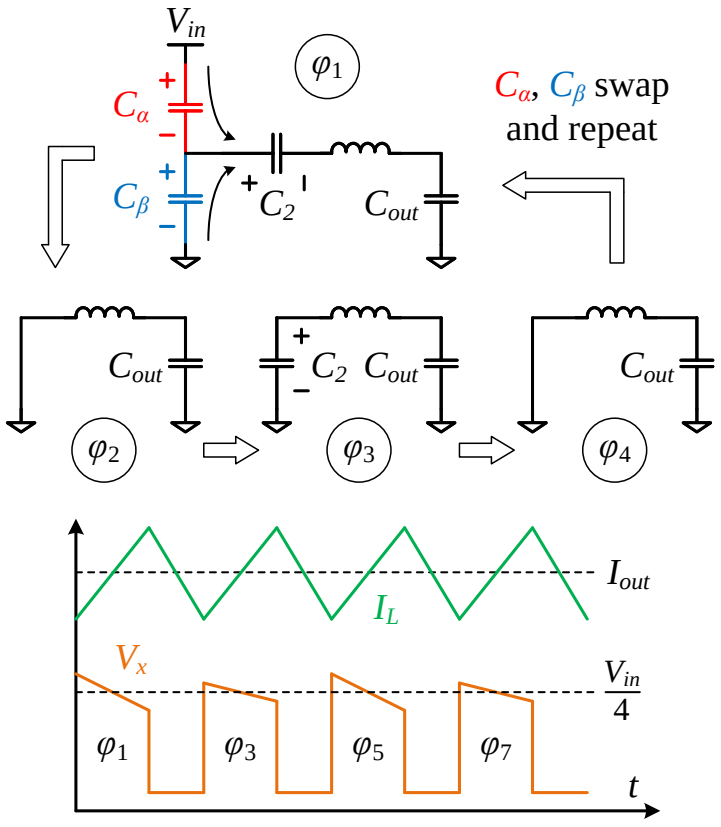

Figure 5.4: Per-phase equivalent circuits and example waveform.

In steady state operation, there are a total of 8 switching phases ($\varphi_1 - \varphi_8$) in a period. The equivalent circuits in each phase and example waveform are shown in Figure 5.4. In phase φ_1, switch $M_{1\alpha}$, $M_{3\alpha}$, $M_{2\beta}$, $M_{4\beta}$ and M_7 are turned on. Flying capacitor C_α and C_β are in series between V_{in} and ground, charging capacitor C_2. The switching node voltage, V_x, is roughly at $V_{in}/4$. In phase φ_2, switch M_7 and M_8 are turned on, connecting the switching node to ground. In phase φ_3, switch M_6 and M_8 are turned on, discharging C_2. The switching node voltage, V_x, equals the voltage on C_2, which is again around $V_{in}/4$. Phase φ_4 is the same as phase φ_2. It is worth noticing that switch $M_{4\alpha}$ and $M_{1\beta}$ are also turned on during $\varphi_2 - \varphi_4$ to avoid completely floating capacitors. The equivalent circuits in phase $\varphi_5 - \varphi_8$ repeat $\varphi_1 - \varphi_4$ except that the first stage flying capacitors, C_α and C_β, swap position. It can be observed that the median node voltage, V_{mid}, is at $V_{in}/2$ during phase φ_1 and φ_5, and at $V_{in}/4$ during $\varphi_2 - \varphi_4$ and $\varphi_6 - \varphi_8$. This is the effect of removing switch M_5 in the hybrid doubler topology, as discussed earlier.

In steady state operation, the output voltage is given by

$$V_{out} = \frac{D_{eff} V_{in}}{4}, \tag{5.1}$$

where D_{eff} represents the effective duty cycle at the switching node. It can be seen that the converter has an output voltage between 0 and $V_{in}/4$.

In this design, power switch sizes are optimized according to the trade-off between the switching loss and the conduction loss. Simulation of a typical operating point (5V:0.9V, 0.25A load current) shows a gate driving loss of 4.7mW and a conduction loss (including switches and the inductor) of 5.2mW. Other mechanisms (switch overlap loss, C_{oss} loss, body diode loss, etc.) contributes an additional 5.0mW loss, and the simulated efficiency under this typical operation is 93.8%.

5.2 Regulation and Active Balance

Hysteretic control (a form of sliding mode control) is widely used in buck converters for its fast transient response, robustness, and simple implementation [87, 88, 89]. If balance is maintained, hybrid SC converters in inductive operation is similar to buck converters, as seen in the example waveform of Figure 5.4. This observation motivates using hysteretic control to achieve fast transient response in hybrid SC converters. First proposed in [68], modified ripple injection control (MRIC) is a hysteretic-based algorithm that achieves both output voltage regulation and active balance for direct hybrid SC converters. This section first reviews the general principle of MRIC and then introduces the newly added phase skipping technique to further accelerate the startup.

5.2.1 Modified Ripple Injection Control

For buck converters, a typical current-mode hysteretic controller generates a feedback signal, V_{fb}, that consists of the output voltage and the inductor current ripple [90]:

$$V_{fb} = V_{out} + k_i \cdot I_{L,AC}, \tag{5.2}$$

where k_i is the current to voltage gain. The feedback signal is then compared to a reference voltage, V_{ref}, such that it is kept inside a hysteresis band around the reference, thus achieving output voltage regulation.

An alternative approach is adding hysteresis to V_{fb}:

$$V_{fb,hst} = \begin{cases} V_{fb} - \Delta V & \text{if } V_{fb} \text{ is rising,} \\ V_{fb} + \Delta V & \text{if } V_{fb} \text{ is falling,} \end{cases} \tag{5.3}$$

where $V_{fb,hst}$ is the feedback signal with added hysteresis; ΔV represents half of the hysteresis window. When comparing $V_{fb,hst}$ and V_{ref}, a fast comparator without hysteresis can

be used instead.

These two equivalent methods are shown in Figure 5.5. In an ideal case, the controller reacts instantaneously to any state deviation, achieving fast transient response. However, in practice, sensing the inductor current ripple, $I_{L,AC}$, requires either a series resistance of the output capacitor or a passive network that involves trade-offs between die area, power consumption, and bandwidth. To overcome this challenge, it was explored in [90] that an emulated $I_{L,AC}$ (a signal that is generated to resemble $I_{L,AC}$ but not necessarily from direct sensing) also works. In this design, voltage-current characteristic of the inductor is used to emulate $I_{L,AC}$, as depicted in Figure 5.6.

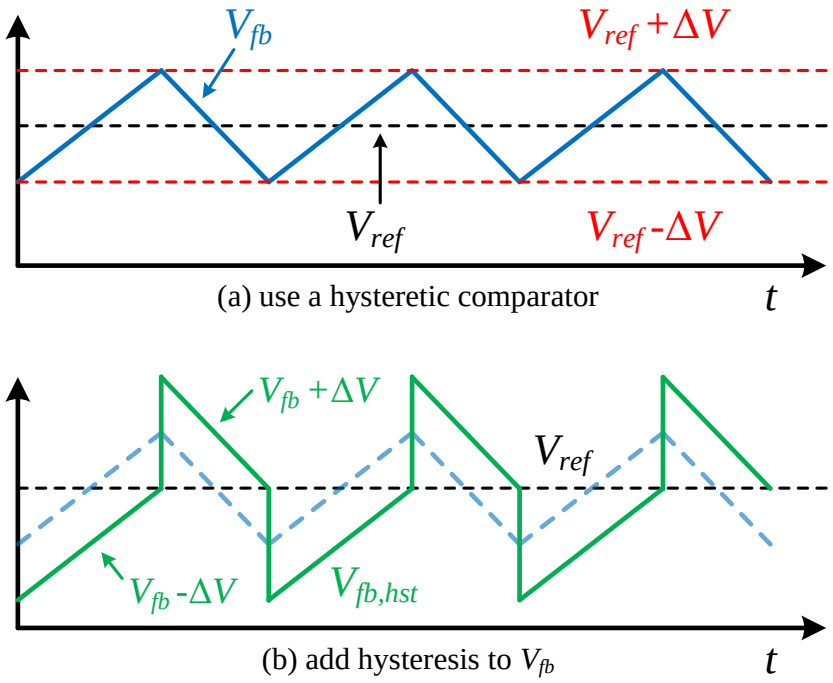

Figure 5.5: Two equivalent approaches of current-mode hysteretic control.

Here the classification in Chapter 4 is carried over: phases where the switching node is connected to one or more flying capacitors ($\varphi_1, \varphi_3, \varphi_5, \varphi_7$) are called high phases, H_j ($j = 1, 2, 3, 4$); phases where the switching node is connected to ground ($\varphi_2, \varphi_4, \varphi_6, \varphi_8$) are denoted as the ground phase, G. In balanced steady state, the switching node voltage,

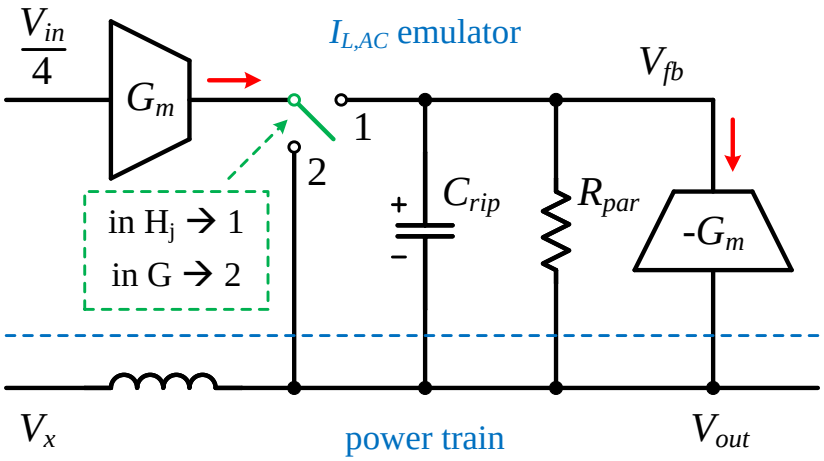

Figure 5.6: Emulating the inductor current ripple, $I_{L,AC}$.

V_x, is roughly at $V_{in}/4$ in high phases, and is at zero in the ground phase. Therefore, the slope of the actual inductor current ripple can be written as:

$$\frac{dI_{L,AC}}{dt} = \begin{cases} \frac{1}{L}(\frac{V_{in}}{4} - V_{out}) & \text{in } H_j, \\ -\frac{V_{out}}{L} & \text{in } G. \end{cases} \tag{5.4}$$

The emulator in Figure 5.6 generates the same slope by using two voltage-to-current converters with a gain of G_m to inject modulated current into the ripple capacitor, C_{rip}. The parallel resistor, R_{par}, is sized such that its current is much smaller than the two active branches, but it removes the DC voltage on C_{rip} in steady state. In high phases, C_{rip} is charged by current $G_m V_{in}/4$ and discharged by current $G_m V_{out}$; in the ground phase, C_{rip} is only discharged by current $G_m V_{out}$. The capacitor current can be written in terms of the derivative of its voltage:

$$\frac{dV_{C_{rip}}}{dt} = \begin{cases} \frac{G_m}{C_{rip}}(\frac{V_{in}}{4} - V_{out}) & \text{in } H_j, \\ -\frac{G_m V_{out}}{C_{rip}} & \text{in } G. \end{cases} \tag{5.5}$$

Due to the parallel resistor, $V_{C_{rip}}$ and $I_{L,AC}$ also have the same DC level, which is zero. Comparing (5.4) and (5.5) yields

$$V_{C_{rip}} = \frac{G_m L}{C_{rip}} \cdot I_{L,AC}, \tag{5.6}$$

showing that $V_{C_{rip}}$ can approximate the term $k_i \cdot I_{L,AC}$ in (5.2). With the emulation method, the feedback signal can be generated to achieve output voltage regulation without directly sensing the inductor current.

However, the previous analysis is built on the assumption that the flying capacitors are balanced. To actually achieve balance, an additional sliding mode is required. In the MRIC algorithm, another reference voltage, $V_{ref,bal}$, is generated to compare against the feedback signal with hysteresis, $V_{fb,hst}$, as illustrated in Figure 5.7.

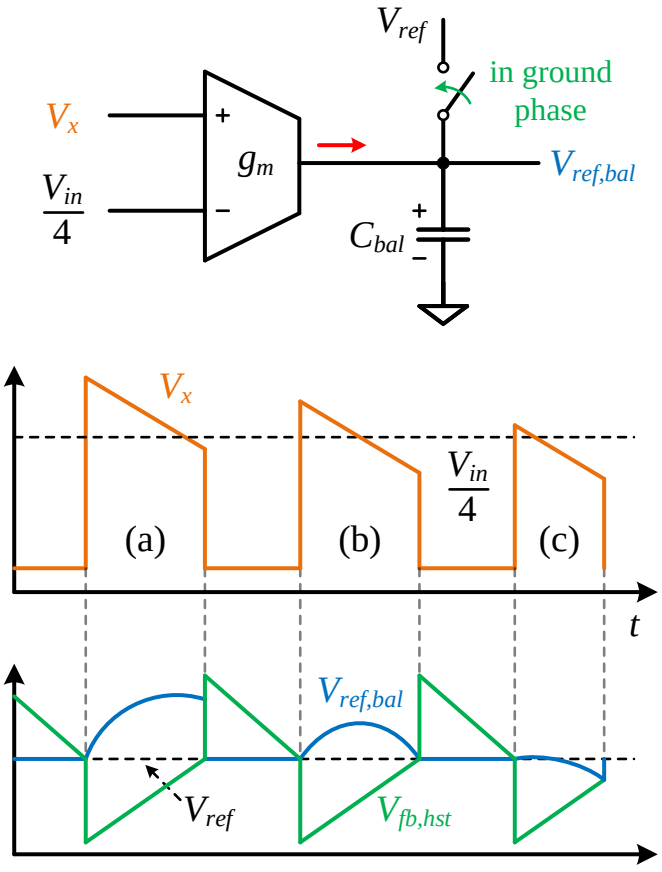

Figure 5.7: Generating the reference voltage with balancing information, $V_{ref,bal}$.

During high phases, an operational transconductance amplifier (OTA) with a gain of g_m charges the capacitor C_{bal} with its output current. In the ground phase, the reset switch turns on and the capacitor voltage returns to V_{ref}. Using the voltage-current relationship of the capacitor, it can be derived that

$$V_{ref,bal}(t) = \begin{cases} \frac{g_m}{C_{bal}} \cdot \int_0^t (V_x - \frac{V_{in}}{4})\, dt + V_{ref} & \text{in } H_j, \\ V_{ref} & \text{in } G, \end{cases} \tag{5.7}$$

where t is the time index with respect to the beginning of a corresponding high phase. The mathematical expression may seem abstract, but it represents the average V_x level in H_j, thus contains information of flying capacitor voltage balance.

In the example waveform of Figure 5.7, there are 3 possible cases for a high phase. In case (a), the average V_x is higher than $V_{in}/4$: the integral in (5.7) is larger than zero, thus $V_{ref,bal}$ is higher than V_{ref} at the end of the phase before reset. In case (b), the average V_x equals $V_{in}/4$: the integral first rises then falls back to zero, thus $V_{ref,bal}$ returns to V_{ref} at the end of the phase. For these two cases, the balancing sliding mode does not take action and the high phase is terminated when V_{ref} intersects with $V_{fb,hst}$. In case (c), the average V_x is lower than $V_{in}/4$: the integral is smaller than zero, thus $V_{ref,bal}$ drops to intersect with $V_{fb,hst}$ earlier than the other two cases. Here at the intersection, the balancing sliding mode terminates the high phase.

The overall effect of such control action is that the duration of a high phase is reduced if the average V_x is lower than $V_{in}/4$. The lower V_x can result from a flying capacitor at low voltage being discharged, or a flying capacitor at high voltage being charged. In either case, this charge transfer is undesired and reducing the phase duration applies a negative feedback on the flying capacitor voltage deviation, leading it back to balance. The stability is proved in Appendix B. From another perspective, this balancing sliding mode aims to regulate average V_x during high phases to $V_{in}/4$, which forces flying capacitors to balance

according to the analysis in Chapter 4.

The balancing sliding mode combined with the previous ripple injection sliding mode, in Figure 5.5(b), forms the MRIC algorithm which achieves both output voltage regulation and flying capacitor voltage balance for direct hybrid SC converters.

5.2.2 Startup Detection and Phase Skipping

For USB power delivery, it is important for the converter to withstand fast line transients, which can result from hard-connecting a USB power cable. This is especially challenging for hybrid SC converters, as the flying capacitor voltages should be kept proportional to the input voltage to avoid switch overstress. Although soft startup methods can be used to slowly ramp up V_{in} [86, 91], it increases the physical size and significantly delays the startup response. It is desired to achieve fast regulation of flying capacitor voltages, so that the converter can safely startup in the worst case scenario.

In the proposed topology, balancing dynamics of the first stage flying capacitors, C_α and C_β, are fast due to the interleaving. However, balancing dynamics of the second stage flying capacitor, C_2, is relatively slow, because its charging and discharging current links the inductor even in transients. During converter startup, the MRIC algorithm shortens the discharging phase of C_2 to raise its voltage, but its voltage can rise faster if the discharging phases are completely eliminated, motivating the phase skipping technique. Among the 8 switching phases, C_2 is discharged in φ_3 and φ_7, thus they are temporarily skipped during startup, accelerating the balancing dynamics. It should be observed that when φ_3 and φ_7 are skipped, φ_2 and φ_4, φ_6 and φ_8 are also merged, respectively, leaving only 4 switching phases during startup: φ_1, φ_2, φ_5, and φ_6.

Startup is detected by comparing the switching node voltage, V_x, with a high threshold, $V_{x,max}$, in phase φ_1 and φ_5, as shown in Figure 5.8. Due to symmetry of the first stage and the nature of interleaving, voltage on C_α and C_β are roughly $V_{in}/2$ even during transients.

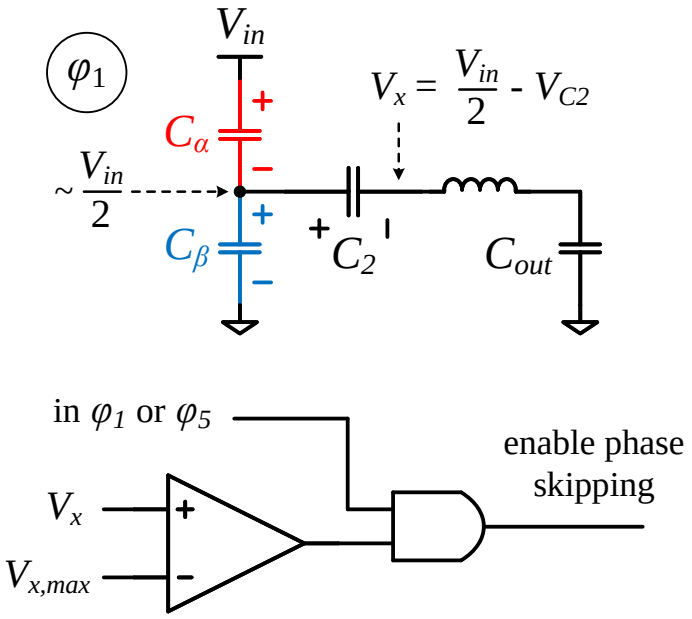

Figure 5.8: Detecting the startup to enable phase skipping.

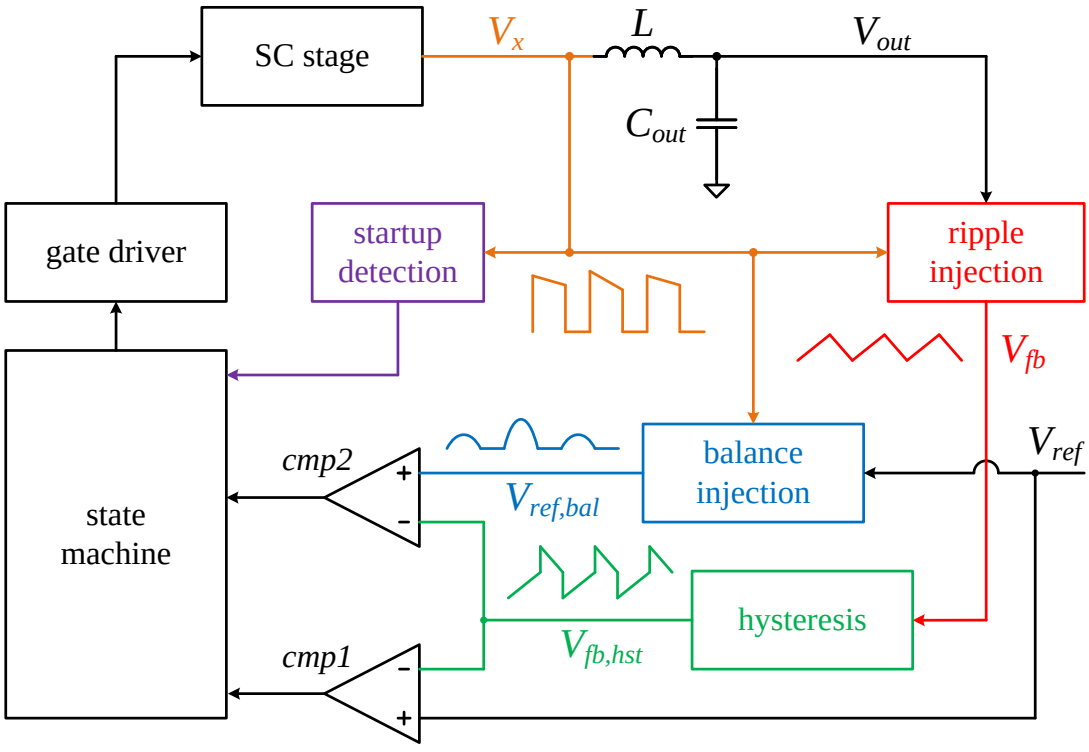

Figure 5.9: Top-level control diagram of MRIC with phase skipping.

Therefore, in phase φ_1 and φ_5, the switching node voltage is given by

$$V_x = \frac{V_{in}}{2} - V_{C_2}. \tag{5.8}$$

The high threshold, $V_{x,max}$, is designed to be properly higher than $V_{in}/4$ so that V_x never reaches $V_{x,max}$ in balanced steady state. But if V_{C_2} is significantly lower than its balanced value ($V_{in}/4$) during transients or startup, V_x will exceed $V_{x,max}$ in φ_1 and φ_5, triggering phase skipping and the converter enters startup mode. If startup is no longer detected, the converter automatically enters regular mode in the next period.

After including startup detection and phase skipping technique, the top-level control diagram is illustrated in Figure 5.9. The switching node voltage indicates whether the converter is in high phases or the ground phase, which is used to emulate and inject $I_{L,AC}$ to V_{out}. The resulting feedback signal, V_{fb}, is added hysteresis to form $V_{fb,hst}$, which is then compared to the reference voltage, V_{ref}, by *cmp1* to maintain output voltage regulation. In balancing sliding mode, V_{ref} is injected with balancing information contained in V_x to generate $V_{ref,bal}$. A second comparator, *cmp2*, compares $V_{fb,hst}$ with $V_{ref,bal}$, and its output triggers the termination of high phases that has a low V_x, forcing the flying capacitors to balance. The switching node voltage, V_x, is also used to detect startup or extreme line transients. Under these scenarios, the state machine is modified to skip φ_3 and φ_7 to accelerate balancing dynamics of C_2.

To appreciate the effectiveness of the balancing sliding mode, simulation is conducted to compare closed-loop operation against open-loop operation, where the voltage on flying capacitor C_2 is weakly regulated by natural balance, as illustrated in Figure 5.10. For the simulation setup, the converter is initially in balanced steady state. At $t = 50\mu s$, a forced deviation (-0.5V) is applied to mimic disturbances (such as line and load transient, false switching, etc.). In open-loop operation, it takes 3.5ms for V_{C2} to return to balance; in closed-loop operation, V_{C2} recovers within $25\mu s$, which is over 100 times faster.

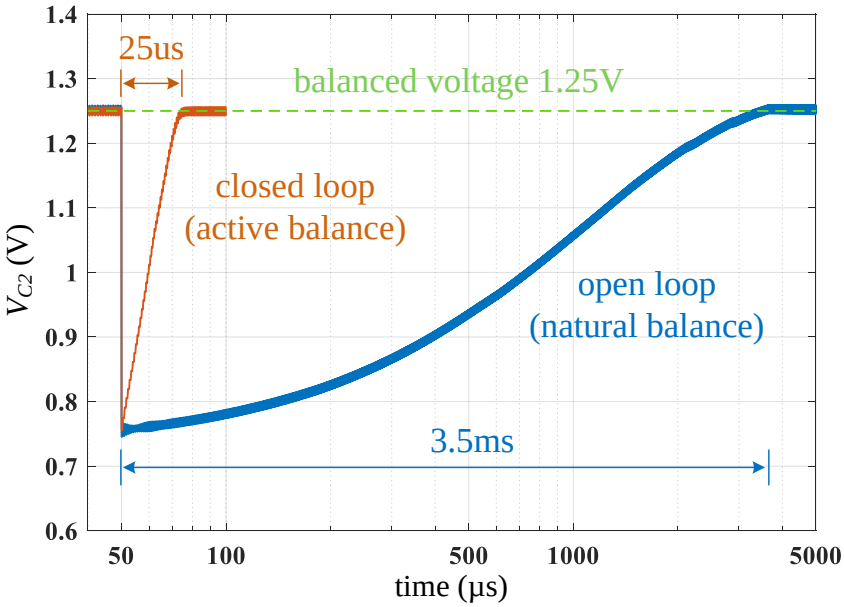

Figure 5.10: Simulated balancing dynamics in open-loop and closed-loop operation.

5.3 Gate Driving and Circuit Implementation

In this design, all gate driving circuits including bootstrap capacitors are fully integrated, eliminating the need for external driving supplies. Additionally, several design techniques significantly reduce bootstrap capacitor area. This section introduces the fully integrated gate driving strategy and then describes the implementation of key circuit blocks.

5.3.1 Fully Integrated Gate Driving

The first stage of the converter uses 5V power switches with a nominal threshold voltage (V_{th}) of 0.78V. Considering the trade-off between conduction loss and switching loss, a 2.4V driving voltage has the best overall efficiency in simulation. In the prototype, they are driven at $V_{in}/2$ (2.5V) since the rail is easy to generate and close to optimum. The gate driving schematic of $M_{1\alpha}$, $M_{1\beta}$, $M_{4\alpha}$, and $M_{4\beta}$ is shown in Figure 5.11. Switch $M_{1\alpha}$ and $M_{1\beta}$ are bootstrapped from V_{in} during their off state. When signal A goes high, bootstrap capacitor $C_{BS,1\alpha}$ supplies charge to turn on $M_{1\alpha}$ while $C_{BS,1\beta}$ is charged to $V_{in}/2$ through

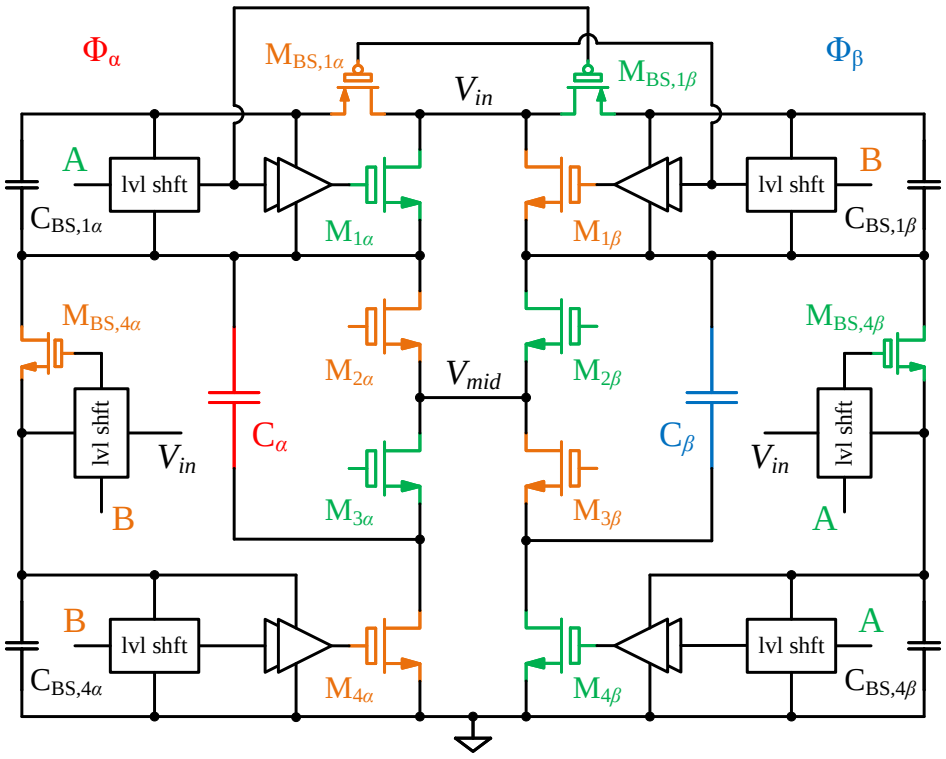

Figure 5.11: The gate driving schematic of $M_{1\alpha}$, $M_{1\beta}$, $M_{4\alpha}$, and $M_{4\beta}$.

$M_{BS,1\beta}$. When signal B goes high, $C_{BS,1\beta}$ supplies charge to turn on $M_{1\beta}$ while $C_{BS,1\alpha}$ is charged back to $V_{in}/2$ through $M_{BS,1\alpha}$.

Different from the case of $M_{1\alpha}$ and $M_{1\beta}$, the bootstrap capacitor of $M_{4\alpha}$ and $M_{4\beta}$ are charged when the corresponding power switch turns on, hereby referred to as synchronous bootstrap. For example, when signal A goes high, $C_{BS,4\beta}$ supplies charge to turn on $M_{4\beta}$, connecting the bottom plate of C_β to ground. Almost immediately after, C_β charges $C_{BS,4\beta}$ back to $V_{in}/2$ through $M_{BS,4\beta}$. Note that a N-channel transistor is used for the bootstrap switch, reducing the on resistance and accelerating the charge recovery of $C_{BS,4\beta}$. The symmetric circuitry in Φ_α operates similarly but 180° out of phase.

In the case of synchronous bootstrap, the bootstrap capacitor only needs to supply a small amount of initial charge to turn on the power switch before being charged back to its nominal voltage, as opposed to traditional bootstrap where the bootstrap capacitor drives the power switch through charge sharing. Therefore, given that the charge recovery pro-

cess is fast, synchronous bootstrap reduces the required bootstrap capacitance without the penalty of lower driving voltage. In this prototype, traditional bootstrap capacitors ($C_{BS,1\alpha}$, $C_{BS,1\beta}$) are 650pF each, implemented with metal-insulator-metal (MIM) capacitors. The synchronous bootstrap capacitors ($C_{BS,4\alpha}$, $C_{BS,4\beta}$) are 310pF (52% smaller) each. Since their bottom plates are always grounded, they are implemented with stacked metal-oxide-semiconductor (MOS) and MIM capacitors for higher density.

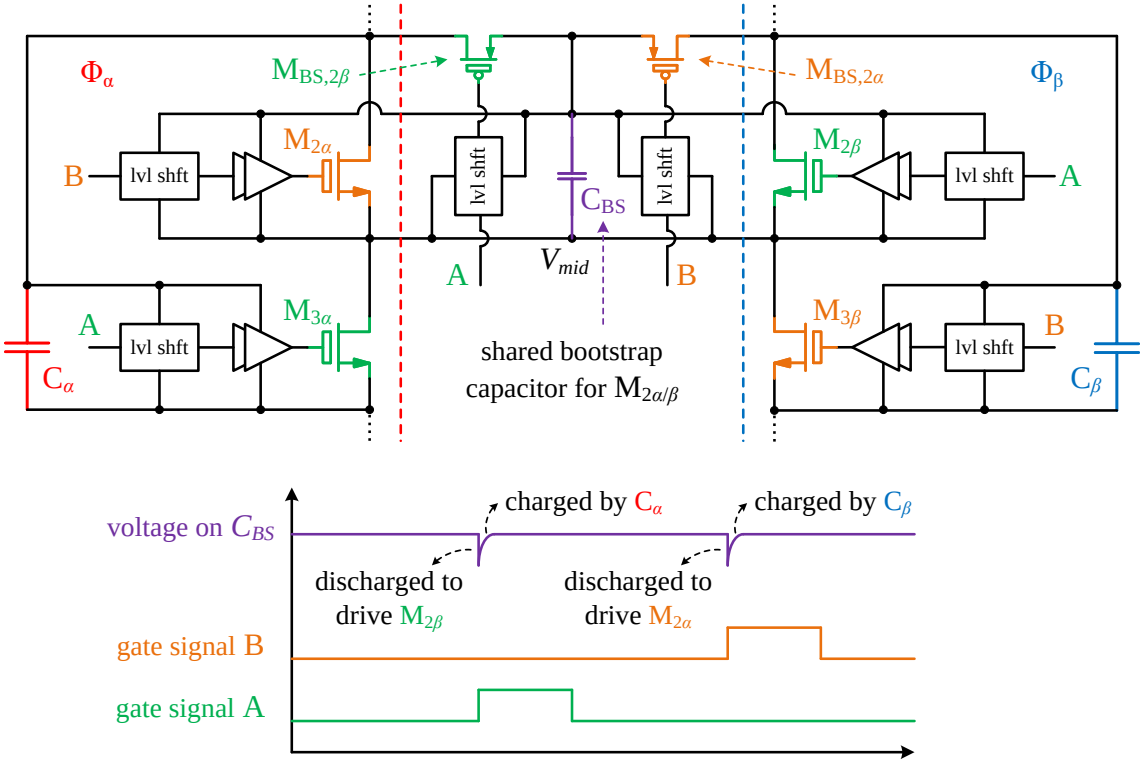

Figure 5.12: Gate driving of $M_{2\alpha}$, $M_{2\beta}$, $M_{3\alpha}$, and $M_{3\beta}$ with example waveform.

Figure 5.12 demonstrates the gate driving strategy for $M_{2\alpha}$, $M_{2\beta}$, $M_{3\alpha}$, and $M_{3\beta}$ with exemplary waveform of gate signals and bootstrap capacitor voltage. For switch $M_{3\alpha}$ and $M_{3\beta}$, their source terminal is connected to the bottom plate of flying capacitor C_α and C_β, respectively. Therefore, the gate drivers are directly supplied by the corresponding flying capacitor. Switch $M_{2\alpha}$ and $M_{2\beta}$ are synchronously bootstrapped. They have a common source node (V_{mid}) and are never turned on at the same time, which allows the use of a shared bootstrap capacitor. Shown in the example waveform, when signal A goes high,

C_{BS} supplies the initial charge to turn on $M_{2\beta}$ before being charged back to $V_{in}/2$ by C_{α} through $M_{BS,2\beta}$; when signal B goes high, C_{BS} supplies charge to turn on $M_{2\alpha}$ and is charged back to $V_{in}/2$ by C_{β}. In this design, C_{BS} is implemented with MIM capacitor and has a value of $260pF$, which is about the same capacitance as $C_{BS,4\alpha}$ and $C_{BS,4\beta}$, but it supplies the gate drivers for both $M_{2\alpha}$ and $M_{2\beta}$.

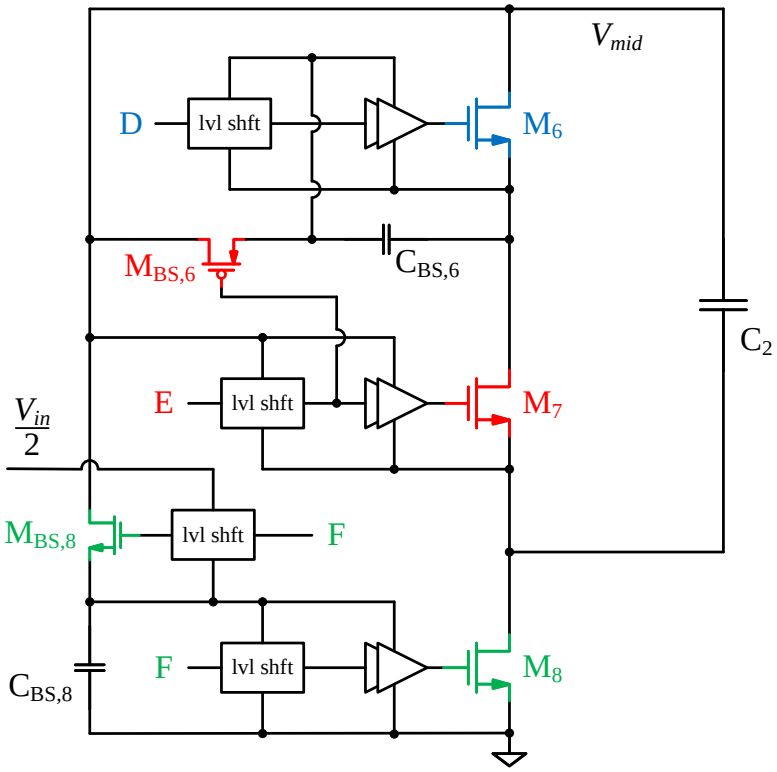

Figure 5.13: The gate driving schematic of M_6, M_7, and M_8.

The second stage of the converter uses 1.8V power switches with a nominal V_{th} of 0.33V. They are driven at $V_{in}/4$ (1.25V). Figure 5.13 shows the gate driving schematic of M_6, M_7, and M_8. Switch M_7 have its source terminal connected to the bottom plate of flying capacitor C_2, thus its driver can be directly supplied. When M_7 turns on, C_2 also charges the bootstrap capacitor $C_{BS,6}$, which supplies the gate driver of switch M_6. Switch M_8 is synchronously bootstrapped from C_2, and the $V_{in}/2$ voltage rail required to turn on the bootstrap switch ($M_{BS,8}$) is provided by $C_{BS,4\beta}$ in the first stage.

5.3.2 Implementation of Key Circuit Blocks

Circuit implementation of the hysteresis injection block, which adds hysteresis to V_{fb} and generates $V_{fb,hst}$, is shown in Figure 5.14. The bias current, I_{bias}, is mirrored to a resistor branch to create the desired half hysteresis window, ΔV. When the converter is in high phases, V_{fb} is rising and the bottom transmission gate turns on, pulling down V_{fb} by ΔV; when the converter is in the ground phase, V_{fb} is falling and the top transmission gate turns on, pushing up V_{fb} by ΔV.

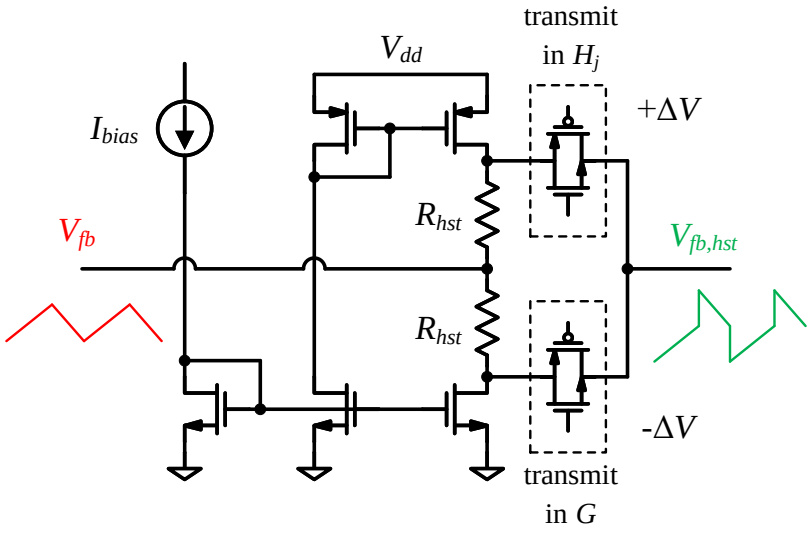

Figure 5.14: Circuit implementation of the hysteresis injection block.

The schematic of the voltage-to-current converter in the $I_{L,AC}$ emulator (Figure 5.6) is illustrated in Figure 5.15. As an example, to convert V_{out} to a proportional current, it is first divided down to provide more headroom for biasing circuits. The resulting $V_{out}/2$ is then buffered by two identically biased transistors, m_1 and m_2, and applied to resistor R_i. After another mirroring, the proportional current can be generated and the transconductance of the voltage-to-current converter is given by:

$$G_m = \frac{1}{2R_i}. \tag{5.9}$$

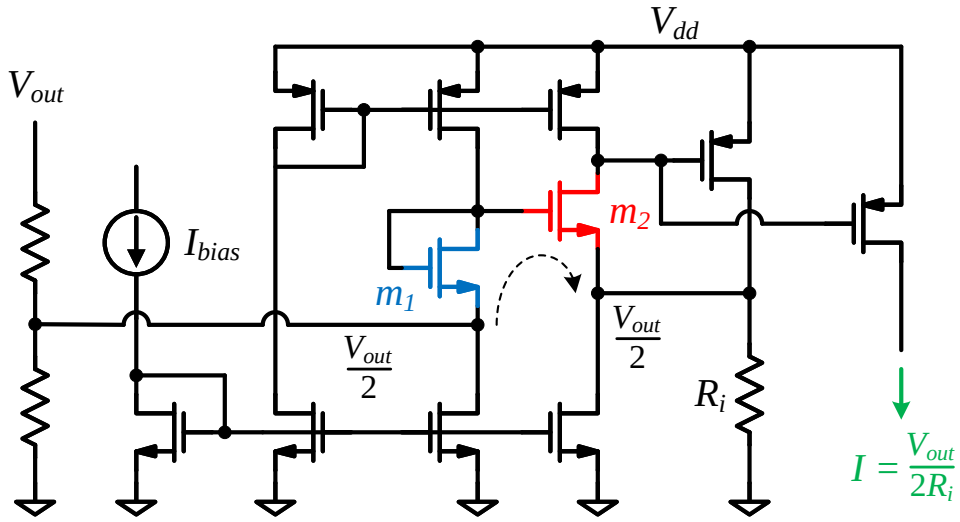

Figure 5.15: Schematic of the voltage-to-current converter.

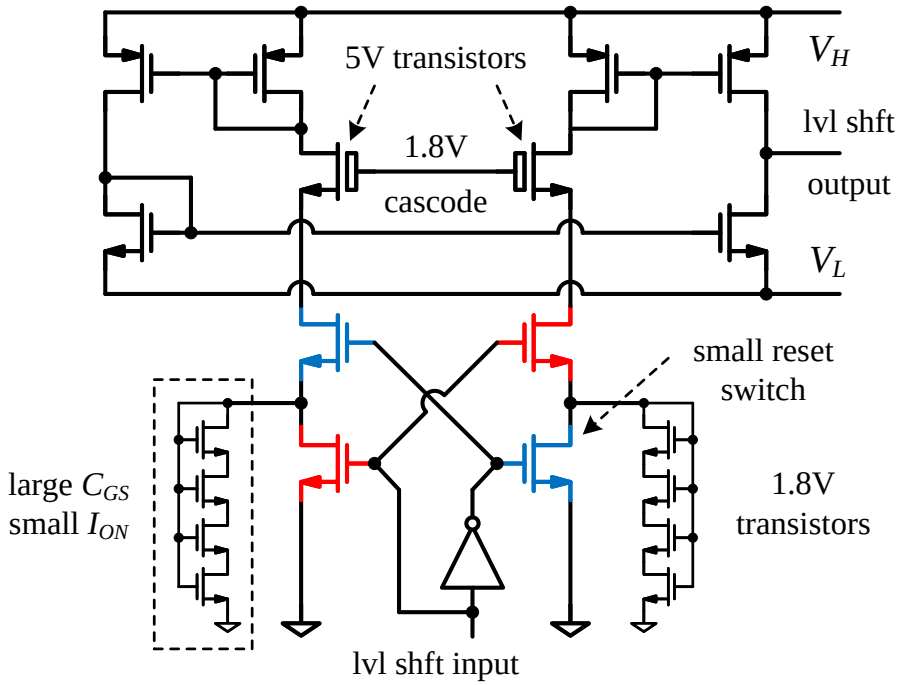

Figure 5.16: Schematic of the level shifter in the second stage.

Figure 5.16 presents the level shifter circuit of gate drivers in the second stage. This design uses transistors with isolated wells to avoid impacts of the body effect. When the level shifter input is high (red switches turn on), a current pulse is generated on the right branch to charge the large C_{GS} of a long-channel diode-connected stack, which afterwards provides a small hold-state current. The current pulse is amplified and rectified in the linear OTA, which pulls the level shifter output to V_H. Meanwhile, C_{GS} of the diode-connected stack on the left branch is discharged by the reset switch. When the level shifter input goes low (blue switches turn on), the current pulse on the left branch is amplified by the OTA and the level shifter output is pulled down to V_L, while the reset switch on the right branch discharges the diode-connected stack. The level shifter in the first stage gate drivers uses a similar cascode-OTA structure; the only difference is that all transistors between the V_L and V_H rails are 5V devices.

5.4 Experimental Results

The converter prototype was fabricated in a 0.18μm bulk CMOS process, with a total die area of 7.82mm^2. Figure 5.17 shows the annotated micrograph of the chip and die-attached capacitors, along with the off-package inductor. Capacitor C_{in}, C_α, and C_β have a nominal value of 4.7μF; capacitance of C_2 is 10μF. Another 10nF on-die capacitor is used to filter V_{out} in the control feedback path. The inductor has a nominal value of 240nH with a DC resistance of 13mΩ.

Figure 5.18 shows the measured efficiency versus load current for multiple conversion ratios. The overall peak efficiency of 96.9% is achieved at 0.15A output with a 5V:1.2V step down. At 5V input, the highest achievable V_{out} is 1.25V ($V_{in}/4$) at empty load. For 5V:1.2V conversion, regulation is lost when the load current exceeds 0.4A, thus higher load current is not recorded in this configuration. The converter maintains up to 85.5% peak efficiency for 5V:0.4V conversion.

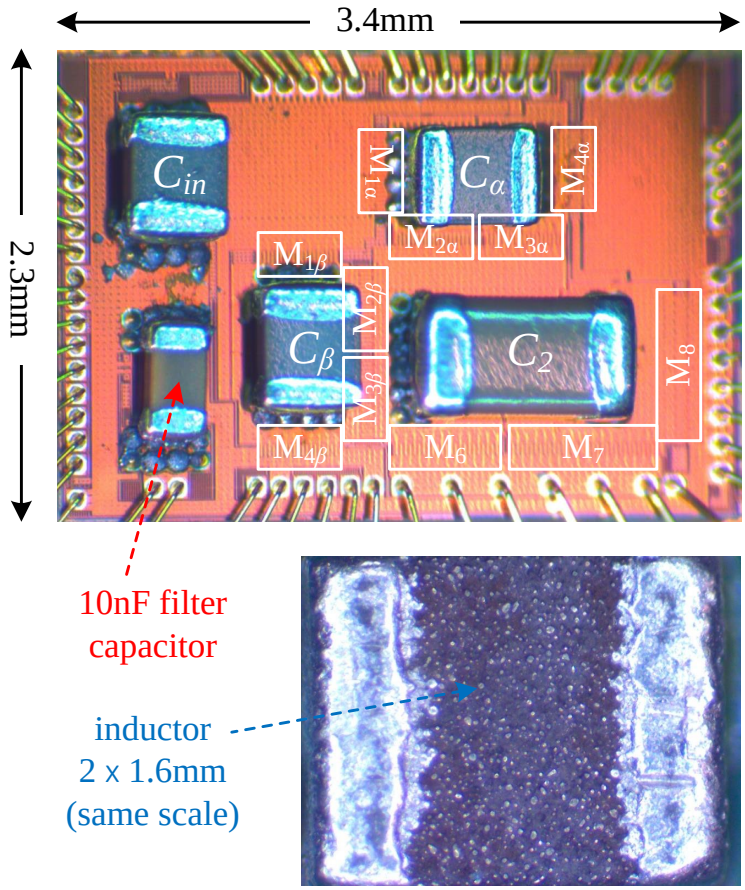

Figure 5.17: Micrpgraph of the chip, die-attached capacitors and off-package inductor.

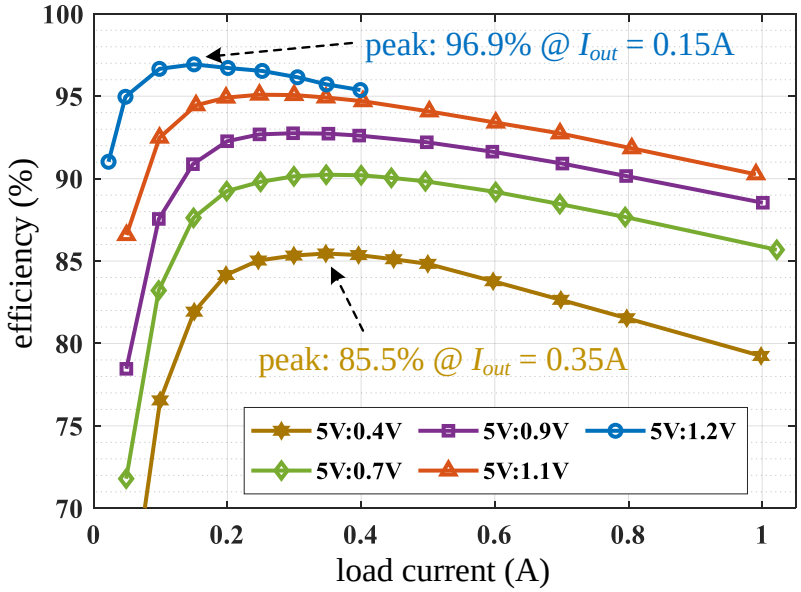

Figure 5.18: Measured efficiency versus load current at $V_{in} = 5$V.

Figure 5.19 shows the measured steady state error (SSE) of output voltage regulation. At 5V input, V_{out} tracks V_{ref} with less than 1.1% SSE for the entire output range of 0.4-1.2V. The fact that SSE is higher at low V_{ref} is caused by the smaller denominator in the calculation, rather than a larger absolute error.

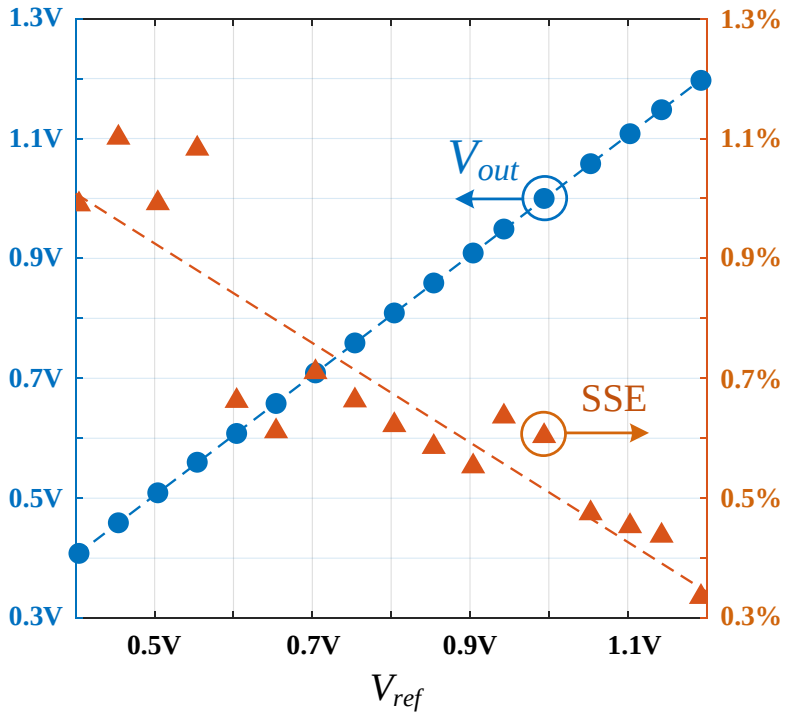

Figure 5.19: Measured V_{out} and its SSE versus the reference voltage.

Full-range (maximum I_{out} step size) load transient is usually challenging for voltage regulators, due to the excessive V_{out} deviation it induces. Figure 5.20 shows the replotted oscilloscope measurement of the full-range load transient response. The rise and fall time are less than $1\mu s$ and the undershoot and overshoot are 32mV and 36mV, respectively. It can be observed from the V_x waveform that flying capacitor balance is maintained, even at empty load ($I_{out} = 0$).

Figure 5.21 shows the measured line transient response, where V_{in} rises from 4V to 5.2V within 4 μs. The output voltage variation ($V_{out} - V_{ref}$) is less than 10mV. Settling time of the flying capacitor voltage is in the order of $10\mu s$, verifying that the active balance is as effective as simulated in Figure 5.10.

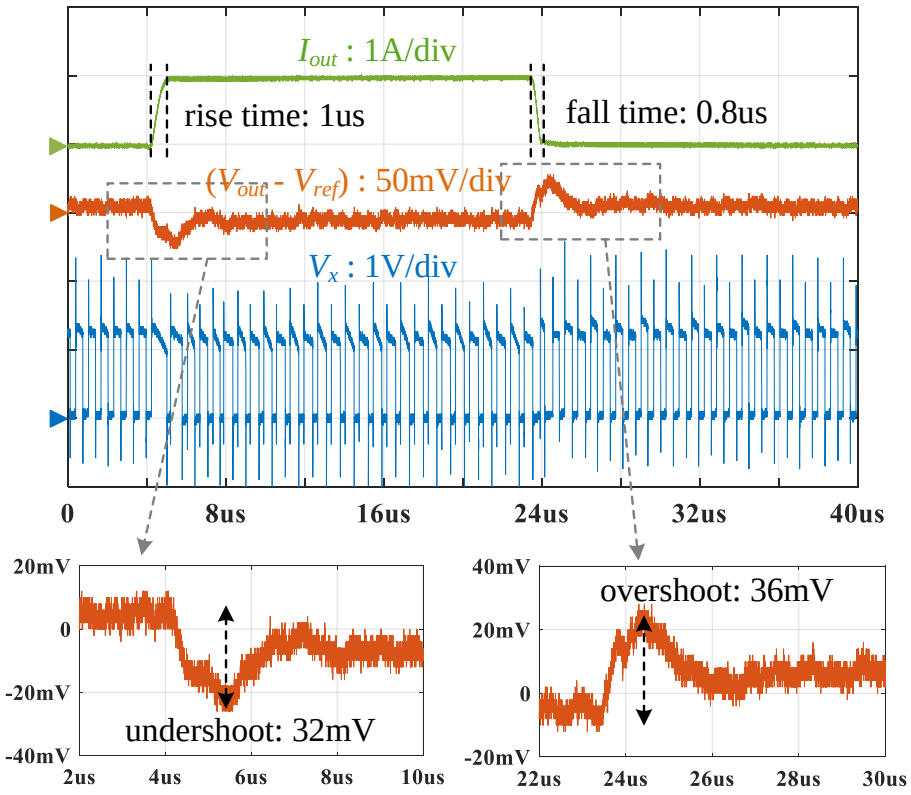

Figure 5.20: Measured full-range load transient response.

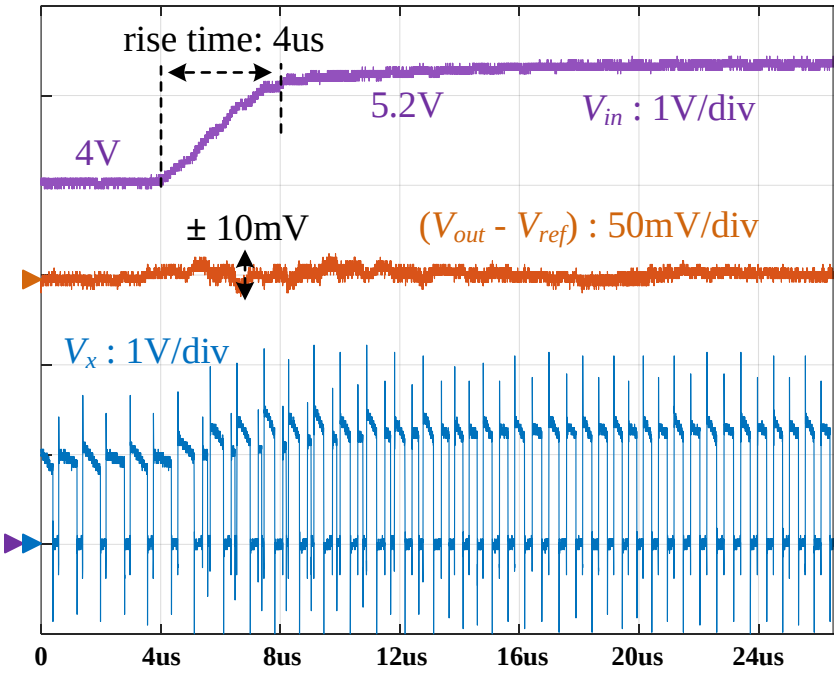

Figure 5.21: Measured line transient response (V_{in}: 4V→5.2V).

Figure 5.22 shows converter startup characteristics with V_{in} rising from 0 to 5V in 8μs (0.62V/μs slew rate). Different stages in the startup process are seen in the V_x waveform. During 0-4μs, V_{in} is rising but no switching event happens as the internal nodes and capacitors are charging up. In 4-7μs, the converter is in the startup mode since no lower pulse of V_x (i.e., φ_3 and φ_7 where C_2 is connected between V_x and ground) is observed, meaning these two phases are skipped. As gate drivers in the second stage wait for C_2 to charge, switch M_7 and M_8 are subject to body-diode conduction, leading to temporarily negative V_x. In 7-12μs, C_2 is charged sufficiently close to its nominal voltage and the converter is in the regular mode, where the control loop is regulating both the output voltage and the flying capacitor voltage. The converter enters the steady state at 12μs.

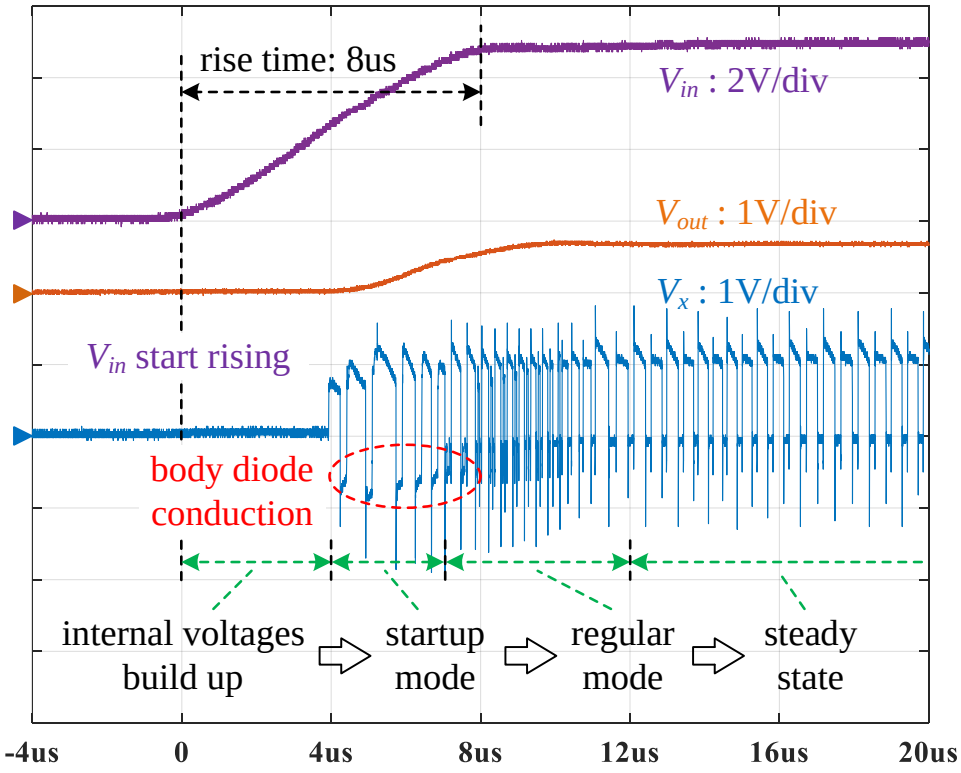

Figure 5.22: Measured startup waveform (V_{in}: 0→5V).

Figure 5.23 shows the worst case startup of the converter in practice. The USB cable, which connects to V_{in}, is directly plugged into the USB adapter. The V_{in} waveform has

an overshoot due to cable inductance, but the converter still safely starts up then maintains balance and regulation in steady state.

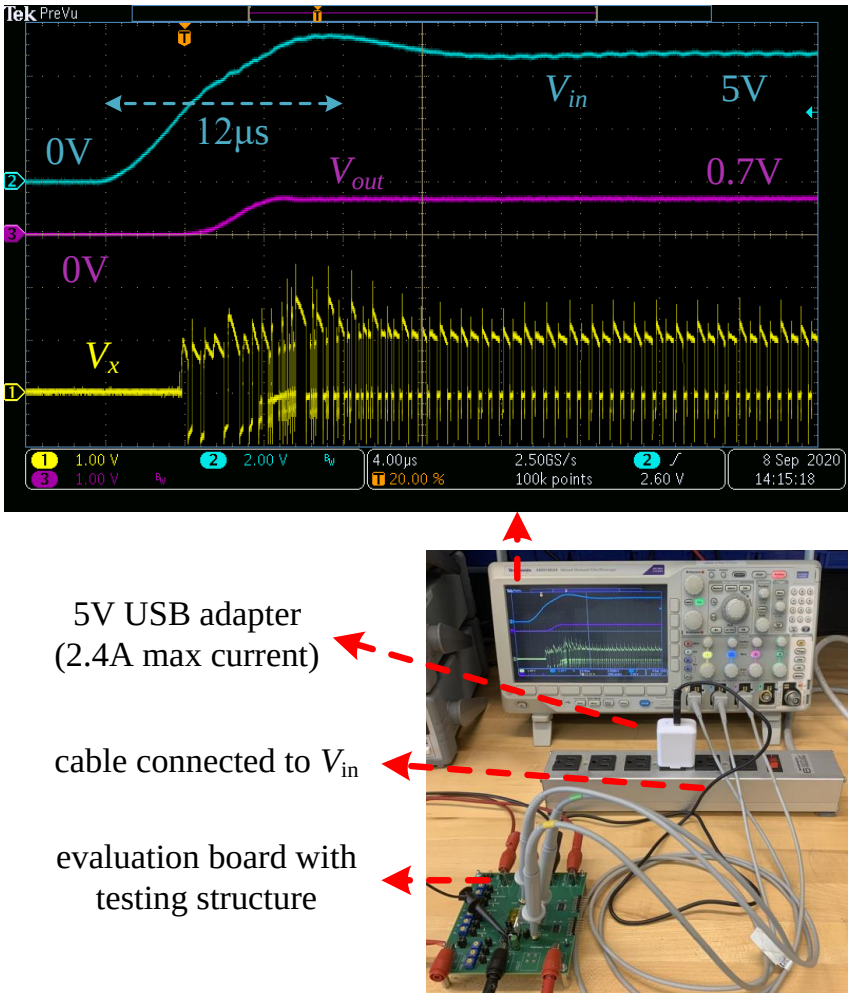

Figure 5.23: Testing the startup with V_{in} directly connected to a USB adapter.

Table 5.1 summarizes the converter performance and compares selected key features with similar prior works. This design achieves higher efficiency at comparable conversion ratios, although showing lower power density against designs in deep-submicron processes (area of die-attached passive components are counted in this work even though they do not occupy additional physical area). The output voltage overshoot and undershoot are also smaller under similar load current step. The major advantage here is the startup time that is over 100 times faster than the closest prior art.

Table 5.1: The performance summary and comparison with similar prior art.

	[92]	[93]$^{\diamond}$	[83]	[94]	[68]	**This Work**
Topology	Hybrid Dickson	3-level Buck	4-level FCML	Buck-Boost	5-level FCML	Hybrid Cascaded SC
Process	65nm	28nm	22nm	90nm	180nm	180nm
V_{in}	3-4.5V	3-4.5V	3.7-5V	2.5-5V	4-5.5V	4-6V
V_{out}	0.3-1V	0.8-1.45V	0.8-1.8V	0.4-9V	0.4-1.2V	0.4-1.2V
power switch count	8×2.5V	4	12×1.2V	5	8×1.8V	8×5V+3×1.8V
number of sw. states	6	4	6	4 or 6	8	8
inductor f_{sw}	1MHz	3MHz	5MHz	up to 3MHz	not reported	1.4-1.6MHz
$I_{out,max}$ (@ V_{out})	1.05A (0.95V)	1A (1.15V)	10A (1.8V)	1A (4.5V)	1.4A (1V)	1A (1.1V)
Control	integrated	integrated	off-chip	integrated	integrated	integrated
Flying capacitor	3x22μF	on-chip	2x13.2μF	10μF	3x4.7μF	2x4.7μF+10μF
Output capacitor	22μF	2μF	18μF	10μF	10μF	14.4μF
Inductor	470nH	2.2μH	10nH	2.2μH	240nH	240nH
Max. power density†	0.1W/mm^2	N/A	0.95W/mm^2	N/A	0.11W/mm^2	0.1W/mm^2
Max. Eff. (@ VCR*)	94.2% (4.4)	89.6% (3.8)	93.8% (2.8)	96.8% (1.2)	92.4% (4.6)	96.9% (4.2)
Max. VCR* (@ Eff.)	8.2 (86.5%)	3.8 (89.6%)	6.3 (85.8%)	12.5 (N/A)	13.8 (80.2%)	12.5 (85.5%)
I_{out} trans. step	N/A	0.35A→0.1A	0→6A	N/A	0→1A	0→1A
V_{out} over/undershoot	N/A	17mV	150mV	N/A	58mV	32mV
V_{in} startup step	N/A	N/A	0→5V	N/A	0→5.5V	0→5V
Duration (slew rate)	N/A	N/A	7ms (0.72V/ms)	N/A	2ms (2.8V/ms)	8μs (625V/ms)

*VCR refers to the step-down voltage conversion ratio, V_{in}/V_{out}.

†The total area includes active die, flying capacitors and inductor. In this work, the area of die-attached passives are also included.

$^{\diamond}V_{out}$ assumed as the average of multiple output.

Chapter 6

Conclusions

6.1 Major Contributions

A discrete-time state-space model for direct-conversion hybrid SC converters was derived in Chapter 2. Active balance is possible only if the SC stage is controllable; estimation of flying capacitor voltages from the switching node voltage is possible only if the SC stage is observable. Criteria for both controllability and observability are given and proved. The dynamics of direct hybrid converters is described by the complete model, which combines the model of the SC stage and the output filter stage.

A state estimator that extracts flying capacitor voltage information from measurement of the switching node voltage was presented in Chapter 3. The averaged output equation of the SC stage provides a theoretical principle, and the implemented algorithm adopted an iterative approach. The impact of non-idealities on the observability was analyzed and quantified. The estimator was tested on a 5-cell FCML converter, showing a 0.25% steady state error and 214μs settling time.

The fundamental cause of natural imbalance and one possible solution were also presented in Chapter 3. When the SC stage is not controllable, an eigenvalue of the system is on the unit circle, meaning that disturbances do not decay to zero in steady state and the

converter is not naturally balanced. A new switching sequence, the modified PSPWM, was proposed to enable controllability in previosuly uncontrollable cases. Both simulation and experimental results show that modified PSPWM strengthens natural balance of a 4-cell FCML converter.

A novel algorithm, the CSS control, was proposed in Chapter 4 to achieve both active balance and output regulation for direct-conversion hybrid SC converters. Active balance is achieved by clamping V_x to the correct final values thus has a simple implementation. While multiple output regulation methods are compatible, in this work, a single-bounded hysteretic scheme is demonstrated. The performance of CSS control was evaluated on a 4-cell FCML converter, showing robust operation and fast transient response.

An integrated cascaded hybrid SC converter for USB power delivery (5V: 0.4-1.2V) was presented in Chapter 5. With partial interleaving, the topology reduces input bypass capacitance and has fast balancing dynamics. Active balance and output regulation were both achieved by the MRIC algorithm, with phase skipping further accelerating startup. Gate drivers were fully integrated, with several proposed techniques reducing bootstrap capacitor area. Experimental results show 96.9% peak efficiency at 5V:1.2V conversion and a startup time of 12μs.

6.2 Future Research Directions

To support higher output current, multi-inductor hybrid topologies are gaining popularity, such as series-capacitor buck [47] and dual-inductor Dickson [95, 96]. Some of them are similar to direct-conversion topologies as one terminal of each inductor is permanently connected to the output. The state-space model developed in Chapter 2 can potentially be extended to these 'direct-like' multi-inductor topologies, because they can be regarded as the combination of a SC stage and a output filter stage as well. However, due to multiple switching node voltages, model dimension (number of state variables) may increase.

CSS control proposed in Chapter 4 features simple implementation and fast transient response, but its performance on discrete designs is still limited by design flexibility and PCB parasitics. The full potential of CSS control may be realized in integrated designs, with possibly better performance than MRIC, because it offers more freedom in terms of the trade-off between active balance and output regulation. However, with dynamic scaling of the ΔV parameter, integrated CSS control does require a high-performance DAC, which can be a major design challenge.

High step-down ratio converters are increasingly demanded in applications spanning data centers, performance computing, and point-of-load. One popular approach to address this challenge is using vertical stacking to reduce the effective input voltage [97, 98]. The cascaded hybrid topology proposed in Chapter 5, in a general sense, is the case where the stacking number equals to 2. Larger stacking numbers were also demonstrated [52], but a scalable and efficient stacking architecture that keeps the benefit of fast balancing dynamics is yet to be proposed. A possible direction is the cyclic operation of flying capacitors that divides down V_{in} [99], but the major challenge is achieving good active device utilization (low switch conduction loss).

Appendix A

Determine the rank of the connection matrix

For an N-cell FCML converter with $D = m/N$, the rank of its connection matrix, $\boldsymbol{C}$, will be determined in this appendix.

In resonant mode (m is an integer), $\boldsymbol{C}$ always has more rows than columns, thus its rank is determined by the number of linearly dependent column vectors. The first column, $\boldsymbol{C_{*1}}$, has the following form:

$$\boldsymbol{C_{*1}} = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \\ -1 \\ 0 \\ \vdots \\ 0 \end{bmatrix}, \tag{1}$$

where there are $(m-1)$ zeros in the middle and $(N-m-1)$ zeros in the end. The i^{th} column is obtained by circular shifting the first column by $(i-1)$ steps.

If a non-zero vector

$$\boldsymbol{V} = \begin{bmatrix} v_1 & v_2 & \cdots & v_{N-1} \end{bmatrix} \tag{2}$$

can be found such that

$$\sum_{i=1}^{N-1} v_i \cdot \boldsymbol{C_{*i}} = \mathbf{0}, \tag{3}$$

then $\boldsymbol{C}$ is not full-rank, and vice versa.

Solving (3) gives:

$$v_i = \begin{cases} 0 & i = m \text{ or } i = N - m, \\ v_{(i+N-m)\%N} & \text{otherwise,} \end{cases} \tag{4}$$

where the symbol '$\%$' represents the modulo operation.

In the case that m and N are not co-prime, their greatest common factor is denoted as g ($g > 1$). Solution (4) becomes

$$\begin{cases} v_1 = v_{g+1} = \cdots = v_{N-g+1}, \\ v_2 = v_{g+2} = \cdots = v_{N-g+2}, \\ \vdots \\ v_{g-1} = v_{2g-1} = \cdots = v_{N-1}, \\ v_g = v_{2g} = \cdots = v_{N-g} = 0, \end{cases} \tag{5}$$

which leads to

$$\begin{cases} \boldsymbol{C_{*1}} + \boldsymbol{C_{*(g+1)}} + \cdots + \boldsymbol{C_{*(N-g+1)}} = 0, \\ \boldsymbol{C_{*2}} + \boldsymbol{C_{*(g+2)}} + \cdots + \boldsymbol{C_{*(N-g+2)}} = 0, \\ \vdots \\ \boldsymbol{C_{*(g-1)}} + \boldsymbol{C_{*(g+1)}} + \cdots + \boldsymbol{C_{*(N-1)}} = 0. \end{cases} \tag{6}$$

There are $(g-1)$ linear dependency among the column vectors, therefore, the rank of the connection matrix, $\boldsymbol{C}$, is $(N-g)$.

However, in the case that m and N are co-prime, their greatest common factor is one. Iterating (4) yields

$$v_1 = v_2 = \cdots = v_{N-1} = 0, \tag{7}$$

indicating that $\boldsymbol{C}$ is full-rank.

In inductive mode (m is not an integer), the largest integer that is smaller than m (floor) is denoted as m_f; the smallest integer that is larger than m (ceiling) is denoted as m_c. The connection matrix at duty cycle $D = m_f/N$ and $D = m_c/N$ are denoted as $\boldsymbol{C_f}$ and $\boldsymbol{C_c}$, respectively. The rank of $\boldsymbol{C}$ can be determined by:

$$\text{rank}(\boldsymbol{C}) = \text{rank}(\begin{bmatrix} \boldsymbol{C_f} & \boldsymbol{C_c} \end{bmatrix}). \tag{8}$$

Following similar derivation in the case of resonant mode, it is straightforward that $\boldsymbol{C}$ is always full-rank in inductive mode.

Appendix B

Stability of the Balancing Sliding Mode

In the MRIC algorithm, the balancing sliding mode achieves balance by shortening high phases where V_x is too low. Its stability will be proved in this appendix.

At the beginning of a high phase, assuming that the initial switching node voltage is slightly lower than the balanced value, different control actions may be performed to determine the phase duration, as shown in Figure 1.

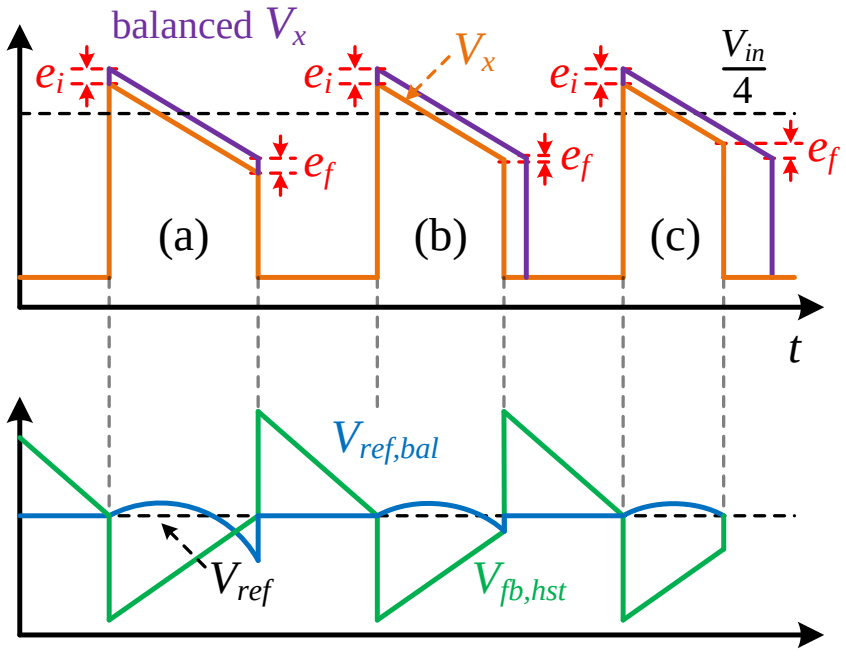

Figure 1: Example waveform of three different high phases: (a) duration not reduced. (b) duration reduced by MRIC. (c) duration further reduced.

Case (a) represents that the high phase is ended when $V_{fb,hst}$ reaches V_{ref}, meaning the duration is not influenced by the balancing sliding mode. Case (b) represents that the high phase is terminated when $V_{fb,hst}$ reaches $V_{ref,bal}$, which is the same as MRIC. Case (c) represents that the high phase is terminated when $V_{ref,bal}$ reaches V_{ref}, meaning the phase duration is further reduced compared to MRIC. In all three cases, balancing error is defined as the difference between the actual V_x and its balanced value, with the initial and final error in that phase denoted as e_i and e_f, respectively.

In case (a), the phase duration is not changed by the balancing sliding mode, thus the imbalance error also remains the same from the beginning to the end of the phase, and the error gain, $k_{e,a}$, is given by

$$k_{e,a} = \frac{e_{f,a}}{e_{i,a}} = 1. \tag{9}$$

In case (c), both V_x and its balanced value are symmetric with respect to $V_{in}/4$. Therefore, $V_{f,c} = -V_{i,c}$, and the error gain is given by

$$k_{e,c} = \frac{e_{f,c}}{e_{i,c}} = -1. \tag{10}$$

in case (b), the phase duration is between that of case (a) and (c), so is the error gain:

$$-1 < k_{e,b} < 1. \tag{11}$$

Therefore, in MRIC, which is the same as case (b), $|e_{f,b}| < |e_{i,b}|$, meaning the absolute imbalance error at the end of the state is always smaller than at the beginning of the state. Because the imbalance error is always decreasing, in the limit as time or the number of switching cycles goes to infinity, the error must converge to zero (similar to having discrete-time eigenvalues within the unit circle), thus stability is guaranteed.

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