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Low Power High Gain Op-Amp using Square Root based Current Generator

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I. Introduction

Operational amplifiers designed using bipolar junction transistor (BJT) consumes more power [1], so they remain unsuitable for most of the modern application specific integrated circuits (ASICs). Op-amps designed using metal-oxide-semiconductor field effect transistor (MOSFETs) is gaining importance in present signal processing architectures [4] due to their potential for low power operation. Their use however impaired by low trans conductance to drain current ratio (gm/Id <= 28) when compared to the Bipolar junction transistors gm/Id ratio of about 40 [4, 5], poor matching and the low output impedance of the strong inversion region [6]. Two stage Operational amplifier, though a two poles system, essentially performs as a single pole system having one dominant pole due to one internal node of the high impedance, the other high impedance node makes non-dominant pole which is kept at sufficiently high frequency, beyond the unity-gain bandwidth (UGB) by utilizing the suitable compensation techniques. These compensation techniques consume considerable chip area and require complex design [7] than dominant pole approach (pole splitting) used in classical Op-amp architecture . Classically, Miller effect was used to reflect a large capacitance to output of the differential high gain first stage. However, a feed-forward path is also available that results in positive zero (affects phase like a pole) thereby reducing phase margin. Usually, a nulling resistance is added in series with compensating capacitor to control position of this zero [4] which also consume additional chip area.

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If the self cas code (SC) structure of Fig. 1 is biased in such a way that transistor M2 operates in the sub threshold region, a very high voltage gain can be obtained and resulting larger capacitance at the output limits its frequency response, a condition advantageous for input differential stage of Operational amplifier .

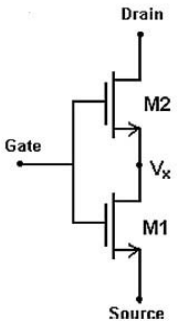

Fig. 1 : Self cascode

In sub threshold region the gm/Id is approximately equal to 28 while in strong inversion region it is much lower than 28. The larger capacitance at the output of input differential stage which in corporate Self Cas code structures can minimize or eliminate the need for an on-chip compensating capacitor thereby reducing occupied chip area. The sub threshold operation of SC additionally results in low power, low distortion and low noise [6] suggests guidelines to optimize Op-amp performance by obtaining higher gain, low power consumption, less distortion and a smaller value of compensating capacitor.

This paper presents a high gain(121.9dB) ,low power (11.89uW), CMOS Op-amp having structural simplicity of the classical Widlar architecture. Cadence simulations for 0.18um CMOS technology have been carried out at ±0.65V supply.

II. Op Amp Design using Self Cascode

The proposed two stage Op-amp has been shown in Fig.2 which utilizes the sub threshold biased Slef Cascode structures with the input stage of classical Widlar architecture.

To minimize the need for compensation capacitor, the differential input stage utilized sub threshold biased SC structures based on split length MOSFETs. This has been achieved by sizing Self Cascode transistors with inverse aspect ratio and

operate them with the low bias current to ensure very high gain which is relatively independent of the drain currents and results in reduced non-linear distortion . A higher voltage gain has been achieved due to sub threshold operated transistors resulting in reduced channel length modulation. Since, sub threshold gain and the gain-bandwidth product (GBW) of a MOSFET is a constant quantity, a change in Id9 affects band width of the structure.

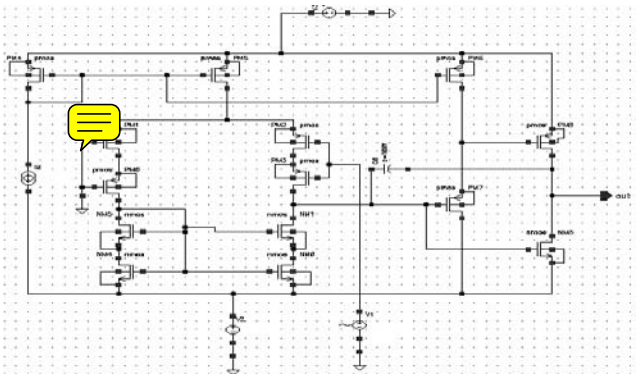

Fig. 2 : High gain opamp structure

Keeping inverting input (V_in) at zero volts and applying the input signal at non-inverting input of Op-amp (Vþin), the voltage gain of this stage is

$$ADI = g_{m(eff)}.R_{out(DI)} \quad (1)$$

where, gm(eff) is the effective transconductance of SC consisting of M2a and M2b, and output resistance of differential input stage is given by,

$$Rout(DI) = R_{out(SC)2} \| R_{out(SC)4} \quad (2)$$

The output stage (M5 to M7 and M10) is used to drive the external loads and require large currents. Due to small bias current of sub threshold biased SC structures, their use at output can be ruled out. Cascode / Regulated cascode structures can be used in place of M5 and M6, as they can deliver very high gain without compromising transistor's UGB [25]. However, position of its dominant pole at low frequency require large compensation capacitance to move this pole at higher frequencies and to make phase margin positive. Additionally, high output compliance voltage due to stacked transistors reduces the output swing by at least 2 Vds(sat), while increase in transistor counts increases the consumed chip area and power. Since differential input first stage provide most of the gain, this stage is designed to provide moderate gain (≈20dB) with very high x_3dB (higher than UGB of the first stage) to place poles of this stage at much higher frequency to improve phase margin. Class-AB configuration has been chosen to deliver efficiency of the order of Class-B configuration and to avoid dead zones during transitions. Transistor M7 acts as a level shifter to bias M5 and to set the output quiescent current to ensure low power operation.

Due to very high open loop gains, Op-amps are used with negative feedback and require compensation to avoid Barkhausen's condition for sustained oscillations, thereby ensuring closed loop stability . In the classical pole splitting technique, with the increase in output stage gain, the dominant pole frequency decreases and the non-dominant pole location increases to split the poles apart and to enhance the stability. Under unity gain condition (worstcase scenario) a phase margin of 63^0 provide the best compromise between rise time and settling time [2].

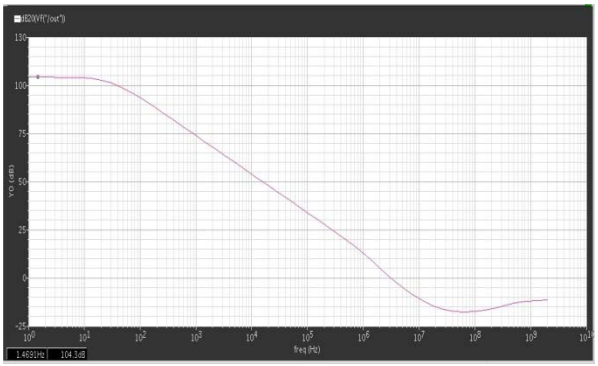

Fig. 3 : AC response of opamp shown in fig.2

In the modified compensation technique utilized here, the aspect ratio of MOSFETs used in the two stages of Opamp are optimized to generate a parasitic capacitance at the output of first stage to minimize the need for additional onchip compensation capacitance of value suitable for good phase margin (>60°). Cascoded devices with wider W (M3b and M4b of the differential input first stage) increases their gm which ultimately reduces the effective resistance ($1/g_{m3b}$) and increases parasitic capacitance CP [Eq. 11]. The reduction in $1/g_{m3b}$ dominates the increase in CP, and places the mirror pole at higher frequency, away from the dominant pole. A wider MOSFET (M4b) increases the parasitic capacitance CQ to further move the dominant pole , towards the origin in the s-plane. The larger channel length devices with subscripts 'a' enhances their output resistances due to reduced channel length modulation which ultimately increases the voltage gain of differential input first stage. The output stage is optimized to deliver highest ω_3dB which diminishes the effect of pole from this stage and the mirror pole from input differential stage, resulting in better phase margin(>60°) of the Op-amp.

III. Square Root based Current Generator

A low variation current generator can be designed by choosing the equation $I = \sqrt{I_1 I_2}$ .MOS transistors are used to implement the circuit. By using transistors in the sub threshold region, we can implement circuit using a translinear loop, the following equation(see fig.4).

$$I = I_1^{1/(k+1)} . I_2^{k/(k+1)}$$

Where k is the subthreshold coupling coefficient. We note thatthis equation is dimensionally correct. A circuit implementation of this "feedback" is shown in Fig. 5.

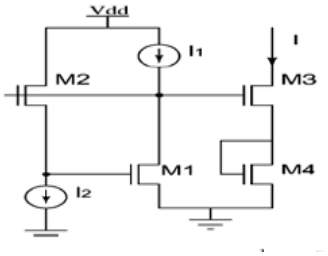

Fig. 4 : Translinear loop

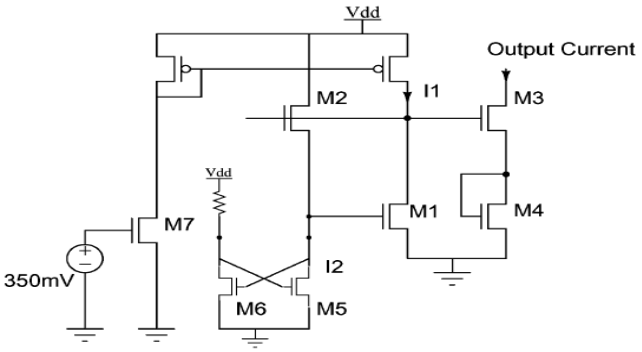

Fig. 5 : Square Root Based circuit

Transistor M6 and the resistor R invert M1 gate voltage. transistor M5 produces I2 and also adjusts it to negatively correlate with I1. The current I1 itself is generated using an nMOS transistor M7 and mirrored into transistor M1 using an pMOS current mirror. Fig. 6 shows a Monte Carlo scatter plot of I1 and I2 . We see from the plot that as I1 varies with the process, I2 varies inversely. Also, by plotting I1 and I2 on log scales, we verify that ΔI1/I1 and ΔI2/I2 are linearly related.

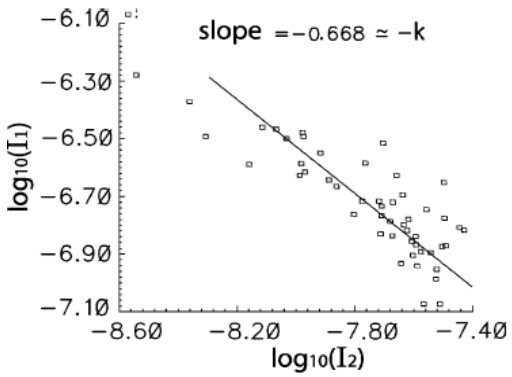

Fig. 6 : Scatter Plot

Fig. 7 shows the Monte Carlo histograms of the input nMOS transistor current and the output of the square-root circuit. We obtain an improvement of a factor of three in the current spread. These simulations include all the variations, including the mismatches between the local transistors, variations in A (the gain of the common source stage).

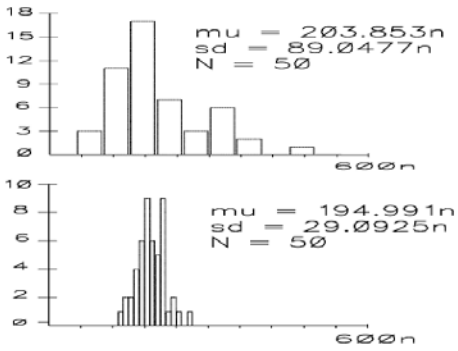

Fig. 7 : Histograms of the output current from a single transistor (top) and square-root circuit(bottom)

These do not get reflected output current variations as the negative correlation between the ΔI1/I1 and ΔI2/I2 is still maintained. Only the proportionality constant is being modified. Thus, these variations are suppressed to the first order. Also note that this result does not include the impact of the changes on the gate of transistor M7.

IV. Proposed Architecture

In the proposed architecture we replace the current source of the opamp (see Fig.2) with the above discussed square root based current generator which help in reduce impact of process variations on the circuit and help in reduce post fabrication efforts. So with the help of square root based current generator the better controllability over gain can be obtained.

Fig .8 shows the proposed architecture having square based current generator . and the AC frequency response is shown in fig.9. we observe that the circuit exhibits a higher gain of 121.9dB and also consumes a very less power of 11.89 μw due to the subthreshold region operation of MOSFETS in square root based generator..

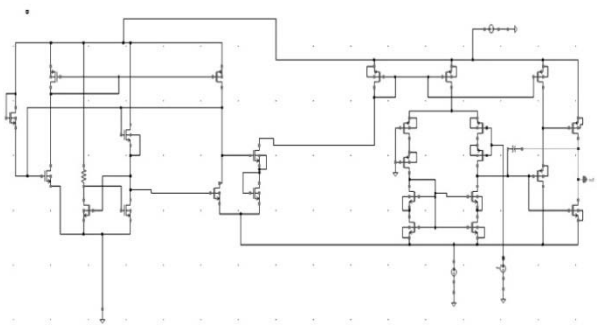

Fig. 8 : Proposed architecture

V. Measured Results

A high gain low power opamp has been designed by replacing the ideal current source in fig.(2), by a single MOSFET which is shown in work [1] and and the outputs are compared to verify the circuit sqrt based current source i.e proposed architecture operation at different conditions.

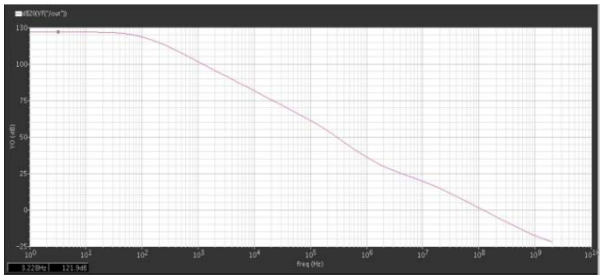

Fig. 9 : AC response of proposed architecture

Figure 10 shows the gain at different temperatures. It can be observed that the temperature variations are less compared to that of existing work[1]. The power dissipation of the proposed work is shown in fig 10.

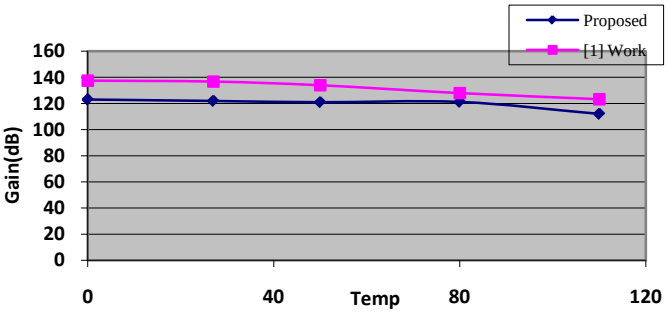

Fig. 10 : Gain at different temperatures

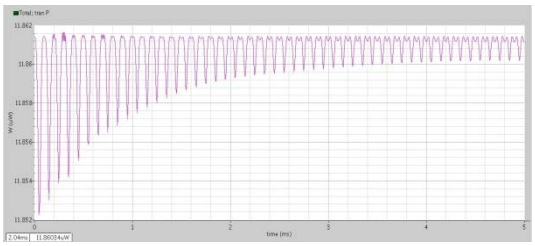

Fig.11 : Power consumption of the proposed structure

The power consumption of proposed architecture at different temperatures can be seen infig.12.

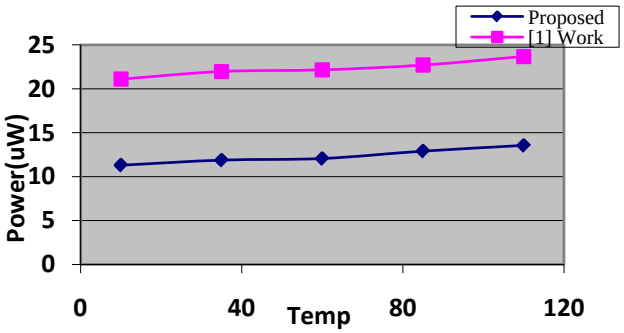

Fig.12 : Power Consumption at different temperatures

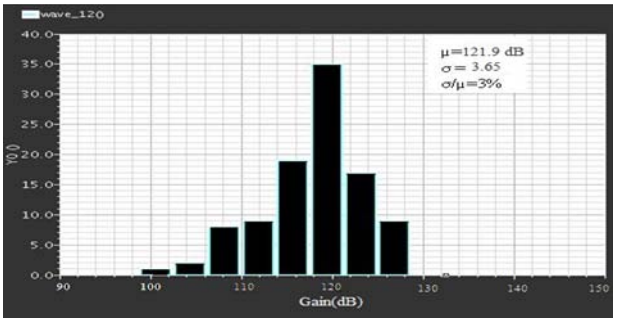

Figure 13 : Histogram of gain for proposed architecture

By taking Vth and Tox variations of 10% into consideration the statistical analysis has been performed and the hisogram of gain is shown in fig. 13. A low variation of standard deviation over mean of 2.9% is achieved by using the proposed opamp.

The following table shows the comparison between the proposed work and the reference work.

Table I: Comparison of present work and proposed work

Parameter	OPAMP in fig.2 (current source is replaced by a MOSFET)	Sqrt based current source OPAMP
Power	21.1uW	11.89uW
Technology	250nm	180nm
Phase Margin	62.1	60.3
Supply voltage	±1V	±0.65V
SR+/SR-(V/us)	2.285/2.339	4.67/4.46
UGB	3MHZ	10MHZ
Open loop gain	127db	121.9db

VI. Summary

Hence an ultra high gain, low power process, temperature compensated opamp has been designed in CMOS 180nm process and with a gain of 121.9dB and low power of 11.89 μw. though the gain is reduced compared to the existing OPAMP, a better UGB, tolerance to process, temperature variations and low

power of 11.89uw has been achieved with the replacement of current source by the Square based current generator as the current source in the OPAMP.

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