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A Neural Network Approach to Transistor Circuit Design

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A Neural Network Approach to Transistor Circuit Design

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Abstract- Transistor amplifier design is an important and fundamental concept in electronics, typically encountered by students at the junior level in electrical engineering. This paper focuses on two configurations that employ neural networks to design bipolar junction transistor circuits. The purpose of this work is to determine which design best fits the required parameters. Engineers often need to develop transistor circuits using a particular topology, e.g., common emitter, common collector, or common base. These also include a set of parameters including voltage gain, input impedance, and output impedance. For the most part, there are several methodologies that can provide a suitable solution, however the objective of this work is to indicate which external resistors are necessary to yield useful designs by employing neural networks. Here, a neural network has been trained to supply these component values for a particular configuration based on the aforementioned parameters. This should save a significant amount of work when evaluating a particular topology. And it should also permit experimentation with several designs, without having to perform detailed calculations.

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I. Introduction

Many transistor circuits are designed using bipolar junction transistors (BJTs) or MOSFETs. MOSFET designs are usually easier to analyze due to the high gate impedance so this paper focuses on the BJT, and in particular, the common emitter configuration. There will be two types of ac equivalent circuit analyzed in this paper. The first will assume that the emitter bypass capacitor is ideal, i.e. infinite capacitance, and the second will consider a finite capacitor impedance, which significantly increases the complexity of the problem. The coupling capacitors tend to play a lesser role in the ac design parameters so the ideal approximation of these components is reasonably close to the non-ideal case. The output impedance of the source and the input impedance of the load can be factored in after developing the initial model.

The calculations are relatively simple when considering a common emitter amplifier circuit with an ideal bypass capacitor, but a much greater amount of effort is needed for the non-ideal case. The former will be considered first. For a given transistor the designer works through a set of calculations to determine the resistor values, then often has to modify them to achieve the proper gain (Av), input impedance (Rin), output impedance (Ro), and voltage difference between the collector and emitter (Vce). When working with an ideal bypass capacitor, it is not difficult to determine the proper parameters, but for the finite bypass capacitor the problem is significantly more challenging. This work is mainly intended for engineers, but also professors who may need to evaluate specific amplifier designs and grade the circuits supplied by their students. With regard to professors, if a student submits a design, it is the role of the instructor to evaluate the configuration to determine whether it meets the expected parameters. In other words, the resistor values, and/or the bypass capacitor value needs to be defined. If each student, or team, in a lab is expected to create a different design it will be necessary for the instructor to evaluate each solution to determine whether it meets the given criteria so this work should streamline the procedure.

This paper is organized as follows. First, the design procedure for the dc equivalent common emitter circuit is introduced along with some of its defining equations. Next, the expressions needed to solve for the ac equivalent circuits are developed. This is followed by a brief discussion of the neural network architecture. The next section addresses the finite bypass capacitor and the equations required to analyze the modified circuit. Finally, some conclusions will be discussed and some thoughts for further work.

II. The Common Emitter Amplifier

The common emitter amplifier circuit is one of the basic configurations introduced when studying the BJT [Sedra and Smith, 2015], [Jaeger, 1997]. It is a voltage amplifier with a reasonably high input impedance and voltage gain. The output impedance can be a bit high as well, but this can be handled by being certain that the input impedance of the follow-up stage is much higher, as for example, an emitter follower circuit. In a transistor circuit there are the dc bias values and the ac signal, but one must look at each of them separately in order to compute the proper operating points.

An example circuit is shown in Fig. 1 where the 2N3904 NPN transistor is used with $\beta=160$. The ac input is Vi while the output is taken across the load resistor RL on the right.

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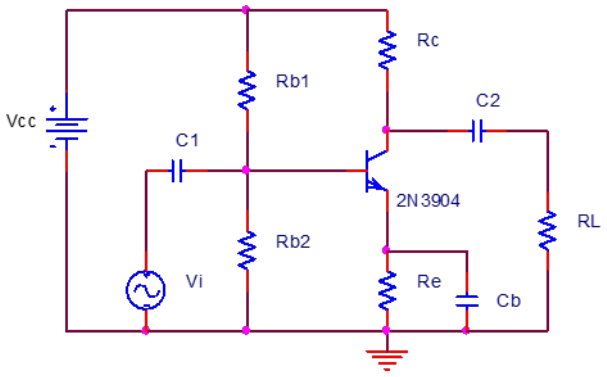

Figure 1: Common emitter amplifier circuit

Initially, the dc circuit is analyzed with all capacitors considered as open circuits in order to find the currents and voltages from the power supply and biasing resistors. The coupling capacitors isolate the dc component and its circuit equivalent is shown in Fig. 2.

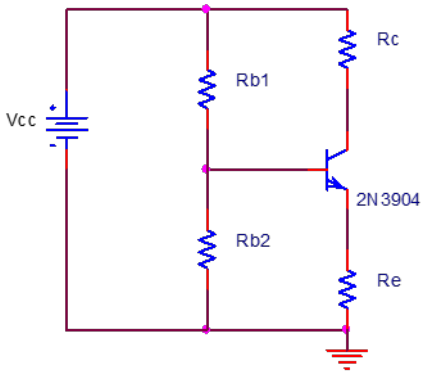

Figure 2: The dc equivalent circuit of a common emitter amplifier with ideal capacitors

To determine the dc biasing values the base resistors and source are replaced with their Thevenin equivalent and a single loop circuit is analyzed. For this circuit the Thevenin expressions are as follows where IBis the dc base current:

$$V_{th} = V_{cc}\left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) \text{ and } R_B = R_{B1} \parallel R_{B2} \qquad (1)$$

So the loop expression becomes:

$$-V_{th} + R_B\, I_B + 0.7 + (\beta+1) I_B\, R_E = 0 \qquad (2)$$

After the dc bias values have been determined those sources are set to zero and only the ac components are considered. Recall that the dc voltage sources become short circuits to ground when set to zero. The ac equivalent of the transistor circuit is shown in Fig. 3 using the hybrid – π model. This model is usually used when the emitter is at ac ground. The ac values of resistance, voltage gain, etc. are determined from the dc bias currents.

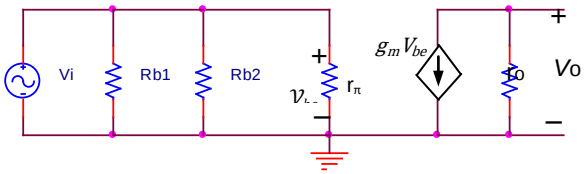

Figure 3: This is the ac equivalent circuit of the common emitter amplifier with an ideal bypass capacitor

The development of most of the ac equivalent expressions can be found in many texts on microelectronics so they are only summarized here. The total collector current ic is approximated where vbeis the ac base to emitter voltage and VTis the thermal voltage which is usually approximated at 25 mV so that.

$$i_C \approx \underbrace{I_C}_{DC}\left[1+\left(\frac{v_{be}}{V_T}\right)\right] = \underbrace{I_C}_{DC} + \underbrace{\left(\frac{I_C}{V_T}\right)v_{be}}_{ac} \qquad (3)$$

From now on the ac component is of interest. By superposition the DC sources are shut down, which means that they act like short circuits to ground. By looking at the right hand term from above it can be seen that the ac equivalent is:

$$i_c = \left(\frac{I_C}{V_T}\right)v_{be} \qquad (4)$$

This is the reciprocal of resistance and is referred to as trans conductance, with symbol gm: where

$$g_m = I_C / V_T \qquad (5)$$

$$\text{therefore: } i_c = g_m\, v_{be} \qquad (6)$$

The ac input resistance of the transistor is defined as input voltage divided by input current so the resistance seen at the base is

$$r_\pi = v_{be}/i_b = v_{be}/(g_m\, v_{be}/\beta) = \beta/g_m \qquad (7)$$

Alternatively

$$r_\pi = \beta/(I_C/V_T) = \beta/(\beta\, I_B/V_T) = V_T/I_B \qquad (8)$$

For the finite bypass capacitor circuit the T-model of the BJT will be used so se resistance seen from the emitter to the base will be needed and is written as

$$r_e = \alpha/g_m \qquad (9)$$

where. Since the emitter current is (□ + 1)ib it is easy to figure that the resistance seen at the base is

$$r_\pi = (\beta+1) r_e \qquad (10)$$

The voltage gain is

$$A_v = \frac{v_{ce}}{v_{be}} = -g_m R_C \tag{11}$$

The voltage gain is

$$A_v = \frac{v_{ce}}{v_{be}} = -g_m \left(R_C \parallel r_o\right) \tag{12}$$

III. Experimental Procedure

Neural networks are most commonly considered as pattern recognition systems.This author has used them to develop a method of impedance matching using feed- forward neural networks [Hemminger, 2005].They are non-linear systems and are often employed to differentiate between input patterns [Pao, 1989],[Graupe 2013], [Hagan and Demuth].

In order to train the neural networks in this project a set of "for" loops was created in MATLAB for the four biasing resistors. For all of the tests, the resistor values ranged as shown in table 1.

Table 1: Resistor values used to develop output parameters

Resistor	Start Value	Step Value	Stop Value
Rb1	6 kΩ	250Ω	10 kΩ
Rb2	4 kΩ	250Ω	7 kΩ
Rc	1 kΩ	100Ω	3 kΩ
Re	400Ω	100Ω	1.5 kΩ

The values of Rin, Ro, Av, and Vce were calculated for all of the resistor combinations. Once this was completed a neural network was trained using the new input values of Rin, Ro, Av, and Vceto compute the four biasing resistor values. In developing the network, the inputs and outputs were normalized to a magnitude of 1 to ensure convergence. For the ideal bypass capacitor circuit there were 5,349 training patterns, limited to realistic values. For example, the gain, Av, was limited to a magnitude of 210, while Vce was held to the range of 2 volts to 12 volts. The test sets consisted of a larger number of patterns, none of which had been used in training.

The neural network package in MATLAB was utilized to train the networks, employing the Levenberg-Marquardt algorithm, using one hidden layer of 18 sigmoidal (Tanh) neurons each [Demuth and Beale]. Smaller numbers of nodes yielded unacceptable results and more nodes or more than one hidden layer did not provide any improvement in performance. The network was trained for 2000 epochs resulting in a mean-squared error (mse) of 6.4x10-7. Further training did not seem improve performance. A comparison between the neural network results and those by direct calculation is shown in table II. Fig.4 shows the architecture of the neural network. This network employs hyperbolic tangent activation functions to map the transistor parameters to the values of the resistors.

Note that the number of patterns changes with all of the training and testing scenarios.This occurs because as the values of the biasing resistors change, the number of the voltage gains and values of Vce change, and one or the other can fall out of the ranges specified earlier. Only those that fall within those ranges are employed in the tests.When using the resistance values illustrated in table I the output parameters have the ranges shown in table III. It is not required that these ranges be followed precisely but it is likely a good practice to stay within them when considering an input set.

Table 2: Statistical performance of neural network

Data type	Number of patterns	Upper base resistor Rb1 (mse)	Lower base resistor Rb2 (mse)	Collector resistor Rc (mse)	Emitter resistor Re (mse)
Training set	5439	112	58	0.275	0.457
Test Set 1	6306	93	45	0.202	0.288
Test Set 2	10875	93	45	0.202	0.286
Test Set 3	17427	86	42	0.206	0.292
Test Set 4	21534	86	42	0.206	0.294

The training set was included for comparative purposes.

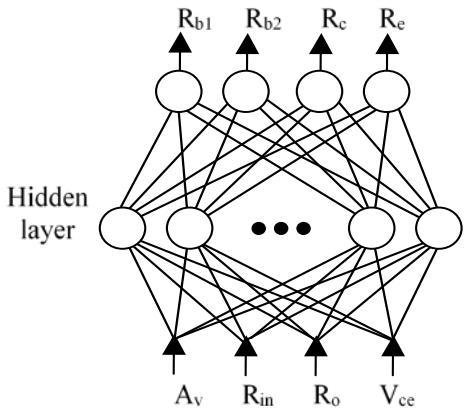

Figure 4: Architecture of the neural network with 18 hidden nodes

Table 3: Input Parameter Ranges

Parameter	Minimum Value	Maximum Value
Rin	566 Ω	1.67 kΩ
Ro	947 Ω	2.18 kΩ
Av	-210 v/v	-92 v/v
Vce	2.41 v	9.11 v

It is important to realize that not all input parameter combinations are feasible. For example, if the

base bias resistors are kept to a low value the collector and emitter currents can be greater, resulting in a smaller value of Vce. In this case it would not be appropriate to set a small value of dc input resistance and a large value of Vce, since they can be mutually exclusive. However, by judiciously choosing realistic inputs the results can be close to the desired values. Some examples are shown in table IV. The requested parameters are shown with the percent error between the network output and the calculated values. By "tuning" the input parameters the percent errors can be reduced to acceptable values. In this case the voltage gain was the main focus.

Table 4: Statistical performance of neural network

Rin (Ω)	% error	Ro (Ω)	% error	Av	% error	Vbe	% error
900	-4.13	960	-0.65	-172	-5.10	7.0	8.48
880	-4.27	960	-0.66	-172	-2.85	7.0	5.38
880	-6.03	960	-0.76	-172	-0.84	7.0	-0.84

The resistor values from the last trial from table IV were used in a P-Spice simulation. The values were Rb1=30.0 kΩ,Rb2=15.24 kΩ, Rc=995 Ω, and Re=730 Ω. The results are summarized in table V along with the percent errors.

Table 5: Comparison of neural network results against the P-Spice simulation

Parameter	Neural Network	P-Spice	% difference
Rin	827 Ω	804 Ω	0.37
Ro	953 Ω	881 Ω	2.5
Av	-170 v/v	-180 v/v	5.8
Vce	5.671 v	5.56 v	2.0

IV. Using A Finite Bypass Capacitor

If the bypass capacitor does not have zero impedance the problem is much more realistic, but requires a significant amount of additional work to analyze. Here, rather than using the hybrid – π model it is more appropriate to use the T-model since it is easier to include the emitter impedance. This is illustrated in Fig. 5

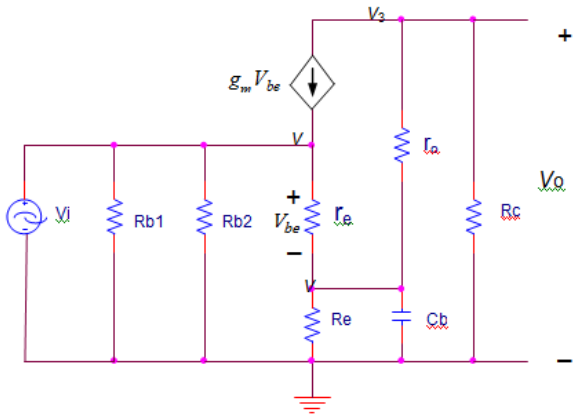

Figure 5: The T-model is used here in order to address the finite bypass capacitance Cb

The circuit was analyzed by employing nodal analysis at the three essential nodes with an input function of I amps at 3 kHz in order to determine the input impedance and other parameters. After simplifying the expressions, three equations in three unknowns were used to determine Rin, and Av. Note that the impedance of the capacitor was only evaluated in magnitude, since the phase would have little effect on the overall result. The three nodal equations are listed here in (13).

$$v_1\left[\frac{1}{R_{b1}}+\frac{1}{R_{b2}}+\frac{1}{r_e}-g_m\right]+v_2\left[g_m-\frac{1}{r_e}\right]=I \qquad (13a)$$

$$v_1\left[\frac{-1}{r_e}\right]+v_2\left[\frac{1}{r_e}+\frac{1}{R_E}+\left|\frac{\omega C}{-j}\right|+\frac{1}{r_o}\right]+v_3\left[\frac{1}{r_o}\right]=0 \qquad (13b)$$

$$v_1[g_m]+v_2\left[-g_m-\frac{1}{r_o}\right]+v_3\left[\frac{1}{r_o}+\frac{1}{R_C}\right]=0 \qquad (13c)$$

The input impedance was evaluated as $R_{in}=v_1/I\ amps$, and the gain was calculated as $A_v=v_3/v_1$.

Once this was completed a current source was applied to the output to find the output impedance, resulting in the following simultaneous equations.

$$v_1[g_m]+v_2\left[-\frac{1}{r_o}-g_m\right]+v_3\left[+\frac{1}{R_C}+\frac{1}{r_o}\right]=I \qquad (14a)$$

$$v_1\left[\frac{-1}{r_e}\right]+v_2\left[\frac{1}{r_o}+\left|\frac{\omega C}{-j}\right|+\frac{1}{R_E}+\frac{1}{r_e}\right]+v_3\left[-\frac{1}{r_o}\right]=0 \qquad (14b)$$

$$v_1\left[-g_m+\frac{1}{r_e}+\frac{1}{R_{b1}}+\frac{1}{R_{b2}}\right]+v_2\left[g_m-\frac{1}{r_e}\right]=0 \qquad (14c)$$

After setting the source to zero the resulting output impedance was calculated as . In order to achieve the necessary parameters it required two 3x3 matrix inversions per iteration and convergence took significantly longer than when considering the ideal bypass capacitor, requiring roughly 3000 epochs. Increasing the number of epochs beyond that number did not improve performance in any measurable way. There were 10 trials for the bypass capacitors from 10μF to 100μF as illustrated in table VI. At first it seemed like the capacitors could be incorporated in the original design as an output parameter of the network along with the resistances but since only the magnitudes of the impedances were considered this presented a problem. Having the capacitor impedance and the emitter resistance combined resulted in an overall impedance that could not be resolved into separate elements. For this reason 10 trials, one for each capacitor value, were conducted to provide proper training. Actually, this is not really a problem because the necessary parameters for each topology can be learned by the network in a matter of minutes and the value of the bypass capacitor is not that critical when only 10 μF increments are being considered. The input frequency of 3 kHz was chosen since this is a good mid-band parameter for audio signals. Requiring the input frequency to be a variable caused problems with convergence, so for the present it was fixed at the aforementioned value. Finite values of bypass capacitance are rarely studied in undergraduate electronics courses, where most curricula assume that the bypass capacitor is ideal with infinite capacitance. This makes the analysis much simpler but not very realistic unless the capacitor used in the physical circuit is fairly large in value. It is interesting, and obvious, that as the capacitance increases, the results from the second design merge with those from the first one. This includes the training errors for each scenario.

Table 6: Statistical performance of neural network after 3000 epochs

Capacitor Value in µF	Number of patterns	Upper base resistor Rb1 (mse)	Lower base resistor Rb2 (mse)	Collector resistor Rc (mse)	Emitter resistor Re (mse)
10	14294	389	218	2.17	1.84
20	13500	437	264	3.44	1.87
39	11982	490	247	2.22	1.80
40	10652	403	219	.037	2.12
50	8884	121	65	0.08	1.36
60	8541	117	59	0.19	1.13
70	8244	56	40	0.14	0.38
80	7987	197	67	0.56	1.25
90	7920	177	72	0.71	0.74
100	7843	148	58	0.11	0.57

Table VII contains the results starting with a 10□F bypass capacitor, and ending with 100□F.It lists the solutions from P-Spice and compares them with the outputs from the neural network. For comparative purposes, the input parameters were kept the same as in the last line in table IV. Here it is seen that at lower capacitances the voltage gain is lower and the input impedance higher, which one would expect. As the capacitance increases the results from the network approach those yielded from the ideal bypass capacitor approximation, which one would also expect. In this table the value of Vce is not listed since it is not dependent on the value of the bypass capacitor and remains constant. It is noteworthy that once a capacitance of 60 – 70□F is reached there is little change in the parameters of interest.

Table 7: The calculated data is from P-Spice. The value of Vce is the same for all of these tests at 5.56 volts

Capacitor Value in µF	Rin (Ω)	% error	Ro (Ω)	% error	Av v/v	% error
10	1163	4.0	952	-3.26	128	-3.76
20	932	3.7	939	-2.13	161	+1.85
39	884	3.88	932	-1.39	170	+1.66
40	867	2.97	931	-1.40	174	+2.11
50	860	3.66	931	-1.40	176	-2.87
60	852	2.67	930	-1.29	177	-3.11
70	846	3.11	928	-1.08	177	-1.85
80	846	2.55	926	+0.11	177	-1.06
90	844	2.11	923	+0.98	177	-1.87
100	842	1.87	922	1.64	177	-1.67

V. Conclusions And Further Work

This has been an interesting and rewarding research project. It is hoped by this author that engineers and faculty members will find these results useful. The fascinating part of this project comes particularly from the results of including the non-ideal bypass capacitance. Non-ideal bypass capacitors are rarely emphasized when teaching about, or working with, transistor circuits, at least at the introductory level. This neural network paradigm should be useful to engineers and faculty members when looking for solutions to various designs. The approach described in this paper can resolve and verify several transistor designs and illustrates the efficacy of neural networks as a development tool for amplifier circuit biasing. An extension of this work will be to expand this technique to other amplifier circuits, e.g., the common collector and common base models employing both the BJT and the MOSFET. An additional objective is to determine a set of input parameters that will yield accurate results without having to adjust them as illustrated in table IV.

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