Global Journal of Computer Science and Technology: A Hardware & Computation
Volume 15 Issue 1 Version 1.0 Year 2015
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 0975-4172 & Print ISSN: 0975-4350

Investigating the VLSI Characterization of Parallel Signed Multipliers for RNS Applications using FPGAs

By Mr. Pradeep. N, Mr. S. Elango, Dr. P. Sampath & Ms. Gayathri
Bannari Amman Institute of Technology, India

Abstract- Signed multiplication is a complex arithmetic operation, which is reflected in its relatively high signal propagation delay, high power dissipation, and large area requirement. High reliability applications such as Cryptography, Residue Number System (RNS) and Digital Signal Processing (DSP)'s effective performance is mainly depend on its arithmetic circuit's performance. Trend of using Residue Number System (RNS) instead of Constrain over-whelming Binary representation is promising technique in VLSI Systems and Multiplier is the basic building block of such systems. In this paper we have considered signed Modified Baugh Wooley Multiplier and Modified Booth Encoding (MBE) Multiplier logic for analysis and synthesized on best suited application platform. Analysis has taken account of Delay, Number of Logic Element requirements; Number of Signal Transition for particular sample input and its Power Consumption were analyzed for both Modified Baugh Wooley Multiplier and Modified Booth Encoding Multiplier.

Keywords: baugh wooley multiplier, modified booth encoding (mbe), computer arithmetic, signed multiplier, verilog hdl, xilinx ise, altera quartus.

GJCST-A Classification : B.7.1

Strictly as per the compliance and regulations of:

Investigating the VLSI Characterization of Parallel Signed Multipliers for RNS Applications using FPGAs

Mr. Pradeep. N [α], Mr. S. Elango [σ], Dr. P. Sampath [ρ] & Ms. Gayathri [ω]

Abstract- Signed multiplication is a complex arithmetic operation, which is reflected in its relatively high signal propagation delay, high power dissipation, and large area requirement. High reliability applications such as Cryptography, Residue Number System (RNS) and Digital Signal Processing (DSP)'s effective performance is mainly depend on its arithmetic circuit's performance. Trend of using Residue Number System (RNS) instead of Constrain over-whelming Binary representation is promising technique in VLSI Systems and Multiplier is the basic building block of such systems. In this paper we have considered signed Modified Baugh Wooley Multiplier and Modified Booth Encoding (MBE) Multiplier logic for analysis and synthesized on best suited application platform. Analysis has taken account of Delay, Number of Logic Element requirements; Number of Signal Transition for particular sample input and its Power Consumption were analyzed for both Modified Baugh Wooley Multiplier and Modified Booth Encoding Multiplier. Analysis of Multiplier is described in Verilog HDL and Simulated using two different simulators namely Xilinx ISIM and Altera Quartus II. Then for comparative study, both multipliers are synthesized with Xilinx Virtex 7 XCV2000T-2FLG1925 and Altera Cyclone II EP2C35F672C6 and same parameter as discussed above are also evaluated. Booth Recoding provides overall advent of 9.691% in terms of area and approximately 43 % in terms of Delay compared to Modified Baugh Wooley Multiplier implemented using FPGA Technology.

Keywords: baugh wooley multiplier, modified booth encoding (mbe), computer arithmetic, signed multiplier, verilog hdl, xilinx ise, altera quartus.

I. Introduction

Multiplication is a most generally used operation in wide computing systems. In fact multiplication is nothing but addition since, multiplicand adds to itself multiplier number of times, gives the multiplication value between multiplier and multiplicand. But considering the fact that this kind of implementation really takes huge hardware resources and the circuit operates at utterly low speed. In order to address this so many ideas have been presented so far for the last three decades. Each one is aimed at improvement according to the requirement. One may be aimed at high clock speeds and another may be aimed for low power or less area occupation. Either way ultimate job is to come up with an efficient architecture which can address three constraints of VLSI speed, area, and power. Among three constrains, speed is the vital one which requires more attention. If we observe closely multiplication operation involves two steps one is producing partial products and adding these partial products [3].

Thus, the speed of a multiplier hardly depends on how fast generate the partial products and how fast we can add them together.Since the multipliers have a significant impact on the performance of the entire system, many high performance algorithms and architectures have been proposed [1-12]. The very high speed and dedicated multipliers are used in pipeline and vector computers.

Residue Number System (RNS) reduces the delay of carry propagation, thus offering significant speed up over the conventional binary system. This characteristic is advantageous when repetitive arithmetic operations on long operands have to be performed. RNS has been adopted in the design of Digital Signal Processors (DSP) .The low power consumption of RNS compared to conventional arithmetic circuits for the implementation of Finite Impulse Response (FIR) filters inspired lot of work against it. Therefore, RNS may be an interesting candidate for building processing circuits in deep submicron technologies.

The rest of the paper is organized as: Section-II describes Baugh-Wooley Multiplication Section-III provides deep understanding about Modified Booth Encoding techniques, Comparative results and its analysis are exploited in Section-IV and Finally Conclusion of the paper illustrated in Section –V.

II. Baugh Wooley Multiplier

The Baugh-Wooley multiplication is one of the efficient methods to handle the sign bits and this approach has been developed in order to design regular multipliers[2], suited for 2's complement numbers.

Let us consider two n-bit signed numbers, X (Multiplicand) and Y (Multiplier), to be multiplied

Author α σ: PG Student, ECE Dept, Bannari Amman Institute of Technology, Sathyamangalam. e-mail: bpradeepn@gmail.com
Author ρ: Assistant Professor, ECE Dept, Bannari Amman Institute of Technology, Sathyamangalam.
Author ω: Associate Professor, ECE Dept, Bannari Amman Institute of Technology, Sathyamangalam.

$$X = -x_{n-1}2^{n-1} + \sum_{i=0}^{n-2} x_i 2^i \quad [1]$$

$$Y = -y_{n-1}2^{n-1} + \sum_{i=0}^{n-2} y_i 2^i \quad [2]$$

where the xi's and yi's are the bits in X and Y, respectively, and x_{n-1} and y_{n-1} are the sign bits.

The product, P= X * Y, is then given by the following equation:

P = X * Y

$$= \left(-x_{n-1}2^{n-1} + \sum_{i=0}^{n-2} x_i 2^i\right) * \left(-y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} y_j 2^j\right)$$

$$= x_{n-1}y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} x_i y_j 2^{i+j}$$

$$-2^{n-1}\sum_{i=0}^{n-2} x_i y_{n-1}2^i - 2^{n-1}\sum_{j=0}^{n-2} x_{n-1}y_j 2^j \quad [3]$$

The final product can be obtained by subtracting the last two positive terms from the first two terms.

Instead of pursuing subtraction operation, it is possible to obtain the 2's complement of the last two terms and add all terms to get the final product.

The final product (3), P=X * Y becomes:

P = X * Y

$$= x_{n-1}y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} x_i 2^i \sum_{j=0}^{n-2} y_j 2^j$$

$$+2^{2n-1}\sum_{i=0}^{n-2} \overline{x_i y_{n-1}}\,2^i + 2^{n-1}\sum_{j=0}^{n-2} \overline{x_{n-1}y_j}\,2^j \quad [4]$$

$$-2^{2n-1} + 2^n$$

Simple 4x4 Baugh-wooley multiplication is exhibited in figure 1.

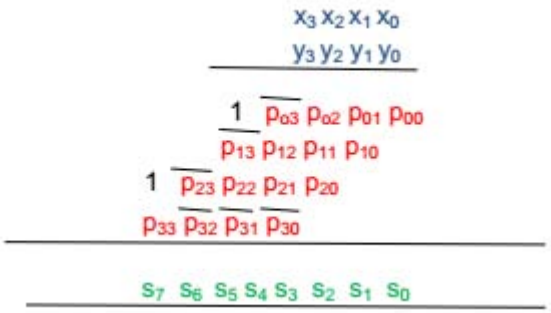


Figure 1

The same multiplication logic can be extended for different multiplier strength such as 4,8,16,32,64 bit-length and the efficiency is analyzed with simulation and synthesis tool .Baugh-wooley implementation require n2 AND gates and n(n-1) ADDERS as shown in figure 2.

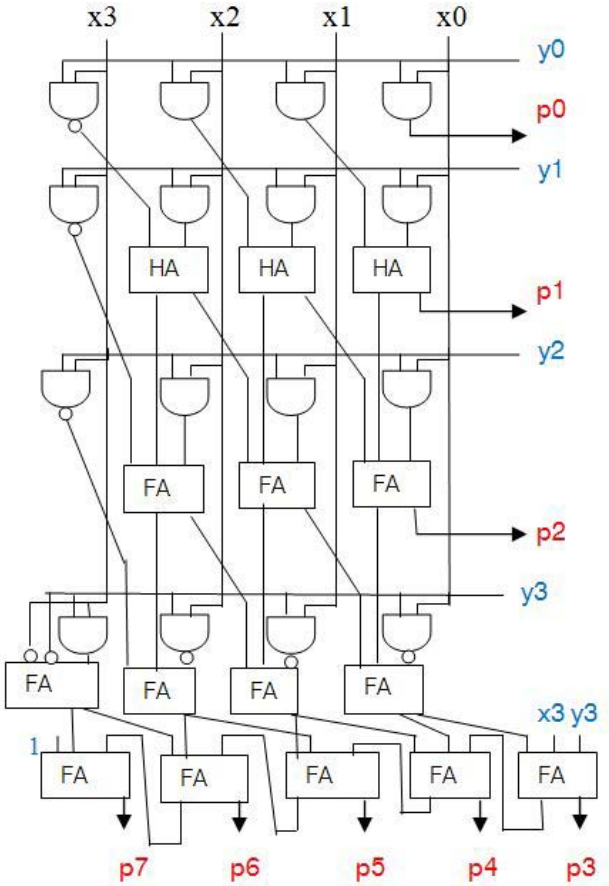


Figure 2

III. Booth Multiplier

The modified-Booth algorithm [1] is more preferred and extensively used for high-speed multiplier circuits. Modified Booth Multiplier is one of the different techniques for signed multiplication This multiplier architecture is based on Radix 4(2^2) Booth multiplier. In order to improve the architecture, we have made 2 enhancements as in [14]. The first is to use efficient Wen-Chang's Modified Booth Encoder (MBE) since it is proved as the fastest scheme to generate a partial product.

a) Algorithm of the Modified Booth Multiplier

Booth Multiplication consists of three[10-14] steps:

1. The first step to generate the partial products;
2. The second step to add the generated partial products until the last two rows are remained;
3. The third step to compute the final multiplication results by adding the last two rows.

The modified Booth algorithm reduces the number of partial products by half in the first step. We

used the modified Booth encoding (MBE) scheme proposed in [1], It is known as the most efficient Booth encoding and decoding scheme. To multiply M by N using the modified Booth algorithm starts from grouping N by three bits and encoding into one of {-2, -1, 0, 1, 2}.Figure 3 exhibit the general architecture of MBE.

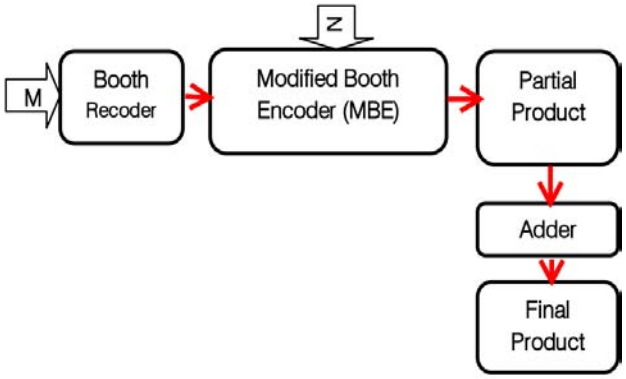


Figure 3

Table 1 : Modified Booth Encoder Logic [1]

b_3	b_2	b_1	Operation	Explanation
0	0	0	0	Add 0
0	0	1	A	Add Multiplicand
0	1	0	A	Add Multiplicand
0	1	1	2A	Two times Add Multiplicand
1	0	0	-2A	2's Complement of Multiplicand and Add 2 times.
1	0	1	-A	2's Complement of multiplicand and Add
1	1	0	-A	2's Complement of multiplicand and Add
1	1	1	0	Add 0

In this case, the multiplicand is offset one bit to the left to enter into the adder while for the low-order multiplicand position a 0 is added. Each time the partial product is shifted two bit positions to the right and the sign is extended to the left.

During each add-shift cycle, different versions of the multiplicand are added to the new partial product depends on the equation derived from the bit-pair recoding table above.

Here are some examples for understanding:

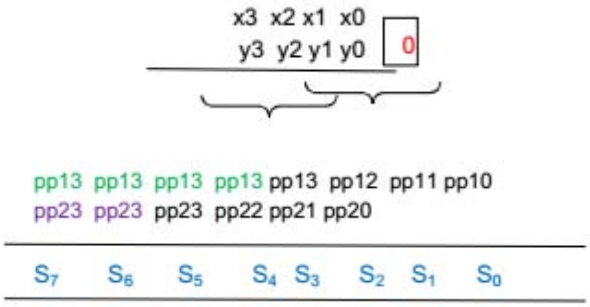


Figure 4

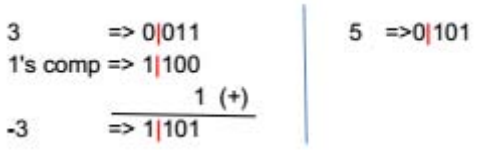
The new MBE recorder [14] is designed in accordance to the area efficient wen-chang's Modified Booth Encoder (MBE) since it is proved to be the efficient architecture on trend, and Table (1) presents the truth table of the new encoding scheme. The way of application and calculation procedure is expressed in the following examples.

For the ease of understanding, the main two different categories of signed multiplication are taken into consideration that is multiplication of a negative multiplicand and positive multiplier in example-1 and both negative multiplicand and multiplier in case of example-2 are clearly described for understanding.

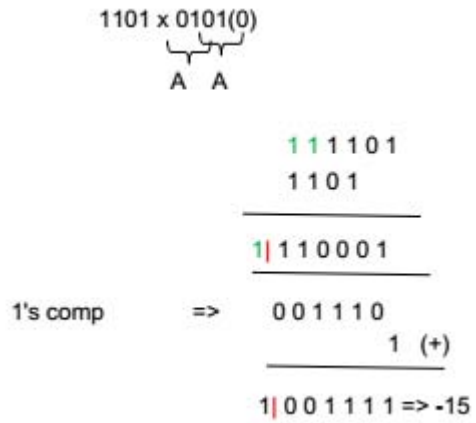
Example 1: For One negative and One positive number.

Consider -3 x 5

Step-1: binary conversion and 2's complement



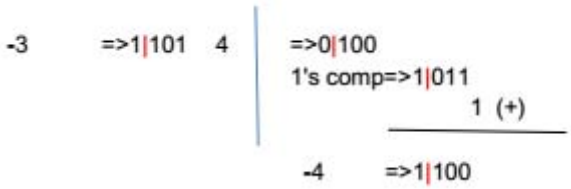
Step-2: Multiplication by Modified booth recoding



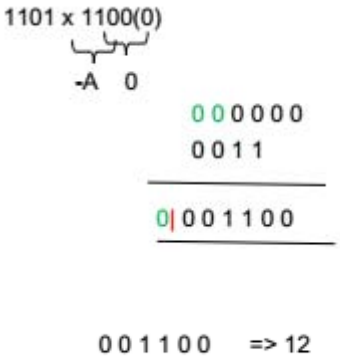
Example 2: For Both Negative Numbers.

Consider -3 x -4

Step-1: Binary conversion and 2's complement



Step-2: Multiplication by Modified booth recoding



Once the partial products are generated then the addition process is very similar to the array multiplier.

IV. Results and Analysis

The Multiplier were taken for analysis was described using structural Verilog HDL and synthesized to produce a gate level net list using two different synthesizer namely Xilinx ISE Design Suite 14.3, Altera Quartus II 12.0 with reference to Virtex7 XCV2000T-2FLG1925 and Cyclone II EP2C35F672C6 FPGA respectively. The multipliers were simulated and analyzed at different strengths such as 4 x 4, 8 x 8, 16 x16, 32 x 32 and 64 x 64 as shown below in table [2-4] .

a) Area Analysis

In FPGA based design, Area requirement of the design is proportional to logic utilization i.e in Xilinx - Number of Slice LUTs Required and in Altera its Number of Logic Elements Required. For 16 x 16 bit strength Booth Consume 20.5% lesser area than Baugh-Wooley Multiplier.

b) Delay Analysis

In FPGA based Design, EDA tools having inbuilt capability to predict the Delay of the design. In Xilinx - Timing Analyzer Tool and in Altera Time Quest Timing Analyzer Tool were used for delay analyze. Various Delay analysis shows Modified Booth has about 43% performance efficient over Baugh-Wooley.

c) Power Analysis

Power Evaluation of the design done at various levels such as Total Thermal power Dissipation (mW-milli Watt's), Core Dynamic Thermal power Dissipation (mW), core static Thermal power Dissipation (mW), I/O Thermal Power Dissipation(mW). Among the various power levels dynamic power varies with design to design it decides the efficient architecture.

Dynamic Power Requirement of the design is decided based on number of signal transition (or) activity during simulation time. Here analysis has been made using Power Play Power Analyzer from Altera. Power Analyzer required an input file of Signal Activities and Value Changed Dump (VCD) File to evaluate the power of the design. Here we have measure the signal activities count for 20 different Samples for 100ns simulation and the same sample is forced for other design also in order to evaluate the exact power difference between the design. power Analysis with powerplay analyzer tool for 4 x 4 bit shows 46.90% Modified Booth consume less than Baugh-wooley Multiplier and found consistence for all strength.

Table 2 : Area analysis using Altera Quartus-II

Multipliers Strength	Multiplier Name	No. of IOBs	Altera Cyclone II EP2C35F672C6	
			No. of Logic Elements Required	Delay (ns)
4x4	BAUGH	16	30	15.650
	BOOTH	16	28	10.173
8x8	BAUGH	32	164	36.994
	BOOTH	32	150	25.082
16x16	BAUGH	64	698	99.377
	BOOTH	64	538	42.826
32x32	BAUGH	128	2,874	325.172
	BOOTH	128	2,284	87.473
64x64	BAUGH	256	10,122	956.214
	BOOTH	256	9,542	189.886

Table 3 : Area and Delay analysis using Xilinx ISE

Multipliers Strength	Multiplier Name	No. of IOBs	Xilinx Virtex7 XCV2000T-2FLG1925	
			No. of Slice LUTs Required	Delay (ns)
4x4	BAUGH	16	20	15.91
	BOOTH	16	18	10.14
8x8	BAUGH	32	104	55.93
	BOOTH	32	96	22.15
16x16	BAUGH	64	452	191.84
	BOOTH	64	354	40.87
32x32	BAUGH	128	1851	670.46
	BOOTH	128	1595	81.19
64x64	BAUGH	256	7392	1838.32
	BOOTH	256	6480	159.28

Table 4 : Power Analysis (Time interval of 100ns with 20 different samples)

Multipliers Strength	Multiplier Name	Altera Cyclone II EP2C35F672C6				
		Number Signal Transition during simulation for 100ns	Power estimation			
			Total Thermal Power Dissipation (mW)	Core Dynamic Thermal Dissipation (mW)	Core Static Thermal power Dissipation (mW)	I/O Thermal power Dissipation (mW)
4x4	BAUGH	1857	169.92	1.13	80.12	86.67
	BOOTH	986	166.13	1.01	80.01	86.59
8x8	BAUGH	20911	223.47	4.81	80.30	138.36
	BOOTH	10291	223.39	5.28	80.30	138.30
16x16	BAUGH	498261	351.24	27.12	80.74	243.39
	BOOTH	51942	345.25	19.86	80.72	244.67
32x32	BAUGH	9606019	642.20	115.05	81.75	445.40
	BOOTH	469336	601.67	82.31	81.61	437.74
64x64	BAUGH	19212038	1302.34	331.53	83.13	887.68
	BOOTH	1877344	1278.88	360.30	83.24	836.34

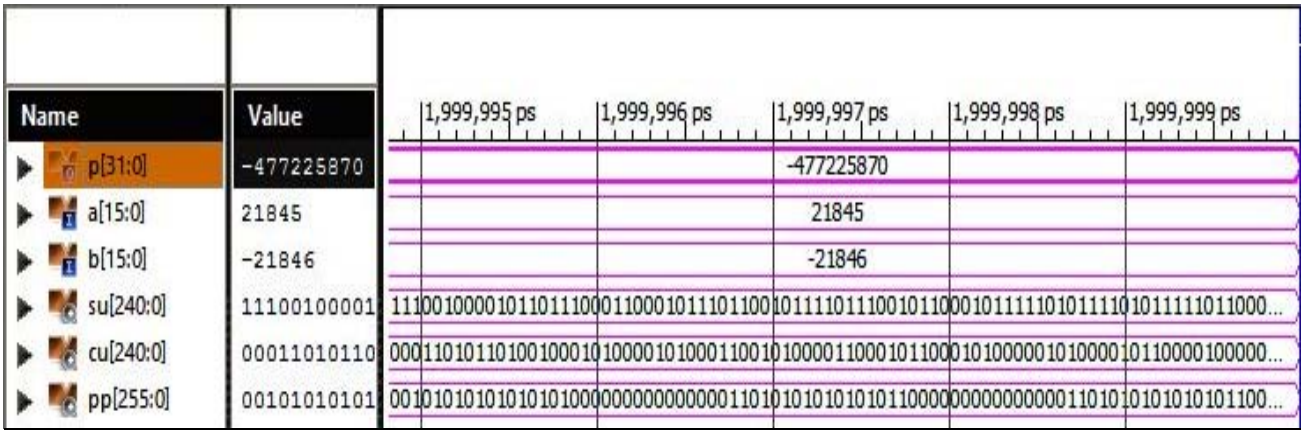


Figure 5

The Xilinx Simulation result for booth-32 x 32 bit is exhibited below in the Figure 5, and then the structure level port-map model is synthesized as Gate-level Netlist for signal Transition calculation. Modified Booth's 64 x 64 bit simulation result on Altera Quartus-II is illustrated in the Figure 6, and then synthesis summary is depicted inFigure7-11.

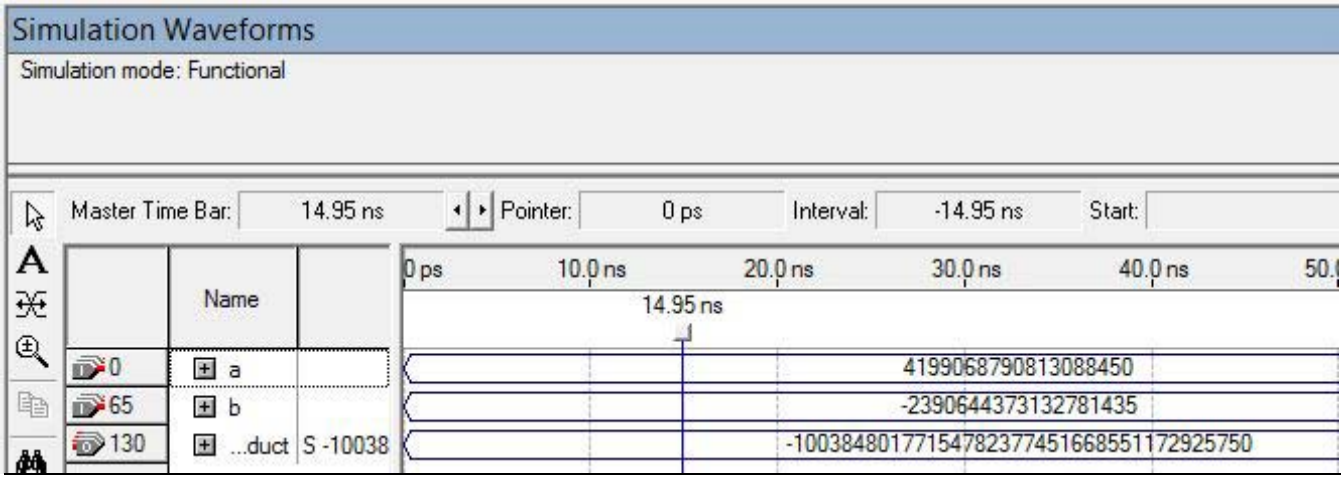


Figure 6

The Figure 7-plot graph Xilinx Area-Multiplier strength versus No. of LUT's, figure 8- Graph plot for Xilinx Delay-Multiplier strength versus delay time (ns). Figure 9-plot for Altera Area-Multiplier strength versus No. of LUT's figure and 10-Altera Delay-Multiplier strength versus delay time (ns).and finally figure 11 Graph plot for Altera Powerplay power-strength versus power dissipation (mW).

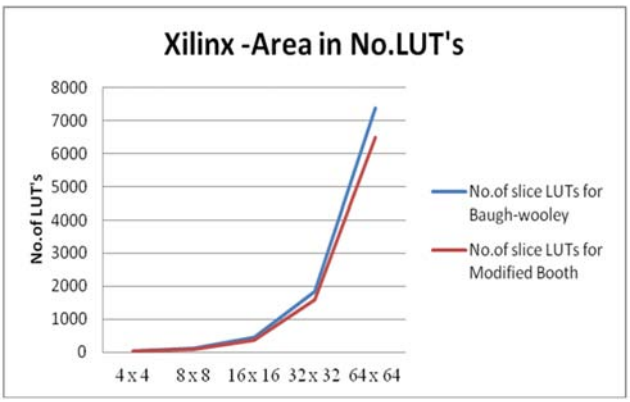


Figure 7

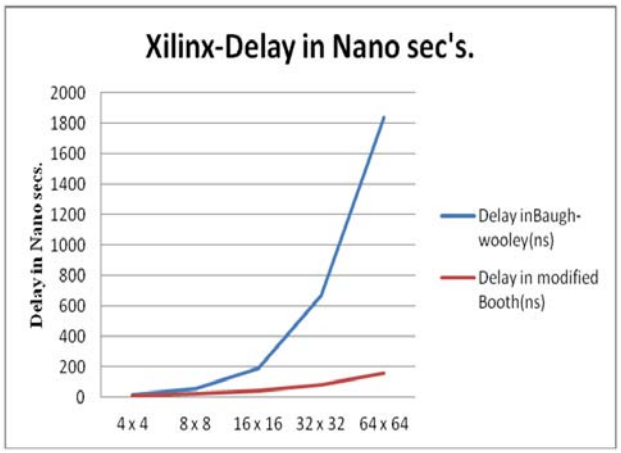


Figure 8

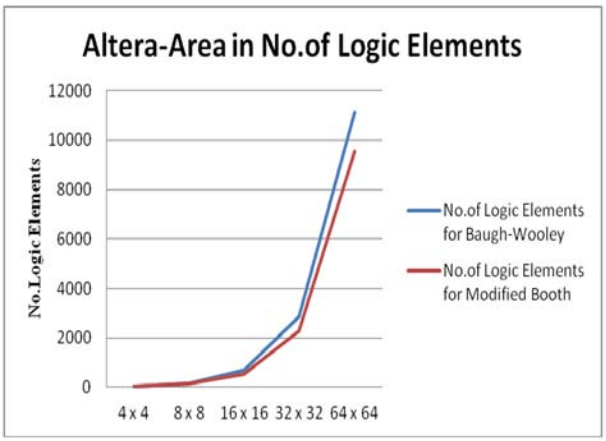


Figure 9

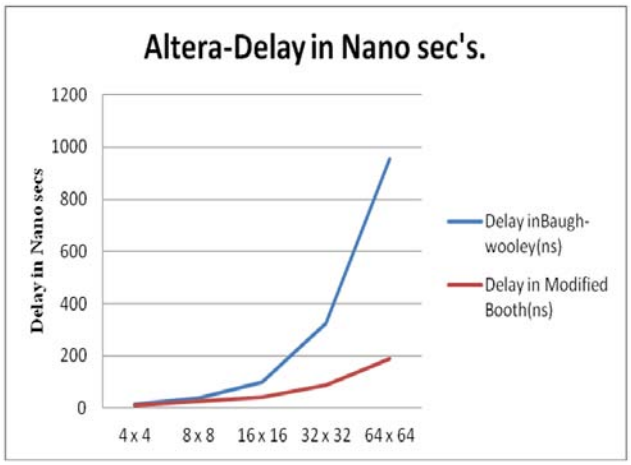


Figure 10

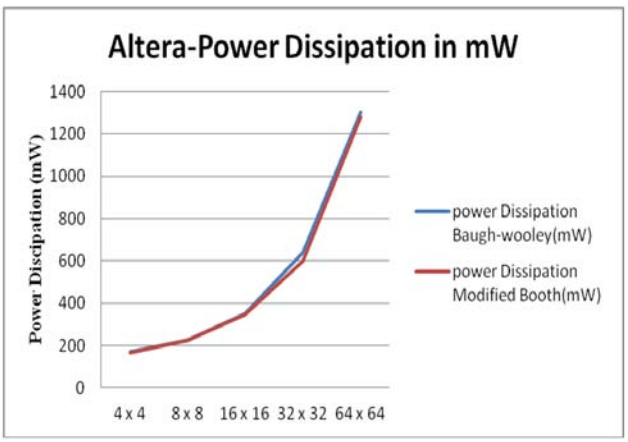


Figure 11

V. Conclusion

Our work has covered analysis of advanced signed multiplier architecture such as Baugh Wooley Multiplier and Modified Booth Encoder (MBE) Multiplier at various strength such as 4 x 4, 8 x 8, 16 x 16, 32 x 32 & 64 x 64 and the Result analysis with various VLSI Parameters like (Delay, Number of Logic Element requirements, Number of Signal Transition for particular sample input and its Power Consumption). As the Multiplier strength grows Area Curve shows a moderate difference while the delay performance of booth compared to that of Baugh wooley is approximately 4 times better(i.e,, for 32 x 32 Baugh wooley needs ~325 ns while booth complete it with ~90 ns). Modified Booth proves great result in all forms of VLSI constraints and works effectively with desired specification needed for highly reliable RNS application and for further optimization Multi-Modulo Residue architecture are advisably wise choice. Thus Signed Booth multiplier performs superior than state of art multiplier and its efficiency can be utilized for further optimization of Multi-Modulo Residue architecture for all modulus in special moduli set.

References Références Referencias

1. K. N. Vijeyakumar, Dr. V. Sumathy and S. Elango "VLSI Implementation of Area-Efficient Truncated Modified Booth Multiplier for Signal Processing Applications" The Arabian Journal for Science and Engineering, Volume. 39, No.11, 7795-7806, 2014.
2. Pramodini Mohanty "An Efficient Baugh-Wooley Architecture for both Signed & Unsigned Multiplication" International Journal of Computer Science & Engineering Technology (IJCSET),3. 2012.
3. G.W. Bewick, "Fast Multiplication: Algorithms and Implementation," Ph.D. dissertation, Stanford University, Stanford, CA, 1994.
4. R. Muralidharan and C. H. Chang, "Hard multiple generator for higher radix modulo multiplication," in Proceedings 12th International Symposium. Integrated Circuits, Singapore, 546–549, 2009.
5. A. Dandapat, S. Ghosal, P. Sarkar, D. Mukhopadhyay (2009), "A 1.2- ns16×16-Bit Binary Multiplier Using. High Speed Compressors", International Journal of Electrical, Computer, and Systems Engineering,234-239, 2009.
6. Kiat-seng yeo and Kaushik Roy, "Low-Voltage, Low-Power, VLSI Subsystems Tata MC-Graw Hill.
7. S. L. Freeny, "Special-purpose hardware for digital filtering," Proceedings, .IEEE, 63-4- 633–647 1975.
8. C. S. Wallace, "A suggestion for parallel multipliers," IEEE Transaction on Electronic and Computer, 13-1-14–17,1964.
9. O. Hasan and S. Kort, "Automated formal synthesis of Wallace tree multipliers,"in Proceedings 50th Midwest Symposium Circuits and System, 2007.
10. J. Fadavi-Ardekani, "M × N booth encoded multiplier generator using optimized Wallace trees," IEEE Transaction. on Very Large Scale Integration.(VLSI) System,1-2-120–125,1993.
11. F. Elguibaly, "A fast parallel multiplier-accumulator using the modified Booth algorithm," IEEE Transaction. Circuits System. II, Analog Digitial. Signal Process., 47-9-902–908, 2000.
12. K. Choi and M. Song, "Design of a high performance 32 × 32-bit multiplier with a novel sign select Booth encoder," in Proceedings on IEEE International. Symposium on Circuits System, 2-701–704, 2001.
13. Y. E. Kim, J. O. Yoon, K. J. Cho, J. G. Chung, S. I. Cho, and S. S. Choi, "Efficient design of modified Booth multipliers for predetermined coefficients," in Proceedings on IEEE International. Symposium on Circuits and Systems, 2717–2720, 2006.
14. W.-C. Yeh and C.-W. Jen, "High-speed booth encoded parallel multiplier design," IEEE Transactions on Computers, 49-7-.692–701, 2000.
15. J.-Y. Kang and J.-L. Gaudiot, "A simple high-speed multiplier design," IEEE Transactions on Computers ,55-10-1253–1258,2006.
16. O. Salomon, J.-M. Green, and H. Klar, "General algorithms for a simplified addition of 2's complement numbers," IEEE Journal on Solid-State Circuits,30-7-839–844, 1995.
17. E. de Angel and E. E. Swartzlander, Jr., "Low power parallel multipliers,"in Workshop VLSI Signal Process. IX, 199–208, 1996.
18. N. S. Szabo and R. I. Tanaka, Residue Arithmetic and its Application to Computer Technology. New York: McGraw-Hill, 1967.
19. M.A. Soderstrand et al., Residue Number System Arithmetic Modern Applications in Digital Signal Processing. IEEE Press 1986.
20. Paliouras and T. Stouraitis, "Novel High-Radix Residue Number System Multipliers and Adders," Proceedings IEEE International Symposium on Circuits and Systems, pp. 451-454, 1999.

This page is intentionally left blank