Global Journal of Computer Science and Technology
Software & Data Engineering
Volume 13 Issue 10 Version 1.0 Year 2013
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 0975-4172 & Print ISSN: 0975-4350

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GJCST-C Classification : *D.2.5*

Strictly as per the compliance and regulations of:

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Abstract - This paper presents a delay measurement technique using signature analysis, and a scan design for the proposed delay measurement technique to detect small-delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock Generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors. The evaluation with Rohm 0.18- m process shows that the measurement time is 67.8% reduced compared with that of the delay measurement with standard scan design on average. The area overhead is 23.4% larger than that of the delay measurement architecture using standard scan design, and the difference of the area overhead between enhanced scan design and the proposed method is 7.4% on average. The data volume is 2.2 times of that of test set for normal testing on average.

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I. Introduction

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems. If small-delay defects cannot be detected in LSI screening, the chips will behave abnormally under particular operations in certain applications, and their lifetime may become very short due to the vulnerability to the transistor aging. Therefore to keep the reliability after shipping, Enhancing the quality of the testing for the smalldelay defect detection is an urgent need. The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects.

However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. Therefore development of the embedded delay measurement technique is required. Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurements techniques. In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation. However, it has a drawback. The measurement time of the technique depends on the time for the scan operation. These days, the gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical. Noguchi *et al.* proposed the self testing scan-FF. The flip flop reduces the required number of scan operations, which makes the measurement time practical. They also proposed the area reduction technique of the self testing scan-FF. However, the area overhead of these methods is still expensive compared with the conventional scan designs. This paper presents a scan-based delay measurement technique using signature registers for small-delay defect detection.

The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging. The rest of this paper is organized as follows. In section II, preliminaries are discussed. Section III explains the proposed method. Section IV

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shows the experimental results. Finally, Section V concludes this paper.

II. Preliminaries

a) Related Works

These days, various methods for small-delay defect detection have been proposed. The path delay fault testing with a normal clock width is the most popular and is widely used. In this method, we choose the longer paths to detect the smaller cumulative delay due to the small delay distributed on the paths. The larger the cumulative delays, the higher the probability of the detection of the distributed small delay. However, the coverage of the small delay defect detection largely depends on the normal clock width, which is a problem of this method. On the other hand, to solve the problem, methods with delay fault testing using a variable clock generator have been proposed. The delay fault testing with a smaller test clock reduces the slack of the paths. Therefore the smaller delay defects which cannot be captured with the normal clock width can be captured with the appropriate smaller test clock width. Lieu*et al.* proposed a small-delay defect detection method consisting of two test phases using both a tighter test clock and a normal clock. In this method, the transition delay fault testing with a tighter test clock width which is calculated basedon the characterized delay distribution is applied in the first phase. After that, path or transition delay fault testing is applied with a normal clock width in the second phase. The quality of the method is higher than the conventional one phase test with normal clock width. Yan. proposed a delay testing scheme that identifies small-delay defects in the slack interval by comparing switching delays of a neighboring die on a wafer. In this method, a fault site is sensitized multiple times continuously with reducing the test clock width by the slack interval. The abnormal switching delays are detected by comparison with the test results in the neighboring die. Another work detects small-delay defects by analyzing the failing frequency, which is the minimum frequency that the delay fault testing fails when the path is sensitized multiple times continuously with increasing the test clock frequency. Generally, the variable clock testing requires a variable on-chip clock generator. Various variable on-chip clock generators have been proposed. In variable clock testing, the test clock frequency should be optimized to each test vector. To improve the test quality, various optimization methods of the test clock and test set have been proposed. These days, small-delay defect detection methods using on-chip delay measurement techniques have been proposed. The direct measurement of the real delay of each path of each chip screens outlier chips robustly even in the presence of process variation or the gap between real and simulation environment. It realizes higher fault coverage of small-delay defects than the simulation based ones. In addition, it can be used not only for the detection of small delay defects, but also for the debugging. Because modern chips are too huge and complex, LSI CAD tools cannot optimize the design enough. Hence, the manufactured first silicon chip usually does not meet the specification in spite of the tighter release to production (RTP) schedule.

Therefore silicon debugging and design for debugging (DFD) become much more important in modern chips. Various silicon debugging technologies and DFD methods have been proposed. On-chip delay measurement provides accurate information of the delay of inside paths for the debugging of small-delay defects. Most of the conventional works of on-chip delay measurement are classified to either a proposal of an embedded delay Fig.1.On-chip variable clock generator measurement circuit or that of a scan architecture for scan-basedon-chip delay measurement with a variable clock generator. Some works proposed embedded delay measurement circuits of modified vernier delay line (VDL). Datta *et al.* proposed the embedded delay measurement circuit with high resolution. It is the first work of an embedded measurement circuit of modified VDL to the best of our knowledge. Tsai *et al.* proposed the area efficient and noise-insensitive modified VDL with coarse and fine parts namely BIDM. Pei *et al.* also proposed the area efficient modified VDL. The feature of this method is delay range of each stage of VDL .The delay ranges increase bya factor of two gradually, which reduces the required stages. Therefore the area is smaller than Data's work. The modified VDLs achieve high resolution. However they require redundant lines to feed the input and output signals of the measured paths, which needs the compensation of the delay effect of the redundant lines. Tanabe *et al.* solved the problem by removing the delay of the redundant lines from the measured delay using some additional embedded circuits. The proposed technique is categorized to the scan-based one.

b) Variable Clock Generator

In the proposed method, the clock width should be reduced continuously by a constant interval as explained later. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator is indispensable for the proposed method. In this paper, we use the on-chip variable clock generator proposed by Noguchi. Fig. 1 illustrates the circuit.

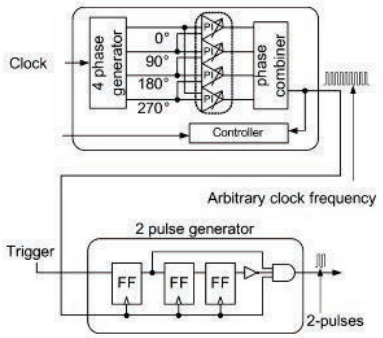

Figure 1 : On-chip Variable Clock Generator [2]

The circuit consists of the phase interpolator-based clock generator and the 2-pulse generator. The phase interpolator-based clock generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulsetest clocks with arbitrary timing in response to a trigger signal.

Some of the specification and the evaluation results are shown in Table I.

Table 1 : Specification and Measurement Result

Process	90nm CMOS
Occupied area	300 [μm] × 128 [μm]
Input clock	1.5GHz 4phase
Output clock	1GHz to 2GHz 4phase
Functions	· Frequency control · Jitter generation · Duty ratio control · Phase control
Timing (Phase) Step resolution	5.2ps (2.8°)
Step error (5 chip measured)	±1.3ps ~ ±2.4ps (±0.7° ~ ±1.3°)
Cumulative timing error (5 chip measured)	Best chip Worst chip ±5.4ps ~ ±11.2ps (±2.9° ~ ±6.3°)

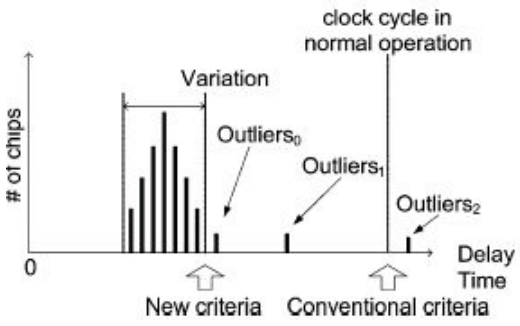

Figure 2 : Decision of test clock width based on path delay distribution obtained by chip measurement

c) Small-Delay Defect Detection with Delay Measurement of Chips

The proposed method uses the Noguchi's small-delay defect detection technique. In this technique, the test clock width for delay fault testing of each path is determined with the normal path delay distribution of each path. This strategy has already been applied to various small-delay detection techniques. But its originality is to obtain the path delay distribution with the delay measurement of the paths of the fabricated chips. Fig. 2 shows the path delay distribution of a path obtained by the delay measurement of the fabricated sample chips. The horizontal axis is measured delay. The vertical axis is the number of chips. The chips which have delay inside the range Variation are normal chips. The chips which have delay outside the range Variation, namely, are abnormal chips. The delay is the outside of the clock cycle in normal operation. Therefore it will be detected by conventional delay fault testing with the clock cycle in normal clock operation which is Conventional criteria. The delay and are within the clock cycle in normal operation. The conventional delay fault testing regards them as good chips. However because the delay is outside Variation, it will cause improper operations under particular operation in certain applications and may cause improper operations after shipping due to the effect of aging. In Noguchi's technique, the test clock cycle is set to the upper limit of the distribution of normal chips, which are new criteria. Then all the outlier chips are detected by the delay fault testing. In small technology, the path-delay distribution calculated by simulation is different from that of the fabricated chips. Therefore the quality of its strategy is higher than that of simulation based ones. Because the Noguchi's technique requires the measurement of the explicit paths, the paths should be single-path sensitizable. The aim of the technique is to screen the chips.

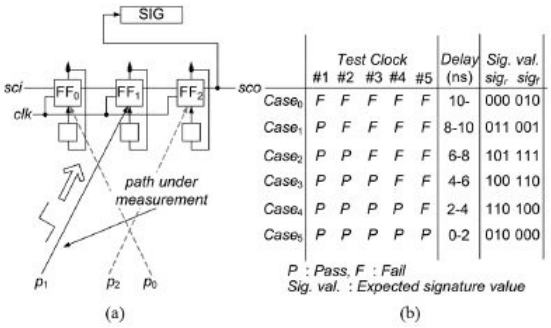

Figure 3 : Concept of proposed delay measurement. (a) Basics of proposed measurement, (b) Signature Table

Which have abnormal delay in gates or wires Therefore the test Set for the measurement should detect all the transition faults which are sensitized through single-path sensitizable paths. The proposed method is a new delay measurement technique for the small-delay defect detection technique.

III. Delay Measurement Technique using Signature Registers

This section explains the proposed measurement method. Section III-A presents the

concepts of the proposed method. Section III-B explains the implementation of the proposed method. Section III-C describes the measurement sequence. The data volume and area overhead should be realistic compared with the conventional scan designs for DFT. Section III-D explains the reduction method of the tester channel. Section III-E describes the scheme for the decision of the number of the required extra latches to keep the cost realistic. To apply the proposed method and realize short measurement time, some constraints should be put on ATPG. Section III-F explains the ATPG constraints. Section III-G describes the measurement time and data volume. Finally, Section III-H describes the test response tracing mode for finding lowest failing frequency or diagnosis with transition fault test vectors.

a) Basics

This section explains the concept of the proposed delay measurement. The target paths of the proposed method are single path sensitizable. Basically, the proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement. Fig. 3(a) shows the basics of the proposed method. This example has three flip flops, and each flip flop has the input line (bottom), the output line (upper), and the clock line. Each flip flop is connected to an extra latch. At first, we assume that each flip flop has its own extra latch. The value of each flip flop is stored in the correspondent latch, and the value of each latch can be loaded to the correspondent flip flops in arbitrary timing. In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation. It reduces the time for multiple sensitization of a path drastically. The horizontal line through these flip flops represents the scan path. The symbols and represent the scan input and output, respectively. The rectangle SIG represents the signature register using the linear feedback shift register as its basic component. The input of SIG is connected to the output of the last flip flop. More detail structures of the flip fops and the signature register are shown in Figs. 4 and 5, respectively.

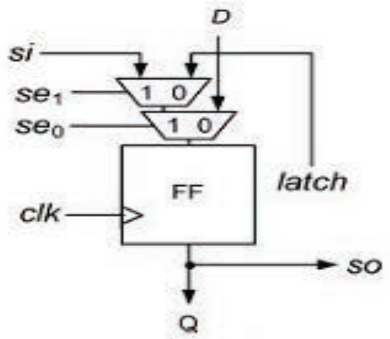

Figure 4 : Scan Flip Flops for Proposed Measurement

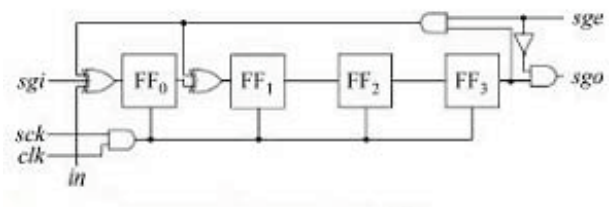

Figure 5 : Four Bit Reconfigurable Signature Register

Here, we measure the delay of. In this example, we assume that the clock width of normal operation is 10 ns, and the resolution of the delay measurement is 2 ns. First, SIG is initialized with reset operation. Second, the target path is tested continuously 5 times with the test clock reduced gradually by the resolution. The multiple clock width testing is realized by the variable clock generator explained in Section II-B. The test clock of the 1st testing (#1) is 10 ns. After the test, the test response is sent to SIG through the scan path with two clock shift out operation. The test clock of the second testing (#2) is 8 ns. Similarly, the test clock width of the third, fourth, and fifth testing's (#3, #4, #5) are the difference between 2 ns and the previous test clock width. Each test response is sent to SIG with two clocks. After the above 5 times of delay fault testing's, the signature value of SIG is retrieved. To estimate the delay, the retrieved signature value is compared with the expected signature values of the signature table. Fig. 3(b) shows the signature table in this example. The table has four columns. The first column is the cases of the measurement. The second column is the sequences of the test responses of #1–#5. The third column is the path delay value. The fourth column is the signature values of each case.

Here, and are the signature values for rising and falling transition testing's, respectively. The delay of each path is decided as more than 10, 8–10, 6–8, 4–6, 2–4, or 0–2ns, with 2ns resolution. The sequences of the test responses of the 5 times measurement are shown in Fig. 3(b). The symbols indicate the cases with path delays, more than 10, 8–10, 6–8, 4–6, 2–4, 0–2 ns, respectively. The symbols and represent the pass and fail of a testing, respectively. In case of rising transition testing, and, and in case of falling transition testing, and. The retrieved signature value is compared with the expected signature values on the table, and decides the delay value. When the number of flip flops is, clock width is, the measurement resolution is, and the continuous testing time is, the delay measurement sequence of a target path is as follows. Here, we assume that the test vector is already stored in the latches. The end point of the measured path is.

Step 1: Initializing SIG.
Step 2: Test vector is loaded from the latches.
Step 3: Test clock width is set to normal clock width.
Step 4: Test clock is applied.
Step 5: The test response is sent to SIG which is connected to the output of with clocks.
Step 6: If testing time is equal to, go to Step 7 after the signature value of SIG is retrieved, otherwise go back to Step 2 after the test clock width is updated to
Step 7: The delay value is estimated by comparing the retrieved signature value and the signature table.

b) Implementation

In this subsection, we explain the implementation of the proposed measurement system. First we explain the important components to understand the whole system. After that, the whole system is presented.

i. *Scan Flip Flop for Measurement*

Fig. 4 is the gate level description of the scan flip flop for the proposed measurement. The lines, and are the input, output, and clock lines, respectively. The line is connected to an extra latch which provides the test bit to the flip flop. The lines and are the input and output for constructing the scan path. The input is connected to of an adjacent scan flip flop or the scan input. The output is connected to of an adjacent scan flip flop or the scan output. The flip flop has two multiplexers. The lines and are the inputs of the upper multiplexer controlled by the output of the upper multiplexer and are the inputs of the bottom multiplexer controlled by When, the flip flop is in normal operation mode. When and, the flip flop is in scan operation mode. When the flip flop loads the value stored in the latch connected to the latch line.

ii. *Reconfigurable Signature Register*

The signature register for the proposed measurement requires the following functions to meet the demand of the proposed measurement.

- Capturing the test response in arbitrary timing.
- Shifting out the signature data in arbitrary timing.

Fig. 5 shows the architecture of the signature register for the proposed measurement. The length of the signature register in this example is four bit. Therefore it has four flip flops. The signature register can be configured to a shift register. The line controls the configuration. When, it works as a signature register. When, it works as a shift register.

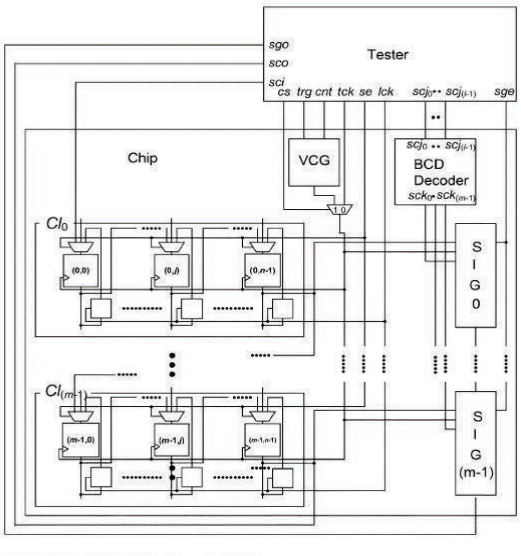

Figure 6 : Proposed Measurement System

The line is the input of the signature register. During measurement, test responses are sent to. The line is clock line. The clock line is controlled by. When, the signature register does not capture the input value. When, the signature register captures the input value synchronizing with the positive edge of. By controlling, the signature registers capture only the target test response. When, this circuit is configuring to the shift register. The input is. The output is. As explained later, the measurement system requires multiple signature registers generally. The input and output are connected to the output and the input of adjacent signature registers to construct a long shift register for sending all the signature values to the external tester.

iii. *Whole System*

Fig. 6 shows the proposed measurement system. The proposed system consists of the low cost tester and the chip with the variable clock generator (VCG) explained in Section II-B and a BCD decoder. The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flip flops and the signature registers independently. The reset operations are controlled by the tester. The low cost tester controls the whole measurement sequence. The clock frequency is slower than the functional clock. The line retrieves the signature data from the signature registers to estimate the measured delay. The line sends the test vectors to the scan input of the chip. The line gets the data of the flip flops from the scan output of the chip. In the proposed measurement sequence, is not used. However, it is used to check the flip flops or the additional latches before the measurement. The line is the clock control line. The proposed measurement uses both the slow tester clock and the fast double pulse generated by on-chip VCG. The lines elect the slow and fast clock. If is 1,

the fast clock is sent to the clock line of the components. Otherwise the slow tester clock is sent. The lines and are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of. The line controls the width of the double pulse. The line controls the scan flip flops. The line controls the latches for storing test vectors. The lines are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers. As explained later, the decoder is used to reduce the input lines for the control data of the signature registers. The is the enable signal for the signature registers. The flip flops in the chip are classified to the clusters. Here, we assume that each cluster has flip flops, and thus the number of the flip flops is. In general, the number of the flip flops of the last cluster is, where is the number of flip flops, or. The coordinate written in the flip flops indicates the location. The number is the cluster id. The number is the order in the cluster. The output of the flip flop of which is the tail flip flop of each cluster is connected to the flip flop of which is the head flip flop of. These lines construct the scan chain. The output of the tail flip flop of each cluster is connected to the input of the corresponding signature register. The path whose test response is captured by the flip flops included in is measured by. The control lines of the signature registers are connected to the BCD decoder.

c) Measurement Sequence

Here, we explain the measurement sequence. First, the measurement sequence of the paths simultaneously sensitized in a test vector is explained in Section III-C1. After that, the whole measurement sequence is explained in Section III-C2.

i. *Measurement Sequence per a Test Vector*

When the measurement system has signature registers, Paths can be measured in parallel maximally. To reduce the measurement time, we measure multiple paths simultaneously. We explain the measurement strategy using the example depicted in Fig. 7. In this example, the proposed method is applied to the circuit with six flip flops. These flip flops are classified to the two clusters and. The cluster includes, and includes. The cluster has the signature register. The cluster has the signature register. The clock line controls these flip flops. The control lines controls the capture operation of, and controls the capture operation of. The paths are sensitized simultaneously by the test vector. The test response of is captured by The expected test response is The paths and are measured by. The paths and are measured by. The combination of the two paths, one of which is selected from and, the other of which is selected from and, can be measured simultaneously.

IV. Experimental Result

In this section, we present the experimental results. The proposed method is compared with the conventional methods. The clock frequencies are the same as that of Noguchi's methods that is, the normal clock frequency is 100 MHz, and the scan clock frequency is 10 MHz the length of the signature register is 8 bit. The test set consists of test vectors which detects all single-path sensitizable transition faults. The paths sensitized by these test vectors are measured. In this evaluation, the average delay of signal propagation of the measured paths is assumed to be the half of the clock width. Usually the length of the sensitized paths for transition delay defect detection is relatively short because ATPG seeks the paths whose length is as short as possible for the cost of test generation. From this point of view, we believe that this assumption is valid. In this evaluation, the test set for the measurement is generated by podem-based ATPG algorithm, which is implemented by C++. The back track limit is 200. For the evaluation, relatively larger ISCAS'89 benchmark circuits are used. The measurement time using the proposed scan design and standard scan design is calculated by the (1) and (3), respectively. The results of area are obtained by synthesis with Synopsys design compiler using Rohm 0.18 m process. The data volume of these methods is calculated by the (4) and (5), respectively. In this evaluation, area overhead, area overhead including the area of VCG, and the routing overhead are defined as follows. , where the area of the circuits is implemented the evaluated method except VCG, and is the area of the non-scan circuit except clock generator. Where the area of the circuits is implemented the evaluated method including VCG. The area of VCG is obtained from the paper. Note that, and include the area of the wires. , where and are the routing area of the evaluated circuit and non-scan circuit, respectively. The reduction ratio of measurement time is defined as, where and is the measurement time of the evaluated method and that of standard scan, respectively. The increase ratio of the data volume is defined as, where and is the data volume of the evaluated method and that of standard scan, respectively.

a) Comparison with Conventional Scan-Based Measurement

Tsig=time required for {whole scan-in + double pulse + SIG data

Table 1 : Measurement Time

Circuit	EMB	T_{sig}	R_1
S5378	635.4	181.2	71.5
S9234	703.1	135.5	80.7
S38584	4025	1011.5	72.6
Ave			74

Table 2 : Comparison with Delay Measurement using Embedded Delay Measurement Circuit

Circuit	EMB	SIG	R
S5378	46.7	181.2	3.9
S9234	164.5	135.5	0.8
Ave			2.3

The result of the measurement time is shown in Table III. Here, we show the result when and, respectively. The sub columns (ms) and (ms) are the measurement time of standard scan design and the proposed method, respectively. According to the result, when and are 67.8% and 71.9%, respectively. The reduction ratio when is 4.1% higher than when. It is because the impact of the time for scan-in operation of each test vector on the measurement time decreases as increases.

V. Conclusion

The proposals of this paper are as follows:

- The proposal of the delay measurement method using signature analysis and variable clock generator.
- The proposal of a scan design for the delay measurement of internal paths of SoC.

The first proposal can be applied not only SoC but also field programmable gate array (FPGA). Because the process of FPGA is getting extraordinary smaller these days, the small delay defect becomes serious problem in FPGA, too. In this meaning, the application of the proposed method to FPGA is also useful. A future work is the low cost application of the proposed measurement to FPGA. When we measure short paths the measurement error can increase for the IR drop induced by higher test clock frequency. It can reduce the test quality. Another future work is the reduction and the avoidance of the measurement error caused by the IR drop.

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