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Architecture and Hardware Solutions Symbolic Information Processing

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Abstract - The failure of some national projects AXES to expected results. According to experts one of the reasons is the lack of adequate theoretical apparatus for generating high-branching processes, unjustified detraction of opportunities enumerative models representative of AXES, which have their own laws paralleling computing, can not be reduced to algorithmic rules. This fact determines the need to develop innovative approaches to problem solving and organization of AXES interrelated levels of system design symbolic computation, from the linguistic level to the appropriate software and appropriate hardware level.

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Architecture and Hardware Solutions Symbolic Information Processing

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I. Introduction

According to estimates of scientific authority in the modern computer technology , one of the leading trends of development of computer technology is the creation of homogeneous processing devices and information storage for the supercomputer and multiprocessor systems (MPS), focused on the implementation of parallel computing [1]. It is known that the main object processing symbolic information stands in various models of representation [2]. In this regard, the strategic relevance for the design supercomputers IBM and (MPS) are the questions of creating methods, architectures, and circuit design alternative for intelligent processing of information. The importance of models and techniques for intelligent processing of information associated with the emergence and rapid development of artificial intelligence (AI), in which we study a model of knowledge representation and processing. The main substantive aspects of AI problems and processes of AXES in them are the following. First, the basic format of knowledge representation and processing is currently a character format, essentially having a higher level of organization of parallel computations than the number format. Second, efficient processing of knowledge - is the realization of constructive processes of branching for multiple data with a variety of parameters, the dynamic variation of the structure and size of the data instances, by default require non-standard multi-processor architecture tour.

Originating in the 80th years of XX century as an independent branch of computer science, computer systems have traditionally included in the AXES interdepartmental, national and international scientific and technical programs and projects to create computer systems and new generation, that determines the strategic importance of research and processing of symbolic computation knowledge. Notable historical examples of such programs and projects are the West-European project ESPRIT, an American project ALVEY, Japanese project to create the fifth-generation machines (1982-1991) And the Japanese project to create a computer with a "fluid intelligence", the Russian project to create a supercomputer "Elbrus", etc. strategic importance to the problems of AXES gives a constant interest defense ministers of key countries, linking national security with the advanced development of parallel computing systems based on non-traditional (non-von Neumann) architecture.

Some national projects AXES did not lead to the expected results of my. According to experts one of the reasons is the lack of an adequate theoretical apparatus for generating high-branching processes, unjustified disparagement opportunities enumerative models representative of AXES, which have their own laws parallel computing, can not be reduced to algorithmic rules. This circumstance determines the need to develop fundamentally new approaches to solving problems of AXES and the organization of interrelated levels of engineering systems, symbolic computation, from the linguistic level to the appropriate software and hardware level.

II. Methods of Managing the Processing of Symbolic Information

The tasks of AXES with the elements of intelligent computing are understood as a search problem and the parallel generation of new states from the available set of initial states and a set of mathematical rules that are permissive nature of the execution, i.e. based on enumerative systems. On one side, the term "permissive rules" enumerative system is specified in accordance with the agreement of Post as an alternative to firing rules. For this reason, many treatment options, and constructive processes enumerative branching system simulates the algorithmic

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system with a serial product of branching processes in a linear space-time. Other hand, enumerative systems, the term "permissive rules" can be specified as equal to the firing rules [4, 5]. The consequence of this method of refinement is a parallel implementation of branching processes with a structural mechanism for the generation of new states permanently to the desired number of copies of copies of data.

Nevertheless, the implementation of parallel computations on an equal basis associated with the dynamic generation of specific objects that provide a quantitative assessment of the branching process along different trajectories computation. Static methods parallelism inherent in processing numerical information, based on the placement of a dynamically modifiable set of branching processes in homogeneous computing modules. For problems of AXES such methods are not applicable in due to the lack of reliable information about the structure of a graph problem AXES. Obscurity graph structure calculations also leads to the substitution of enumerative system on its equivalent algorithmic model and unproductive expenditures of time series-return mechanism of generation of new states in the search graph [6]. These differences between numeric and symbolic computations on a theoretical level, make it necessary to use different system architecture solutions, and micro-level implementation of the A subsystem of parallel symbolic computation.

A subsystem at the level of implementation of parallel computing are three control method of the computing process, consisting of many interacting flows: flow control commands (the traditional von Neumann method), flow control, flow control requirements (switching).

Flow control commands have limited opportunities to engage in branching processes, AXES, as additional time required for the dynamic placement costs between sub-cores of the system and loss of time for data synchronization. At the same time with increasing number of processor cores total load factor of the system is significantly reduced and the problems of real complexity is reduced to 5-10% [3]. These values do not allow us to consider how the flow control commands as a promising option for the computer systems AXES

For parallel computing is a potentially attractive model calculations, flow control [3]. According to this model, any computational process is directed graph of data flow. In this graph nodes (vertices) are computer operators, and the arcs of the graph moving special data structures – Tokens. Special structures (tokens) contain field offices, describing the formats and types of operands. The coincidence of the operands to the format and automatically determines the type of command being executed, and its readiness to perform. Refusal of addressing memory cells and the transition to management through conformity the various data fields token characterized the fundamental difference between computers of AXES from the machines with the von Neumann architecture for A subsystem level. The detection of all operands relating to the common vertex of the graph is executed by named tops is an indication of initialization and computation processing unit for the given tops. Such principle of the manage eliminates the problem of synchronization and racing flows, provides an asynchronous data flow promotion by pipelined to the ring of computers that control the flow of data. Composition operators computing, communications between nodes in a graph are defined in advance at the stage of writing the program, thereby setting the graph structure. Computers Architecture Data Flow Implement the direct execution of the graph. It is provides parallelism of computing processes, given program, and excludes the conflict situations in these. The main feature of the model calculations, flow control, command execution is not on the counter, and when ready input operands for the current nodes of the graph. Execution of this Rule leads to an asynchronous execution of multiple commands at the nodes of the graph, which resulted in its input from the arcs are absorbed, and the output arcs are generated by the results of computations in a node.

This way, parallel computing model on the data flow using a limiting parallelism peculiar task that meets the requirements of the tasks of the AXES in the generation of high-branching processes with varying duration of execution. Another feature of the competitive method and models of flow control is to use a of homogeneous set of devices on an equal basis, that provides the maximization of load devices in the asynchronous command execution on parallel graph computation, At the same time known the data flow machines (MIT SDA, MDFM, MIT TTDA (England), LAU System (France), NEC Image Pipelined Processor (Japan), and others) are still oriented to the processing of numerical information, which is characterized by an explicit task graph computations In contrast, the AXES the task in most cases are not finished making a graph that defines the limitations of direct accepts of the method of flow control.

Flow control requirements is a hybrid variant control that is based on the union of a sequence of commands in a single unit with a control in its flow control and flow control between blocks of commands. In essence, task is described poorly connected graph macro level (block commands) having a low rate of exchange flows between macro level.

Table 1: Ways to control sub system level

	Flow control commands	Data flow control	Flow control requirements
description	The usual execution of the operators at their place of in the control system	"Greedy" execution of all operators for which all operands are available	"Lazy" execution of the operators, without which there can be the results of the further calculations
advantages and	Full control Easy to realization of complex data structures and control structures	The high degree of parallelism high performance	Execution only the necessary operators The independence of computing
disadvantages	low efficiency complexity programming	Complexity of control data structures Costs of unnecessary storage resources on the operands complexity of control	Time costs for the transfer of markers The complexity of public access to the structures of local representation

III. Functional Nodes and Circuit Solutions for Ibm Axis

The known of hardware solutions can be classified as AXES in their relation to micro-level hardware solutions (circuit design implementation), A subsystem (structural and functional organization), and systemic levels (a common system architecture AXES).

At the micro level we are talking about the functional nodes, blocks, and device-properties of that support basic operations, elements of the programming language in their simplest form. On the one hand, these functional units have a rigid specialization and poorly suited for general-purpose microprocessors with software control. On the other hand, commonality of processes manipulation of symbols as with abstract images, belonging to the basic pattern of thinking, "condition-action" allow us to consider these functional units as the basis for computer AXES . Availability and use of abstract computing systems (machines) for manipulating the symbols will lead to the formation of self-class operating devices with non-traditional organization extend the instruction set of modern microprocessors. Digital Converters character-oriented branching symbolic computation and the generation of a set of symbolic structures (form image shape), ultimately, justify the existence of the justification of individual devices, high-performance machines and systems that process symbolic information and knowledge, as opposed to parallel processing of numeric data and numeric computer IBM.

As a promising technical solutions for computer systems AXES level devices and functional units [1, 3] the leading scientists in the field of view Tues hardware blocks (**Table 2**) for standard operations of AXES. Continue to comment on possible hardware units for the axis and branching of computational processes.

Table2 : AXES operations circuitry-level realization

AXES operations	hardware blocks
Calling functions recursion	hardware stacks register window
typing of data	Operating register-memory tagging of memory The apparatus of parallel testing tags
sorting	VLSI-graders
Pattern matching, identification	finite state machines associative memory device matrix Converters
Modification of the fragments of character structure, reconfiguration	associative memory device character tasovateli The positional shift memory
garbage Collection	Multifunctional VLSI-graders
handling multiple response	Distributed hierarchical arbiters
Binary substitution character data	Iterative schemes for processing unitary codes

Hardware stacks, and methods for quick access to the stacks are designed to speed up function calls. This is especially useful for functional paradigm of AXES and the family of programming languages LISP. Quick operations with the stack are also useful in the implementation of Prolog. When backtracking made numerous write operations on the stack and reading from the stack.

The current stage of development of the functional units of AXES involves the use of new abstract data structures (Table 1), such as deck. To control the pointer on the group of available vertices:

Another circuitry organization associated with the creation of hybrid structures to store and access items on a stack-based organization, complemented by:

1. The reconfiguration of the stack to the associative

structure with a parallel search and access.
2. Reconfiguration of the stack in a hierarchical structure of the shear to jump to the "deep" elements of the stack.

The following non-standard functional unit intended for computer IBM AXES is tagged memory. In conventional computer IBM Von Neumann type does not distinguish between data and program, which are stored as binary strings of fixed length. Semantics of the data determines only manipulated by the program rather than the actual contents of memory, which are stored as binary strings of fixed length. Semantics of the data determines only manipulated by the program rather than the actual contents of memory. In contrast, involves a self-sufficient representation tagged representation at all levels of memory. Currently, tagging- a powerful mechanism and hardware-software tool data typing, management calculations. The most significant use of tagged memory associated with the model calculations, flow control, and machines and data streams (first of all Manchester Data Flow Machine [3]).

The most common method of hardware realization of data tagging is to add a few bits of each word, determine its type. Check the type of data in the process can be supported by additional hardware, first of all associative memory, and perform the selection of priorities and amputation unpromising branches in the graph algorithms. A distinctive feature of tagging is the task type the command being executed. Special structures (tokens) contain field offices, describing the sizes and types of operands. The coincidence of the operands by size and type of data fields in memory command automatically determines the type of command being executed. Refusal of addressing memory cells and the transition to management through compliance data fields characterizes the fundamental difference between computers AXES from the machines with the Von Neumann architecture.

The third major operation AXES - hardware support for pattern matching. Analysis of empirical data shows, Up to 90% of the time of the enumerative production system (PS) in expert systems can be spent on the process of mapping, iterative nature of the bearing. In such a way hardware realization of this operation leads to more efficient generation of branching processes and the character generating a set of candidates solutions to common principles.

Hardware processing blocks unitary binary codes. Finally, a distinguishing feature of the processes and objectives AXES is to replace character-format data unweighted binary code, in particular in the problems of searching, comparing, and comparison, identification of character data and other operations of the higher forms of computing. Such codes were named as the unweighted unitary codes, they are characterized by the possibility of applying logic and arithmetic operations, and specific processing is not dependent on the size of the bit lengths of codes. Typical examples are the functional units of digital compressors, comparators, code converters. These sites, along with high-speed distributed by the arbitrators, are the basis of responses of multiple processing units.

Character shuffle for problems-axis is not sufficient to investigate the organization of branching in symbolic computation is the use of switching converters Data, oriented on structural change in the relations between the elements. Switching converters information regarding the functional units of numerical processing is not widely used, while symbolic calculations are based structural transformation of local or global. They are associated with dynamic changes in the computation of relations of subordination or repetition of elements of symbolic structures. Structural reforms could be considered as the composition of the reconfiguration of the data structures and inter-element rearrangements controlled in these structures.

Hardware support for this operation seems justified to use the matrix and Hypercube organizations operating parts to create two-and multi-operand switching shuffle - Switching Networks Kautsa, Stone, manipulators Fan, banyan network, shuffle register with cubes of memory [3].

IV. Conclusion

The current stage of development of computer systems, IBM AXES has a short but vivid history. It is characterized by the accumulation of quantitative theoretical and hardware and software organization of symbolic computing and knowledge processing. Intellectualization of calculations, i.e. transition from data processing to knowledge processing systems in the near future will lead to massive use of computer and telecommunications equipment to enhance the intellectual capabilities of man. The basis of a new class of computing, process-oriented analysis, understanding and synthesis of new knowledge will make their own circuit solutions, based on the basic elements of the future - the optics. Optical components and functional units will ask a variety of data due to reconfiguration and compression, as well as to parallel processing on non-specific operations, while the spatial reconfiguration of the elements of the matrix, and associative processing fragments of characters in a smart storage devices.

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