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## FAXY: Fault Aware Routing Algorithm Based On XY Algorithm for Network on Chip

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*Abstract* - The performance of Network-on-Chip (NoC) largely depends on the underlying routing techniques. In this paper we present and evaluate a Fault aware routing algorithm scheme called FAXY based on XY routing algorithm. The simulation results show the effectiveness of FAXY by comparing it with XY routing schemes under different traffic patterns. Simulation results depict that the proposed routing algorithm is able to route packet even in the case of faulty links or switches in the NoC. Moreover, simulation results demonstrate the advantage of FAXY routing algorithm in terms of average packet latency, packet loss rate compared with XY routing algorithm in the presence of permanent faults. For the proposed algorithm, it can get much less average packet latency (10%) and lead to less than average 15% packet loss rate.

Keywords : network on chip, routing algorithm, fault aware. GJCST-F Classification : C.2.2



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# FAXY: Fault Aware Routing Algorithm Based On XY Algorithm for Network on Chip

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Abstract - The performance of Network-on-Chip (NoC) largely depends on the underlying routing techniques. In this paper we present and evaluate a Fault aware routing algorithm scheme called FAXY based on XY routing algorithm. The simulation results show the effectiveness of FAXY by comparing it with XY routing schemes under different traffic patterns. Simulation results depict that the proposed routing algorithm is able to route packet even in the case of faulty links or switches in the NoC. Moreover, simulation results demonstrate the advantage of FAXY routing algorithm in terms of average packet latency, packet loss rate compared with XY routing algorithm in the presence of permanent faults. For the proposed algorithm, it can get much less average packet latency (10%) and lead to less than average 15% packet loss rate.

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#### I. INTRODUCTION

lavered architecture called Network on Chip(NoC) [1] has been proposed for global communication in complex SoCs to meet the performance requirements. In NoC each core is connected to switch by a network interface.Cores communication with each other by sending packets via a path consisting of a series of switches and inter switch links. Fig. 1 shows an abstract view of a NOC in this architecture. As shown, each tile is composed of a resource(R) and a switch or router(S). The router is connected to the four neighboring tiles and its local resource via channels. Each channel consists of two directional point-to-point links between two routers or arouter and a local resource [2, 3].

The problem of defining communication protocols for these NoCs is not an easy matter since the resources used in traditional networks are not available on-chip. The communication in NoCs takes place via data packets, which are delivered between the communicating components.

The paths the packets are routed through the network are determined by the routing algorithm. Communication and performance of the entire system are significantly affected by the routing algorithm [4].The performance of NoC largely depends on the underlying



*Fig. 1:* The typical structure of a 4\*4 NoC

routing technique, which chooses a path for a packet and decides the routing behavior of the switches. Routing algorithms can be generally classified into two types: deterministic and adaptive. In deterministic routing, the path is completely determined by the source and the destination address. On the other hand, a routing technique is called adaptive if, given a source and a destination address; the path taken by a particular packet depends on dynamic network conditions (e.g. congested links due to traffic variability). One main advantage of using deterministic routing is its simplicity in terms of routers design. Because of the simplified logic, the deterministic routing provides low routing latency. In this paper we present and evaluate a Fault aware routing scheme called FAXY which a packet first traverses along x dimension and then along the y dimension. The proposed routing algorithm is able to route packet even in the case of faulty links or switches in the NoC. Simulation results demonstrate the advantage of FAXY in terms of average packet latency, packet loss rate compared with XY routing algorithm in the presence of permanent faults. FAXY can get much less average packet latency and lead to less than average 15% packet loss rate.

#### II. RELATED WORK

The idea of NoC is derived from large-scale computer networks and distributed computing. However, the routing techniques for NoC have some unique design considerations besides low latency and high throughput. Due to tight constraints on memory and computing resources, the routing techniques for

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NoC should be reasonably simple [5]. Several previous works have investigated different routing algorithms that are tolerant to permanent and/or temporary errors. In order to ensure successful message transmission through the network, several copies of the same packet may be sent on the network links [7]. Similarly, probabilistic flooding algorithms can be employed to flood packets to the entire network, which will finally reach to the destination [8]. These techniques increase network load and may create congestion when the heavily loaded. Different deterministic network is routing algorithms have been proposed to detour the faulty link(s) in the case of permanent faults [9]. Recently, a fault tolerant routing algorithm was proposed to avoid routing on the faulty links [10]. In this paper, we present a fault-aware dynamic routing algorithm for NoC applications. Our algorithm has the ability to locate the faulty links to avoid them in order to increase the overall network throughput and prevent packet losses.

#### III. PROPOSED ROUTING ALGORITHM

In proposed routing algorithm, a new faultaware routing algorithm based on XY routing, namely fault-aware XY (FAXY), is used as a representative of deterministic routing scheme because of its simplicity and wide popularity. Obviously, XY routing is a minimal path routing algorithm and is free of deadlock and live lock [11]. As shown in Fig.3, With FAXY routing, a packet first traverses along X dimension and then along the Y dimension. When a packet traverses along the X dimension and a link is masked because permanent fault, its traverses along Y dimension in order to increase the overall network throughput and prevent packet losses. The mask is used in order to increase the overall network throughput and prevent packet losses.Our algorithm incorporates the acknowledgment signal to reroute the packets around faulty links [12].

| FA-XY Routing Algorithm (Source, Destination, SwitchAddress) {  |
|---|
| Compute destS, destRow, destCol, switchRow, switchCol From Source, Destination and SwitchAddress  |
| If (destS == switchAddr) { Send Flit to Current Switch (local Node) and Exit } else if (destRow == switchRow) { If (destRow == switchRow) { If (destCol < switchCol) { Send Flit to Left Switch is not Mask) } else if (destCol > switchCol) { If (Physical Link connected to Right Switch is not Mask) { Send Flit to Right Switch } } |
| <ul> <li>} else if (destRow &lt; switchRow) {         If (Physical Link connected to Top Switch is not Mask) {             Send Fiit to Top Switch;         } else if (destCol-s switchCol) {                  If (Physical Link connected to Right Switch is not Mask)                       Send Fiit to Right Switch;</li></ul>      |
| <ul> <li>} else if (destRow &gt; switchRow) {         if (Physical Link connected to Bottom Switch is not Mask){             Send Flit to Bottom Switch;         } else if (destCol&gt; switchCol) {</li> </ul>   |
| If (Physical Link connected to Right Switch is not Mask)<br>Send Filt to Right Switch;<br>} else if (Physical Link connected to Left Switch is not Mask)<br>Send Filt to Left Switch;<br>}<br>}   |

Fig.2: Pseudo code of FA-XY routing algorithm

#### IV. EXPERIMENTAL RESULTS

In order to evaluate the FAXY routing algorithm, developed a Java based simulator, namely we gpNoCsim [13]. We simulate several square mesh networks with XY and FAXY routing algorithms. The efficiency of each type of routing is evaluated through latency, throughput and average packet loss percent curves. Each simulation is run for a warm-up period of 10000 cycles. Thereafter, performance data are collected after 100,000 packets are sent. The network size during simulation is fixed to be 6\*6 tiles. All of the input ports have a FIFO size of 5 flits. Fig.3 shows the network throughput and Fig.4 shows switch throughput, respectively. As shown in Fig. 3 and Fig.4, FAXY routing performs better than XY routing algorithm under different fault percent schemes. The fault percent is the number of faulty switches of network that has one link with permanent fault. The packet injection rate (i.e., the number of packets injected to the network per cycle) is fixed to 150 (packets/cycle).







*Fig.4*: Switch throughput for XY and FAXY routing algorithms

As in previous work [3, 6], the performance of the routing scheme is evaluated through latencythroughput curves. For a given packet injection rate, a simulation is conducted to evaluate the average packet latency. It is assumed that the packet latency is the duration from the time when the first flit is created at the source core, to the time when the last flit is delivered to the destination core. For each simulation, the packet latencies are averaged over 50,000 packets. Latencies are not collected for the first 5,000 cycles to allow the network to stabilize. It is assumed that the packets have a fixed length of 5 flits and the buffer size of input channels is 5 flits. As shown in Fig.5, FAXY routing performs better than XY routing algorithm. FAXY routing algorithm is able to achieve a lower packet latency rate than XY for the same traffic pattern and the injection rate (10%).



*Fig.5 :* Average packet latency for XY and FAXY routing algorithms

Fig.6, show the average packet loss rate. As shown in Fig.6, FAXY can achieve average 15% less packet loss rate. Similar to other work in the literature, we assume that the packet loss rate is percent of the packet is created and do not received in the destination node.



*Fig.6*: Average packet loss rate for XY and FAXY routing algorithms

### v. Conclusion

In this paper, we presented a new approach for fault aware routing algorithms on NoC, namely FAXY routing. We investigated the effect of permanent errors, and packet injection rates on the performance of our algorithm.Simulation results demonstrated the advantage of our routing algorithm in terms of packet loss percent and latency compared to XY routing algorithms in the presence of permanent faults. Our algorithm can achieve average 10% less latency and average 15% less packet loss rate.

#### **REFERENCES REFERENCES REFERENCIAS**

- 1. L.Benini and G.D.Micheli, "Networks on chips: a new SOC paradigm", IEEE computer, 35:70-78, Jan 2002.
- J.Henkel, W.Wolf, and S.Chakradhar,"On-chip networks: A scalable, communication-centric embedded system design paradigm", VLSI Design, pp.845-851, India, 2004.
- 3. J.Hu and R.Marculescu, "DyAD Smart routing for networks-on-chip," DAC, pp. 260-263, USA, 2004.
- T.Schonwald, J.Zimmermann, O.Bringmann, "Fully Adaptive Fault-Tolerant Routing Algorithm for Network-on-chip Architectures",10th Euromicro Conference on Digital System Design Architectures, Methods and Tools (DSD 2007).
- 5. T.T.Ye, L.Benini, and G. De Micheli, "Packetization and routing analysis of on-chip multiprocessor networks," Journal of Systems Architecture, vol. 50, pp. 81-104, 2004.
- 6. G.M.Chiu, "The odd-even turn model for adaptive routing", IEEE Transactions on Parallel and Distributed Systems, 2000, vol.11, pp. 729 38.
- 7. S.Manolache, P.Eles, and Z.Peng, "Fault and energyaware communication mapping with guaranteed latency for applications implemented on noc", in Proceedings of IEEE/ACM Design Automation Conference, DAC, 2005, pp. 266-269.
- M.Pirretti, G. Link, R. Brooks, N.Vijaykrishnan, M.Kandemir, and M. Irwin, "Fault tolerant algorithms for network-on-chip interconnect", in Proceedings of IEEE Computer society Annual Symposium on VLSI, 2004, pp. 46-51.
- 9. D. Greenfield, A.Banerjee, J.-G.Lee, and S.Moore," Implications of rent's rule for noc design fault-tolerance", Proceedings and its in of International Symposium on Networks-on-Chip. 2007, pp. 283-294.
- 10.M.Ali, M.Welzl, and S.Hessler, "A fault tolerant mechanism for handling permanent and transient failures in a network on chip", in Proceedings of International Conference on Information Technology, ITNG, 2007, pp. 1027-1032.
- 11.L.M.Ni and P.K.Mckinley, "A survey of wormhole routing techniques in direct networks", IEEE Int, Conference on Computer, 26:62-76, Feb. 1993.

- 12. A.Hosseini, T.Ragheb, Y.Massoud,"A Fault-Aware Dynamic Routing Algorithm for on-Chip-Networks", IEEE, 2008.
- 13. H.Hossain, M.Ahmed, A.Al-Nayeem, "GPNocSim-A General Purpose Simulator for Network-onchip", Dhaka, Bangladesh, ICICT-2007.