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Mimicking biological neurons with a nanoscale ferroelectric transistor†

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Neuron is the basic computing unit in brain-inspired neural networks. Although a multitude of excellent artificial neurons realized with conventional transistors have been proposed, they might not be energy and area efficient in large-scale networks. The recent discovery of ferroelectricity in hafnium oxide (HfO_2) and the related switching phenomena at the nanoscale might provide a solution. This study employs the newly reported accumulative polarization reversal in nanoscale HfO_2-based ferroelectric field-effect tran-sistors (FeFETs) to implement two key neuronal dynamics: the integration of action potentials and the subsequent firing according to the biologically plausible all-or-nothing law. We show that by carefully shaping electrical excitations based on the particular nucleation-limited switching kinetics of the ferro-electric layer further neuronal behaviors can be emulated, such as firing activity tuning, arbitrary refractory period and the leaky effect. Finally, we discuss the advantages of an FeFET-based neuron, highlighting its transferability to advanced scaling technologies and the beneficial impact it may have in reducing the complexity of neuromorphic circuits.

1. Introduction

The conventional von Neumann computer architectures might prove highly inefficient in the near future, mainly due to the prohibitive time and power consumption in transferring an immense amount of data between the processor and the memory.[1] Neuromorphic computing emerges as an appealing alternative, inspired by the low-power operation of the human brain.[2] The basic computing elements in such an architecture are neurons, which are massively interconnected to each other by plastic synapses.

In recent years, much effort has been directed in developing artificial synapses using emerging nonvolatile memory devices, with the aim of building dense crossbar synaptic arrays.[3] Such arrays, coupled with artificial neurons realized in complementary metal–oxide–semiconductor (CMOS) technology, as depicted in Fig. 1, are recognized to be one possible path to building energy and area efficient neuromorphic systems.[4–7] However, the CMOS neurons, even their simplest realizations (such as Axon-Hillock neuron[8] in Fig. 1(b)) often comprise a large capacitor (to emulate the integration of post-synaptic potentials) and several transistors (for amplification, threshold and firing functions). Any further attempt of modeling additional neuronal dynamics (*e.g.* spike-frequency adaptation, refractory period, *etc.*) or lowering the power consumption results in a drastic increase in the number of transistors.[9] Therefore, to map more than 10^{10} neurons present in the human brain[10] in a compact and low-power hardware realization, other electronic elements might be more suitable than pure CMOS neurons. Recently, several proposals in this regard have been suggested, which usually exploit some sort of accumulative switching and/or transient and oscillatory behavior in nanoscale memory devices.[11–16]

Ferroelectric materials have been newly recognized as an attractive framework for alternative devices and unconventional computing. Based on the voltage-controllable polarization reversal, memristive behavior in a ferroelectric tunnel junction (FTJ) has been demonstrated[17] and biological learning rules, such as spike-timing dependent plasticity, have been implemented.[18] In this study, we explored the feasibility of a nanoscale ferroelectric field-effect transistor (FeFET) to electrically mimic the biological neuron. An FeFET resembles the conventional transistor, with the exception of having a ferroelectric material in the gate stack, capable of modulating the transistor conductivity by its spontaneous polarization charge. FeFETs have been under intense study for nonvolatile memory applications,[19,20] which has lately been intensified after the discovery of ferroelectricity in hafnium oxide (HfO_2).[21–26] As

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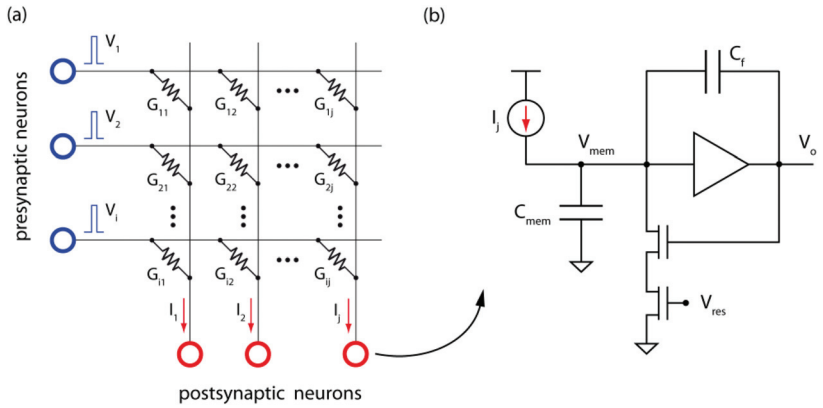

Fig. 1 (a) Neural network consisting of a crossbar synaptic array connecting presynaptic neurons to postsynaptic neurons. Synapses are represented by a variable conductance G and can be implemented with nonvolatile memory devices, whereas neurons are illustrated by circles and can be rea lized with pure CMOS components. (b) Schematic of an Axon Hillock CMOS neuron circuit:[8] the input synaptic currents are integrated on the mem brane capacitance C_{mem}, which is connected to the amplifier. Once the amplifier threshold voltage is reached, the output voltage V_o increases (neuron fires), activating the positive feedback through capacitor C_f, which produces a sudden increase in V_{mem}. This is followed by the discharge of C_{mem} at a rate set by the bias voltage V_{res}, allowing for the reset of both V_c and V_{mem}, therefore starting a new integration and fire cycle. Such a circuit might not be suitable for large scale neural networks and simpler solutions might be preferable.

the scaling of these devices proceeds, additional integration possibilities as well as novel switching phenomena start to appear.[22] Very recently, it has been reported that ultra-scaled FeFETs (having 10 nm-thick ferroelectric HfO_2 and 30 nm-long channel) display an accumulative switching behavior under certain electrical conditions,[27] contrasting the classical binary switching mode. The accumulation has been attributed to the progressive polarization reversal through localized ferroelectric nucleation. In the present study, we exploited this property and the resulting highly nonlinear switching response to electrically emulate two prominent neuronal dynamics, namely, the integration of action potentials and the subsequent firing, according to the biologically plausible all-or-nothing law. Moreover, we explored the implementation of an arbitrary refractory period and the possibility to tune the spiking dynamics upon simple voltage–time pulsing schemes, which were a direct consequence of ferroelectric nucleation mechanisms governing the device physics. Finally, we discuss the guidelines for implementing the leaky integrate-and-fire activity as well as the benefits of using FeFET-based neurons. Therefore, the aim of this study was to demonstrate key neuronal dynamics with simple electrical experiments, which might set the basis for simulating or building real ferroelectric neuronal circuits.

2. Results and discussion

(A) FeFET characteristics

Fig. 2a and b show a transmission electron microscopy (TEM) image and a schematic illustration of our FeFET device, respectively. The gate stack consists of the dielectric (interface) layer (1.2 nm silicon oxynitride SiON), the ferroelectric layer (10 nm silicon-doped HfO_2) and the top gate electrode (TiN and polysilicon).[22] The device has nanoscale dimensions with 30 nm and 80 nm for the length and width of the transistor, respectively. Fig. 2c shows the I_D–V_G curves of the device corresponding to the two polarization (P) states, namely, polarization down ($P\downarrow$) and polarization up ($P\uparrow$). Application of a positive gate pulse $V_G = V_P$ larger than the coercive voltage (V_C) of the ferroelectric sets the polarization downwards, which results in the program (PRG) transition from high threshold voltage (V_T) to low-V_T state. Alternatively, on applying a sufficiently negative pulse V_N, the polarization reverses, resulting in the erase (ERS) transition from low-V_T to high-V_T state. The FeFET-based memory devices rely on this reversible switching between the two states, which are separated by several orders of magnitude in drain current (see ESI Fig. S1†). Generally, in the scaled devices considered in this study, both transitions are abrupt in terms of switching voltage and time. For instance, Fig. 2d shows the PRG switching for three different V_P values, which is explored by increasing the pulse duration t_P while keeping the respective V_P constant (inset of Fig. 2d). The transition is sharp and the switching time decreases with the increase in V_P. This voltage–time dualism is characterized by a specific exponential relationship,[22] which has been attributed to the nucleation-limited switching in this type of FeFET devices.

(B) Integrate-and-fire behavior

Artificial neuron models often neglect complex neuronal dynamics to allow for the simulation and hardware implementation of large-scale networks. While some neuron circuits operate in biologically realistic time-constants (in the millisecond regime and typically using CMOS transistors in the sub-threshold and weak-inversion domain), other implementations perform at highly accelerated time scales (up to 10^5-fold faster than the nervous system). This is mainly conducted to reduce the power and silicon area consumption while adopting transistors in the strong-inversion regime and lower capaci-

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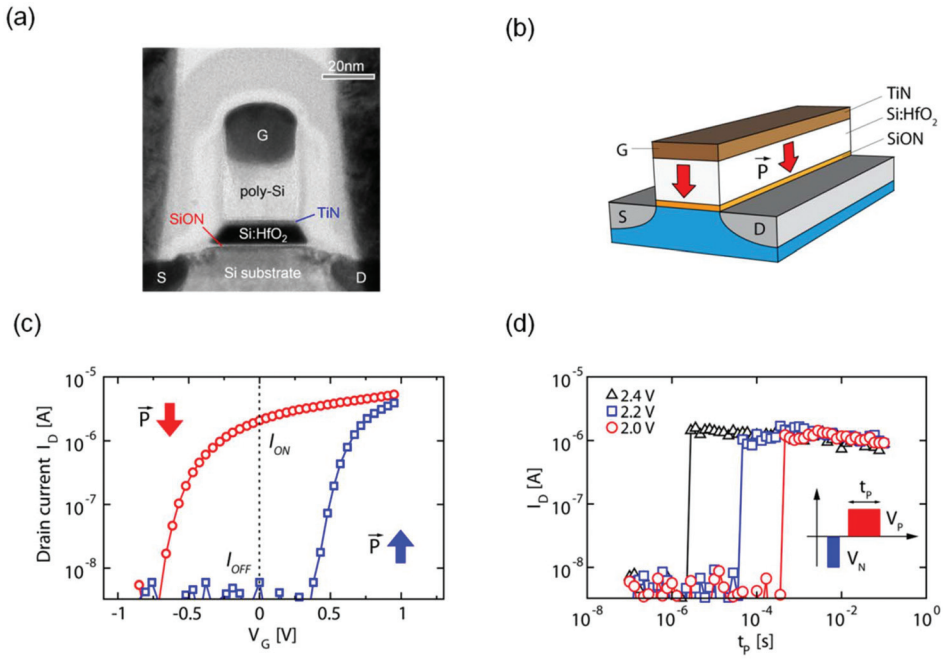

Fig. 2 FeFET structure and switching characteristics: (a) cross sectional TEM image of a device having L = 30 nm and W = 80 nm for the channel length and width, respectively. 'G', 'D' and 'S' indicate gate, drain and source terminals, respectively. (b) FeFET schematic indicating the structure of the gate stack, having the polarization vector P pointing downwards. (c) I_D V_G curves collected for the two polarization states by sweeping V_G from 1 V to 1 V in 500 μs while keeping drain voltage V_D = 100 mV. This fast sweep limits the current resolution to 10 nA. A higher resolution and thus $I_{ON}/I_{OFF} > 10^5$ can be achieved by a longer V_G sweep (ESI Fig. S1†). (d) Abrupt switching from OFF to ON state upon varying pulse duration t_P in the excitation scheme shown in the inset for three different V_P values. I_D is extracted from I_D V_G curves at V_G = 0 V, as indicated by the vertical dashed line in (c).

tance values.[9] Generally, integrate-and-fire (IF) neuron models are widely adopted owing to their relatively simple mathematical description yet sufficient accuracy in capturing essential biological features.[28] They are characterized by two prominent dynamics: the integration of weighted synaptic inputs that arrive from other neurons and the subsequent firing after a certain threshold is reached. This simple behavior will be implemented using an FeFET in this study.

The sharp transition in Fig. 2d shows that the device remains seemingly unperturbed under pulses having t_p shorter than the switching threshold. For instance, a pulse having V_P = 2.2 V and duration lower than t_p = 10 μs has no influence on the OFF state of the device. However, it has been recently reported that even such sub-threshold (sub-coercive) excitations can induce an accumulative effect within the ferroelectric material, which eventually leads to switching.[27] In fact, by applying identical gate pulses (V_P = 2.2 V, t_P = 1 μs), as shown in Fig. 3(a), each of which is insufficient for switching, the device remains in the OFF state as expected. However, after the 21st pulse is received, the FeFET abruptly undergoes the PRG transition to the highly conductive state, as illustrated in Fig. 3(c). The sharp OFF to ON switching takes place when a continuous conduction pathway is formed in the channel between the source and drain terminals. We assume that this happens when after a sufficient number of pulses have been reached, a critical number of nanodomains is nucleated, which triggers the abrupt polarization reversal of the entire grain connecting the two terminals. For any lower number of pulses, the dispersed nanodomains are not capable of inducing a significant charge inversion in the channel, leading to the absence of the conduction path (OFF state).[27] Note also, that this is a different scenario from the one occurring in FTJs, where the tunneling current flows through the ferroelectric and each nucleated domain contributes to the overall current, as usually described by the parallel conduction model.[17] The sharp OFF to ON transition is also exemplified in Fig. 3(b), showing the I_D–V_G curves as the number of excitation pulses increases.

Herein, we highlight the analogy to the IF neuron. The accumulation operation mode upon sub-threshold input pulses prior to the PRG transition can be regarded as the process of integration of synaptic inputs, whereas the subsequent highly nonlinear switching can be regarded as the firing event. It should be noted that the firing has an all-or-nothing character, indicating that the FeFET-based neuron either does not externally respond to the sub-threshold excitations or it displays a full-fledged firing signal (PRG switching) after all the necessary pulses have been received. Interestingly, this represents a strong similarity to the all-or-nothing law found in biological neurons, where the action potential is elicited in its full magnitude only if the exciting stimulus exceeds the threshold.[29]

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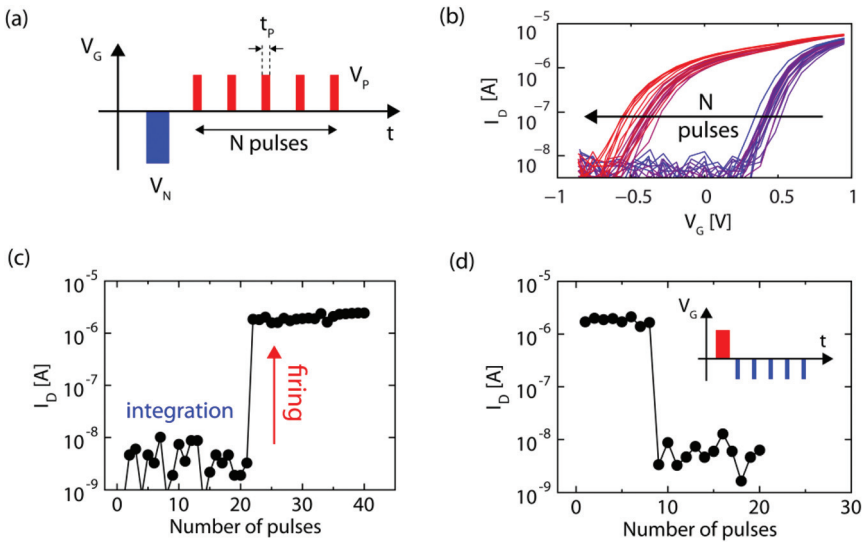

Fig. 3 Accumulative switching in FeFETs: (a) pulsing scheme for the accumulation in the OFF state consists of a train of identical pulses having amplitude V_P and duration t_P; (b) evolution of I_D V_G curves as the number of incoming pulses increases (from blue to red). A clear jump from high V_T to low V_T is observed; accumulative switching (c) from OFF to ON state with pulses V_P = 2.2 V, t_P = 1 μs and (d) from ON to OFF with negative pulses V_N = 3.25 V, t_P = 1 μs. The accumulative switching in our devices is invariant with respect to the time interval length between single pulses[27] (in this experiment: Δt = 100 ns). Analogy to IF neuron: integration of gate pulses (accumulation regime) → integration of postsynaptic potentials; abrupt switching after a critical number of pulses → action potential firing after a threshold is exceeded.

The accumulation behavior is also found when starting from the ON state and applying negative sub-threshold pulses, which eventually lead to the abrupt ERS transition, as shown in Fig. 3(d). This symmetry in the accumulation property is a direct consequence of the equivalence of the two polarization states within the ferroelectric. Moreover, this finding is reflected in the fact that both transitions (from $P\uparrow$ to $P\downarrow$ and from $P\downarrow$ to $P\uparrow$) are ruled by the nucleation of ferroelectric domains.

(C) Firing dynamics

It has been shown that the number of pulses to be integrated prior to switching substantially depends on the choice of pulse parameters, *i.e.*, amplitude V_P and duration t_P.[27] This property was attributed to the field-time dependence of the ferroelectric nucleation. Fig. 4(a) and (b) illustrate this phenomenon for varying t_P and V_P in the waveform of Fig. 3(a), respectively. It can be seen that the longer the t_P (the larger the V_P), the lower is the number of pulses necessary to induce switching. It is straightforward to recognize that this property can be exploited to modulate the firing dynamics of an FeFET-based neuron. For instance, Fig. 4c shows a possible pulsing scheme for implementing the integration-and-fire operation, discharging (FeFET resetting) and arbitrary refractory period: as soon as the FeFET undergoes the PRG transition (firing) upon a train of V_P pulses (which is detected by sensing a larger drain current flow in the resulting ON state), a negative pulse V_{reset} is applied at the gate to reset the device to the OFF state upon inducing the ERS transition. It should be noted that such a pulse can be tailored with a proper amplitude and duration to reproduce the desired refractory period. In fact, the switching to the OFF state is ruled by an exponential dependence between V_{reset} and t_{reset}, which is similar to the one between V_P and t_P shown in Fig. 2(d). Depending on the value of V_{reset}, t_{reset} can range from hundreds of milliseconds to nanoseconds (see, for instance, Fig. 3b of ref. 22). In this way, the refractory period can be chosen arbitrarily to match the biologically plausible as well as the accelerated-time neural dynamics.

Hence, with this pulsing scheme, a complete IF cycle can be emulated, after which a new cycle can begin. Fig. 4(d) shows the experimental results for different pulse amplitudes (V_P) while keeping t_P = 1 μs, where several IF cycles were consecutively repeated. For resetting the neuron in the OFF state, a single pulse V_{reset} = −4 V, t_{reset} = 1 μs was adopted. As a result, the output firing activity can be considerably modulated by changing the input excitation strength.

It should also be noted that the specific t_P and V_P firing dependence of an FeFET-based neuron can be exploited for implementing the weighted synaptic input from a presynaptic neuron. It is conceivable to take t_P (or alternatively V_P) as weighted input so that a larger pulse width (pulse amplitude) corresponds to a larger weight. Although the choice is directly related to the specific circuital implementation of the neural network, it might be argued that t_P is a more suitable parameter in this regard, given the almost linear relationship in the log–log graph between the number of pulses until firing and t_P.[27]

(D) Leaky behavior

The accumulative switching presented so far appears to be invariant with respect to the time distance between the incoming pulses.[27] This indicates that the leaky behavior is absent

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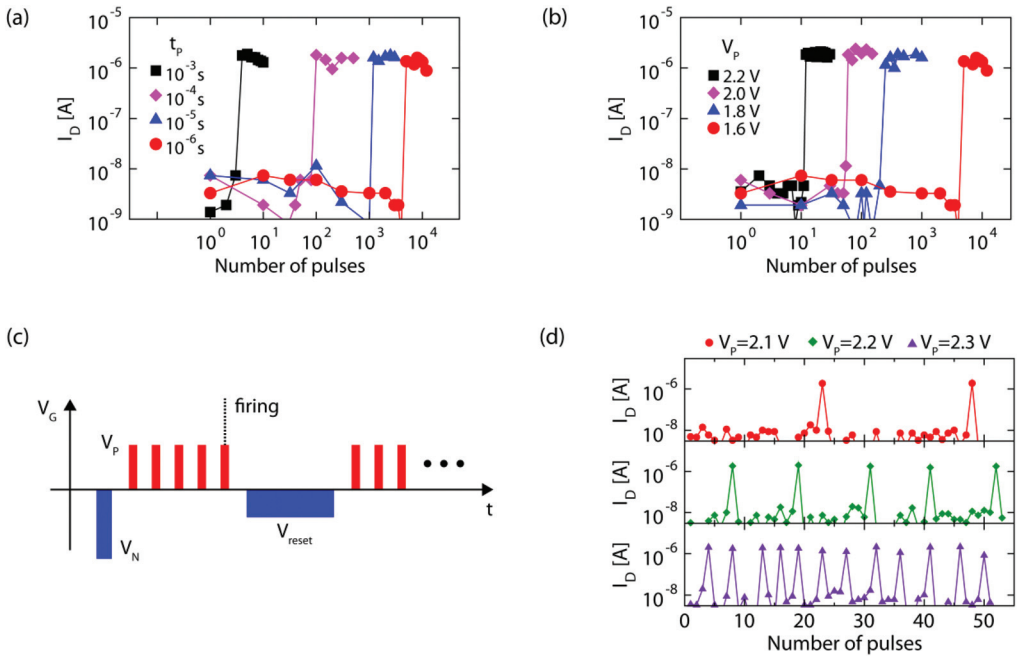

Fig. 4 Integrate and fire dynamics: (a) accumulative switching upon varying t_P while keeping V_P = 1.6 V; (b) accumulative switching upon varying V_P while keeping t_P = 1 μs; (c) pulsing scheme for implementing an IF cycle and an arbitrary refractory period, after which a new IF cycle begins; (d) consecutively repeated IF cycles for different V_P while keeping t_P = 1 μs.

and therefore, our devices are perfect integrators. However, to implement the leaky effect, the accumulation efficiency has to decay as the time interval between input pulses increases. One conceivable option is to modulate the depolarization field E_{dep} since it directly influences the electrostatic landscape within the ferroelectric. In other words, E_{dep} plays a significant role in the stability of the polarization state and is known to be particularly critical for metal–ferroelectric-insulator field effect transistors.[30] E_{dep} arises from an incomplete polarization surface charge compensation by the confining layers and can be approximated as follows:[30]

$$E_{dep} = P\left[\varepsilon_0\varepsilon_F\left(\frac{C_{IS}}{C_F}+1\right)\right]^{-1} \quad (1)$$

where ε_0 is the vacuum permittivity (8.85×10^{-12} F m^{-1}), P, ε_F and C_F are the polarization, dielectric constant and capacitance of the ferroelectric, respectively, and C_{IS} is the series capacitance of the interface layer and semiconductor.

According to eqn (1), by increasing the interface layer thickness, and/or decreasing the ferroelectric layer thickness, the depolarization field will increase. This in turn will tend to inhibit the nucleation of opposite ferroelectric domains, thus making the integration of excitation pulses less efficient. In fact, it has been already shown that a thicker interface (3 nm) leads to a severe degradation of polarization retention.[31] A similar effect could be potentially obtained by increasing the value of the remnant polarization, which is achievable by changing the dopant species, their concentrations, annealing conditions as well as deposition techniques.[32–35]

In addition, it should be noted that such a decrease in polarization retention capability could be exploited for a spontaneous reset operation. In fact, by appropriate engineering of the gate stack, where the $P\downarrow$ state appears markedly less stable than $P\uparrow$ state, a spontaneous decay from ON to OFF state after an integrate-and-fire cycle could be achieved. By doing this, the negative reset pulse shown in Fig. 4c and the relative circuitry could be completely avoided.

Herein, we show an attempt to electrically induce the leaky effect and thus emulate the depolarization field. This was performed by applying a negative bias V_{inh} during the time intervals between single input V_P spikes, as depicted in Fig. 5(a). In fact, V_{inh} generates an electric field in the gate stack, which points upwards and tends to inhibit the creation of new $P\downarrow$ ferroelectric domains. Therefore, it has a similar effect to the one produced by the depolarization field in a device having a thicker interface and V_{inh} = 0 V. Fig. 5(b) shows that V_{inh} indeed reduces the integration efficiency, *i.e.*, as $|V_{inh}|$ increases, the number of V_P pulses required for switching increases, with a very steep increase for $V_{inh} < -3$ V. In other words, the leakage effect could be induced electrically.

(E) Discussion

The described IF activity of an FeFET-based neuron might have several advantages when it comes to area/energy considerations and neuronal dynamics mimicking.

(1) Reduced circuital complexity: the capacitor C_{mem} in Fig. 1(b), which generally occupies a large area in the circuit, is not necessary. In fact, the integration of electrical stimuli is inherent to the accumulative operation mode of an FeFET.

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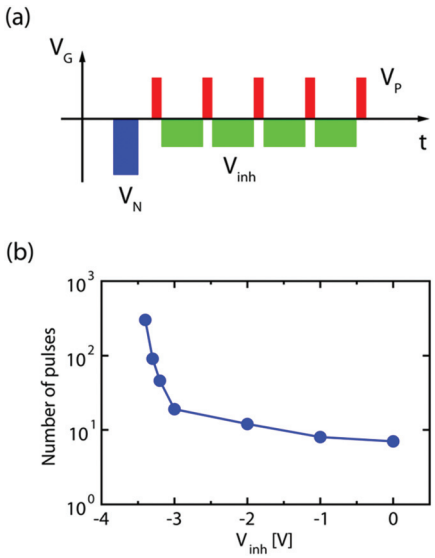

Fig. 5 Electrical emulation of the leaky effect: (a) inhibit voltage V_{inh} was applied in the intervals between consecutive V_P pulses (t_{inh} = 10 μs). V_{inh} emulates the effect that would have the depolarization field in a device having a thicker interface as it tends to reduce the integration efficiency of V_P pulses. (b) Number of pulses required for switching increases as V_{inh} increases in magnitude, which is equivalent to an increase in the leakage effect. It should be noted that V_P is always kept constant at 2.2 V, t_P = 1 μs. The device used herein is different from the device shown in Fig. 2 and 3 and has slightly different switching voltages.

Moreover, no or only limited amplification circuitry as well as no thresholding circuits (such as comparators) are needed. FeFETs are characterized by an intrinsic gain, which is directly reflected in the large I_{ON}/I_{OFF} ratio. The all-or-nothing type of switching is *per se* abrupt, highly nonlinear and clearly distinguishable.

Typically, a neuron circuit consists of (i) a temporal integration block, (ii) a spike generation block, (iii) a refractory period block, and (iv) a spike-frequency or spiking threshold adaptation block.[9] From the presented results, the functionality of (i) and (iii) can be already implemented with an FeFET. Furthermore, the functionality of block (iv) can be attained when adjusting the constant negative input bias (or, alternatively, the device back-bias, see point (3)) to tune the firing activity of the neuron. However, since the FeFET switches after N received pulses, it abruptly increases the drain current, but does not generate a spike. Therefore, a spike generation block has to be implemented with additional CMOS components. As shown in ESI Fig. S4,† we propose a possible realization of the FeFET-based neuron circuit, inspired by the work of Lazzaro *et al.*[36] It is to be understood, however, that this circuit is a first draft at present and has to be analyzed in more detail through further research. However, we show that by adopting an FeFET, a neuron circuit including blocks (i)–(iv) can be realized by adding just a small number of CMOS devices.

(2) Symmetry: both positive and negative excitations can be integrated, according to the data shown in Fig. 3(c) and (d). This property might provide a great flexibility for a neuron circuit design and might be used to implement both excitatory and inhibitory synaptic stimuli. Moreover, it represents an advantage over some other nanoscale neuron proposals. For instance, phase-change neurons are highly asymmetric in this regard as they rely on the accumulative crystallization of the material, whereas a gradual amorphization is generally not feasible.[13,16]

(3) An FeFET-based neuron is CMOS compatible, scalable and transferrable to other technologies: HfO_2 is a well-known and largely exploited material in microelectronics industry. Moreover, ferroelectricity in HfO_2 is very robust to scaling[37] and has been reported for film thicknesses below 3 nm.[38] Furthermore, it has been proved compatible with a variety of deposition techniques and substrates, thus making it transferrable to different and more advanced technologies. For instance, a successful fabrication of FeFETs in a fully depleted silicon-on-insulator (FDSOI) technology has been demonstrated.[24] ESI Fig. S3† shows that these devices display a distinct ferroelectric switching. In this light, we have experimentally confirmed the integrate-and-fire activity in such an ultra-scaled device (having 20 nm and 80 nm for transistor length and width, respectively), as shown in Fig. 6. An additional advantage of this technology is the presence of the back-bias electrode (ESI Fig. S3†), which can be used to tune the threshold voltage of the transistor and thus provide further functionalities.[39]

(4) Stochasticity: the ferroelectric nucleation is a stochastic process, which causes a certain fluctuation of the switching voltage/time,[40] and consequently of the number of pulses for switching when repeating the IF cycles several times[27] (visible also in Fig. 4d). This stochasticity can be harnessed for emulating the probabilistic activity of the biological neuron, which is believed to have an important role in information processing in the nervous system.[41] It has been often convenient to describe the neuronal noise by some additive random process, *e.g.*, Poisson process.[28] Interestingly, the nucleation of ferroelectric domains can also be approximately described by a Poisson process,[42] which was experimentally demonstrated for

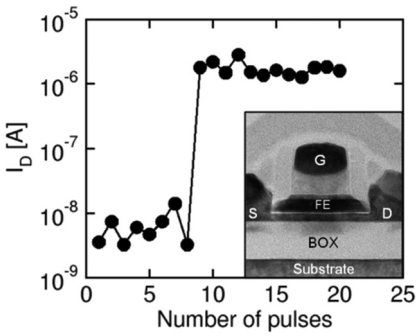

Fig. 6 Integrate and fire behavior in an ultra scaled FDSOI FeFET having channel length L = 20 nm and channel width W = 80 nm upon a train of pulses V_P = 2 V, t_P = 1 μs. Inset: TEM image of a device. 'G', 'S', 'D', 'FE', and 'BOX' indicate gate, source, drain, ferroelectric layer, and buried oxide, respectively.

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our devices.[22] By exploiting this similarity, complex circuits necessary for introducing randomness in neural networks could be avoided.

It should be, however, noted that the all-or-nothing IF property presented in section (B) is typically present in small-area FeFET devices, such as the device presented in this study. In contrast, large-area devices (usually for the channel length larger than 100 nm) are characterized by a gradual PRG transition upon the same excitation pattern shown in Fig. 3a (see ESI Fig. S2†). This can be explained by a considerably larger number of switchable ferroelectric domains within the gate stack than in small-area FeFETs. Nevertheless, gradual integration could also be employed for artificial neurons, provided that such an FeFET is coupled to a thresholding circuit, which will create an output spike once its internal threshold is crossed. This realization might be similar to the floating gate-based neuron.[43] The great advantage of the large-area devices is their relatively low device-to-device variability, which, instead is larger in the state-of-the-art small-area devices.[24,44]

With the reference to Fig. 1(a), not only neurons but also the synapse matrix can be realized with ferroelectric elements. There has been a growing body of research that has tried to employ ferroelectric switching for emulating the gradual synaptic weight using classical ferroelectrics.[18,45–47] Very recently, the focus has been shifted to the research on hafnium oxide-based synapses.[48–51] It is, therefore, conceivable to couple ferroelectric neurons and synapses to create all-ferroelectric neural networks. Within this context, an FeFET-based neuron presented in this study might open up a completely new set of opportunities for the future of neuromorphic computing.

3. Conclusions

We showed that the accumulative polarization reversal and the resulting abrupt drain current increase in a nanoscale FeFET device could be used to emulate the integration of postsynaptic spikes and the all-or-nothing firing operation of the biological neuron, respectively. The gate voltage pulse shaping allows the implementation of several additional key neuronal dynamics, such as arbitrary refractory period, firing activity modulation and leaky behavior owing to the particular voltage–time dependence of the accumulative switching. Although the presented results are obtained on non-optimized devices, they provide the first powerful insights in possible neuromorphic applications. Further device optimization, including ferroelectric film composition, doping and/or annealing, along with the gate stack engineering might offer additional or novel properties, such as the intrinsic leaky behavior and the self-resetting operation. Moreover, the inherent switching stochasticity of FeFETs might be employed for mimicking probabilistic computing of real neurons. The proposed FeFET-based neuron is fully compatible with existing integrated circuit fabrication. In addition, the synaptic weights could be implemented in a circuit by using emerging ferroelectric devices, paving the way for building all-ferroelectric neural networks. This might not only substantially reduce the system complexity, but also endow neuroscience with a new framework for exploring and understanding the human brain computation.

4. Experimental

The FeFETs prepared in this study contained a TiN/Si:HfO_2/SiON/Si gate stack fabricated in the following way: first, a 1.2 nm thick interfacial nitrided SiO_2 layer (SiON) was grown on the p-doped silicon substrate, followed by the deposition of a 10 nm silicon-doped HfO_2 layer grown from $HfCl_4$ and $SiCl_4$ in a water-based atomic layer deposition (ALD) process at 300 °C. At this step, 4 mol% silicon doping was introduced in order to induce the ferroelectric orthorhombic phase in the film after annealing. The metal gate electrode was obtained by physical vapor deposition (PVD) of TiN, which was consequently contacted with polysilicon. Then, a two-step lithographic process defined the lateral dimensions, *i.e.*, 30 nm and 80 nm for transistor length and width, respectively. The source and drain n^+ regions were obtained by phosphorous ion implantation, which were then activated by a rapid thermal annealing (RTA) at around 1000 °C. This resulted in a polycrystalline Si:HfO_2 ferroelectric layer.

All electrical measurements were performed using a Keithley 4200-SCS Semiconductor Analyzer.

Conflicts of interest

There are no conflicts to declare.

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