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Fabrication and Characterization of AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors for High Power Applications

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A Tata e Mathieu
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Abstract

AlGaN/GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) are promising candidates for next generation high-efficiency and high-voltage power applications. The excellent physical properties of GaN-based materials, featuring high critical electric field and large carrier saturation velocity, combined to the high carrier density and large mobility of the two-dimensional electron gas confined at the AlGaN/GaN interface, enable higher power density minimizing power losses and self-heating of the device. However, the advent of the GaN-based MIS-HEMT to the industrial production is still hindered by technological challenges that are being faced in parallel. Among them, one of the biggest challenge is represented by the insertion of a gate dielectric in MIS-HEMTs compared to Schottky-gate HEMTs, which causes operational instability due to the presence of high-density trap states located at the dielectric/III-nitride interface or within the dielectric. The development of a gold-free ohmic contact technology is another important concern since the high-volume and cost-effective production of GaN-based transistors also depends on the cooperative manufacturing of GaN-based devices in Si production facilities, where gold represents an undesidered source of contamination. In fact, even though over the past years there have been multiple attemps to develop gold-free ohmic contacts, there is still no full understanding of the contact formation and current transport mechanism.

The first objective of this work was the investigation of a gold-free and low-resistive ohmic contact technology to AlGaN/GaN based on sputtered Ta/Al-based metal stacks annealed at low temperatures. A low contact resistance below 1 Ω mm was obtained using Ta/Al-based metal stacks annealed at temperatures below 600 °C. The ohmic behavior and the contact properties of contact resistance, optimum annealing temperature and thermal stability of Ta/Al-based contacts were studied. The nature of the current transport was also investigated indicating a contact mechanism governed by thermionic field emission tunneling through the AlGaN barrier. Finally, gold-free Ta/Al-based ohmic contacts were integrated in MIS-HEMTs fabricated on a 150 mm GaN-on-Si substrate, demonstrating to be a promising contact technology for AlGaN/GaN devices and revealing to be beneficial for devices operating at high temperatures.

The optimization of the MIS-gate structure in terms of trap states at the dielectric/III-nitride interface and inside the dielectric in MIS-HEMTs using atomic layer deposited (ALD) Al_2O_3 as gate insulator was the second focus of this work. First, the MIS-gate structure was improved by an O_2 plasma surface preconditioning applied before the Al_2O_3 deposition and by an N_2 postmetallization anneal applied after gate metallization, which significantly reduced trap states at the Al_2O_3/GaN interface and within the dielectric. Afterwards, the effectiveness of these treatments was demonstrated in Al_2O_3-AlGaN/GaN MIS-HEMTs by pulsed current–voltage measurements revealing improved threshold voltage stability. Lastly, it was shown that also the lower annealing temperatures used for the formation of Ta/Al-based ohmic contacts, processed before gate dielectric deposition, are beneficial in terms of trap states at the ALD-Al_2O_3/GaN interface, representing a new aspect to be considered when using an ohmic first fabrication approach.

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7.2 Comparison of the calculated and measured on-state drain-to-source resistance $R_{DS,on}$ of MIS-HEMTs with Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts. The input parameters of $R_c^{S/D}$ and R_{sh} for the calculation were obtained in Section 5.2 taking into account the Al_2O_3 passivation layer. 85

1 Introduction

Today more than ever, the continuous increase of the global consumption of electric energy urgently demands for more efficient energy convertion systems capable of handling and delivering higher power levels. In fact, traditional power systems based on silicon are quickly approaching their physical limits in terms of power density, conversion efficiency and possibility to operate at higher frequency and higher temperatures. To meet the future expectations of power electronics, novel semiconductors have been exploited as alternative to silicon.

Owing to the outstanding physical properties of large bandgap energy of 3.43 eV, high electric breakdown field of 3.3 MV/cm and large saturation velocity of about 2.5×10^7 cm/s, GaN is one of the most promising semiconductor for the future generation of energy efficient power electronics.[1, 2] Beside the unique intrinsic material properties, one of the most attractive property of GaN is the possibility to exploit the polar nature of GaN-based materials to form AlGaN/GaN heterostructures. Featuring a two-dimensional electron gas at the heterointerface with high carrier density and high mobility values exceeding 2000 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$, AlGaN/GaN heterostructures enable the fabrication of high electron mobility transistors (HEMTs) which can significantly outperform the traditional Si power devices in terms of breakdown strength, on-resistance and switching speed, achieving higher power density and higher energy efficiency.[3, 4] First demonstrated by Khan et al. in 1993,[5] GaN-based HEMT lateral devices are now commercially available in the power electronics market.[6] Neverthless, technological challenges are being still faced in parallel in order to bring the GaN technology to an industrial maturity and cost-effective level suitable for mass markets.[7]

One of the most serious problems that limit the performance of AlGaN/GaN HEMTs is the high leakage current at the Schottky-gate electrode.[8] For this reason, the Schottky-gate is replaced by a metal-insulator-semiconductor (MIS)-gate structure providing reduced power consumption, larger gate bias swing and better immunity to gate breakdown,[9] which are important requirements especially for power switching devices. However, in contrast to Si-based devices, the introduction of an insulator in MIS-HEMT devices is complicated by the absense of a high-quality native oxide for GaN. Due to the wide bandgap of GaN-based materials, trap states at the dielectric/III-nitride interface and within the dielectric can be deeply located in the bandgap and lead to long charge/discharge processes which strongly affect the device performance.[10] Various dielectric materials have been employed, being Al_2O_3 and SiN_x the most promising gate dielectrics.[11] However, even though excellent device characteristics have been reported, trap states in MIS gate structures still remain one of the biggest challenge for GaN-based MIS-HEMTs. In particular, the commercialization of these devices has been hindered by concerns over the gate dielectric reliability. In this respect, the delivery of a gate dielectric with low interface and bulk trap density and robust reliability under stringent electrical and thermal stresses is still of primary importance.

Another major concern for GaN-based devices is represented by the absence of high quality and large freestanding GaN substrates. For this reason, GaN-on-Si platforms are typically used for device fabrication. As a consequence, the cost-effective and large-scale production of GaN-based devices sees the manufacturing of these devices in existing Si facilities as the most natural strategy for a significant price reduction accompanied by improved handling capabilities. However, this comes with the stringent requirement of developing a manufacturing process for GaN-based devices which is fully compatible with the restrictions of Si fabs in terms of source of contaminations.[12] In particular, since conventional source and drain ohmic contacts have been using gold (Au)-containing metallization schemes, the development of Au-free ohmic contacts with a low contact resistance is a key aspect to enable the processing of GaN-based devices in Si production lines.[13] In general, the fabrication of low-resistive ohmic contacts is mainly complicated by the absence of metals which are able to prevent the formation of a Schottky barrier between the metal and wide bandgap GaN-based materials. In this respect, low-resistive and Au-free ohmic contacts seem even more challenging than Au-containing contacts. Another important aspect is that conventional Au-containing contacts require thermal annealing treatments at high temperatures (>800 °C) for contact formation. Lower annealing temperatures below 600 °C would be also preferable to beneficially add flexibility and opportunities in device process integration. For these reasons, enourmous efforts have been devoted to the study and development of low-resistive and Au-free ohmic contacts to GaN-based materials annealed at low temperatures. The latters have recently contributed to first demonstration of Au-free complementary metal-oxide-semiconductor (CMOS)-compatible AlGaN/GaN HEMT processing on 200 mm Si substrates in a Si fab.[14] Neverthless, the topic of ohmic contacts still contains several open scientific issues among which the reproducibility of Au-free ohmic contacts with contact resistance below 1.0 Ω mm and even more the mechanism of ohmic contact formation represent the most challenging and debated.

The focus of this work was the fabrication, characterization and optimization of AlGaN/GaN MIS-HEMTs for high-power electronics. The thesis is structured as follows: in Chapter 2, the fundamental concepts of heterostructure field-effect transistors are introduced and the operation principles of Schottky-gate HEMTs are presented. Chapter 3 introduces the requirements of the epitaxial materials used to obtain high performance AlGaN/GaN devices. The challenges encountered in the integration of a MIS-gate in HEMT devices for power applications and the difficulties in the realization of low-resistive ohmic contacts to AlGaN/GaN heterostructures are also highlighted. In Chapter 4, the experimental fabrication and characterization methods applied in this work are briefly described. Chapter 5 focuses on the development and investigation of low-temperature and Au-free ohmic contacts to AlGaN/GaN heterostructures using sputtered Ta/Al-based metal stacks. In Chapter 6, the MIS-gate module of AlGaN/GaN heterostructure capacitors using ALD-Al_2O_3 as gate insulator is investigated and optimized in terms of trap states at the dielectric/III-nitride interface and inside the dielectric. Chapter 7 concludes with the process integration in AlGaN/GaN MIS-HEMTs of the developed Au-free ohmic contacts and of the optimized MIS-gate module, which result beneficial in terms of on-state drain-to-source resistance degradation in devices operating at high temperature and device threshold voltage stability under positive gate bias stress, respectively. Finally, overall conclusions and outlooks are given.

2 Fundamentals of heterostructure field-effect transistors

In this chapter, the fundamentals of heterostructure field-effect transistors (HFETs) are reviewed. In particular, the unique intrinsic properties of the group III-nitrides are briefly described in the view of their application into AlGaN/GaN heterostructures, which also benefit from the high-density and high-mobility two dimensional electron gas (2DEG) confined at the heterojunction interface. Finally, the operation principles of AlGaN/GaN HEMTs with a Schottky-gate are introduced and the main electrical parameters which are used to characterize the device performance are presented.

2.1 Group III-Nitrides

The basic group of III-nitrides is composed by the binary compound semiconductor materials of aluminum nitride (AlN), gallium nitride (GaN) and indium nitride (InN). The superior intrinsic properties of these materials compared to silicon (Si), silicon carbide (SiC) or other III-V compound semiconductors make them extremely suitable for a wide variety of applications. Particularly, the III-nitrides have a wide range of direct bandgap energies from 0.7 eV to 6.2 eV which covers emission wave lengths from the infrared to the deep ultraviolet. The wide range of the emission spectra can be tuned through the material composition and be tailored for various optoelectronic applications, such as light-emitting diodes, lasers, photodetectors and solar cells. The wide tuning range of the bandgap energies of III-nitride materials is also very suitable for electronic applications, allowing for extremely high critical breakdown field strength and excellent capability to operate at high temperatures as well as low electron effective mass and high electron mobility.

Table 2.1: Electrical properties at 300 K of group III-nitride bulk materials in comparison to competing semiconductors. Data taken from [12, 15, 16, 17, 18, 19].

	AlN	**GaN**	**InN**	**GaAs**	**4H-SiC**	**Si**
Energy bandgap (eV)	6.2	3.43	0.7	1.42	3.26	1.12
Dielectric constant	8.5	9.5	15.3	12.9	9.7	11.7
Electron mobility (cm^2/Vs)	300	1200	3200	8500	800	1500
Breakdown field (MV/cm)	8.4	3.3	1.4	0.4	3.5	0.3
Saturation velocity ($\times 10^7$ cm/s)	1.4	2.5	1.8	0.7	2.0	1.0

In this perspective, GaN is one of the most promising III-nitride material for high-voltage electronics compared to conventional semiconductors. Its large bandgap energy of 3.43 eV results in an electric breakdown field of about one order of magnitude larger than in Si. Additionally, even though GaN exhibits about the same electron mobility than Si, the larger saturation velocity of GaN which can be achieved at high electric fields offers a great potential to target high-frequency and high-power switching applications, such as DC-DC converters, DC-AC converters or switching power amplifiers. Table 2.1 compares the inherent material properties of III-nitride materials to the competing semiconductors. A comprehensive overview of the material properties of group III-nitride semiconductors and their electronic applications is given by Rüdiger Quay.[20]

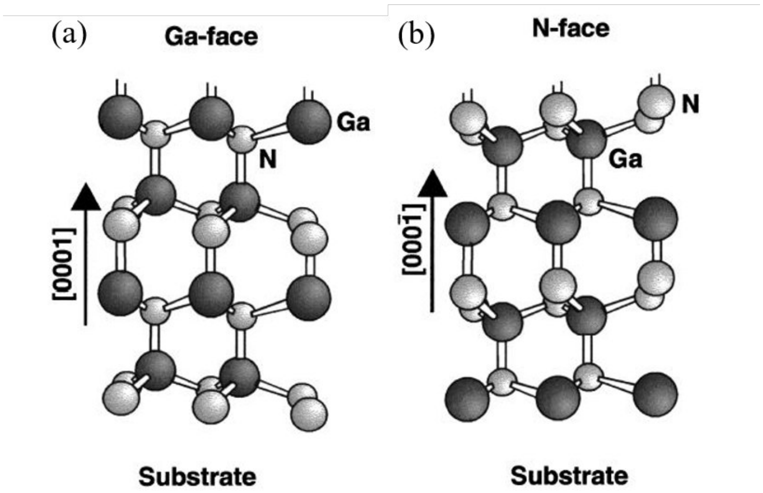


Figure 2.1: Crystal structure of wurtzite (a) Ga-face and (b) N-face GaN, taken from [21].

The great potential of III-nitride materials additionally stems from the presence of a strong spontaneous and piezoelectric polarization arising from the crystal structure of these materials. The group III-nitrides AlN, GaN, and InN can crystallize in the three crystal structures of wurtzite (hexagonal), zinc-blende (cubic), and rock-salt (cubic). The wurtzite structure is currently utilized for electronic applications since this phase is thermodynamically stable at ambient conditions. The unit cell of the wurtzite lattice is hexagonal and consists of alternating closely-packed hexagonal planes of cations and anions pairs stacked along the *c*-axis. The non-centrosymmetric nature of the wurtzite structure in combination with a pronounced ionic character of the metal-nitrogen bond of III-nitrides lead to polar faces and a strong macroscopic polarization along the *c* direction. Since this polarization effect occurs in the equilibrium lattice of III-nitrides at zero strain, it is called spontaneous polarization. Bernardini et al. predicted that the spontaneous polarization is very large in wurtzite group-III nitrides compared to other III-V compound materials and its magnitude increases from GaN over InN to AlN.[22] The wurtzite crystal structure of GaN is schematically represented in Figure 2.1. Due to the inversion asymmetry along the *c*-axis in the wurtzite phase, the crystal surface of GaN can have either Ga-face or N-face polarity when grown along the [0001] and [000$\bar{1}$] directions, respectively.[21] With a few exceptions,[21, 23, 24] most research in III-nitride optoelectronic and electronic devices in the past has focused on bulk materials grown in the Ga-polar direction.

In addition to the spontaneous polarization, the strong ionicity of the crystal structure of III-nitrides induce a large piezoelectric polarization when a stress is present in the crystal lattice.[22] The stress can originate from a pure mechanical deformation of the III-nitride crystal or during the growth of heterostructures composed by two materials with different lattice constant. The piezolectric polarization is induced by the displacement of the atoms in the crystal lattice to accomodate the stress and depending on the nature of the stress, tensile or compressive, the resulting piezoelectric polarization can act in either the same or opposite direction with respect to the spontaneous polarization. The relation between mechanical deformation and electrical polarization is established by the piezoelectric constants. The piezoelectric constants of wurtize group III-nitrides are reported to be up to ten times larger than in conventional III-V semiconductor compounds.[22]

Taking advantage of the polar nature of III-nitride materials combined with the use of heterostructures, the large polarizations and resulting electric fields can be used to induce high sheet charge densities at the interface. Particularly, when an AlGaN layer is grown on top of GaN, a sheet charge bound to the AlGaN/GaN interface is induced by the spontaneous and piezoelectric polarization in the AlGaN/GaN heterostructure. If the polarization induced charge density is positive, this results in the confinement of a two-dimensional electron gas at the interface of the AlGaN/GaN heterostructure with high carrier density and high mobility without any intentional doping. Especially in wurtzite AlGaN/GaN based transistor structures, the piezoelectric polarization is more than five times larger compared to AlGaAs/GaAs structures and it leads to a significant increase of the sheet carrier concentration at the interface.[21] The superior properties of GaN-based materials together with the excellent tranport properties of the 2DEG AlGaN/GaN channel make the AlGaN/GaN heterostructure system very suitable for high-frequency and high-power device applications. In the following section the fundamentals of the AlGaN/GaN heterostructure are introduced.

2.2 AlGaN/GaN heterostructures

The AlGaN/GaN heterostructure consists of a thin AlGaN barrier layer grown on top of a relatively thick GaN channel/buffer layer. A confinement potential capable of hosting a 2DEG is formed in the conduction band of the GaN near the interface resulting from a discontinuity in the bandgap and in the polarization at the AlGaN/GaN heterointerface. Most importantly, in contrast to heterostructures formed with conventional III-V semiconductors, such as AlGaAs/-GaAs heterojunctions, where the formation of a 2DEG requires a doping of the semiconductor, in AlGaN/GaN systems the 2DEG can be formed even using undoped layers, resulting in a significant improvement of the electron mobility due to the reduction of Coulomb scattering with ionized impurities. The formation of the 2DEG at the AlGaN/GaN heterojunction relies on the presence of spontaneous and piezoelectric polarization in AlGaN and GaN layers.[21] In particular, the spontaneous polarization is present in both layers due to the inherent crystal lattice of III-nitride materials, while the piezoelectric polarization arises in the AlGaN barrier from strain induced by the lattice mismatch between GaN and AlGaN layers. No piezoelectric polarizations are instead present in the GaN buffer layer since it is fully relaxed due to its relatively large thickness in the range of 1-3 µm. In the absense of external electric field, the total polarization of the AlGaN and GaN layers is the sum of the spontaneous and piezoelectric polarization, causing a polarization sheet charge density defined by

$$\sigma_P = P(AlGaN) - P(GaN) = P_{SP}(AlGaN) + P_{PE}(AlGaN) - P_{SP}(GaN), \tag{2.1}$$

where P is the total polarization, P_{SP} is the spontaneous polarization and P_{PE} is the piezoelectric polarization. Because the value of the piezoelectric constants and spontaneous polarization increase from GaN to AlN, the total polarization of a strained or even unstrained AlGaN layer is larger than the one of a relaxed GaN buffer layer [$|P(AlGaN)| \geq |P(GaN)|$]. Fundamental analyses of polarization induced interface charges in GaN-based heterostructures are given by Oliver Ambacher et al.[21, 25, 26] The various existing theoretical models on the origin of the two dimensional electron gas are reviewed and discussed by Benoit Bakeroot et al.[27]

In the case of strained AlGaN on Ga-face GaN, the orientation of the piezoelectric and spontaneous polarization is parallel and a positive sheet charge density $+\sigma_P$ is induced at the AlGaN/GaN interface.[26] Therefore, free electrons will tend to compensate this polarization induced positive charge and will accumulate in the quantum well in the GaN layer close to the interface, forming a 2DEG channel with a sheet carrier concentration n_s. A schematic illustration of the polarization components in tensile strained AlGaN on Ga-face GaN and the corresponding electron accumulation and formation of 2DEG at the interface is shown in Figure 2.2. Note that, the tensile strain in the AlGaN barrier introduces a piezoelectric polarization component in the same direction than the spontaneous polarization which enhances the polarization induced sheet charge and the corresponsing 2DEG concentration. In the case of undoped (Ga-face) AlGaN/GaN heterostructures, the 2DEG can have a sheet charge carrier concentration up to 1×10^{13} cm^{-2} with a very high electron mobility in the range of 2000-2200 cm^2 V^{-1} s^{-1}, due to the absence of scattering related to the impurity doping in the channel.

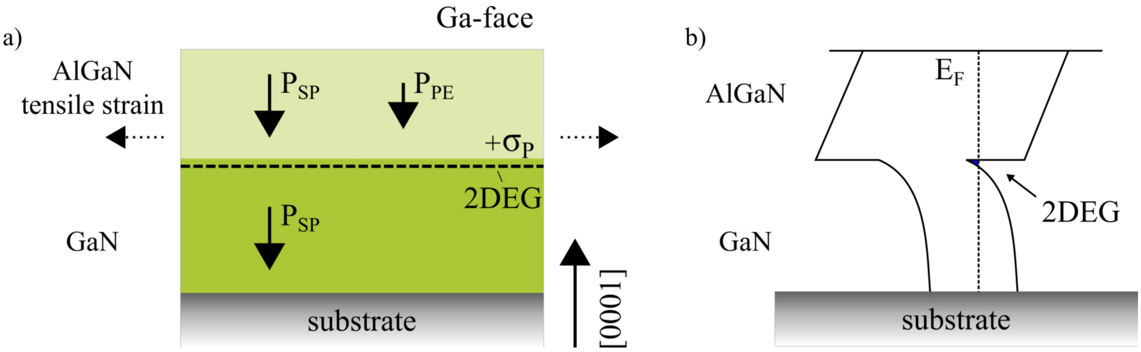


Figure 2.2: (a) Spontaneous polarization and piezoelectric polarization and induced interface charges and 2DEG in Ga-face tensile strained AlGaN/GaN heterostructure. P_{SP} denotes the spontaneous polarization and P_{PE} the piezoelectric polarization. (b) Schematic band diagram of AlGaN/GaN heterostructure illustrating the electron accumulation and formation of 2DEG located in the GaN at the AlGaN/GaN interface.

The polarization induced 2DEG sheet charge density of AlGaN/GaN heterostructures mainly depends on the Al content *x* and the thickness of the $Al_xGa_{1-x}N$ barrier layer. Figure 2.3 reports the theoretical prediction of the sheet carrier concentration of polarization-induced 2DEGs and their dependence on Al concentration and AlGaN barrier thickness for Ga-face AlGaN/GaN, calculated by Ambacher et al.[25] The sheet carrier concentration increases with increasing the Al concentration in the barrier due to the increase of strain in the layer resulting in stronger piezoelectric and spontaneous polarization. This dependency offers the possibility to tune the sheet carrier concentration of the 2DEG by the Al concentration instead of barrier doping. The increase of n_s with increasing Al content is limited by the strain relaxation of the barrier layer during growth, causing a reduction of the piezoelectric component for higher Al concentration.[26] Regarding the dependence of n_s on the AlGaN barrier thickness, a minimum thickness of the AlGaN barrier layer is required in order to form the 2DEG. Above this critical thickness, n_s increases with increasing the barrier thickness and saturates for barrier thickness above 30 nm. A further increase of the AlGaN barrier thickness would lead to a relaxation of the layer, causing a reduction of the polarization and hence, to a decrease of the sheet carrier concentration.

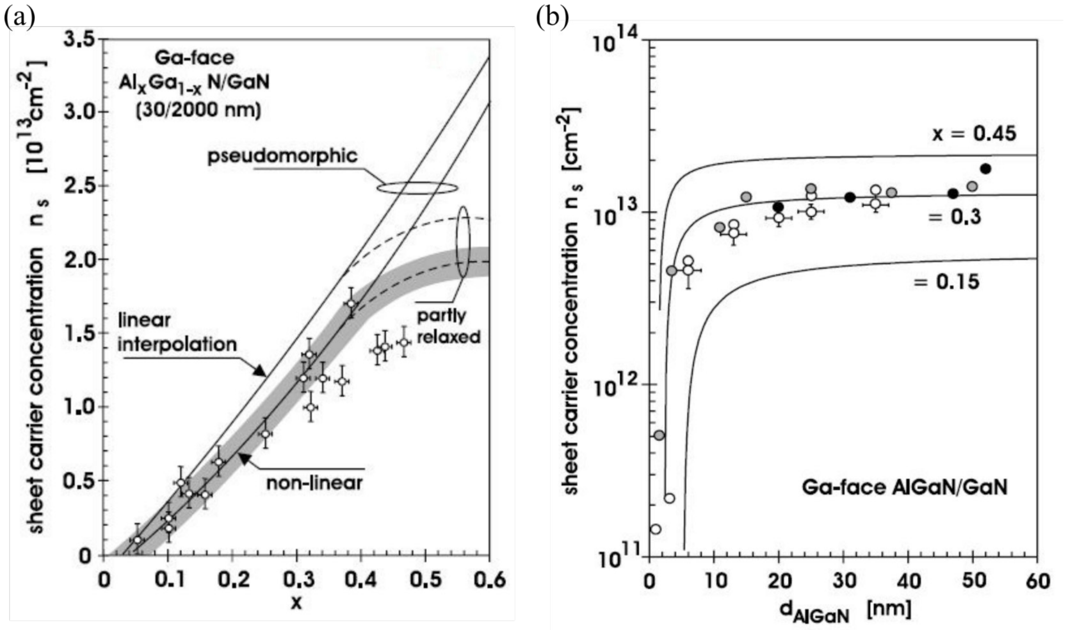


Figure 2.3: Dependence of the 2DEG sheet carrier concentration n_s on (a) the Al content x and (b) the thickness of the $Al_xGa_{1-x}N$ barrier layer d_{AlGaN}, taken from [21]. In (a), the theoretical predictions (solid lines) are compared to experimental data (symbols). The sheet carrier concentration is calculated using a linear interpolation of the physical properties of the binary compounds (upper solid curve) and considering the nonlinear behaviour of piezoelectric and spontaneous polarization (lower solid curve). The grey area represents the uncertainty of the calculated values of n_s. The dashed lines depicts the dependence of n_s on the alloy composition taking into account the relaxation of the $Al_xGa_{1-x}N$ barrier with increasing Al content.

Despite the outstanding transport properties of AlGaN/GaN heterostructures, various scattering mechanisms limit the value of the electron mobility of the 2DEG. In particular, at room temperature the maximum electron mobility is limited by polar optical phonon scattering.[28] At low carrier densities, impurity and piezoacoustic scattering diminish the mobility. For higher densities, these scattering processes are screened which lead to an increase of the mobility up to 2000-2200 cm^2 V^{-1} s^{-1}.[21] At very high sheet carrier density, the 2DEG is located closer to the AlGaN/GaN interface and, depending on the interface quality, the mobility can be limited by short-range scattering mechanisms such as interface roughness scattering and alloy disorder scattering. Interface roughness scattering act on electrons moving in the 2DEG channel due to the non-abrupt interface between AlGaN and GaN. Alloy disorder scattering is caused by the penetration of a finite part of the 2DEG wavefunction, which is mostly confined in GaN, into the AlGaN barrier. An overview of the various scattering mechanisms occuring in III-V semiconductors can be found in [29, 30]. A theoretical computation of the electron mobility of AlGaN/GaN heterostructures including the main scattering mechanisms is given by Hsu et al.[31]

From an application point of view in transistor structures, the optimization of AlGaN/GaN heterostructures targets a high 2DEG density and high mobility simultaneously. In this respect, a too high Al content creates a large lattice mismatch, which causes high structural defects and rough interfaces limiting the 2DEG mobility. Therefore, design parameters of the AlGaN/GaN heterostructure typically used are Al content of 20-25 % and AlGaN barrier thickness of 15-30 nm.

2.3 High Electron Mobility Transistor

The AlGaN/GaN heterostructure is the basis of the so called high electron mobility transistor. The first breakthrough of high electron mobility transistors fabricated with an AlGaN/GaN heterojunction was demonstrated only in 1993 by Khan et al.[5] A schematic illustration of a basic AlGaN/GaN HEMT device is shown in Figure 2.4.

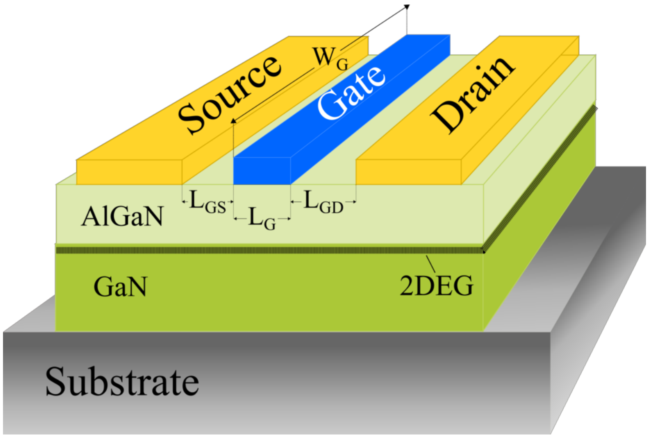


Figure 2.4: Schematic of AlGaN/GaN HEMT device. W_G indicates the gate width of the device. L_{GS} is the gate-to-source distance, L_G is the gate length and L_{GD} is the gate-to-drain distance.

The device benefits from the high-density and high-mobility 2DEG confined at the AlGaN/GaN interface and it has generally three terminals: gate (G), source (S) and drain (D). Source and drain contacts are ohmic contacts with a linear current-voltage characteristic to ensure a current flow from metal to semiconductor without affecting the device operation. The gate contact is a Schottky contact which allows to switch the transistor on and off by controlling the sheet carrier density in the 2DEG channel underneath the gate contact. In particular, since the 2DEG is present at the AlGaN/GaN interface without any external voltage applied, the HEMT is a normally-on device and a sufficient negative gate voltage is required to fully deplete the 2DEG under the gate and turn off the device. In the on-state, by applying a voltage between source and drain, a current between the drain and source terminals flows through the two dimensional conducting channel. Figure 2.5 shows a schematic of the band energy diagrams underneath the gate contact in the on- and off-states of an AlGaN/GaN HEMT device.

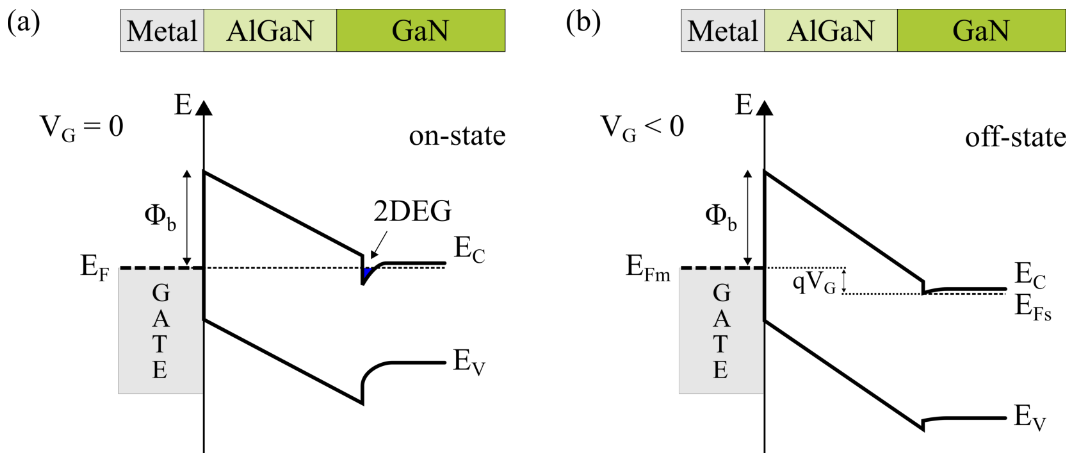


Figure 2.5: Schematic of band energy diagrams (a) under zero gate voltage and (b) under negative gate bias. In (a) the 2DEG conductive channel is formed at the AlGaN/GaN interface. E_C is the conduction band minimum, E_V the valence band maximum, E_{Fm} the Fermi level in the metal, E_{Fs} the Fermi level in the semiconductor, Φ_b the Schottky barrier height and V_G the gate voltage.

Without gate voltage applied, the 2DEG charge carrier density is distributed in the energetically lowest subbands of the quantum well or confinement potential, which are located below the Fermi energy (see Figure 2.5a). By decreasing the gate bias towards negative values, the conduction band and the subbands are pulled up and moved away from the Fermi level in the GaN, resulting in the depopulation of the subbands, untill the 2DEG has vanished (see Figure 2.5b).

The drain-to-source current (I_{DS}) of the HEMT can be controlled by changing the 2DEG sheet charge concentration under the gate electrode through the gate voltage. The 2DEG sheet carrier density along the channel, considering a lateral potential gradient between source and drain and neglecting the extrinsic series resistance of source and drain, is given by [32]:

$$n_s(x) = \frac{1}{q} C_G \left(V_{GS} - V_{th} - V(x)\right), \tag{2.2}$$

where q is the elementary charge, C_G is the gate-to-channel capacitance, V_{GS} is the gate-to-source voltage, V_{th} is the threshold voltage and V(x) is the acceleration voltage at a certain location x along the channel. In the HEMT schematic of Figure 2.4, C_G is given by $\varepsilon_0\varepsilon_{AlGaN}/d_{AlGaN}$, where d_{AlGaN} is the thickness of the AlGaN layer which is the only layer located between the gate electrode and the 2DEG. Note that, as discussed later, additional layers in the gate stack (e.g. GaN-cap or dielectric layers) add a series capacitance to the one of the AlGaN barrier which reduces the gate-to-channel capacitance. The threshold voltage V_{th} of the device is related to the gate voltage V_G at which the 2DEG sheet carrier density becomes zero at the source side.

Similarly to the case of the long-channel metal-oxide-semiconductor field-effect transistor (MOSFET),[33] the drain-to-source current density J_{DS} in the HEMT device is proportional to the density of electrons in the channel and, assuming a constant mobility μ, it can be expressed as follows

$$J_{DS}\left(x\right) = -\mu W_G q n_s\left(x\right)\frac{dV\left(x\right)}{dx}, \tag{2.3}$$

where W_G is the gate width of the device. The drain-to-source current I_{DS} is obtained integrating J_{DS} along the channel and depending on the drain-to-source voltage V_{DS} applied, various regimes of operation of the transistor can be defined.

When $V_{DS} \ll (V_{GS} - V_{th})$, the transistor operates in the linear regime. The n_s is laterally homogeneous and can be expressed as $n_s = C_G(V_{GS} - V_{th})/q$.[32] Therefore, the transistor acts like a resistor with a sheet resistance $1/(qn_s\mu)$ modulated by the gate voltage. In this regime, the current increases linearly with increasing V_{DS} according to:

$$I_{DS} = q\mu n_s\frac{W_G}{L_G}V_{DS} = q\mu\frac{W_G}{L_G}C_G\left(V_{GS} - V_{th}\right)V_{DS}. \tag{2.4}$$

For larger values of V_{DS} such that $V_{DS} \leq (V_{GS} - V_{th})$, the transistor still operates in the linear regime but the drain-to-source current increases with the increase of V_{DS} following a behavior well approximated by

$$I_{DS} = q\mu\frac{W_G}{L_G}C_G\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]. \tag{2.5}$$

At $V_{DS} = V_{DS,sat} = (V_{GS} - V_{th})$ the 2DEG channel is pinched-off at the drain side and the I_{DS} stays constant, independent of V_{DS}. In the saturation regime, the current reaches a saturation value which can be approximated by

$$I_{DS} = I_{DS,sat} = \frac{1}{2}\mu\frac{W_G}{L_G}C_G\left(V_{GS} - V_{th}\right)^2. \tag{2.6}$$

From the transfer (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) characteristics of HEMT devices, practical electrical parameters can be extracted to characterize the performance of the device, as schematically shown in Figure 2.6.

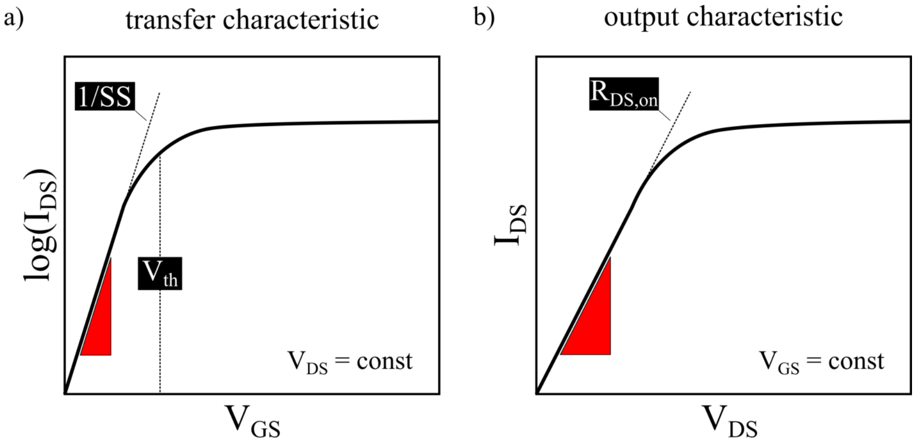


Figure 2.6: Schematic of HEMT (a) transfer and (b) output characteristics. The device parameters threshold voltage V_{th}, subthreshold slope SS and on-state drain-to-source resistance $R_{DS,on}$ are indicated.

The V_{th} of the device can be extrapolated from the transfer characteristic by various methods.[34] The peak transconductance method is used in this work. The transconductance represents the change in drain-to-source current I_{DS} resulting from a variation of the gate-to-source voltage V_{GS}, for a fixed value of V_{DS}:

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const}. \tag{2.7}$$

Another important parameter extracted from the I_{DS}-V_{GS} characteristic is the subthreshold swing (SS). The SS is the reciprocal value of the subthreshold slope in the subthreshold region and it indicates how sharply the drain-to-source current drops with the gate voltage. In the subthreshold region ($V_{GS} < V_{th}$), since the only charge carrier conduction from source to drain stems from electrons with a sufficiently high thermal energy to overcome the gate controlled potential barrier, this diffusion-limited subthreshold current is independent of V_{DS}, but varies exponentially with V_{GS}. By analogy with MOSFETs, the expression for the subthreshold slope in HEMTs is given by

$$SS = \left(\frac{\partial V_{GS}}{\partial(\log_{10} I_{DS})}\right)^{-1} = \ln(10)\frac{k_B T}{q}\left(1 + \frac{C_{GaN,depl}}{C_G}\right), \tag{2.8}$$

where k_B is the Boltzmann constant, T the absolute temperature and $C_{GaN,depl}$ is the capacitance of the depleted GaN buffer layer. Note that, since $C_{GaN,depl}$ is very small compared to C_G, values of the subthreshold swing close to the theoretical limit of $ln10\ (k_B T/q) \sim 60$ mV/dec at room temperature can be achieved. A low value of SS would increase the efficiency of the device to switch from the on-state to the off-state and vice versa. However, for Schottky-gate AlGaN/GaN HEMTs, the off-state drain current is strongly limited by the gate leakage currents due to the lack of an additional insulating material with a high conduction band offset under the gate metal.[35, 36]

The switching efficiency of the device is also given by the on-state drain-to-source resistance $R_{DS,on}$, which is another key parameter of AlGaN/GaN HEMT devices. As schematically shown in Figure 2.7, the $R_{DS,on}$ of a HEMT can be expressed as:

$$R_{DS,on} = R_c^S + R_{sh} L_{GS} + R_{sh}\left(V_{GS}\right) L_G + R_{sh} L_{GD} + R_c^D. \tag{2.9}$$

Here, $R_{DS,on}$ is given per unit gate width in Ω mm. $R_c{}^S$ and $R_c{}^D$ are the contact resistances of source and drain, respectively, L_{GS} is the gate-to-source distance, L_G is the gate length and L_{GD} is the gate-to-drain distance. R_{sh} is the sheet resistance of the 2DEG channel. A lower $R_{DS,on}$ is also preferred to achieve higher values of the saturation current and to reduce the energy power losses.

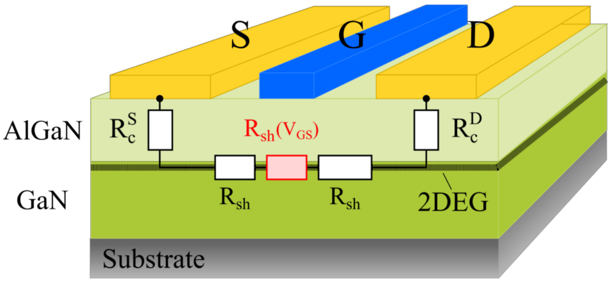


Figure 2.7: Schematic of the resistive elements contributing to the $R_{DS,on}$ of an AlGaN/GaN HEMT device.

The R_{sh} of the 2DEG channel depends on the sheet carrier density and mobility as follows:

$$R_{sh} = \frac{1}{q n_s \mu}. \tag{2.10}$$

Since the sheet carrier density and mobility are related to parameters of the heterostructure such as Al content and thickness of the AlGaN barrier layer, as discussed before, the optimization of the heterostructure in terms of n_s and μ results in a lower sheet resistance and higher power density of the device. Typical values of the sheet resistance range between 400 Ω sq^{-1} and 600 Ω sq^{-1}. Note that, since R_{sh} depends on the sheet carrier density, the contribution of R_{sh} coming from the region beneath the gate is a function of the gate voltage (see Figure 2.7). The $R_{DS,on}$ can be extracted from the inverse slope of the linear region of the output characteristic of HEMT devices (see Figure 2.6b).

The AlGaN/GaN HEMTs with a Schottky-gate have been making steady progress in high-frequency and high-power performances.[8, 37, 38, 39] However, HEMT devices suffer from an exceedingly high gate leakage current which makes a metal-insulator-semiconductor (MIS)-gate absolutely necessary for reduced power consumption as well as failure protection, especially in power switching transistors. In one part of the next chapter, AlGaN/GaN HEMTs with a Schottky-gate will be compared to metal-insulator-semiconductor (MIS)-HEMT devices.

3 Properties of epitaxial material and process modules for high device performance

A brief introduction to material design aspects of the AlGaN/GaN epitaxial layers suited for realizing high performance AlGaN/GaN devices is given in the following. Afterwards, the focus is moved to the main properties of gate and ohmic contacts process modules targeting high efficiency and reliable (MIS-)HEMT devices. Specifically, the main requirements that the gate dielectric layer integrated into MIS-gate structures has to meet for power applications are summarized and the influence of this additional layer on the device performance is discussed. Finally, fundamental concepts of ohmic contacts are reviewed and the main properties of the ohmic contacts to AlGaN/GaN heterostructures are described, with a particular attention to the current understanding on the contact formation and to the state of the art of gold-free ohmic contacts.

3.1 AlGaN/GaN epitaxial layers on Si

The AlGaN/GaN heterostructure is commonly grown by metal organic chemical vapor deposition (MOCVD) on foreign substrates, typically sapphire, silicon carbide or especially silicon, due to the lack of high-quality and cost-effective bulk GaN substrates. Taking advantage of the higher growth rates and cost-effective growth of the MOCVD process, this method has been predominantly used to fabricate transistors for power switching applications. In particular, AlGaN/GaN epitaxial material grown by MOCVD on silicon substrates is being now widely used as platform to realize (MIS-)HEMT devices for power electronics. Figure 3.1 shows a schematic cross-section of the typical epitaxial layer structure used for the fabrication of GaN-on-Si (MIS-)HEMTs.[7]

The extensive use of silicon as substrate material for GaN-based devices is mostly due to the low substrate cost, the availability of large-area substrates and the potential integration with the well developed Si electronics technology. The (111) Si plane is used because it supports the epitaxial growth of Ga-polar GaN in the [0001] direction,[40] which is the most used structure for electronic applications, as discussed in Section 2.1. Nevertheless, the production of high quality and crack-free GaN layers on silicon presents many challenges. The large lattice constant mismatch between Si and GaN results in a high dislocation density in the GaN channel layer which affects the crystalline quality of the material and significantly contributes to buffer leakage.[41] Even more severe, the large difference in the thermal expansion coefficients of Si and GaN leads to a large tensile stress during cooling from the growth temperature to room temperature, often resulting in cracking of

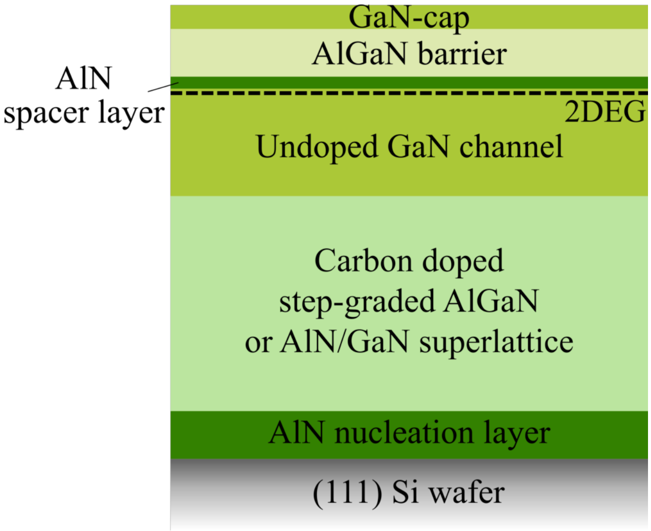


Figure 3.1: Schematic cross-section of the typical epitaxial layer structure used for the manufacture of GaN-on-Si HEMTs.

the GaN layers. Several strain management procedures have been developed to overcome these problems. In general, complex buffer layers including step-graded AlGaN layers or AlN/GaN superlattices are implemented to counteract the tensile strain and mitigate crack formation in the GaN epitaxial layers and to reduce the number of dislocations.[42, 43, 44] The detailed stack design is normally proprietary of the material supplier. A nucleation layer of AlN is also typically used to initiate growth and to prevent the reaction of Ga with Si which causes gallium silicide formation, often called meltback etching, and large growth defects. The control of residual impurities or the introduction of dopants in the GaN buffer layers is also of major importance as they can influence the resistivity of GaN-based materials, which in turn affects bulk leakage currents and electrical isolation between active devices and eventually device reliability. For example, carbon doping in the range of 10^{16} - 10^{17} cm^{-3} is often intentionally included during growth of the GaN buffer to compensate the unintentional doping and achieve highly insulating buffer layers. The presence of carbon doping has been demonstrated to suppress the vertical leakage current and to enhance the breakdown voltage,[45] but it has also been linked to current degradation mechanims due to trapping effects in the buffer layer.[46]

The top epilayers of the AlGaN/GaN 2DEG structure have been also extensively studied and designed in order to achieve high device performance.[47] The optimization of AlGaN/GaN heterostructure in terms of sheet carrier concentration and electron mobility, discussed in Section 2.2, has to also take into account the boundary conditions imposed from the growth of the epitaxial material. In fact, because of the lattice mismatch between AlN and GaN, the $Al_xGa_{1-x}N$ barrier layer thickness needs to be reduced with increasing the Al content x to avoid cracking. Relaxation of the AlGaN layer with the increasing thickness can be suppressed by growing a very thin GaN cap layer on top.[48] The GaN cap layer also helps to protect the AlGaN surface and to reduce gate leakage currents in the case of Schottky-gate devices. Another important aspect is the use of a thin AlN interlayer with a thickness of a few monolayers inserted between the GaN channel and the

AlGaN barrier layer. The larger energy bandgap of AlN compared to AlGaN gives a larger effective conduction band discontinuity which leads to a better confinement of the 2DEG wavefunction in the GaN channel layer at the AlN/GaN interface. This effect mainly mitigates alloy scattering at the AlGaN/GaN interface, thus enhancing the 2DEG electron mobility (see Section 2.2).[49] However, as discussed in Chapter 5, the higher energy barrier introduced on the Al(Ga)N barrier side of the heterojunction interface also poses challenges to achieve low-resistive ohmic contacts.[50, 51]

A comprehensive and more detailed overview on the various growth methods for GaN-based systems, on the substrate properties with respect to the requirements of III-N-based electronic devices and on the epitaxial layer design of AlGaN/GaN systems are given in [12, 20].

3.2 MIS-gate HEMTs

Despite AlGaN/GaN HEMT being a strong candidate for high-frequency and high-power applications owing to the enhanced mobility and saturation velocity, one of the key problems degrading its performance and reliability is the relatively high Schottky-gate leakage currents, resulting in reduced power efficiency and weak device failure protection.[52] The use of a metal-insulator-semiconductor (MIS)-gate where an insulator is introduced as gate dielectric layer at the metal/semicondutor interface, is an efficient way to supress the gate leakage currents. The significant reduction of gate leakage currents in the so called MIS-HEMTs compared to Schottky-gate HEMTs enables reduced power consumption, larger gate bias swing and better immunity to gate breakdown.[9, 53, 54] A comparison of the band diagrams of GaN-capped AlGaN/GaN heterostructures with Schottky-gate and MIS-gate is schematically illustrated in Figure 3.2.

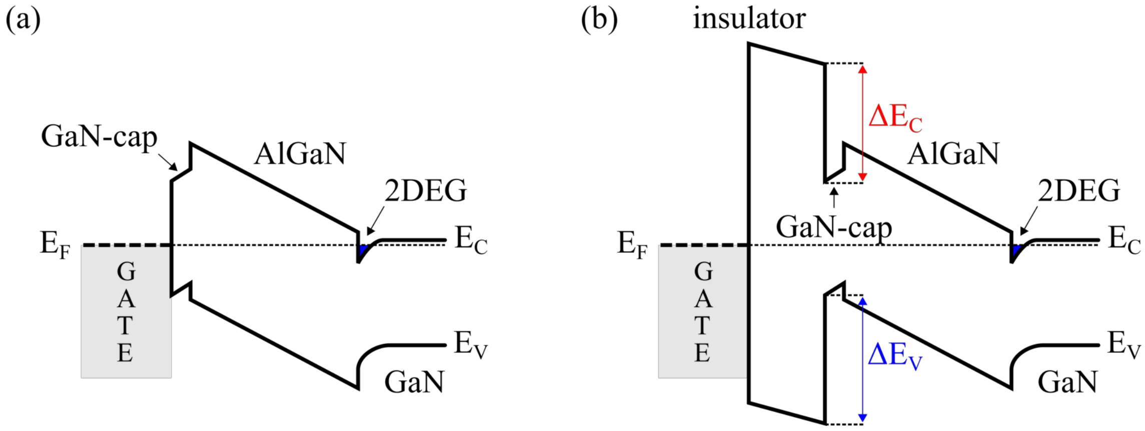


Figure 3.2: Comparison of band diagrams of (a) Schottky-gate and (b) MIS-gate without gate voltage applied. E_C and E_V are the conduction and valence bands of GaN, respectively. ΔE_C and ΔE_V are the conduction and valence band offsets of GaN with respect to the insulator. E_F denotes the Fermi energy.

The wide bandgap of the insulator introduces a larger energy barrier compared to the case without insulator, preventing the potential flow of electrons from the 2DEG channel to the metal gate. In Schottky-gate HEMTs, the situation is particularly critical under forward gate bias. In this case, the energy conduction band of the metal gate is pulled down so that the effective energy barrier represented by the AlGaN confining the electrons in the 2DEG at the AlGaN/GaN interface is significantly lowered. This represents a strong limiting factor especially in power switching applications where a large gate swing is required to prevent the device failure in case of faulty gate voltage over-shoots that often occurs in circuits. For this reason, MIS-HEMT devices are promising candidates to surpass Schottky-gate HEMTs as power switching devices.[8, 39, 55]

3.2.1 Gate dielectrics

The design of the MIS-gate for GaN-based HEMTs requires to consider the properties of bandgap, band offset with respect to GaN, permittivity, breakdown field and chemical stability of insulators. For a sufficient suppression of the gate leakage current even at forward bias, a large bandgap material as well as large bandgap offsets to GaN are necessary. On the other hand, dielectric materials with a high value of permittivity are preferred in order to obtain a high gate-to-channel coupling. In fact, in the case of a MIS-gate structure consisting of an insulator/GaN-cap/AlGaN/GaN structure (see Figure 3.2b), the gate-to-channel capacitance C_G is given by

$$C_G = \left(\frac{1}{C_{GaN-cap}} + \frac{1}{C_{AlGaN}} + \frac{1}{C_{ins}} \right)^{-1} = \varepsilon_0 \left(\frac{d_{GaN-cap}}{\varepsilon_{GaN-cap}} + \frac{d_{AlGaN}}{\varepsilon_{AlGaN}} + \frac{d_{ins}}{\varepsilon_{ins}} \right)^{-1}, \tag{3.1}$$

where ε_0 is the vacuum permittivity, ε is the relative permittivity, C is the capacitance per unit area and d is the layer thickness. The subscripts $GaN\text{-}cap$, $AlGaN$ and ins indicate the values of the physical quantities corresponding to the GaN-cap, AlGaN and insulator layers of the MIS-gate stack. The gate-to-channel capacitance of MIS-HEMTs accounts for the additional insulator layer introducing a capacitive element connected in series to the ones of the GaN-cap and AlGaN layers. This leads to a reduction of the gate-to-channel capacitance with respect to the conventional HEMTs without dielectric, which in turn is detrimental for the transconductance of the device. As one can see from Equation 3.1, the use of high permittivity dielectric layers is favourable to reduce the capacitive contribution of the gate dielectric and to obtain a stronger coupling between the gate and the 2DEG channel.

Various dielectric materials have been employed to convert a Schottky-gate to a MIS-gate.[8, 11] Figure 3.3a reports the relationship between bandgap and permittivity for relevant insulators and nitride compounds, while Figure 3.3b shows the band offsets between those insulators and GaN, calculated by Robertson and Falabretti.[56] Even though SiO_2 posseses large bandgap and large band offset to GaN and high performance MIS-HEMTs using SiO_2 have been already demon-

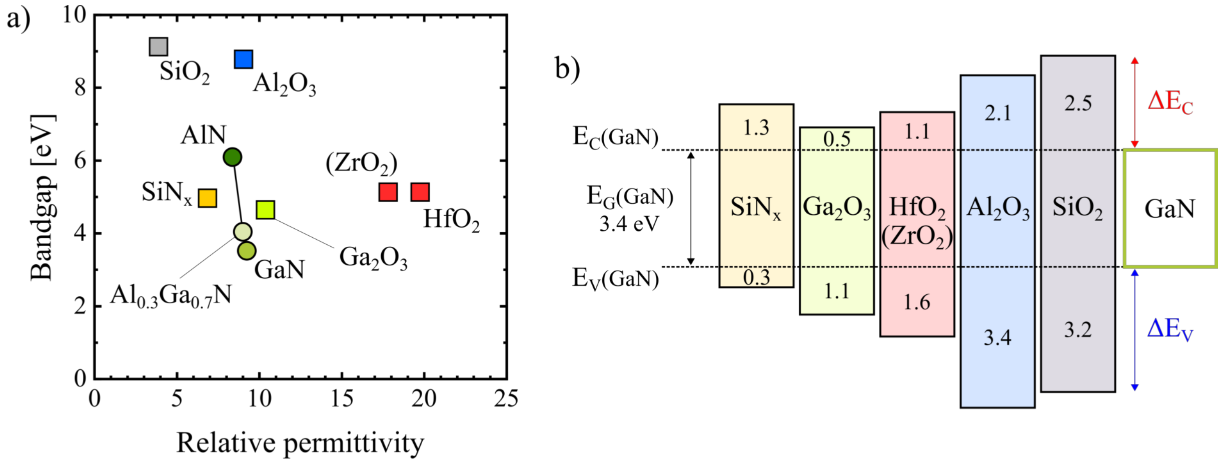


Figure 3.3: (a) Energy bandgap versus permittivity for various insulators and GaN compounds. (b) Conduction and valence band offsets, ΔE_C and ΔE_V respectively, of various dielectric materials with respect to GaN, calculated by Robertson and Falabretti.[56] The conduction band E_C and valence band E_V of GaN are marked as dashed lines. The energy bandgap E_G of GaN is also indicated.

strated,[53, 57, 58] its relatively low dielectric constant represents a disadvantage compared to other dielectrics. MIS-gate structures employing SiN_x and Ga_2O_3 and high permittivity dielectrics such as HfO_2 and ZrO_2 have been instead reported to be relatively suscettible to leakage problems, due to the relatively low band offsets with respect to GaN.[8, 11] However, among these dielectrics, SiN_x deposited in-situ or by low-pressure chemical vapor deposition (LPCVD) is now emerging as promising candidate.[59, 60] On the other hand, Al_2O_3 is very attractive as gate dielectric for AlGaN/GaN MIS-HEMTs because of its large bandgap and conduction-band offset to GaN, relatively high permittivity as well as high breakdown field (∼10 MV/cm) and thermal and chemical stability against AlGaN.[9, 61, 62, 63] Additionally, the considerable technological progress in the atomic layer deposition (ALD) process enables the deposition of high-quality Al_2O_3 films to gate structures in GaN transistors. For these reasons, Al_2O_3 deposited by ALD as gate dielectric of MIS-HEMT devices is further investigated in this work.

In terms of device reliability, the device behavior is modified with the incorporation of dielectrics. If the dielectric is deposited both underneath the gate as well as between the gate and the ohmic contacts of source and drain, it functions both as gate dielectric and passivation layer.[10] The use of various dielectrics as passivation layer has been reported to mitigate the effects of drain current-collapse and leakage currents at the (Al)GaN surface due to the passivation of trap states at the heterostructure surface.[10, 64, 65, 66] Neverthless, the performance and device reliability of MIS-HEMTs is still mainly limited by trapping effects under the gate caused by trap states located at the dielectric/III-nitride interface or within the dielectric. The intrinsic defectiveness of the dielectric layer and that of the corresponding interface with the III-nitride epitaxial structure are still intensively investigated for optimization of devices.

3.2.2 Dielectric trapping effects

The insertion of a gate dielectric introduces new reliability problems related to the presence of interface traps at the insulator/GaN interface or bulk traps within the dielectric. Interface trap states can lead to dynamic charge/discharge processes which are critical especially in the case of wide bandgap GaN-based materials where traps can be deeply located in the bandgap and can result in a significant threshold voltage instability due to their extremely slow detrapping behavior. Similarly, bulk traps inside the gate dielectric, especially border traps near the interface, could exchange carriers with the channel under forward and reverse gate bias stress, also resulting in gradual shift of the threshold voltage and possible gate degradation. The V_{th} instability due to trapping related to the gate dielectric under different bias conditions in AlGaN/GaN-based MIS-HEMTs has been often reported.[67, 68, 69, 70] These trapping mechanisms are especially critical under forward gate bias where electrons can spill-over from the 2DEG channel towards the dielectric by overcoming the AlGaN barrier.[71, 72, 73, 74] A schematic illustration of the band diagram of a MIS-gate structure at zero gate voltage bias and under forward gate bias and the corresponding trap states involved is shown in Figure 3.4.

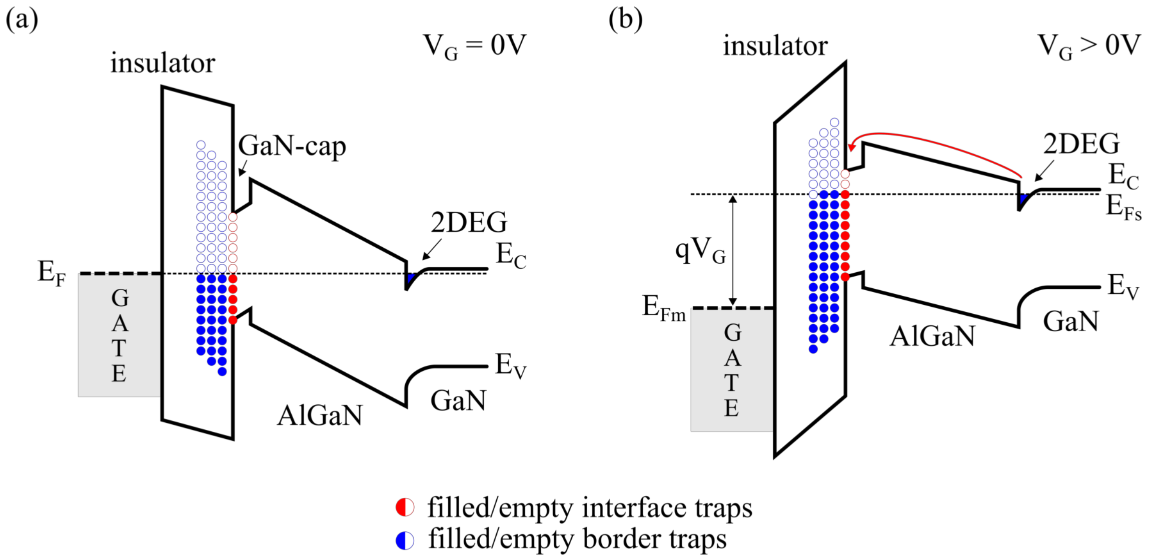


Figure 3.4: Schematic band diagrams of the GaN-capped AlGaN/GaN heterostructure with insulator as gate dielectric at (a) zero bias (V_G = 0 V) and (b) under forward bias (V_G > 0 V). Electrons can overcome the AlGaN barrier from the 2DEG channel and be trapped in the states located at the insulator/GaN interface or within the insulator. E_F denotes the Fermi energy at 0 V gate voltage, while with a gate voltage applied E_{Fm} is the Fermi level in the metal and E_{Fs} is the Fermi level in the semiconductor.

The minimization of trap states at the dielectric/III-N interface and of border traps within the dielectric, affecting long term gate reliability and device performance, is a critical challenge for GaN-based MIS-HEMTs. In the same way, the accurate characterization of trap states is essential to understand the reliability issues associated with the MIS-gate and to evaluate the effectiveness of various insulators employed as gate dielectric as well as of process variations for interface treatment. The most widely adopted techniques to characterize interface traps are conductance dispersion technique, frequency and/or temperature dependent capacitance voltage measurements, photo-assisted capacitance-voltage analysis and pulsed measurement techniques. In general, the evaluation of the interface traps is challenging due the presence of two interfaces which complicates the potential distribution over the structure and due to the low emission rate of electrons in wide bandgap GaN-based semiconductors.[74, 75, 76] For example, the conventional conductance method may lead to an underestimation of the interface trap states due to the presence of the additional capacitance introduced by the AlGaN barrier.[77] A comprehensive overview comparing the methods commonly used to characterize interface traps in GaN-based MIS-HEMT devices and their main limitations is given by Narayanan et al.[78]

In the next chapter, the frequency-dependent capacitance-voltage method and the pulsed current-voltage measurement technique are presented. Using these methods, the characterization of trap states at the Al_2O_3/III-N interface and the evaluation of device performance in terms of V_{th} stability under forward gate bias stress condition are performed in Chapters 6 and 7.

3.3 Ohmic contacts to 2DEG

An ohmic contact is defined as a metal/semiconductor contact which has a negligible junction resistance compared to the total resistance of the device. In this way, the voltage drop across the ohmic contact is small compared to the one across the active region of the device and the necessary current can be supplied without significantly perturbing the device performance. Ohmic contacts exhibit linear current-voltage characteristics and are fundamental building blocks of any semiconductor device as they provide the link between the device and the external circuitry. However, obtaining good ohmic contacts to AlGaN/GaN heterostructures is inherently difficult due to the wide energy band gap of GaN-based materials which typically leads to large values of the Schottky barrier height at the metal/semiconductor interface.[13, 79]

3.3.1 Basic physics of ohmic contacts

In general, when a metal is placed in contact with a semiconductor, a Schottky barrier is formed at the metal/semiconductor interface. In the case of an ohmic contact, this potential barrier is absent or transparent for charge carrier tunneling. The physical parameter describing the perfomance of ohmic contacts is the specific contact resistivity ρ_c, which is independent of the contact geometry and is typically expressed by $\Omega\ \mathrm{cm}^2$. In general, given the current density J and the applied voltage V, the specific contact resistivity can be defined as

$$\rho_c = \left(\frac{dJ}{dV}\right)^{-1}_{V=0}. \tag{3.2}$$

In ohmic contacts, the specific contact resistivity depends on the metal/semiconductor Schottky barrier height Φ_B and on the doping level of the semiconductor N_D. Depending on the doping level N_D of the semiconductor, different mechanisms dominate the carrier transport at the metal/semiconductor interface.[19, 80] The conduction mechanisms for a metal/n-type semiconductor are schematically illustrated in Figure 3.5.

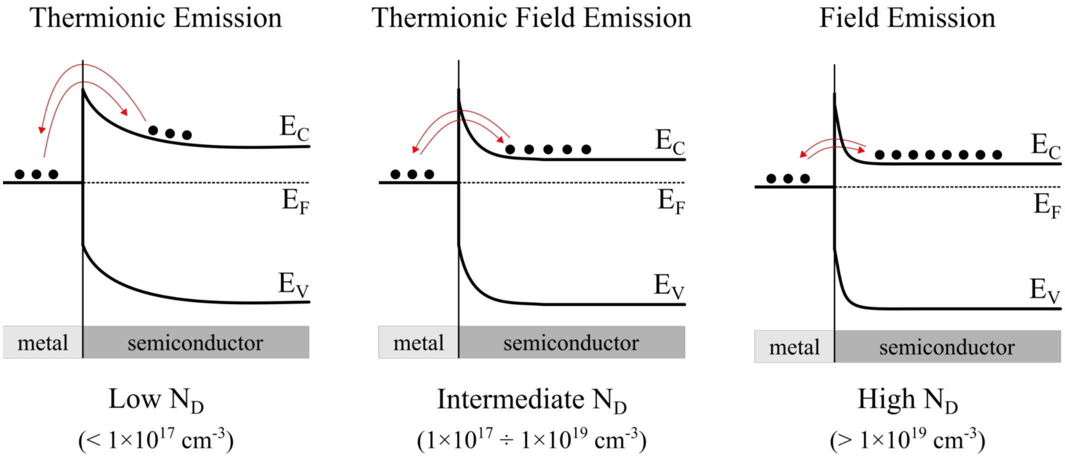


Figure 3.5: Schematic illustration of the different carrier transport mechanisms through a metal/n-type semiconductor barrier for different doping level N_D.

For lightly doped semiconductors, thermionic emission (TE) dominates the carrier conduction with electrons thermally excited over the barrier. In this case, the ρ_c can be described as

$$\rho_c = \frac{k_B}{qA^{**}T} \exp\left(\frac{\Phi_B}{k_B T}\right), \tag{3.3}$$

where A^{**} is the modified Richardson constant.[19]

In the intermediate doping range, thermionic field emission (TFE) becomes dominant consisting of electrons thermally excited to an energy level where the barrier is sufficiently narrow to permit tunneling. For TFE, the specific contact resistivity is given by [81, 82, 83]

$$\rho_c = \left(\frac{k_B}{qA^*}\right) \frac{k_B}{\sqrt{\pi\left(\Phi_B + u_F\right) E_{00}}} \cosh\left(\frac{E_{00}}{k_B T}\right) \sqrt{\coth\left(\frac{E_{00}}{k_B T}\right)} \exp\left[\frac{\Phi_B + u_F}{E_0} - \frac{u_F}{k_B T}\right], \tag{3.4}$$

where u_F is the Fermi level position with respect to the conduction band edge and A^* is the effective Richardson constant given by

$$A^* = \frac{4\pi q m^* k_B^2}{h^3}, \tag{3.5}$$

being m^* the effective electron mass of the considered semiconductor and h the Planck´s constant. E_{00} is the characteristics energy defined as

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\epsilon\epsilon_0 m^*}}, \tag{3.6}$$

and

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{k_B T}\right). \tag{3.7}$$

For high doping density, the barrier width is narrow enough so that electrons can tunnel directly through the interface by field emission (FE). In this regime the ρ_c is expressed by [81, 82, 83]

$$\rho_c = \left[\frac{A^*\pi qT}{k_B \sin\left(\pi c k_B T\right)}\exp\left(-\frac{\Phi_B}{E_{00}}\right) - \frac{A^* q}{c k_B^2}\exp\left(-\frac{\Phi_B}{E_{00}} - c u_F\right)\right]^{-1}, \tag{3.8}$$

where

$$c = \frac{1}{E_{00}}\ln\left(\frac{4\Phi_B}{u_F}\right). \tag{3.9}$$

Previous Equations 3.3, 3.4 and 3.8, describing each regime of carrier transport, contain different functional dependences dominating the behavior of ρ_c. These are summarized in the following for simplicity:

$$\rho_c \propto \exp\left(\frac{\Phi_B}{k_B T}\right), TE \tag{3.10}$$

$$\rho_c \propto \exp\left[\frac{\Phi_B}{E_{00}\coth\left(\frac{E_{00}}{k_B T}\right)}\right], TFE \tag{3.11}$$

$$\rho_c \propto \exp\left(\frac{\Phi_B}{E_{00}}\right), FE \tag{3.12}$$

Particularly, as shown in Chapter 5, for fixed values of Φ_B and N_D, the dependence of the specific contact resistivity with temperature, which is much more pronounced in TE and TFE, can be used to investigate and differentiate the mechanism of carrier transport through the metal/semiconductor interface of ohmic contacts.

A more practical parameter commonly used which represents the total resistance of the metal/semiconductor junction is the contact resistance R_c. The contact resistance depends on the area of the contact and is expressed in Ω. For lateral devices, R_c is expressed in Ω mm since it is typically given per unit gate width of the device. As discussed in Section 4.3, the R_c is the parameter which is directly accessible by measurements using the transfer length method (TLM). Also, this parameter is useful because it is closely related to the overall on-state drain-to-source resistance of HEMT devices (see Section 2.3). The relation between ρ_c and R_c in a metal/semiconductor contact can be seen anagously to that between the resistivity and resistance in a resistor. However, as discussed in Section 4.3.1, since for lateral devices such as AlGaN/GaN HEMTs the actual contact area which is crossed by the current can be different from the physical area of the contacts, obtaining the specific contact resistivity from the contact resistance can be difficult and requires to take into account the nature of the current flow and contact geometry.

3.3.2 Formation of ohmic contacts to AlGaN/GaN

Low-resistive ohmic contacts to AlGaN/GaN heterostructures are difficult to achieve due to the wide band gap of AlGaN and to the absence of metals with work function low enough to prevent the formation of a Schottky barrier at the metal/semiconductor interface. In fact, a thermal annealing is required to induce some metal/semiconductor interactions in order to favour ohmic contact formation with a change of the contact characteristics from non-linear to linear.[13, 84]

Titanium has been the most popular metal used for ohmic contacts to AlGaN/GaN. In fact, even though Ti with a work function of 4.33 eV forms a Schottky contact to GaN and AlGaN, Ti-based metallization schemes have been successfully applied to GaN and later on to AlGaN/GaN systems to achieve reliable and low-resistive ohmic contacts. Specifically, most of the conventional ohmic contacts to AlGaN/GaN are metallization schemes based on Ti/Al layers provided of a x/Au stack (x = Ni, Ti, Pt, Pd, Mo, etc.) as capping layers.[13, 85, 86, 87, 88] Au has been mainly employed because it is suitable to both prevent oxidation and lower the metal stack resistivity,[89] while the x-layer is used in order to limit interdiffusion of Au with layers underneath. The ohmic contact formation generally requires a high temperature annealing ($\geq$800 °C) which leads to contact resistance values below 1 Ω mm. An extensive review and collection of relevant literature results on ohmic contacts to GaN-based materials is given by Greco et al.[13]

The current understanding of the actual mechanim of ohmic contact formation to AlGaN/GaN heterostructures is not clear yet. In fact, in this case the mechanim of contact formation is even more complicated than in the case of GaN due to the presence of the 2DEG at the AlGaN/GaN interface which is separated from the metal contact by the AlGaN barrier. For Ti/Al-based ohmic contacts annealed at high temperatures, the most established mechanism involves the extraction of nitrogen from the AlGaN barrier, forming TiN protrusions penetrating the AlGaN along threading dislocations.[86, 90, 91, 92, 93, 94] The latters are most likely responsable of a direct contact between the metal penetrating the AlGaN and the 2DEG, which can in turn lead to a more efficient carrier transport with respect to tunneling through the AlGaN. Shriki et al. claim that Au has the main role in the formation of TiN protrusions in Au-containing ohmic contacts.[92] The Ti/Al ratio has been reported to also play a role in the reaction kinetics with the underlaying AlGaN layer and in the formation of protrusions below the contact.[95, 96] Metal protrusions contacting directly the 2DEG have been also observed for Au-containing V-based ohmic contacts.[97] An alternative or additional mechanism for the ohmic contact formation in the absense of TiN protrusions is the formation of N vacancies throught extraction of nitrogen from the AlGaN barrier.[98] The N vacancies can act as n-type doping for AlGaN enhancing the tunneling probability of electrons through the AlGaN potential barrier.[99] However, at this time there is no direct experimental confirmation of the existance of those vacancies linked to the ohmic contact formation to AlGaN/GaN heterostructures.

Althouth the current understanding of the ohmic contact formation is still under debate, low-resistive ohmic contacts have been achieved and successfully implemented in HEMT devices.[7] However, further developments of the ohmic contact manufacturing process are still necessary. Firstly, the high annealing temperatures required for ohmic contact formation can result in an increase of the sheet resistance due to thermal degradation of the heterostructure without proper surface passivation.[100] Also, when using high annealing temperatures the low melting point of Al ($\sim$660 °C) and the use of a Au cap layer are responsible for a rough surface morphology and poor edge acuity of the contacts after annealing,[85, 101, 102] representing a serious concern for downscaling the device. Therefore, the use of a lower thermal budget for the ohmic contacts annealing is necessary to favor thermal stability and add flexibility and opportunities in device process integration, enabling for example the implementation of a gate-first architecture. Secondly, as discussed in the next section, since Au is an undesired source of contamination in Si CMOS technology, Au-containing metal schemes prevent the possibility to manufacture GaN-based devices in the existing Si technology production lines. Therefore, another essential requirement is the replacement of the well extablished Au-containing ohmic contacts with a Si-compatible Au-free ohmic contact technology.

3.3.3 Au-free ohmic contacts to AlGaN/GaN

The manufacturing of GaN-based devices using GaN-on-Si platforms into existing Si facilities comes along with cost benefits with respect to their processing in dedicated III-V fabs, which are unsuited for a cost-effective and large-scale device production. However, Au represents an undesired source of contamination in the Si production lines as it rapidly diffuses into Si at relatively low temperatures forming mid-gap states which can affect the device reliability and lead to premature device failure.[103] Therefore, the replacement of Au-containing ohmic contacts with a fully Si CMOS-compatible Au-free ohmic contact technology to AlGaN/GaN heterostructures is essential for the advent of (MIS-)HEMT devices.

In recent years, different approaches and several Au-free contact schemes have been proposed to obtain low-resistive Au-free ohmic contacts to AlGaN/GaN. Attempts such as intentional doping of the AlGaN barrier,[104] doping of the AlGaN/GaN heterostructures by Si ion-implantation,[105, 106] or n-type doped GaN layers grown underneath the contact,[107] eventually lead to a degradation of the electrical properties of AlGaN/GaN heterostructures. Therefore, as in the case of Au-containing ohmic contacts, the most frequently used approach consisted of using metals with a low work function. Ti-based and Ta-based contacts have been the most explored metallization schemes. Focusing on Au-free contacts annealed at low temperatures, only few studies using Ti-based and Ta-based metal stacks reported of low-resistive ohmic contacts obtained for annealing temperatures lower than 650 °C.[95, 108, 109, 110, 111, 112, 113, 114, 115] For Au-free Ti/Al-based contacts, metal stacks using tungsten as capping layer have achieved contact resistance values of about 0.6 Ω mm when annealed at 600 °C.[108] Even lower values of the contact resistance have been only demonstrated at higher annealing temperatures. Malmros et al reported an extremely low contact resistance of about 0.1 Ω mm using Ta/Al/Ta metal stacks annealed at 550 °C.[109] The use of Ti/Al-based and Ta/Al-based metal stacks has been also successfully combined with a recess technique of the AlGaN barrier to obtain low-resistive and low-temperature annealed ohmic contacts.[110, 111, 116] More complex stacks have been also employed to obtain Au-free ohmic contacts.[7, 117] For example, Van Hove et al. applied a Si/Ti/Al/Ti/TiN ohmic metal scheme annealed at 565 °C to obtain a contact resistance of 0.3 Ω mm,[7] since the addition of a Si-containing layer in the ohmic metal stack was shown to result in a lower contact resistance due to the formation of interfacial Ti-Si alloys.[117, 118]

Despite the great interest in Au-free ohmic contacts to AlGaN/GaN heterostructures, as in the case of Au-containing ohmic contacts, the mechanism responsable for ohmic contact formation is not yet fully understood. In general, low-resistive and Au-free ohmic contacts are more difficult to achieve with respect to Au-containing contacts and their properties depend on the AlGaN/GaN heterostructure properties, such as thickness and Al content of the AlGaN barrier and also on the metal/semiconductor interface.[13, 95, 119] Differently from Au-containing ohmic contacts, in Au-free ohmic contacts the creation of metallic protrusions into the AlGaN/GaN heterostructure have not been reported. In fact, the absense of Au in Ti/Al-based metal stacks has been claimed to favour the intacticity of the AlGaN barrier, preventing the inclusion of metal tips into the barrier with respect to the same metal schemes using Au as capping layer.[92] Similar results have been obtained comparing Au-containing and Au-free V-based ohmic contacts.[120] For these reasons, the most established mechanism for ohmic formation in the case of Au-free Ti/Al-based or Ta/Al-based contacts involves the creation of N vacancies in the AlGaN acting as n-type doping, as a consequence of the out-diffusion of N atoms from the AlGaN barrier layer and the possible formation of TiN or TaN.[92, 109] Also in this case, there is no direct experimental confirmation of N vacancies formation and the behavior of Au-free ohmic contacts to AlGaN/GaN heterostructures remains still unclear and requires further investigations. For this reason, the nature of the current transport in Au-free Ta/Al-based ohmics contacts annealed at low temperatures is analyzed in detail in Chapter 5.

4 Experimental methods

In this chapter the experimental procedures applied in this Ph.D work are explained and discussed. First, the main technological processes used for the fabrication of the different test structures are briefly introduced. Afterwards, the detailed fabrication steps of ohmic contacts and MISH capacitors as well as the process flow of MIS-HEMT devices are presented. Finally, the electrical characterization techniques applied to the fabricated structures and the resulting parameters are described and discussed.

4.1 Processing technology

The main technological processes used in this work are presented and described in the following. In Section 4.2, reference to these processes will be made when describing the fabrication process of the test structures used in this thesis.

4.1.1 Mesa etching

Electrical isolation is one of the primary and essential process steps for the fabrication on AlGaN/GaN heterostructure materials. The 2DEG present at the AlGaN/GaN interface represents a conductive path which can lead to leakage currents flowing between neighbouring structures. Therefore, an electrical isolation is required in order to efficiently isolate the electrical active area of each structure and prevent their electrical interaction. Mesa isolation is the simplest isolation technology consisting in creating islands of active layer by etching through the 2DEG location and physically interrupting the 2DEG path between adjacent structures. The etching of the AlGaN and GaN layers can be realized using either wet chemical etching or dry etching techniques. However, due to the poor etch results of wet chemical etching for the group-III nitrides, dry etching is the most common etching technique used.[121] In particular, among several dry etching methods, the reactive ion etching (RIE) assisted by inductively coupled plasma (ICP) is commonly employed.[122] A major benefit of ICP-RIE compared to pure RIE is the presence of the additional ICP source to separately control the RF plasma generation from the RF power at chuck. As a result, the plasma density and particle energy can be effectively decoupled in order to significantly reduce the possibility of plasma damage at high etching rates. The plasma chemistries to etch AlGaN/GaN are commonly chlorine-based, such as Cl_2/Ar or BCl_3/Cl_2, due to the volatility of the group III-chlorides produced during etching.[123, 124, 125] In this work, ICP-RIE based on a gas mixture of BCl_3/Cl_2 is applied for mesa isolation with etch depth of $\sim$ 300 nm. The etching is carried out by using a Plasmalab System133 from Oxford Instruments with an ICP380 source.

4.1.2 Surface preconditioning

Cleaning and processing of GaN and AlGaN surfaces prior to metal or dielectric depositions have been shown to be of critical importance in the optimization of the device performance.[10] Surface contaminations are indeed present on the GaN and AlGaN surfaces which are commonly related to carbon and oxygen as part of native oxides, absorbates and residual species.[126] For this reason, different treatments based on for example wet chemicals, vacuum or gas annealing and plasma cleaning have been proposed to remove native oxides as well as organic and inorganic contaminations. Among them, O_2 plasma treatments combined with acid wet cleaning revealed to be particularly effective at removing oxides and contaminants, which consist mostly of carbon and oxygen, and resist residuals.[127, 128] In this work, a similar treatment consisting of a partial oxidation of the first epitaxial layers by a remote O_2 plasma, and a subsequent selective removal of the formed oxide by HCl wet cleaning is applied to the GaN surface. The latter will be referred to as surface preconditioning (SPC) and it will be applied in two steps of the fabrication process flow of the different test structures used in this thesis (see Section 4.2). First, it is employed before the metal deposition for the ohmic contacts to remove residuals from the GaN surface and ensure a high quality of the metal/GaN interface. Secondly, the SPC is used prior to the deposition of the gate dielectric of MIS-gate modules with the aim of cleaning and restoring the morphology of the GaN surface affected by the fabrication processes before the dielectric deposition, as for example thermal annealing for the ohmic contact formation. In the latter case, since the quality of the dielectric/GaN interface of the gate module is of critical importance in terms of device reliability, in Chapters 6 and 7, the impact of the SPC treatment on the morphology of the GaN surface and on the electrical properties of the Al_2O_3/GaN interface in MISH capacitors and MIS-HEMT devices is discussed.

4.1.3 Physical vapor deposition

Physical vapor deposition (PVD) refers to a variety of vacuum deposition methods of thin films based on the evaporation of solid precursors into their vapor phase by physical approaches, followed by the condensation of the vapor phase on substrates.[129, 130] PVD processes allow the deposition of mono-layered or multi-layered systems, as well as special alloy composition and structures and are classified based on the method used to evaporate the solid source materials into their vapor phase.[131, 132] In this work, the PVD methods of thermal evaporation and sputtering are applied.

Thermal Evaporation

Deposition by thermal evaporation relies on the vaporization of the source material by heating, e.g. by a resistive heater, an electron beam or a laser pulse. The atomic particles generated from the target are directed to the substrate material in a vacuum environment generating a physical coating by condensation. Evaporation is carried out in high vacuum conditions ($\sim 10^{-6}$ Torr) so that contamination of the substrates is minimal. However, during deposition some contaminant particles can be released from the melted coating material and moved onto the substrate, thereby reducing the purity of the obtained films. Additionally, the large mean free path of the gas molecules at low pressure leads to a poor step coverage and shadowing effects. Moreover, the high-vacuum pressure results in lower energies and less adsorption of the gas species which lead to a poor adhesion of the particles to the substrate. A further important disadvantage is that thin film deposition by thermal evaporation of defined alloy/composite materials and source materials with high melting points (e.g. Ta) are difficult to achieve. Despite the disadvantages, since this technique presents higher deposition rates when compared with the sputtering process, it is usually used for thicker films and coatings with lower surface morphological and stoichiometry requirements. Thermal evaporation is used here for the deposition of Ti/Al/Ni/Au ohmic contacts and Ti/Au gate electrodes of MISH capacitors and MIS-HEMT devices (see Section 4.2). The Al and Au layers are thermally evaporated by a resistive heater, while the Ti and Ni layers are deposited by electron beam evaporation.

Sputtering

Sputtering is a deposition process where atoms of the material to be deposited are released from a solid target by bombardment through energetic particles such as ions and atoms. The atoms released from the target can be then deposited as thin film on the substrate. The simplest approach consists in applying a DC potential between the target (cathode) and the substrate (anode). At a sufficient high electric field, a plasma is then generated by introducing an inert gas, typically Argon (Ar), into the vacuum chamber. Due to the potential difference, the Ar^+ ions are accelerated towards the target surface and generate vapors that will finally condensate on the substrate surface. Sputtering is typically carried out at a higher base pressure than evaporation ($\sim 10^{-2}$ Torr). However, DC sputtering suffers from low deposition rate and is not applicable to non-conductive target materials due to charging effects. Therefore, RF configurations are often used for sputtering insulating materials where the potential between the target and substrate is alternating and the accumulation of charges on the target is avoided. These configurations also allow lower operation pressure ($\sim 10^{-3}$ Torr). The enhancement of the deposition rate at even lower pressure can be obtained by using magnetron sputtering. In this configuration, the employment of magnetrons placed near the target confines the charged plasma particles close to the target surface enhancing the sputtering and deposition rates. One additional method for sputtering films with different compositions is reactive sputtering where the inert gas is mixed with reactive gases (N_2, O_2, etc.) which react with the target vapors to form oxide or nitride films. Therefore, PVD by sputtering can be used to deposit a broader range of materials compared to evaporation, including materials with high melting point and alloys. The use of targets with larger area also permits to cover a larger area of deposition and to obtain a better film uniformity. The higher energy of the sputtered particles gives a better adhesion to the substrate and film densification. Additionally, sputtering results in an excellent step coverage even of sharp topologies due to lower vacuum conditions. Disadvantages of sputtering compared to evaporation are instead lower deposition rate and more difficulty to achieve good lift-off technology due to a greater conformality of the deposited films. In this work, sputtering is carried out by a CT200 PVD tool from Alliance Concept which is used for the deposition of the alternative Ta/Al/x (x= Ta, TiN and TaN) ohmic contacts (see Section 4.2). In particular, magnetron RF sputtering is used for the Ta and Al layers. As previously mentioned, the high melting point of Ta of $\sim$ 3000 °C would be a critical point in case of evaporation. The TiN and TaN used as capping layers are instead deposited by DC reactive sputtering where N_2 is mixed to the vapors sputtered from the Ti and Ta targets to obtain TiN and TaN, respectively.

4.1.4 Atomic layer deposition

Atomic layer deposition (ALD) is a chemical vapor deposition technique based on sequential and self-limiting surface reactions which enable the deposition of highly conformal and uniform ultra-thin films.[133, 134, 135] A typical ALD process consists of several ALD cycles and each cycle includes the following steps:

1. Pulse precursor A into the chamber which reacts with the substrate surface through a self-terminating chemical reaction.
2. Purge with an inert gas (typically N_2 or Ar) to remove the unreacted precursor and reaction by-products.
3. Pulse precursor B which reacts in a self-terminating way with the already adsorbed species (A) on the substrate surface.
4. Excess species of precursor B and reaction byproducts are purged or pumped away from the substrate.

Due to the self-limiting nature of the surface reactions of step 1 and 3, the thickness of ALD films can be precisely controlled at the atomic level and tailored by the number of ALD cycles. Typical ALD growth rates in terms of growth per cycle are 0.5-1 Å/cycle. Moreover, excellent step coverage and conformality even on high aspect ratio and 3D structures can be achieved. Further advantages are that ALD typically involves the use of relatively low deposition temperatures (<350 °C), it is capable of depositing a variety of thin film materials and is extendible to large substrates. Main disadvantages are the slow deposition rate and the high costs of reactants and equipments. The ALD technique is utilized in this work by a customized ALD tool from Roth and Rau for the deposition of Al_2O_3 used as gate dielectric layer in MISH capacitors and MIS-HEMT devices. Trimethylaluminium (TMA) and O_3 are used as precursors for the Al_2O_3 deposition at a deposition temperature of 300 °C with a growth per cycle of 0.09 Å/cycle.

4.1.5 Thermal annealing

Although the actual mechanism of the formation of ohmic contacts to AlGaN/GaN heterostuctures is still not fully understood, the transition from a non-linear to an ohmic characteristic is obtained by applying a rapid thermal annealing (RTA) treatment to the metal stacks used as contacts.[13] In this work, a RTA treatment is performed for the fabrication of ohmic contacts by using an AST SHS-2800 RTP system. Specifically, for the Ti/Al/Ni/Au metal stack a high annealing temperature of 850 °C is applied for 30 seconds in a N_2 atmosphere. Differently, in the case of the Ta/Al/x (x= Ta, TiN and TaN) metal stack lower annealing temperatures ranging between 500 °C and 600 °C applied for 3 minutes in N_2 ambient are sufficient to obtain ohmic characteristics.

Thermal annealing is also employed as postdeposition or postmetallization treatment in order to reduce deep-level traps and interface states at the dielectric/GaN interface.[10] In fact, even if the mechanism of passivation of the critical electronic states is not fully understood, both postdeposition annealing (PDA) in different forms of N_2 plasma and postmetallization annealing (PMA) in N_2 gas ambient have been shown to be effective ways to increase the device performance. For this reason, the PMA treatment in N_2 atmosphere with annealing temperatures ranging between 300 °C and 400 °C for 10 minutes is also used in this work after the metal gate electrode deposition of MISH capacitors and MIS-HEMT devices. The PMA is carried out using an ATV SRO 796 RTA furnace. In Chapter 6, the effects resulting from this treatment on the interface trap states at the Al_2O_3/GaN interface are investigated.

4.2 Fabrication of test structures

The fabrication of the test structures is performed by contact lithography on commercial GaN-capped AlGaN/GaN epitaxial material grown by metal organic chemical vapor deposition (MOCVD) on Si(111)-substrates. The main properties of the used heterostuctures are summarized in Table 4.1. The epitaxial structures differ in terms of GaN-cap and AlGaN barrier thicknesses, Al mole fraction and the presence of an AlN spacer layer. R_{sh} is also indicated which denotes the mean value of the 2DEG sheet resistance of the as-grown epitaxial material.

Table 4.1: Epitaxial heterostructures used in this work.

	Epi I	**Epi II**	**Epi III**	**Epi IV**
Cap	GaN, 3 nm	GaN, 3 nm	GaN, 3 nm	GaN, 2 nm
Barrier	$Al_{0.22}Ga_{0.78}N$, 30 nm	$Al_{0.22}Ga_{0.78}N$, 30 nm	$Al_{0.25}Ga_{0.75}N$, 25 nm	$Al_{0.25}Ga_{0.75}N$, 22 nm
Interlayer	AlN, 1 nm	-	-	-
Channel	GaN	GaN	GaN	GaN
R_{sh} [Ω sq^{-1}]	420 ± 20	480 ± 20	420 ± 20	450 ± 20

The processing of all type of fabricated structures starts with the isolation of the electrical active areas by mesa etching performed with a BCl_3/Cl_2 ICP-RIE process (see Section 4.1). Afterwards, metal and insulator layers are deposited. While the metal electrodes are deposited by physical vapor deposition methods, the insulating layers are grown by atomic layer deposition. In the following, all the fabrication process steps after mesa isolation for ohmic contacts, MISH capacitors and MIS-HEMT devices are presented and described in detail.

4.2.1 Ohmic contacts

After mesa isolation, the fabrication of ohmic contacts continues with patterning the metal pads through optical lithography and lift-off technique. The SPC treatment is applied before the metal deposition to remove resist residuals from the GaN surface and ensure a good metal/GaN contact (see Section 4.1). In this case, the SPC consists of a high power (800 W), remote O_2 plasma treatment for 2 minutes at 100 °C followed by HCl wet treatment for 1 minute. Afterwards, the multilayered metal stack is deposited and subsequently defined by lift-off. Finally, the ohmic contact formation is obtained by RTA treatment. The general process flow is schematically shown in Figure 4.1.

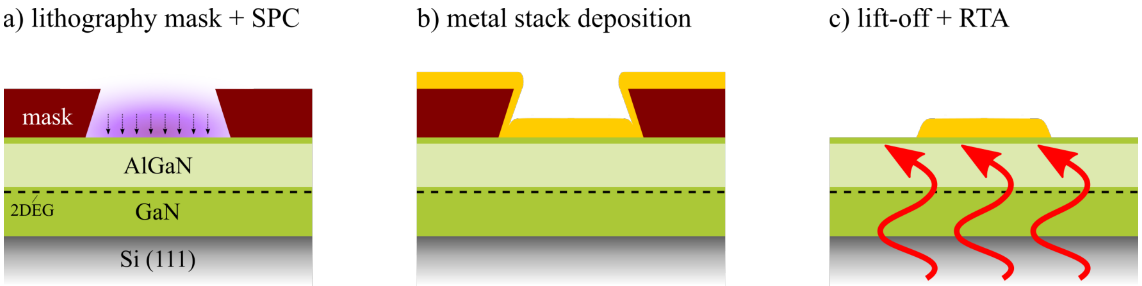
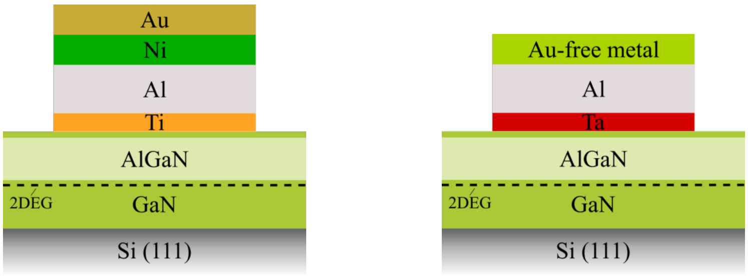


Figure 4.1: Schematic fabrication process for ohmic contacts used in this thesis.

The two metallization schemes employed for ohmic contacts in this work, consisting of Ti/Al/Ni/Au and Ta/Al/x (x= Ta, TiN and TaN) metal stacks, are illustrated in Figure 4.2. As previously described, the Ti/Al-based metallization is a standard scheme used for ohmic contacts to AlGaN/GaN, while the Ta/Al-based metal stack is studied in this work as alternative scheme for low-temperature and Au-free ohmic contacts. The Ti/Al/Ni/Au metal stack with layer thicknesses of 35/200/40/100 nm, respectively, is deposited by evaporation and annealed at 850 °C for 30 seconds in N_2. Differently, the Ta/Al/x (x= Ta, TiN and TaN) scheme is fabricated by sputtering and consists of a Ta/Al stack with an additional Au-free metal capping layer. Ta, TiN and TaN are alternatively investigated as capping layers because of their influence on the thermal stability and resistivity of the metal stack. Different Ta bottom layer thicknesses as well as annealing temperatures are tested hence they both influence the ohmic contact formation and the contact resistance. Details of the investigation about variation of metal composition, layer thickness and annealing temperature are discussed in Chapter 5.

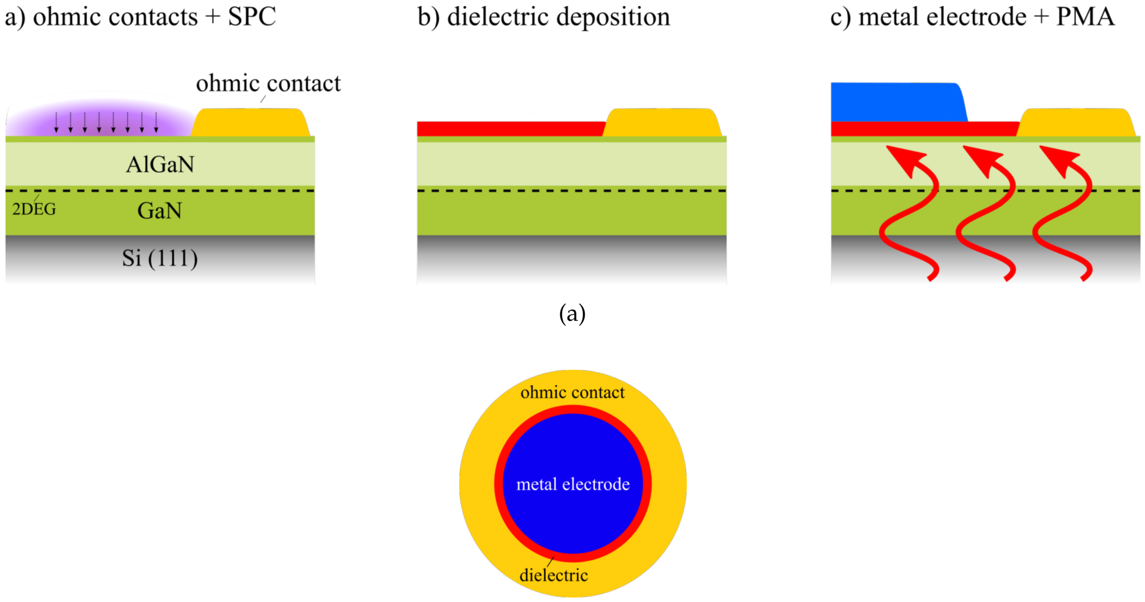

Au
Ni
Al
Ti
AlGaN
2DEG
GaN
Si (111)
Au-free metal
Al
Ta
AlGaN
2DEG
GaN
Si (111)

(a) (b)

Figure 4.2: Schematic of the multilayer metal stacks used in this work to fabricate ohmic contacts to AlGaN/GaN heterostructures: (a) conventional Ti/Al/Ni/Au contact, (b) alternative Ta/Al-based metal stack with a Au-free capping layer.

4.2.2 MISH capacitor

The MISH capacitor structure resembles the gate stack structure of MIS-HEMT devices. For this reason, MISH capacitors are suitable test vehicles to assess the functionality of the dielectric layer in terms of bulk properties and dielectric/III-nitride interface quality which eventually affect the MIS-HEMT performance. The fabrication process steps and the top view of the circular MISH capacitor are shown in Figure 4.3. MISH capacitor test structures with different diameters of the center electrode are used to verify scaling effects with the gate area.


a) ohmic contacts + SPC
b) dielectric deposition
c) metal electrode + PMA
ohmic contact
AlGaN
2DEG
GaN
Si (111)
ohmic contact
metal electrode
dielectric

(a)

(b)

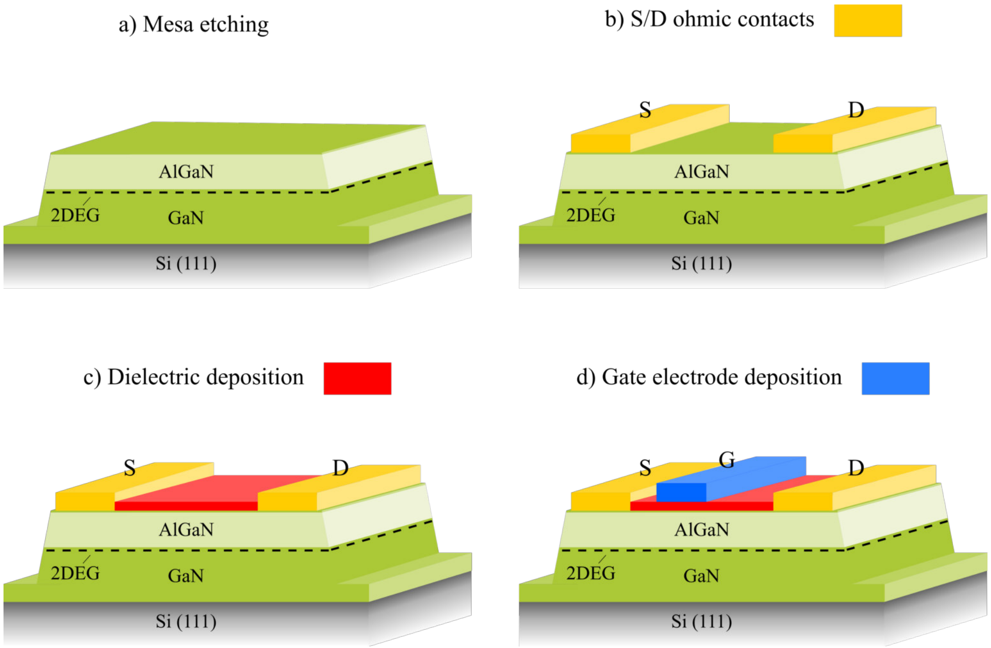
Figure 4.3: (a) Schematic fabrication process and (b) top view of circular MISH capacitors used in this thesis.

Following the mesa etching, the ohmic contacts are fabricated by using the process scheme explained in detail in the previous section. After the annealing for the ohmic contact formation, the SPC treatment is applied to the GaN surface by using a low power (100 W) O_2 plasma for 90 seconds at 100 °C followed by HCl dipping for 1 minute. Next, the dielectric layer is deposited as gate insulator, followed by the deposition and subsequent lift-off of the metal gate electrode. Finally, a PMA treatment is carried out at temperatures ranging between 300 °C and 400 °C for 10 minutes in N_2 ambient.

For the MISH capacitors, the Ti/Al/Ni/Au and Ta/Al/x (x= Ta, TiN and TaN) metal stacks described in previous section are both utilized for the fabrication of ohmic contacts. In particular, even though the Ti/Al-based scheme is mainly used, MISH capacitors with Ta/Al-based ohmic contacts are investigated in Section 6.3 to study the impact of the lower annealing temperature for contact formation on the dielectric/GaN interface quality, compared to MISH capacitors fabricated with the conventional Ti/Al-based contacts annealed at high temperature. Al_2O_3 grown by ALD is used as gate dielectric after the SPC treatment. Lastly, the Ti/Au bilayer stack with layer thickness of 100/150 nm, respectively, is deposited by evaporation as metal gate electrode. Samples of MISH capacitors fabricated with and without SPC and PMA treatments will be compared in Chapter 6 in order to investigate their influence on the dielectric/GaN interface.

4.2.3 MIS-HEMT

The general MIS-HEMT process flow including the main process steps of mesa isolation, ohmic contacts formation, gate dielectric deposition and gate metallization is illustrated in Figure 4.4.


a) Mesa etching

b) S/D ohmic contacts 🟨

c) Dielectric deposition 🟥

d) Gate electrode deposition 🟦

Figure 4.4: Schematic fabrication process flow for MIS-HEMTs used in this thesis. The letters G, S and D represent the gate, source and drain electrodes, respectively.

After mesa isolation by ICP-RIE with BCl_3/Cl_2, source and drain ohmic contacts are deposited, structured and subsequently formed by rapid thermal annealing. Afterwards, the gate module is fabricated by resembling the process steps applied for MISH capacitors. The SPC treatment with a low power (100 W) O_2 plasma for 90 seconds at 100 °C followed by HCl dipping for 1 minute is applied to the GaN surface prior to the gate dielectric deposition. Afterwards, a dielectric layer is grown as a gate insulator followed by the structuring of the metal gate electrode by deposition and lift-off. Note that in the used fabrication scheme, the dielectric functions both as insulating layer beneath the gate electrode as well as passivation layer between the gate and ohmic contacts. Finally, a PMA treatment is applied at temperatures ranging between 300 °C and 400 °C for 10 minutes in N_2 ambient.

For the MIS-HEMT, the Ti/Al/Ni/Au and Ta/Al/x (x= Ta, TiN and TaN) metal stacks described in previous section are both integrated as drain and source ohmic contacts. MIS-HEMTs fabricated with the two metallization schemes will be compared in Chapter 7. As for MISH capacitors, Al_2O_3 grown by ALD is used as gate dielectric after the SPC treatment, while an evaporated Ti/Au bilayer stack of thickness 100/150 nm, respectively, is applied as metal gate electrode. MIS-HEMTs fabricated with and without SPC and PMA treatments will be also compared in Chapter 7.

4.3 Electrical characterization

In the following section, the characterization techniques of transfer length method (TLM), multifrequency capacitance–voltage (C-V) measurements and pulsed current-voltage (I-V) measurements are presented. These are the main electrical methods applied in this work for the investigation of the ohmic contacts and of the dielectric/GaN interface of MISH capacitors and the evaluation of the MIS-HEMTs performance. The I-V, C-V and pulsed I-V measurements are carried out by an Agilent B1505A Power Device Analyzer used in conjunction with a Karl Süss PM8 probe station.

4.3.1 Transfer length method

Ohmic contacts to AlGaN/GaN heterostructures are characterized by the so called transfer length method.[80] Originally proposed by Shockley,[136] this is the most popular characterization method used for planar ohmic contacts to determine the contact resistance R_c, the sheet resistance R_{sh} and the specific contact resistivity ρ_c. In the following, the linear TLM test structures used in this work and related methods to extract the parameters of R_c, R_{sh} and ρ_c from I-V measurements are described and discussed.

TLM structure

The TLM test structure is schematically shown in Figure 4.5. It consists of a linear array of metal pads of identical area separated by increasing spacing distances. The total resistance between each adjacent contacts is measured by forcing a current I and measuring the resulting voltage V between them. In this work, the metal pads are fabricated with $W = L = 100$ µm where W and L are the contact width and the contact length, respectively. The nominal spacing distance d_C between contacts ranges from 5 µm to 30 µm. However, since the exact values of spacing can deviate from the nominal values designed by the lithography mask due to resolution limits during lithography or due to the thermal expansion of the metal pads after annealing, the exact distances between contacts were measured by scanning electron microscopy (SEM) and will be taken into account in the following evaluations. Moreover, in order to eliminate the current flow at the contact edges which can significantly affect the result of the contact resistance, the area where the TLM structure is fabricated is electrically confined through mesa isolation. The actual metal stacks applied as metal pads are described in Section 4.2.

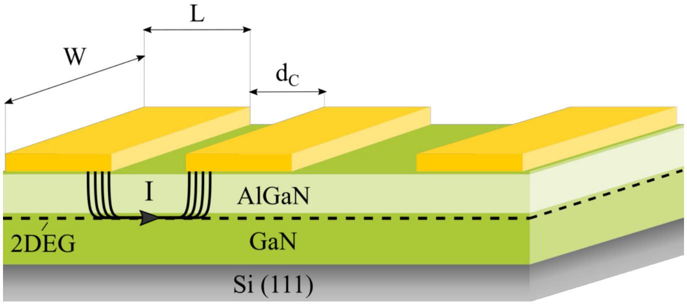


Figure 4.5: Schematic of a TLM test structure with the current flowing between two adjacent metal pads.

Determination of R_c, R_{sh} and ρ_c

The total resistance measured between two adjacent contacts of the TLM test structure can be modeled by the following equation

$$R_T = R_{sh} d_C + 2R_c \tag{4.1}$$

where R_T is the total resistance given per unit contact width in Ω mm, R_{sh} is the sheet resistance between contacts, R_c is the contact resistance, assumed identical for each contact, and d_C is the contact spacing. A schematic illustration of the contributions considered in Equation 4.1 is shown in Figure 4.6a. Note that the resistance R_m of the metal pads is not taken into account in Equation 4.1 because it is usually negligible with respect to the other terms. The values of R_c and R_{sh} can be determined by plotting the resistance measured as a function of the contact spacing and using Equation 4.1 as linear fitting function, as shown in the example of Figure 4.6b. The R_c in Ω mm and R_{sh} in Ω sq^{-1} can be extracted from the intercept and slope of the fitting line, respectively.

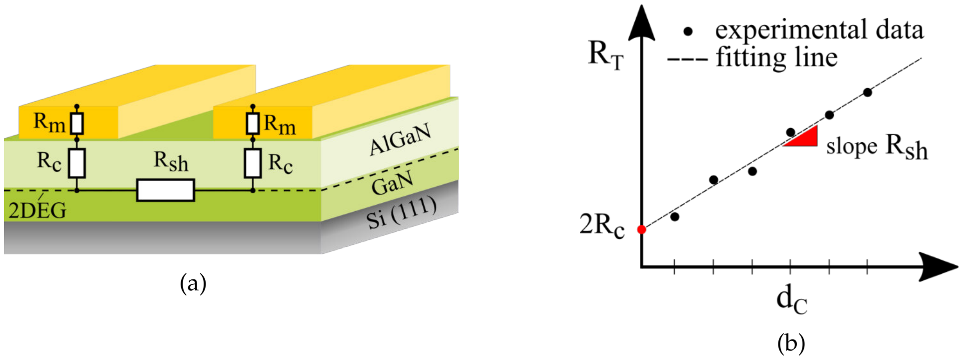


Figure 4.6: (a) Schematic of the different resistive contributions of Equation 4.1. R_m represents the metal pad resistance which is not taken into account because it is usually much smaller than other contributions. (b) Method to extract the contact resistance and the sheet resistance from TLM structure.

Differently from the parameters of R_c and R_{sh}, the specific contact resistivity ρ_c cannot be directly extracted from the measurements but requires a more detailed analysis of the nature of the current flow and contact geometry.[137, 138] During the current transfer from the semiconductor to the metal or vice versa, the current spreads only at the edge of the contact taking the path of least resistance. The fraction of the total contact length through which most of the current spreads is defined as transfer length L_T and is given by the following equation

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}}. \tag{4.2}$$

Typical transfer length values for good contacts ($\rho_c \leq 10^{-6}\ \Omega\ \text{cm}^2$) are in the order of 1 µm or less. For contacts with $L \geq 1.5L_T$, R_c can be expressed in terms of L_T as follows

$$R_c = \frac{\rho_c}{L_T}. \tag{4.3}$$

Note that, given a contact width W, since $L \geq 1.5L_T$ the effective contact area $A_{eff} = WL_T$ through which the current is flowing can be smaller than the actual contact area $A = WL$. Finally, by combining Equations 4.2 and 4.3, the specific contact resistivity can be expressed as follow

$$\rho_c = \frac{R_c^2}{R_{sh}}. \tag{4.4}$$

Due to the long contacts used in this work with L = 100 µm, Equation 4.3 can be applied to extract ρ_c with Equation 4.4. Note that, one limitation of this method is that Equation 4.3 assumes the sheet resistance to be identical under the contacts and between the contacts as a first order approximation. In fact, R_{sh} between the contacts could be different from the one under the contacts due to effects related to the contact formation.[139] In this work, the value of $\mathrm{R_{sh}}$ under the contacts could not be accurately measured via the contact end resistance method due to very long contact stripes in the available design. Finally, as will be further discussed in Chapter 5, another limitation is that for certain contact schemes the metal/semiconductor representation of an areal stripe given by the transfer length L_T and the contact width W is not valid and the approximation given by Equation 4.3 is not applicable.

4.3.2 Frequency-dependent capacitance-voltage method

C-V measurements of MISH capacitors on AlGaN/GaN are commonly used as fast characterization technique in order to evaluate quantities such as layer thicknesses and sheet carrier concentration. Advanced methods are instead required in order to map the interface trap density (D_{it}) at the dielectric/III-N interface. In fact, the presence of a double-interface (dielectric/III-N and AlGaN/-GaN) complicating the potential distribution over the structure, and the low electron emission rate of wide bandgap GaN-based materials make the D_{it} evaluation difficult. In the following, the typical C-V characteristic of a MISH capacitor on AlGaN/GaN is described. Afterwards, the frequency-dependent C–V method reported by Yang et al. [77] is presented since it is used in this work to determine the D_{it} at the dielectric/GaN interface.

C–V characteristics of MISH capacitors

The ideal C–V characteristic of a MISH capacitor composed by a dielectric/GaN-cap/AlGaN/GaN structure is schematically shown in Figure 4.7 and consists of a double-step curve which is a typical feature of the double-interface structure given by the dielectric/GaN and AlGaN/GaN interfaces.[140, 141] In the subthreshold region (below V_{th}) the 2DEG is depopulated and the capacitance is very small. Near V_{th} a rapid change in the capacitance starts to occur due to the electron population of the 2DEG at the AlGaN/GaN interface. Once the 2DEG is populated, the capacitance becomes almost bias independent and is given by the series capacitance of the AlGaN barrier, the GaN-cap, and the dielectric layer. By applying a positive bias, electrons start to overcome the AlGaN barrier layer and accumulate at the dielectric/GaN interface resulting in a second step in the C–V characteristic. This region is referred to as spill-over regime and its onset voltage is here indicated as $V_{spill\text{-}over}$. The capacitance value of the flat part in the spill-over region is given by the dielectric capacitance $C_{dielectric}$.

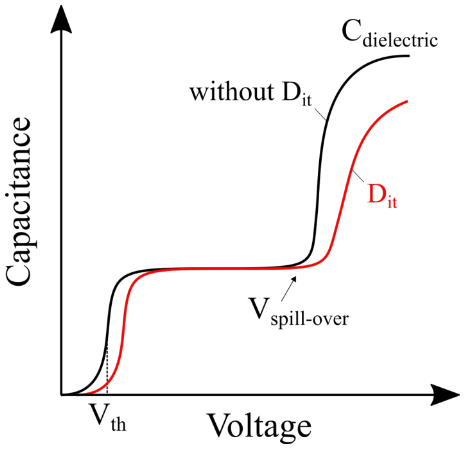


Figure 4.7: Schematic C–V characteristics of a dielectric/GaN/AlGaN/GaN capacitor without (ideal case) and with trap states of density D_{it} located at the dielectric/GaN interface.

The ideal C–V behavior is modified when interface trap states are present at the dielectric/GaN interface (see Figure 4.7).[140, 141, 142] In the spill-over region, once electrons are trapped at the interface the negatively charged states screen the gate electric field resulting in a shift of $V_{\text{spill-over}}$ towards the positive bias direction. Second, they lead to a drastic decrease in the C–V slope of the second step due to the dependence of the traps occupancy on the gate voltage. A schematic illustration of the conduction band diagram of a dielectric/GaN/AlGaN/GaN structure at zero bias applied compared with the spill-over case is shown in Figure 4.8. In case of very high interface state densities, the second step might not be visible even at very high positive bias voltages due to a large positive shift of $V_{\text{spill-over}}$ which cannot be detected due to the increase in leakage currents. On the contrary, near V_{th} the trap occupancy of D_{it} does not depend on the gate voltage and a high D_{it} results in a parallel shift of the corresponding C–V step without any stretch out.[143] Therefore, a qualitative indication of the dielectric/GaN interface quality can be evaluated by considering the stretch out of the C-V slope in spill-over region and the $V_{\text{spill-over}}$ position.

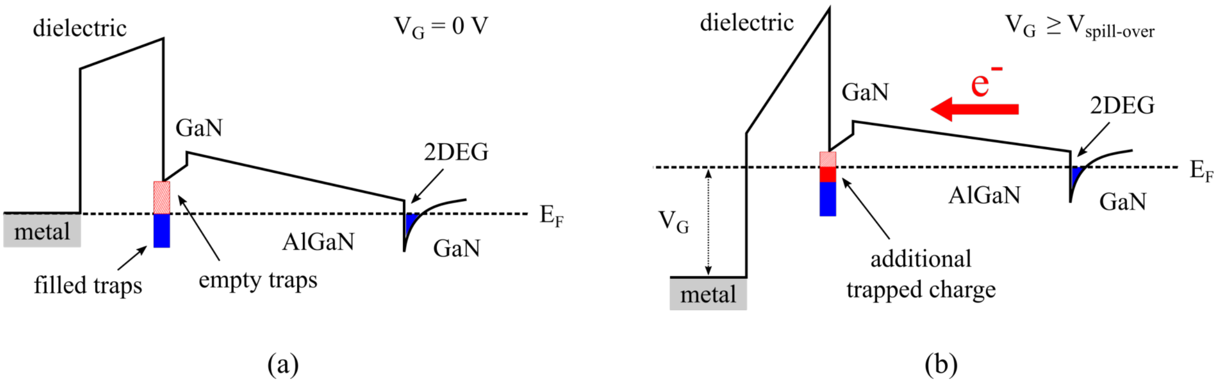


Figure 4.8: Schematic conduction band diagram (not to scale) of a dielectric/GaN-cap/AlGaN/GaN structure at a) zero bias ($V_G = 0$ V) and b) under forward bias in the the spill-over regime ($V_G \geq V_{\text{spill-over}}$). Electrons can overcome the AlGaN barrier from the 2DEG channel and be trapped in the states located at the dielectric/GaN interface. E_F denotes the Fermi energy at 0 V gate voltage.

Determination of D_{it} at the dielectric/III-N interface

The evaluation of the D_{it} at the dielectric/III-N interface is carried out using the frequency dispersion of the C–V characteristics in the spill-over region of the dielectric/GaN/AlGaN/GaN capacitor structures, as schematically shown in Figure 4.9. In forward bias region, E_F is moving upward towards the conduction band at the dielectric/GaN interface and its energy position is defined by the voltage applied (see Figure 4.8b). Once E_F is located at a certain energy position, the only electrons which can respond to the alternating current (AC) signal and be detected are the ones which are trapped and re-emitted from trap states with an emission time τ_e smaller than the period τ related to the frequency of the AC signal ($\tau_e<\tau$). The emission time constant for a trap

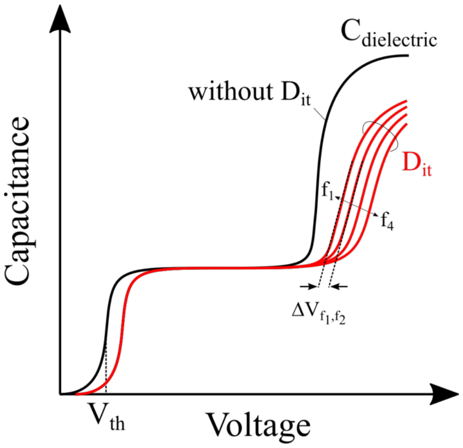


Figure 4.9: Schematic C–V characteristics of a dielectric/GaN/AlGaN/GaN capacitor without (ideal case) and with trap states located at the dielectric/GaN interface for different frequencies. A certain frequency dispersion is obtained due to the presence of interface trap states. The parameter of $\Delta V_{f_1,f_2}$ used in Equation 4.8 is indicated.

level using the Shockley–Read–Hall statistics is

$$\tau_e = \frac{1}{N_c v \sigma} \exp\left(\frac{E_C - E_T}{k_B T}\right), \tag{4.5}$$

where N_C, v, σ, E_C, E_T, k_B, and T are the effective density of states in the conduction band, the thermal velocity, the capture cross-section of the trap, the conduction band minimum, the trap energy, the Boltzmann constant, and the temperature, respectively. The period of the AC signal is given by

$$\tau = \frac{1}{2\pi f}, \tag{4.6}$$

where f is the frequency of the AC signal. Combining Equations 4.5 and 4.6, the maximum trap energy depth $E_{T,f}$ with respect to E_C which can be probed by a certain frequency f can be deduced as

$$E_C - E_{T,f} = k_B T \ln\left(\frac{N_c v \sigma}{2\pi f}\right). \tag{4.7}$$

At a certain frequency f, only charged trap states (depending on the position of E_F) which are in the energy range between E_C and $E_{T,f}$ contribute to the capacitance and lead to the onset of spill-over at $V_{\text{spill-over}}$ in the C–V characteristic. Higher frequencies can therefore only probe energetically shallower states and lead to a positive shift of $V_{\text{spill-over}}$ because a higher voltage is required to raise E_F towards E_C. As a consequence, a smaller-frequency dispersion indicates a reduction of the interface state density. In addition, a D_{it}-E_T energy map can be obtained using the voltage shift of the second step in the C–V curves using the following equation

$$D_{it}\left(E_C - \overline{E_T}\right) = D_{it}\left(E_C - \frac{E_{T,f_1} + E_{T,f_2}}{2}\right) = \frac{C_{dielectric}}{q} \frac{\Delta V'_{f_1,f_2}}{\left(E_{T,f_1} - E_{T,f_2}\right)} \tag{4.8}$$

with

$$\Delta V'_{f_1,f_2} = \frac{C_{AlGaN}}{C_{AlGaN} + C_{dielectric}} \Delta V_{f_1,f_2}, \tag{4.9}$$

where C_{AlGaN} and $C_{dielectric}$ are the capacitance values of the AlGaN and dielectric layer determined by their physical thickness, q is the elementary charge, and $\Delta V_{f_1 f_2}$ is the voltage shift in the second step between C–V curves at frequencies f_1 and f_2. $\Delta V_{f_1 f_2}$ is determined at the midpoint of the capacitance in the second step of the C–V characteristics. Using Equation 4.7, the difference between E_{T,f_1} and E_{T,f_2} is instead given by

$$E_{T,f_1} - E_{T,f_2} = k_B T \ln\left(\frac{f_1}{f_2}\right). \tag{4.10}$$

The described method will be used in this work to obtain D_{it}-E_T energy maps determined accordingly to Equation 4.8 by assuming a capture cross-section σ of 10^{-14} cm^2. Note that, the capture cross-section is not exactly know forehand but changing σ only changes the energy scale by a rigid shift of the D_{it}-E_T energy map.

4.3.3 Pulsed measurements of V_{th} instability under forward gate bias stress

Pulsed I-V measurements are commonly employed as standard dynamic characterization method of charge trapping effects in GaN-based HEMT devices.[67, 78, 144, 145] In particular, this technique is suitable for the investigation of trapping phenomena by minimizing thermal effects related to the self-heating of the device. The basic principle of a typical pulsed I-V measurement is shown in Figure 4.10. The measurement consists of pulsing the gate and drain terminals of the device from a stress phase to a measurement phase. In particular, during the stress phase a fixed charge trapping state is induced in the device by applying a distinct stress condition. In between each stress phase, short measurement pulses are applied to sample the device current and eventually obtain the transfer (I_{DS}-V_{GS}) or output (I_{DS}-V_{DS}) characteristic of the device. In order to minimize possible detrapping effects and self-heating of the device during the measurement phase, the width of the measurement pulse is kept as small as possible within the limit of the measurement system. At the contrary, the duration of the stress phase is typically chosen much longer than the measurement pulse width to reach a steady-state stress condition after each measurement pulse. Since the device is mostly kept in the stress condition during pulsed I-V measurements, the stress phase is also named as quiescent point. The short pulsed measurement phase is instead referred to as non-quiescent point. A quiescent point is typically defined by the set of voltages ($V_{GS,q}$, $V_{DS,q}$), which are the voltage differences applied during the stress phase between, respectively, the gate-source and drain-source terminals of the device. Correspondingly, ($V_{GS,m}$, $V_{DS,m}$) is instead defined as non-quiescent point applied to gate-source and drain-source during the measurement phase. Distinct quiescent conditions can be employed to address traps located in specific regions of the device by monitoring the degradation of the dynamic device parameters.[144]

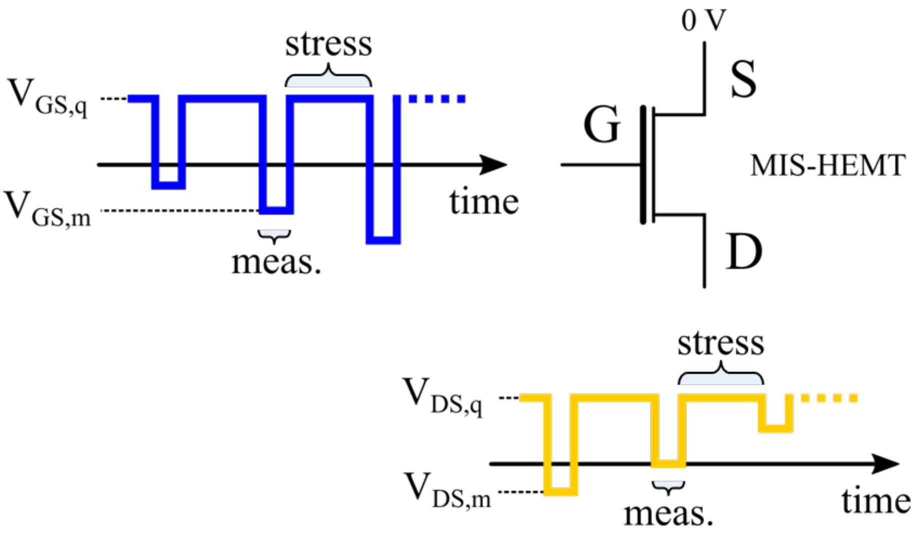


Figure 4.10: Principle of pulsed I-V measurement.

Trap states located at the dielectric/III-N interface or within the dielectric can cause a significant V_{th} instability due to the extremely slow detrapping behavior of wide bandgap GaN-based materials. In particular, serious V_{th} shift induced by forward gate bias stress has been observed due to the spill-over of electrons from the 2DEG channel towards the dielectric/III-N interface. The effects of trapping at the gate insulating stack of MIS-HEMTs promoted by forward gate bias conditions can be investigated by pulsed I_{DS}-V_{GS} measurements. In particular, a certain quiescent positive voltage $V_{GS,q}$ is applied to the gate during the stress phase, whereas source and drain are kept at 0 V in order to ensure trapping mainly at the dielectric/III-N interface ($V_{DS,q}$ = 0V).[144] In between each stress phase, the short measurement pulses consisting of a gate pulse of increasing height $V_{GS,m}$ and a low drain pulse $V_{DS,m}$ are applied to obtain the transfer characteristic of the device. A low $V_{DS,m}$ is used to reduce field-assisted detrapping from interface states. A schematic of a pulsed I_{DS}-V_{GS} measurement in forward gate bias stress condition is shown in Figure 4.11.

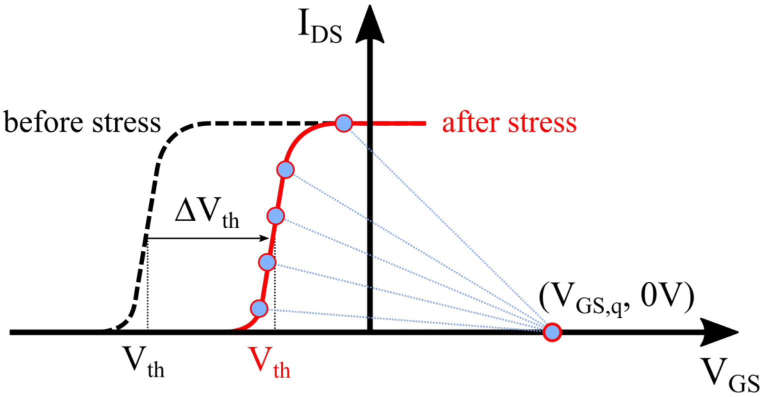


Figure 4.11: Schematic of a pulsed I_{DS}-V_{GS} measurement showing the I_{DS}-V_{GS} characteristics before (dashed curve) and after (solid curve) the application of a forward gate bias stress. After stress, the V_{th} shifts due to trapping at the dielectric/III-N interface or within the gate dielectric.

As already mentioned, the V_{th} shift obtained after positive gate bias stress is not only correlated to interface traps but also to border traps. In fact, during the stress time border traps can be also filled and contribute to the V_{th} instability due to their long emission time. Even though the separate contributions of border and interface traps cannot be disentangled, an effective interface charge density accounting for D_{it} and border traps can be determined as

$$n_{it} = \frac{C_{dielectric}}{q} \Delta V_{th}. \tag{4.11}$$

In Chapter 6, pulsed I_{DS}-V_{GS} measurements under forward gate bias stress will be utilized to investigate the V_{th} stability of AlGaN/GaN MIS-HEMTs using ALD-Al_2O_3 subjected to SPC and PMA treatments.

5 Low-temperature Au-free Ta/Al-based ohmic contacts

Low-temperature and Au-free Ta/Al-based ohmic contacts fabricated by sputtering on AlGaN/-GaN heterostructures are presented and described in this chapter. First, the employment of the Ta/Al-based metallization scheme aiming to achieve ohmic contact formation at low annealing temperatures is introduced. In particular, the transition from a non-linear to an ohmic behavior in relation to the presence of the AlN spacer layer at the AlGaN/GaN interface is discussed. The different layers of the ohmic metal stack are studied as they significantly influence the contact performance in terms of thermal stability and contact resistance. The nature of current transport governing the ohmic behavior is then investigated by analyzing the temperature dependence of the specific contact resistivity. Afterwards, the low-temperature and Au-free Ta/Al-based ohmic contacts are demonstrated on 150 mm GaN-on-Si substrates and compared to the conventional Au-containing Ti/Al-based metallization scheme annealed at high temperatures. This chapter includes the results published in Ref. [146, 147].

5.1 Ta/Al-based ohmic contacts

The low work function of Ta-based systems is utilized to obtain a low Schottky barrier height to AlGaN and achieve low-resistive ohmic contacts after annealing.[13] In only few reports, Au-free Ta/Al-based metal stacks, typically deposited by evaporation, have been employed to fabricate low-resistive ohmic contacts to AlGaN/GaN heterostructures even for annealing temperatures lower than 650 °C.[109, 112] Recently, the latter approach was also successfully combined with a recess technique of the AlGaN barrier to obtain low-resistive ohmic contacts.[111] Here, the Ta/Al-based metallization scheme is investigated in order to optimize its electrical behavior and to further improve the current understanding of the contact mechanism in the case of Au-free ohmic contacts which are annealed at low temperatures. Sputtering is employed as deposition technique due to the high melting point of Ta and to ensure better adhesion, coverage and uniformity compared to the commonly used evaporation method (see Section 4.1.3). Moreover, sputtering is a much more suitable deposition technique for industrial applications and it is compatible with the future prospective of implementing GaN technology in standard Si fabs.

The metal stacks applied to the fabricated samples which are used in this section are listed in Table 5.1. For simplicity, the samples are arranged in groups named as A, B, C and D. Each group was used to study a particular aspect during the experimental work of the low-temperature and Au-free Ta/Al-based metallization scheme under investigation. The starting point of the thickness of the bottom Ta/Al bilayer system was chosen with guidance from the report of Malmros et al. [109] discussing Ta/Al-based ohmic contacts fabricated by metal evaporation. Subsequently, different materials for the capping layer and thickness ratio variation of the bottom Ta/Al bilayer were investigated in order to study their influence on the thermal stability and contact resistance of the metal stack. In more detail, samples of the groups A and B were used to investigate the influence of the AlN spacer layer on the ohmic contact formation. The group of samples C was instead employed to evaluate the impact of the capping layer on the thermal stability of the metal stack during annealing and to investigate the nature of current transport through the metal/semiconductor interface of the ohmic contact. Lastly, group D was used to study the influence of the thickness ratio of the bottom Ta/Al bilayer on the annealing temperature required to reach ohmic behavior and on the contact resistance values.

Table 5.1: List of metal stacks applied to the fabricated samples investigated in this section. The R_c data extracted from TLM structures for samples with ohmic characteristics at annealing temperature ranging between 500 °C and 600 °C are also shown. The "n/o" refers to a non-ohmic behavior obtained after annealing. Refer to Table 4.1 for specifications on the epitaxial materials indicated in the column "Epi".

Sample	**Metal stack**	**Thickness** [nm]	**Epi**	$\mathbf{R_c}$ [Ω mm]		
				500 °C	550 °C	600 °C
A.I	Ta/Al/Ta	5/150/20	I	n/o	n/o	n/o
A.II	Ta/Al/Ta	5/150/20	II	2.7	2	n/o
B.I	Ta/Al/TiN	10/240/20	I	n/o		
B.II	Ta/Al/TiN	10/240/20	I	20 (40 nm recess)		
C.I	Ta/Al/Ta	10/150/20	III	0.94	0.84	n/o
C.II	Ta/Al/TiN	10/150/20	III	0.80	0.77	0.77
D.I	Ta/Al/TiN	5/240/20	III	2.2	2.6	3.6
D.II	Ta/Al/TiN	10/240/20	III	n/o	1.7	1.4
D.III	Ta/Al/TiN	15/240/20	III	n/o	2.6	2.2
D.IV	Ta/Al/TiN	20/240/20	III	n/o	5.1	3.7

It is important to mention that, even though the exact mechanism responsable for the ohmic contact formation is not yet fully understood in Au-free metallization schemes, the properties of the ohmic contacts have been reported to depend on the AlGaN/GaN heterostructure properties such as thickness and/or Al concentration mole fraction of the AlGaN barrier, and on the metal/AlGaN interface.[13, 95, 119] In particular, the ohmic contact formation and the contact resistance appear to strongly depend on the thickness ratio of the bottom bilayer (e.g. Ti/Al or Ta/Al), as also discussed in Section 5.1.4.[13, 98] This aspect implicates that differences in the used epitaxial material or thickness deviations in the nanometer range of the Ta bottom layer from the nominal value could result in considerable deviations in the values of the contact resistance measured for the Ta/Al-based ohmic contacts investigated in this work. Therefore, variations in terms of contact resistance between similar metal stacks belonging to different groups in Table 5.1 are most likely due to differences in the epitaxial materials used and/or in the tool conditions for the sample fabrication. In this context, only samples in the same groups of Table 5.1 can be considered completely comparable as they were fabricated on the very identical substrate material and with comparable process conditions in terms of time and tool calibration.

5.1.1 AlN spacer layer

A thin AlN spacer layer is usually employed between the AlGaN barrier and the GaN channel layer to enhance the 2DEG electron mobility by reducing the alloy disorder scattering along the AlGaN/GaN interface.[49, 148] On the other hand, the wide bandgap of AlN introduces a high energy barrier on the AlGaN barrier side which can pose challenges for the formation of low-resistive ohmic contacts. Observations of degraded contacts or even prevention of ohmic contact formation have been reported for Au-free Ti/Al-based systems fabricated on AlGaN/GaN heterostructures including an AlN spacer layer.[50, 92] For this reason, it is of interest to investigate the influence of the AlN spacer layer on the ohmic contact formation also in the case of the Au-free Ta/Al-based approach annealed at low temperatures.

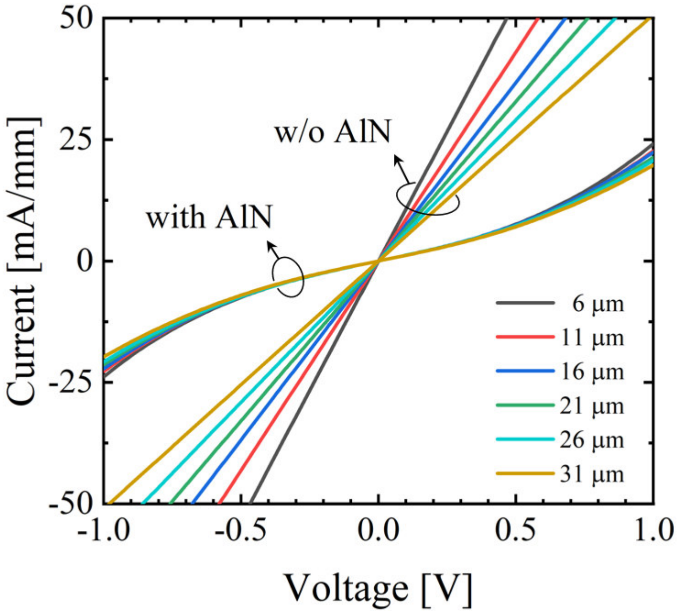
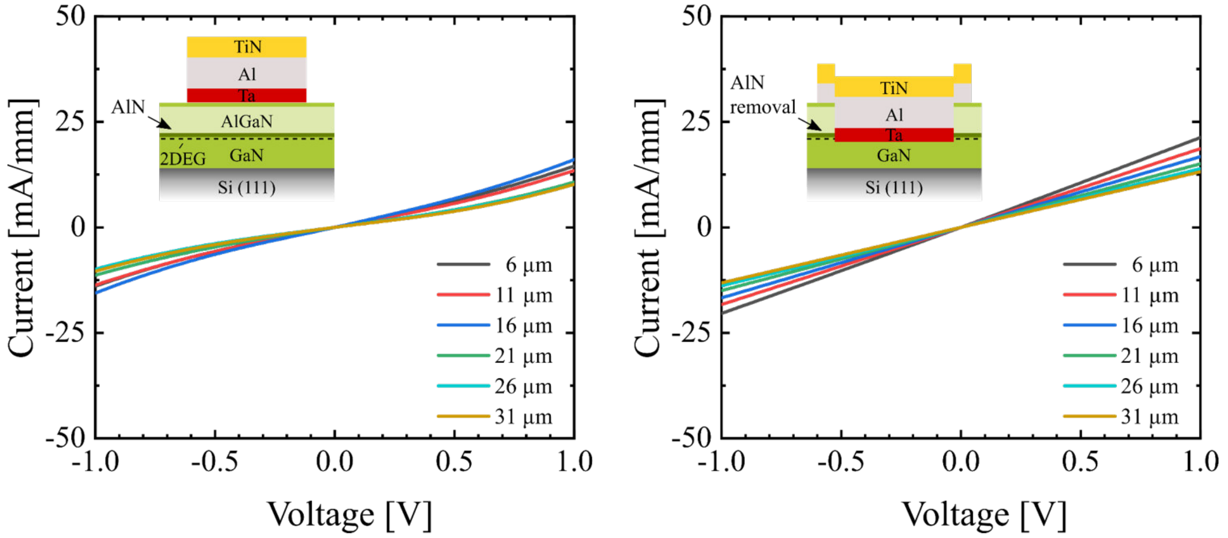


Figure 5.1: I-V characteristics of TLM structures of Ta/Al/Ta metal contacts fabricated on epitaxial material with (Sample A.I) and without (Sample A.II) AlN spacer and annealed at 500 °C. For Sample A.II, TLM analysis revealed R_c = 2.7 Ω mm and R_{sh} = 500 Ω sq^{-1}.

Figure 5.1 compares the I–V characteristics of two TLM structures of identical Ta/Al/Ta metal stacks after annealing at 500 °C, which were fabricated on epitaxial material grown without and with AlN spacer layer, respectively. The used heterostructures consisted both of 30 nm of AlGaN barrier but one without AlN spacer layer (Sample A.I) and the other one featuring 1 nm thick AlN at the AlGaN/GaN interface (Sample A.II). As one can see, the AlN spacer limits the current conduction with respect to the case without AlN and prevents the ohmic contact formation resulting in a non-linear behavior of the I-V characteristics. The contacts of this sample remained non-ohmic even for higher annealing temperatures up to 600 °C. On the contrary, ohmic characteristics with higher currents are already obtained at the annealing temperature of 500 °C in the case of the Ta/Al/Ta metal stack fabricated on the AlGaN/GaN heterostructure without AlN spacer layer. To further evaluate the influence of the AlN spacer layer in relation to the AlGaN barrier thickness, the same Ta/Al/Ta metal stack with the same annealing conditions was also fabricated on two heterostructures similar to Epi I but with thinner AlGaN barrier layers of 20 nm and 5 nm (not reported here). The I–V characteristics still showed a non-ohmic behavior for annealing temperatures up to 600 °C. Therefore, the AlN spacer prevents the ohmic contact formation independently on the AlGaN barrier thickness.



(a)

(b)

Figure 5.2: I-V characteristics of TLM structures of Ta/Al/TiN metal contacts fabricated on Epi I (a) without AlGaN recess (Sample B.I) and (b) with 40 nm recess through the AlGaN and the AlN spacer layer (Sample B.II), annealed at 550 °C. For Sample B.II, TLM analysis revealed a large R_c of about 20 Ω mm.

An additional experiment was instead performed by recessing through the AlN spacer layer. For this purpose, TLM structures of two identical Ta/Al/TiN metal stacks (TiN-capped contacts will be discussed in next section) annealed at 550 °C were fabricated in one case with an intact AlGaN barrier (Sample B.I) and the other one by applying an etching process of 40 nm by ICP-RIE to completely remove the AlGaN barrier and the AlN spacer layer under the contact (Sample B.II). Figure 5.2 shows the results obtained for the two samples described. As one can see, even though the resulting contact resistance of about 20 Ω mm obtained for the recessed sample is quite large, the removal of the AlN spacer layer leads to an ohmic behavior of the contacts after annealing. This result further demonstrates the strong dependency of the ohmic contact formation on the AlN spacer layer. The large value of R_c can be caused by a different contact mechanism in the case of recessed contacts where the contact performance can be highly sensitive to the etching process and the resulting etch profile. An analysis in the direction of local contact geometry for recessed contacts can be found in Ref [149].

As discussed later in Section 5.1.3, this strong sensitivity of the ohmic contact formation on the AlN spacer layer seems to be related to the microscopic type of contact formation. In fact, the high energy barrier introduced by the AlN can degrade the charge carrier transport upon the assumption of a 2DEG-semiconductor-metal current path dominated by tunneling through the AlGaN barrier. This issue seems to be effectively overcome by recessing through the AlN spacer layer. The same approach was applied by Lin et al.,[111] where low-resistive Ta/Al-based ohmic contacts at low annealing temperatures have been obtained for heterostructures containing an AlN spacer layer by recessing beyond the AlGaN barrier. On the contrary, since in the case of Au-containing Ti/Al-based contacts annealed at high temperatures the contact is most likely formed by metal protrusions through the AlGaN barrier directly to the 2DEG, the ohmic contact formation has been reported to be only slightly sensitive to the AlN presence.[92] This is in line with our observations on the used Ti/Al/Ni/Au ohmic contacts annealed at 850 °C showing only a minor increase in ohmic contact resistance of about 20 % with an additional AlN spacer layer located at the AlGaN/GaN interface.

5.1.2 Capping metal layer

The capping metal layer is adopted as protective layer aiming to prevent the oxidation of underlying metals and to improve the overall contact resistance by lowering the metal stack resistivity.[13] For these purposes, Au is commonly employed in Ti/Al-based contacts as it has a strong oxidation resistance and forms highly conductive phases upon annealing.[85, 150, 151] Differently, for Au-free contacts other solutions have been employed to replace Au, such as for example Ta, TiN or W.[95, 109, 110, 112, 113, 116] In this work, Ta, TiN and TaN are applied and compared as capping layers for low-temperature and Au-free Ta/Al-based ohmic contacts. In particular, the TiN-capped metal stack is shown to improve the thermal stability of the metal stack during annealing with respect to Ta-capped schemes. Afterwards, the TiN capping layer is substituted by a TaN layer in order to obtain a better metal stack conductivity which eventually improves the overall contact resistance.

Thermal stability of Ta-capped and TiN-capped ohmic contacts

In the case of AlGaN/GaN heterostructures without AlN spacer layer, the Ta/Al/Ta metal stack showed ohmic behavior already at an annealing temperature of 500 °C, as presented in previous section. However, during the experimental investigation a further increase of the annealing temperature resulted in a low-conductive and non-ohmic behavior of the contacts. Figure 5.3 summarizes the results obtained for the Ta/Al/Ta metal stack (Sample C.I) sequentially annealed for 3 minutes at 500 °C, 550 °C and 600 °C. Although ohmic behavior with promising R_c values of about $0.9 \pm 0.1\ \Omega\,\text{mm}$ are obtained for 500 °C and 550 °C, most of the samples metallized with Ta/Al/Ta became highly resistive and showed a non-ohmic behavior at 600 °C.

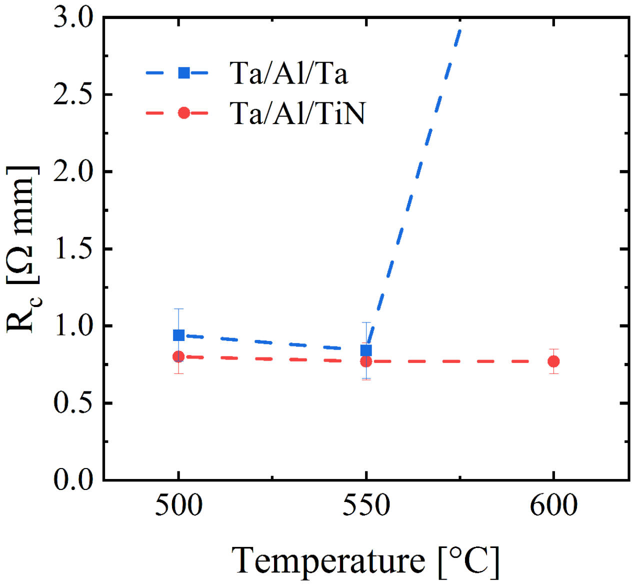


Figure 5.3: Contact resistance R_c versus annealing temperature for sequential annealing of Ta/Al/Ta (Sample C.I) and Ta/Al/TiN (Sample C.II) contacts. Error bars indicate the variation of different TLM structures. The Ta/Al/Ta showed a non-ohmic and highly resistive behavior after annealing at 600 °C.

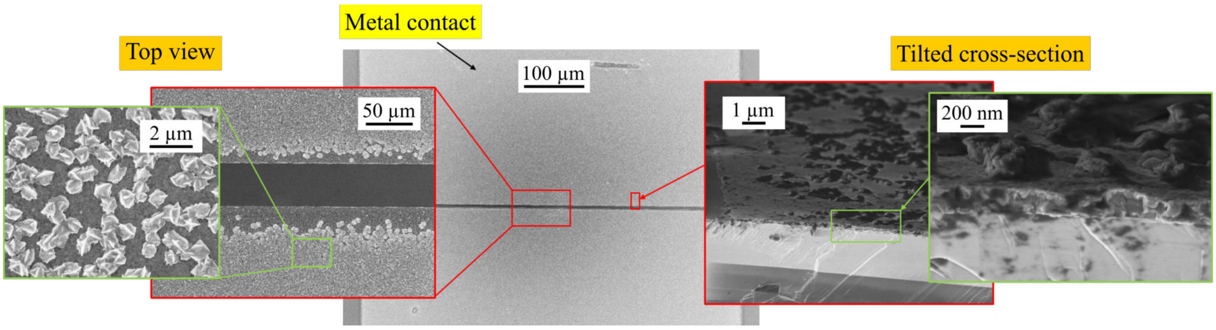


Figure 5.4: SEM images of top view and tilted view of cross-sections of a cleaved 20 nm Ta-capped metal stack after annealing at 600 °C. The metal stack shows a rough surface and grain formation. Electrically, the metal stack conductivity of the contacts annealed at 600 °C resulted to be almost completely lost.

In addition to the nearly complete loss of the metal stack conductivity, the surface morphology of the contacts appeared rough with grain formation on the contact surface. Figure 5.4 shows SEM top-views of the surface and tilted cross-sections of a 20 nm Ta-capped contact annealed at 600 °C. Crystalline structures can be seen with height corrugations up to 50-100 nm in comparison to the almost featureless topography obtained for the as-deposited stacks and layer stacks annealed at 500 °C and 550 °C. The same degradation effect was also observed after annealing at 600 °C for a Ta-capped sample with a thicker Ta capping layer of 40 nm (not shown here).

The origin of the thermal instability of Ta-capped metal stacks annealed at 600 °C was investigated by transmission electron microscopy (TEM) measurements. An example of a TEM image of the cross-section of a Ta/Al/Ta metal stack with 20 nm of Ta as capping layer after annealing at 600 °C is shown in Figure 5.5a. As one can see, Ta strongly diffuses into the Al layer from both the capping

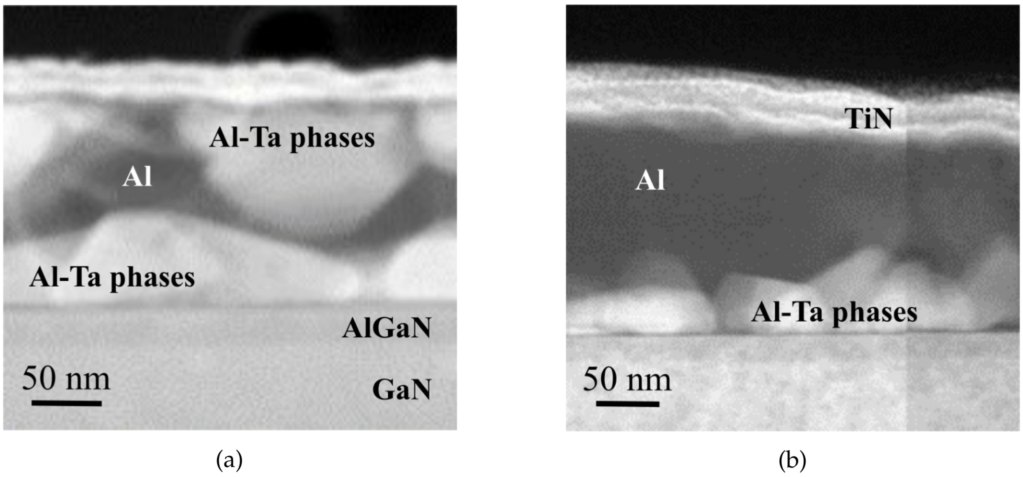


Figure 5.5: Scanning transmission electron microscopy (STEM) darkfield image of cross-section of (a) Ta/Al/Ta and (b) Ta/Al/TiN metal stacks after annealing at 600 °C. Bright trapezoidal and triangular structures reflect most likely crystal grains of $TaAl_3$ phase as shown from the EDX analysis of Figure 5.6.

and bottom layers by forming Ta–Al intermetallic phases during the annealing. In particular, as shown from the energy dispersive X-ray spectroscopy (EDX) analysis of Figure 5.6, $TaAl_3$ is the main phase of the grains formed during annealing. The latter result is in line with other studies and reports indicating $TaAl_3$ as the most stable metallic phase between 600 °C and 1500 °C in case of Ta/Al-based systems.[109, 112, 114, 115, 152] Beside this severe structural change caused by a strong Ta–Al alloying in case of contacts annealed at temperatures above 550 °C, electrical measurements revealed an almost complete loss of conductivity of the metal electrodes. To prevent the strong intermixing between the Ta cap material and Al as well as protection against oxidation, the cap material layer was substituted by TiN. The corresponding R_c values obtained from the

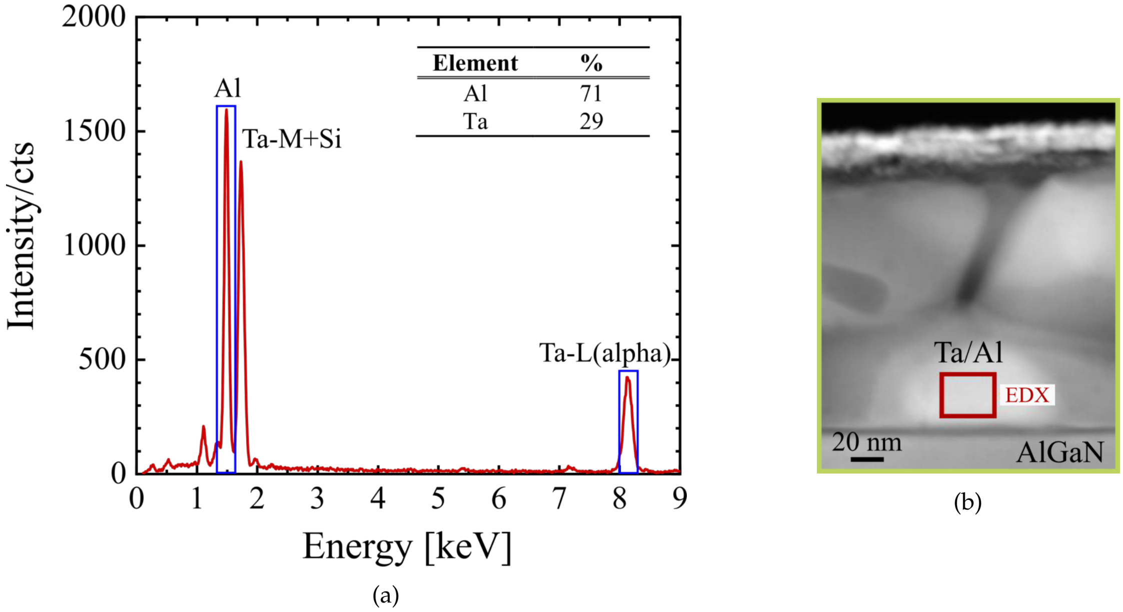
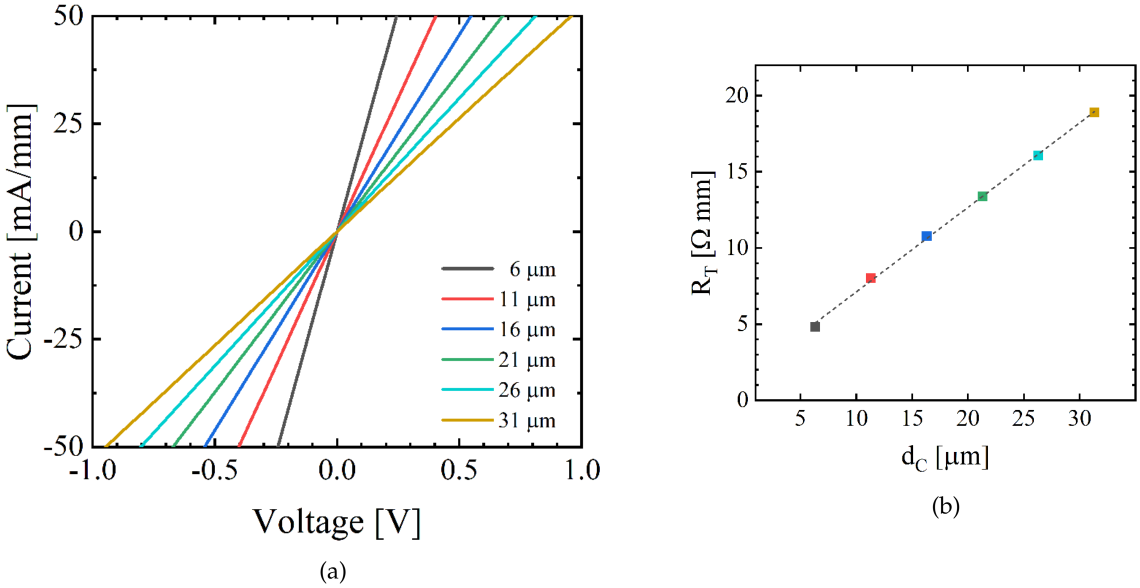


Figure 5.6: (a) EDX spectrum and data (inset) corresponding to the red marked area in (b) which shows an STEM darkfield image of a Ta/Al/Ta metal contact annealed at 600 °C.

TLM structures of Ta/Al/TiN contacts (Sample C.II) after sequential annealing at 500 °C, 550 °C and 600 °C are also reported in Figure 5.3. The values of R_c are in the range of the ones reported at 500 °C and 550 °C in the case of the Ta-capped metal stack. In particular, an R_c of about $0.8 \pm 0.1\ \Omega\,\text{mm}$ was obtained after annealing at 500 °C. In contrast to the Ta-capped metal stack, the Ta/Al/TiN metallization scheme was thermally stable during the annealing at 600 °C and showed an ohmic behavior at this temperature. The I–V measurements and the resulting TLM curves of the TiN-capped metal stack after annealing at 600 °C are shown in Figure 5.7. Moreover, the TEM image of the cross-section of the Ta/Al/TiN metal stack after annealing at 600 °C in Figure 5.5b shows that Ta–Al intermetallic phases are formed in the bottom part of the stack, but in the upper part no significant metal intermixing and grain formation can be observed. The TiN cap improves the mechanical, electrical and chemical stability of the metal stack upon annealing, which is not only important with respect to contact resistance, but also to device integration and potential thermal budgets after contact formation.



(a)

(b)

Figure 5.7: (a) I-V measurements of the TLM structure of the Ta/Al/TiN metal stack (Sample C.II) annealed at 600 °C. In (b) the corresponding TLM curve from which R_c is extrapolated. The values extracted are $R_c = 0.8\ \Omega\,\text{mm}$ and $R_{sh} = 530\ \Omega\ \text{sq}^{-1}$.

Beside material aspects in the metal stack, it is important to notice that independently from the capping layer the AlGaN barrier seems structurally undistorted (see Figure 5.5). Metal protrusions reaching into the AlGaN barrier with few 10 nm extension, as often reported for other high-temperature contacts, could not be observed in the TEM images of Figure 5.5. This aspect will be important and further discussed in Section 5.1.3 where the physical nature of the current transport through the metal/semiconductor interface will be discussed.

Metal stack conductivity of TiN-capped and TaN-capped ohmic contacts

Using the compound metal TiN as capping layer circumvents the alloy formation, thereby making the contacts much more stable under annealing. However, compound metals could have moderate bulk conductivities compared to pure metals which can increase the overall metal stack resistivity, especially if conductive alloys are not formed with the underlying metal layers during annealing. For this reason, a suitable material must be also employed as capping layer in order to ensure a negligible metal pad resistance with respect to the resistance at the metal/semiconductor interface. Table 5.2 shows the resistivity of sputtered TiN and TaN layers measured by four-point method, before and after annealing at 550 °C for 3 minutes in N_2. As reference, the latter are compared to the values obtained for pure Al and Ta layers.

Table 5.2: Resistivity of sputtered metals used in this work measured by four-point method, before and after annealing at 550 °C for 3 minutes in N_2.

Resistivity [Ω m]	before RTA	after RTA
Al	9.4×10^{-8}	9.5×10^{-8}
Ta	8.6×10^{-7}	8.8×10^{-7}
TiN	1.7×10^{-3}	2.7×10^{-3}
TaN	5.9×10^{-6}	6.1×10^{-6}

As one can see, in all cases the annealing has a minor influence on the resistivity value. However, the sputtering process employed for the TiN deposition resulted in a resistivity about four order of magnitude larger than the one obtained for Al and Ta. It is worth mentioning that during the course of the experimental work, the use of TiN caused some practical issues. Its poor conductivity was experienced by difficulties in obtaining good contacts between the probes and the metal pads during measurement except by scratching the metal pads. For this reason, TaN was considered as alternative material to be employed as capping layer. Being a compound material, TaN also prevents a strong intermixing with the underlying metals as in the case of TiN but with a lower resistivity compared to TiN, closer to the values obtained for Al and Ta. Although a detailed analysis of the impact of the capping layer on the overall metal stack resistivity was not performed, TLM structures fabricated with Ta/Al/TiN and Ta/Al/TaN metal stacks with same thicknesses of each metal layer and on the same epitaxial materials resulted in good probe-pad contact and slightly lower contact resistances when TaN was employed as capping layer. TaN was also tested to be thermally stable up to 700 °C. For these reasons, TaN was chosen as suitable capping layer and TaN-capped metal stacks will be used in Chapter 7 for the integration of Ta/Al-based ohmic contacts in MIS-HEMT devices.

5.1.3 Nature of current transport

The nature of the current transport through the metal/semiconductor interface of low-temperature and Au-free Ta/Al-based ohmic contacts is investigated in this section. Temperature measurements of the sheet resistance as well as the contact resistance were performed to assess the temperature dependence of the specific contact resistivity ρ_c, which eventually determines the type of carrier transport mechanism through the metal/semiconductor interface (see Section 4.3).

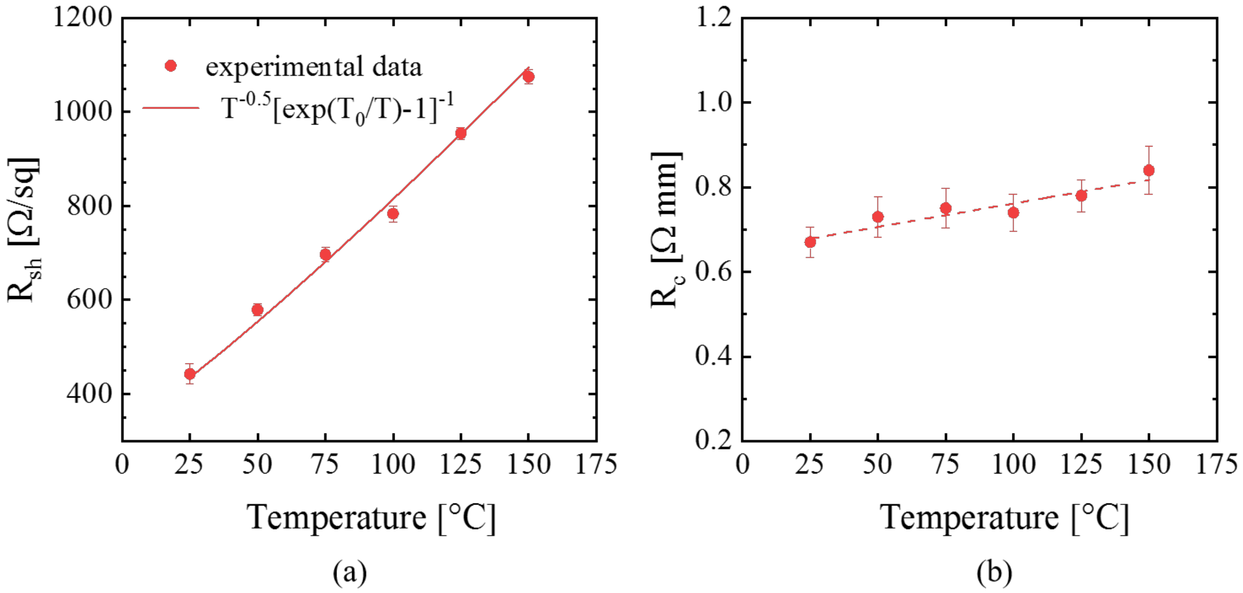


Figure 5.8: (a) R_{sh} and (b) R_c as a function of the temperature for the Ta/Al/TiN metal stack (Sample C.II) annealed at 500 °C. The solid line in (a) shows the fit of the experimental data with the temperature dependence $T^{-0.5}\times[\exp(T_0/T)-1]^{-1}$ in accordance with the mobility reduction due to increased phonon scattering with higher temperatures. The dashed line in (b) is only a guide to the eye.

The analysis was performed on the Ta/Al/TiN metal stack (Sample C.II) annealed at 500 °C for a measurement temperature ranging from 25 °C to 150 °C. Figure 5.8 shows the extracted values of the R_{sh} and R_c as a function of temperature. The sheet resistance of the 2DEG is strongly increasing with increasing temperature, whereas the contact resistance given per unit contact width is only slightly increasing. Since R_{sh} is inversely proportional to the 2DEG mobility μ (see Equation 2.10), the temperature behavior of R_{sh} was found to be in accordance with a model taking into account only the reduction of the 2DEG mobility due to the increased optical phonon scattering for higher temperatures, described by the following temperature dependence:

$$\mu(T) \propto T^{0.5}[exp(T_0/T) - 1], \tag{5.1}$$

where T_0 is the phonon temperature corresponding to the longitudinal-optical (LO)-phonon energy $\hbar\omega_{LO}$.[29, 31] In Figure 5.8, the experimental data of R_{sh}(T) are fitted accordingly to the temperature dependence of Equation 5.1, with T_0 = 1070 K and $\hbar\omega_{LO}$ = 90 meV. As one can see, this simple approximation almost completely describes the dominant temperature behavior of $R_{sh}(T)$. This also indicates that, hence the temperature behavior of R_{sh} is mostly related to the reduction of the carrier mobility with the increasing temperature, the charge carrier density of the 2DEG does not change significantly with temperature, as commonly reported.[153, 154]

The specific contact resistivity as a function of each measurement temperature is shown in Figure 5.9. The latter was calculated from the R_{sh} and R_c for each measurement temperature according to Equation 4.4 assuming an identical sheet resistance under the contacts and between the contacts, as discussed in Section 4.3. The resulting values of ρ_c show a decrease of the specific contact resistivity with increasing temperature. This temperature behavior is expected for a metal-semiconductor-2DEG connection governed by tunneling processes of (thermionic) field emission.[13] However, the specific mechanism of carrier transport is defined by the type of temperature dependence of ρ_c. In this case, the thermionic field emission model described by Equation 3.4 fits the trend of the data better than the field emission model. In the TFE regime, electrons are thermally excited to an energy where the barrier is sufficiently narrow to permit tunneling. For comparison three model curves according to TFE are plotted in Figure 5.9, which reflect the temperature dependence and absolute resistance values.[81, 83] The Schottky barrier height Φ_b and the semiconductor doping N_D are free parameters in the model curves and they are chosen to match the range of the experimental values and serve as guidance for the potential parameter space. Specifically, the range of values of Φ_b and N_D are 0.70 ± 0.05 eV and $3.9 \times 10^{19} \pm 0.5 \times 10^{19}$ cm^{-3}, respectively.

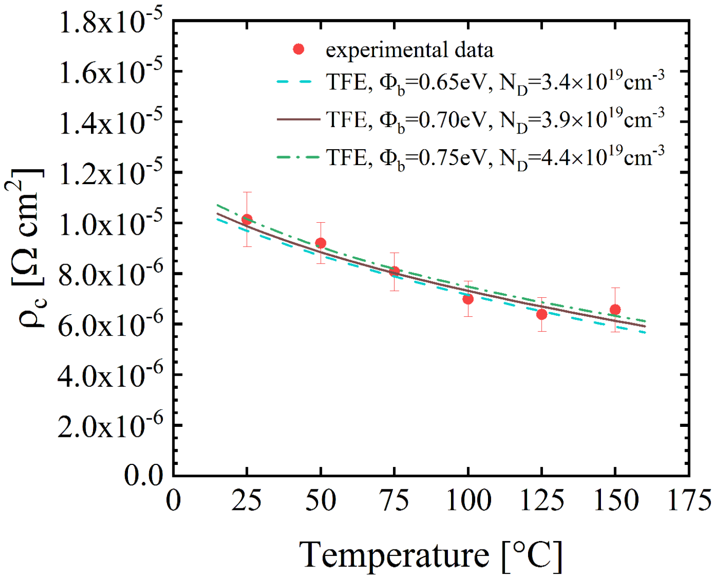


Figure 5.9: Temperature dependence of specific contact resistivity ρ_c for the Ta/Al/TiN metal stack (Sample C.II) annealed at 500 °C for a measurement temperature ranging from 25 °C to 150 °C. The lines represent the fits obtained using the TFE model with $\Phi_b = 0.70 \pm 0.05$ eV and $N_D = 3.9 \times 10^{19} \pm 0.5 \times 10^{19}$ cm^{-3}.

As one can see, although the restricted temperature range and the uncertainty of the measured values do not allow for an unambiguous fitting of Φ_b and N_D, the observed temperature dependence of ρ_c and following analysis support the contact formation with charge carrier transport through the

AlGaN barrier by thermionic field emission. This interpretation of the contact mechanism is also supported by the TEM investigations performed in the previous section showing an undistorted and well-defined AlGaN barrier layer which excludes the presence of a direct metal-2DEG contact due to metal protrusions reaching into the AlGaN barrier, as reported for other high-temperature contacts.[90, 97, 113, 115]

For the charge carrier transport through the AlGaN barrier dominated by TFE, the doping N_D of the semiconductor material has to be initiated by the contact annealing, since the unintentional doping level of the grown heterostructure material is at least two orders of magnitude lower than the range of 4×10^{19} cm^{-3} extracted by the model (see Figure 5.9). The formation of nitrogen vacancies in the AlGaN barrier acting like n-type donors is often reported as potential doping source.[13, 98] For Ta-based contacts, Malmros et al claimed that Ta extracts nitrogen from the GaN layer leaving nitrogen vacancies responsable for the mechanism of conduction.[109] In this work, the latter interpretation is supported by the electron energy loss spectroscopy (EELS) analysis shown in Figure 5.10 which was carried out on Ta/Al/TiN contacts (Samples C.II) after annealing at 550 °C for 3 minutes in N_2. Presence of nitrogen can be observed in the Ta-Al intermetallic phases which are formed at the bottom of the metal stack during annealing, indicating that nitrogen out-diffused from the AlGaN and GaN layers beneath the metal contact. It can also be noticed that the Ta bottom layer is still present at the interface and no Ga is detected in the metal stack.

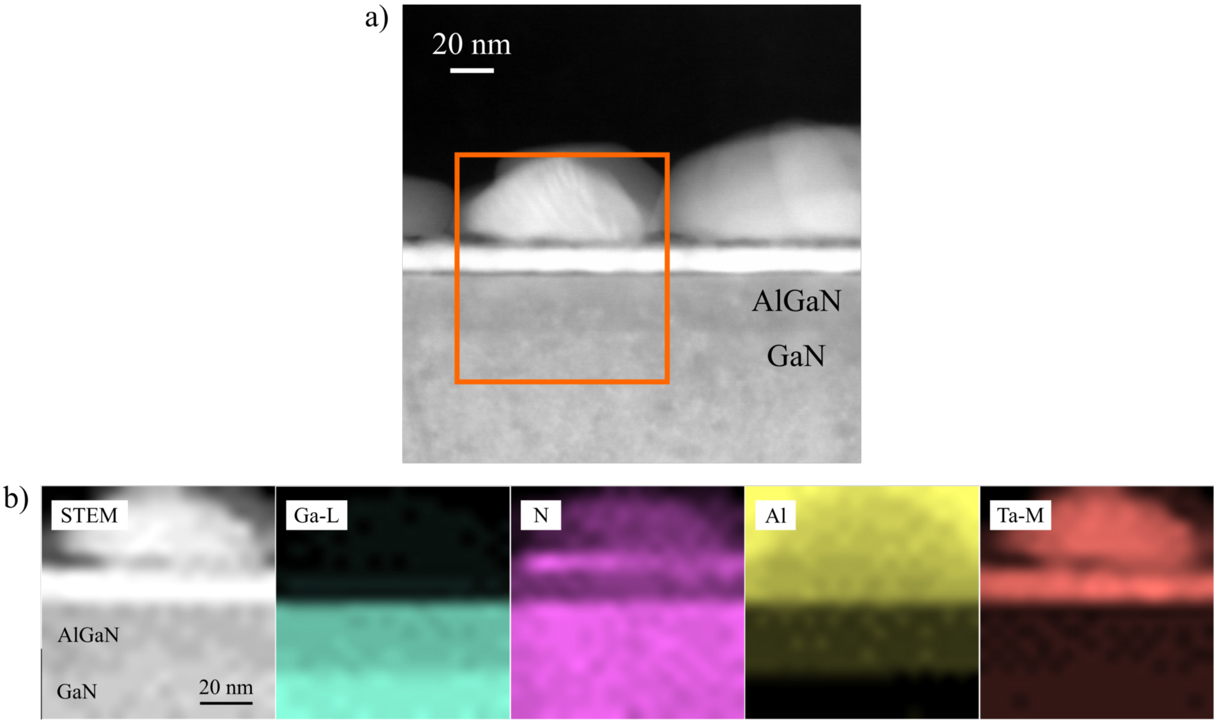


Figure 5.10: (a) STEM darkfield image of cross-section of the Ta/Al/TiN metal stack after annealing at 550 °C. The marked area indicates the area of the contact analyzed in (b) by EELS. While no Ga is detected in the metal stack, presence of nitrogen is revealed into the crystal grains of Ta-Al intermetallic phases formed at the bottom of the metal stack. This indicates that nitrogen out-diffused from the AlGaN and GaN layers beneath the metal contact. The Ta bottom layer is also still present at the interface.

A schematic band diagram of the AlGaN/GaN heterostructure under the ohmic contact which takes into account the presence of an n-type doped region formed after the contact annealing compared to the undoped case before ohmic contact formation is shown in Figure 5.11a. The high n-type doping region initiated by the annealing pulls down the conduction band towards the Fermi level E_F in the AlGaN layer resulting in a thinner potential barrier and higher tunneling probability.

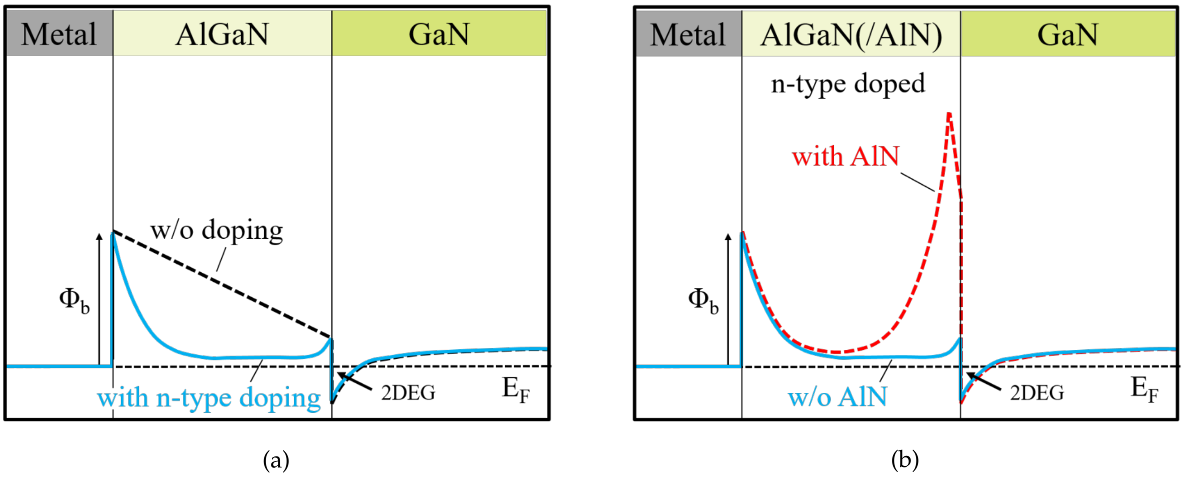


Figure 5.11: Schematic conduction band diagrams of the AlGaN/GaN heterostructure under the contact (a) without (dashed line) and with (solid line) an n-type region in the AlGaN barrier and (b) with the n-type region in the cases without (solid line) and with (dashed line) an AlN spacer layer. The n-type region is supposed to be initiated by the ohmic contacts annealing. E_F and Φ_b denote the Fermi energy and Schottky barrier height, respectively.

Another aspect is that the ohmic contact formation in the case of Ta/Al-based ohmic contacts annealed at low temperatures strongly depends on the presence of an AlN spacer layer at the AlGaN/GaN interface, as discussed before. Therefore, for comparison Figure 5.11b shows a schematic of the band diagram in the case of an AlGaN/GaN heterostructure provided of an AlN spacer layer after ohmic contact formation. With an AlN spacer layer, although the presence of an n-type doping initiated by the contact annealing, the higher energy barrier in the vicinity of the 2DEG channel originating from the larger band discontinuity between the AlN and the GaN layers can impede the carrier conduction. Therefore, following the interpretation of a charge carrier transport through the AlGaN barrier dominated by tunneling, the observation of a strong dependence of the contact formation on the presence of an AlN spacer layer seems to be well explained. This explanation is also in line with the weak dependence on the AlN presence observed for Au-containing Ti/Al-based ohmic contacts annealed at high temperatures where the contact mechanism is most likely given by a direct metal-2DEG connection.

5.1.4 Impact of Ta/Al thickness ratio

In the case of Ti/Al-based ohmic contacts, the ohmic contact formation and the contact resistance value have been demonstrated to strongly depend on the Ti/Al thickness ratio, independently from the capping layer.[13, 95] In particular, for Au-free Ti/Al-based contacts with Ti-rich metal stacks (i.e. Al/Ti thickness ratio below 3), the ohmic contact formation has been mostly achieved by annealing at high temperatures up to 900 °C.[116, 155, 156, 157, 158] On the contrary, for the very few reported Al-rich contacts, the ohmic behavior is obtained at low annealing temperatures around 550 °C.[14, 108] Moreover, once the ohmic behavior is achieved, an optimum annealing temperature exists in terms of contact resistance for each Ti/Al thickness ratio. In particular, it has been demonstrated that Ti-rich contacts require higher annealing temperatures to reach comparable contact resistances to those obtained with Al-rich contacts.[159] However, the dependence of the contact resistance on the Ti/Al ratio becomes weaker at higher annealing temperatures.[160, 161] In the case of Au-free Ta/Al-based ohmic contacts, Malmros et al. studied the behavior of Ta/Al/Ta metal stacks as a function of the annealing temperature for different values of the Al and Ta layers thickness.[109] Even though a clear dependency of the ohmic behavior and contact resistance on the Ta/Al thickness ratio was not indicated, an influence of the thickness of the Al and Ta layers on the optimum annealing temperature and on the contact resistance values was identified, similarly to Au-free Ti/Al-based contacts. The minimum contact resistance was achieved at the optimal annealing temperature of 550 °C for a 1:28 Ta/Al thickness ratio.

To obtain further insights on the influence of the Al and Ta layers thickness on the ohmic contact formation and on the contact resistance value in the case of Au-free Ta/Al-based ohmic contacts, Ta/Al-based metal stacks with different Ta layer thicknesses (or Ta/Al ratios) are compared in this section. In particular, Ta/Al/TiN metal stacks with fixed Al (240 nm) and TiN (20 nm) thicknesses and varying Ta bottom layer of 5 nm, 10 nm, 15 nm and 20 nm (Samples D.I - D.IV) were fabricated and compared for the annealing temperatures of 500 °C, 550 °C and 600 °C.

Figure 5.12 shows the R_c extracted from the described Ta/Al/TiN metal stacks as a function of the annealing temperature. While the samples with Ta bottom layer as thick as 10 nm, 15 nm and 20 nm achieved ohmic behavior at the annealing temperature of 550 °C, the sample with 5 nm of Ta bottom layer showed ohmic behavior already at 500 °C. Moreover, whereas the R_c resulted to increase by increasing the annealing temperature in the case of 5 nm of Ta bottom layer, for the samples with thicker Ta bottom layer, once the ohmic behavior was achieved at 550 °C, the contact resistance decreased for higher annealing temperatures. These results suggest that, while for a thicker Ta layer the decrease of the contact resistance with increasing annealing temperature is most likely related to the progress of the reaction process responsable for the ohmic contact formation, the thin Ta layer of 5 nm might lead to an early consumption of the Ta which prevents the improvement of the ohmic contact formation at higher annealing temperatures. Similar observations have been reported by Van Daele et al for Ti/Al-based ohmic contacts.[96] No clear explanation is instead attributed to the early ohmic behavior achieved at 500 °C for the metal stack with 5 nm of Ta bottom

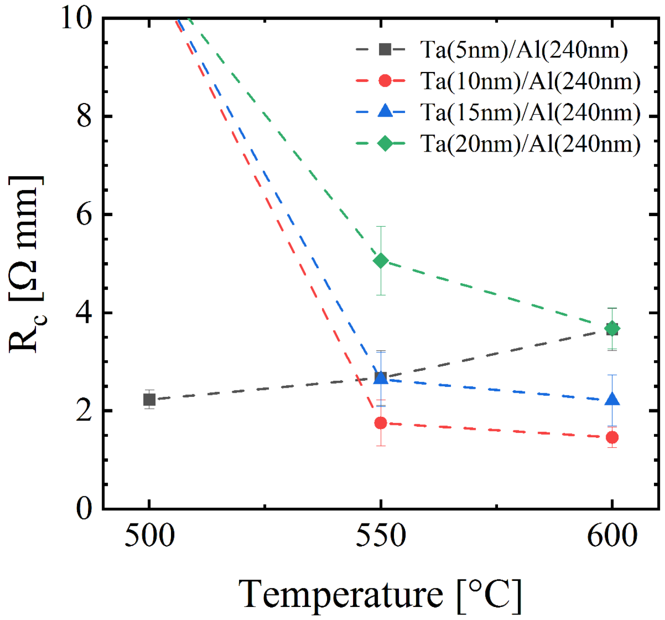


Figure 5.12: R_c of Ta/Al/TiN metal stacks with various Ta thickness (Samples D.I - D.IV) annealed at the temperatures of 500 °C, 550 °C and 600 °C. Error bars indicate the variation of different TLM structures. The metal stack with 5 nm of Ta (Sample D.I) showed an ohmic behavior already at 500 °C with an increasing R_c with increasing annealing temperature. On the contrary, the other metal stacks (Samples D.II - D.IV) with a thicker Ta layer from 10 nm to 20 nm showed the transition to ohmic behavior only at 550 °C and decreasing R_c for higher annealing temperatures. The dashed lines are only guides to the eye.

layer. Apart from the behavior of the sample with 5 nm of Ta bottom layer, a clear trend of the R_c with the variation of the thickness of the Ta bottom layer was obtained for the other samples. At a fixed annealing temperature, the contact resistance of these contacts lowered by decreasing the thickness of the Ta bottom layer. However, this difference seems much higher at the lower annealing temperature of 550 °C where the reaction process responsable for the ohmic contact formation is most likely not completed yet. Similar behaviors at annealing temperatures between 550 °C and 600 °C have been also observed in other works using Ti/Al-based metal schemes showing that contacts with a thinner Ti layer exhibit a lower contact resistance than contacts with thicker Ti layers.[160, 161]

One aspect is that, the former results cannot be uniquely attributed to the thickness of the Ta bottom layer or to the Ta/Al thickness ratio. However, to better visualize the impact of the Al/Ta ratio on the contact resistance, in Figure 5.13 the R_c has been plotted as a function of the Al/Ta thickness ratio t_{Al}/t_{Ta} for the annealing temperatures of 550 °C and 600 °C. Note that, no data are shown in the case of annealing at 500 °C since for this temperature the ohmic behavior was achieved only for the sample with 5 nm of Ta bottom layer. Evidently, from Figure 5.13 appears that an optimal t_{Al}/t_{Ta} exists independently from the annealing temperature. In particular, even though more experiments are required to precisely define the trend of Figure 5.13, an optimum Ta/Al thickness ratio can be estimated to be at about 1:25 Ta/Al thickness ratio, which is comparable with the result obtained by Malmros et al.[109]

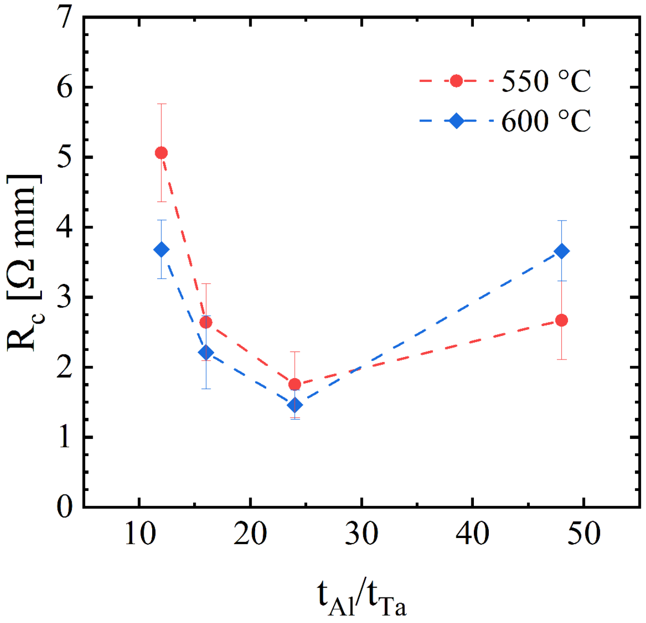


Figure 5.13: R_c as a function of the Al/Ta thickness ratio t_{Al}/t_{Ta} for Ta/Al/TiN metal stacks (Samples D.I - D.IV) annealed at the temperatures of 550 °C and 600 °C. Error bars indicate the variation of different TLM structures. At both annealing temperatures the contact resistance decreases towards a minimum value reached at a t_{Al}/t_{Ta} ratio of about 25. The dashed lines are only guides to the eye.

5.2 Comparison to high-temperature and Au-containing Ti/Al-based ohmic contacts

In this section, the low-temperature and Au-free Ta/Al-based ohmic contacts fabricated by sputtering on AlGaN/GaN heterostructures are demonstrated on 150 mm GaN-on-Si substrates and compared to Au-containing Ti/Al-based ohmic contacts annealed at high temperature. In particular, the Au-free manufacturing process of Ta/Al-based ohmic contacts is shown to give comparable results to conventional Ti/Al-based ohmic contacts and to be suitable for large area substrates. The integration of this contact scheme on large substrates is indeed an important prerequisite for the cooperative manufacturing of GaN-based devices in Si technology production lines.[14, 108, 162] The surface morphology and edge acuity of the two metallization schemes resulting from the use of different annealing temperatures are also presented as of critical concern for the down scaling of the devices. Moreover, since the annealing process can affect the thermal stability of the thin AlGaN layer and the 2DEG structure, the impact of the annealing temperature on the 2DEG sheet resistance before and after passivation is investigated. Finally, the temperature dependence of the sheet resistance as well as of the contact resistance of annealed contacts are discussed in order to investigate the different transport mechanisms in the two metallization schemes and to highlight novel future challenges which can arise from their integration in MIS-HEMT devices.

The details of the Ta/Al/TaN and Ti/Al/Ni/Au metal stacks and respective annealing conditions applied to the samples which are compared throughout this section are summarized in Table 5.3.

Table 5.3: Metal stacks and annealing conditions applied to the fabricated samples investigated in this section. Refer to Table 4.1 for specifications on the epitaxial material indicated in the column "Epi".

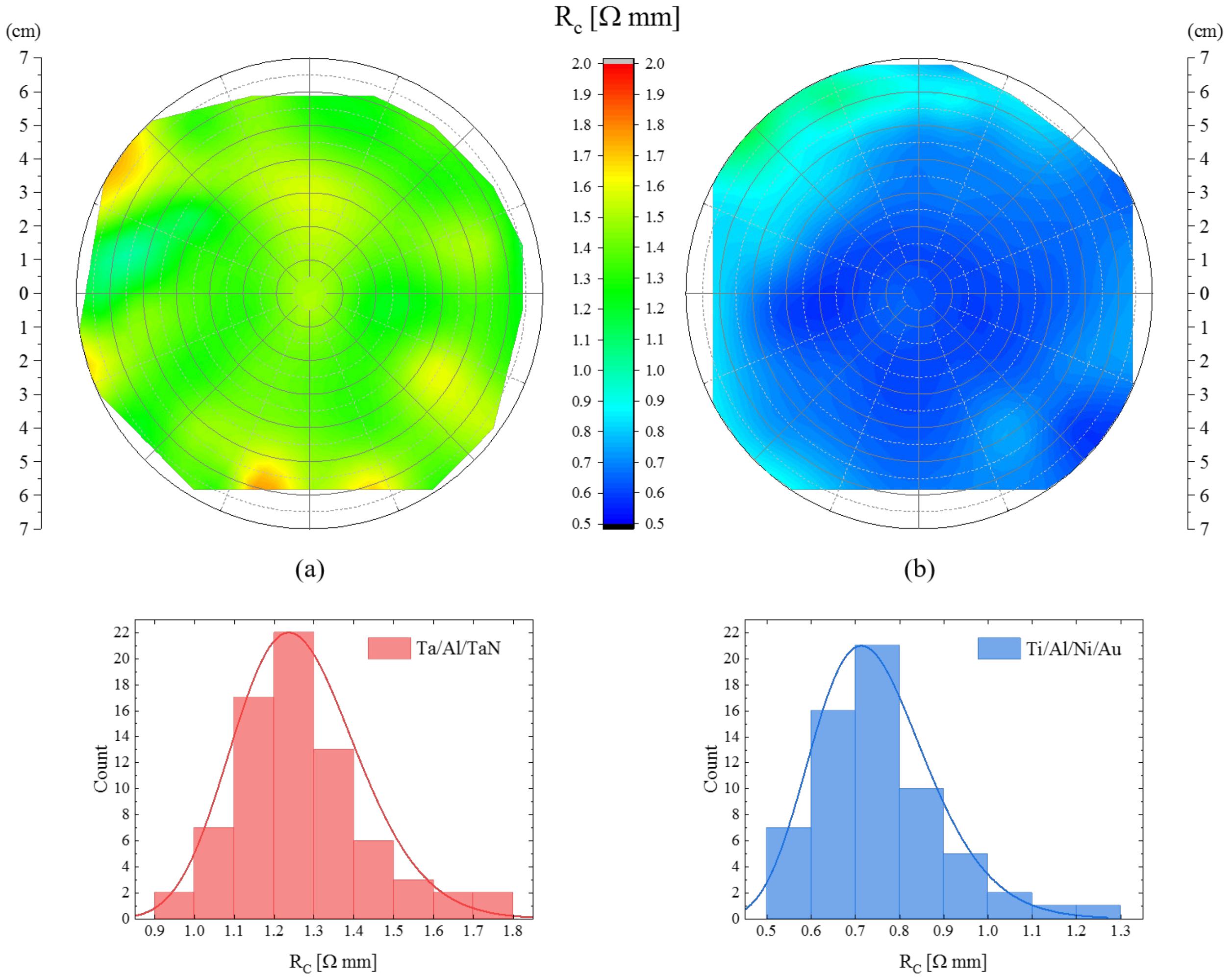
Metal stack	**Thickness** [nm]	**Annealing**	**Epi**
Ta/Al/TaN	10/240/20	550 °C, 3 min	III
Ti/Al/Ni/Au	35/200/40/100	850 °C, 30 sec	III

5.2.1 Contact resistance homogeneity

The functionality of Au-free Ta/Al-based ohmic contacts on large area substrates is a key requirement to develop a Si-compatible GaN technology. A homogeneous and sufficiently low contact resistance value over the entire substrate is mandatory for the fabrication of GaN devices in Si fabs handling 150 mm or even larger wafers. The main challenge is that, conversely to conventional Au-containing contact schemes which are generally more robust in the sense that ohmic behavior is quite easily achieved, Au-free ohmic contacts on AlGaN/GaN heterostructures appear to be strongly sensitive to the AlGaN/GaN heterostructure properties, the metal/AlGaN interface and the layers of the metal stack used.[13, 92, 95, 119] This difference is mainly attributed to the different mechanisms of current transport in the two type of contacts, as later discussed. In the case of Au-containing ohmic contacts annealed at high temperatures, since the contact is most likely given by metal protrusions penetrating into the AlGaN barrier and directly contacting the 2DEG, the ohmic connection is often easily achieved.[88, 90, 163] On the contrary, as discussed in the previous section, for Ta/Al-based ohmic contacts the current transport is instead given by tunneling through the AlGaN barrier which makes the contact formation more sensitive to the metal/semiconductor interaction during annealing and to the structure of the epitaxial layers (layers thickness, AlN spacer layer, etc.). For these reasons, Au-free Ta/Al-based ohmic contacts are here demonstrated on 150 mm GaN-on-Si wafers as a key step for their implementation in standard Si CMOS fabs.

Figure 5.14a and c show, respectively, the map and the corresponding distribution of the contact resistances extracted from TLM structures of sputtered Ta/Al/TaN metal stacks around the entire 150 mm GaN-on-Si substrate, after annealing at 550 °C for 3 minutes in N_2. All contacts revealed ohmic behavior after annealing. Moreover, homogeneous R_c values were obtained over the full substrate with a promising R_c mean value of $1.2 \pm 0.1\ \Omega\,\mathrm{mm}$. Therefore, although the contact resistance has been shown in previous section to be extremely sensitive to the Ta bottom layer, a good homogeneity is obtained. The latter results from the excellent uniformity ensured by the applied deposition method of sputtering (see Section 4.1.3). For comparison, Figure 5.14b and d show, respectively, the R_c map and resulting R_c distribution obtained from Ti/Al/Ni/Au contacts annealed at 850 °C for 30 seconds in N_2 revealing a comparable homogeneity to the one obtained for Ta/Al/TaN contacts and a mean value of R_c of $0.7 \pm 0.1\ \Omega\,\mathrm{mm}$.

Therefore, the Au-free manufacturing process of Ta/Al-based ohmic contacts presented in this work is not only fully Si CMOS-compatible but it also demonstrates feasibility of integration in terms of homogeneity and contact resistance in MIS-HEMT devices fabricated on large area substrates. These results contribute to the development and integration of GaN-based MIS-HEMT devices in Si CMOS facilities for 150-200 mm GaN-on-Si wafers.



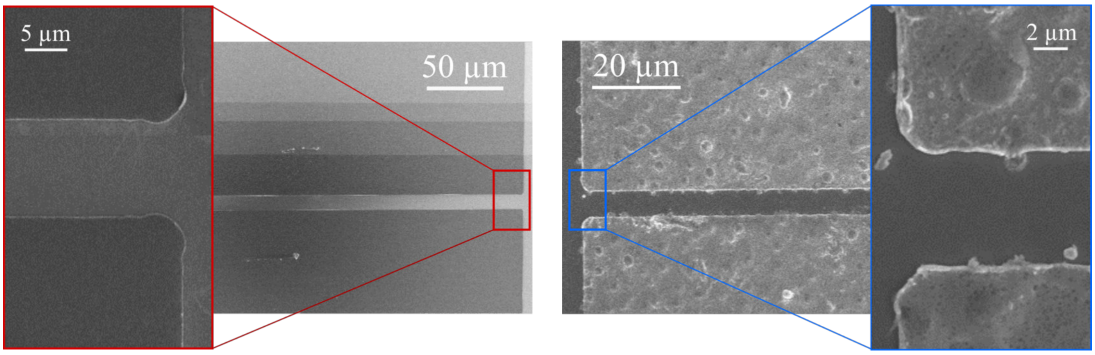
(a) (b)

(c) (d)

Figure 5.14: R_c maps of (a) sputtered Ta/Al/TaN and (b) evaporated Ti/Al/Ni/Au contacts on 150 mm GaN-on-Si wafers annealed in N_2 at 550 °C for 3 minutes and at 850 °C for 30 seconds, respectively. (c) and (d) R_c distributions extrapolated from the R_c maps in (a) and (b), respectively. Excellent homogeneity with R_c mean values of 1.2 ± 0.1 Ω mm and 0.7 ± 0.1 Ω mm are obtained over the entire substrates for Ta/Al/TaN and Ti/Al/Ni/Au contacts, respectively. White regions in (a) and (b) represent areas at the edge of the wafers that were not measured.

5.2.2 Surface morphology and edge acuity

The surface morphology of the ohmic contacts is another critical concern for the down scaling of the device dimensions. In the case of Au-containing Ti/Al-based ohmic contacts, the use of high annealing temperatures results in a rough surface morphology and poor edge acuity attributed to the reaction of Au with Al and/or to the low melting point of Al (∼ 660 °C) which tends to ball up during annealing.[13, 164, 165] On the contrary, one of the advantages of low-temperature and Au-free metallization schemes consists in the improvement of the surface morphology and edge acuity by the elimination of Au and by the use of lower annealing temperatures.[109, 112]



(a) (b)

Figure 5.15: SEM top views of (a) Ta/Al/TaN contacts annealed at 550 °C for 3 minutes and (b) Ti/Al/Ni/Au contacts annealed at 850 °C for 30 seconds. The Ta/Al/TaN metal pads show a smoother surface morphology corresponding to a better edge acuity after annealing.

An example of SEM top-views of the contact surface obtained in the case of sputtered Ta/Al/TaN contacts annealed at 550 °C for 3 minutes compared to Ti/Al/Ni/Au contacts annealed at 850 °C for 30 seconds is shown in Figure 5.15. As one can see, the use of low annealing temperatures results in a smoother surface morphology with sharper edge acuity in the case of Ta/Al-based contacts (Figure 5.15a), compared to the expected rough morphology of the Ti/Al-based contacts using a Au capping layer (Figure 5.15b).

5.2.3 Thermal stability of sheet resistance

Another important aspect which motivates the use of low-temperature and Au-free Ta/Al-based ohmic contacts is related to the impact of the annealing temperature on the thermal stability of the AlGaN/GaN heterostructure. In particular, the 2DEG sheet resistance has been shown to increase after annealing treatments using high temperatures, indicating the annealing for ohmic contact formation as a potential damaging step in a conventional micro-fabrication process.[166, 167, 168]

Figure 5.16 reports the R_{sh} maps obtained for Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts fabricated on 150 mm GaN-on-Si substrates after annealing at 550 °C for 3 minutes and 850 °C for 30 seconds, respectively. As one can see, the use of a lower annealing temperature improves the thermal stability of the heterostructure without passivation in terms of sheet resistance. In fact, given the as-grown R_{sh} of about 420 Ω/sq for both epitaxial materials, R_{sh} increases up to a mean value of about 500 Ω/sq for Ta/Al/TaN contacts annealed at the low temperature of 550 °C (see Figure 5.16a). On the contrary, a larger increase of R_{sh} up to a mean value of 660 Ω/sq is obtained for Ti/Al/Ni/Au contacts annealed at the high temperature of 850 °C (see Figure 5.16b).

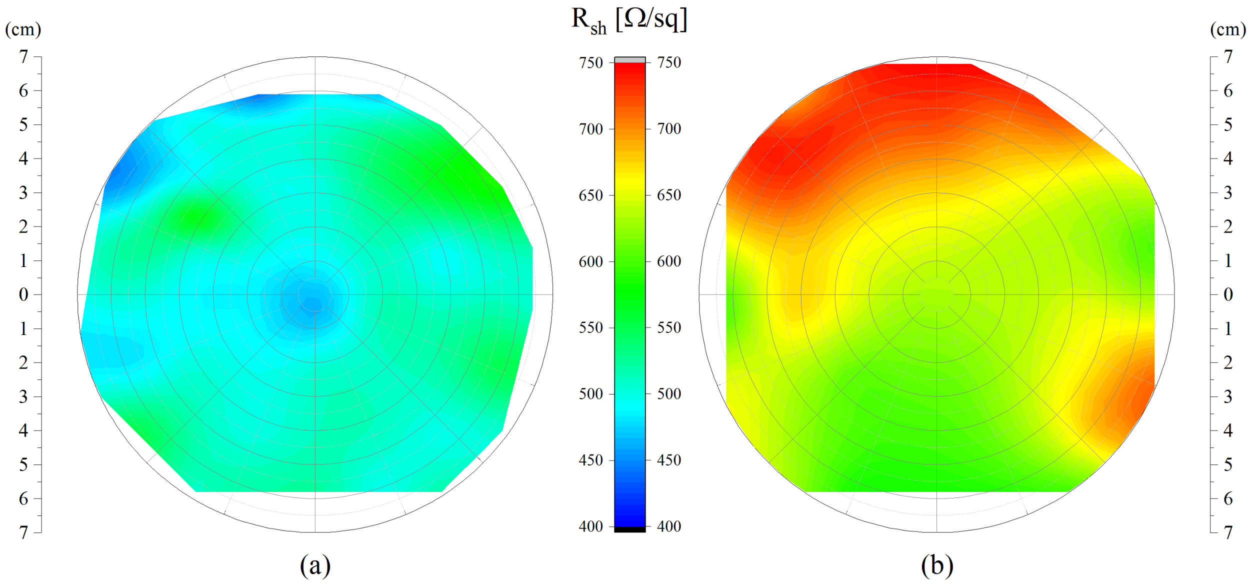


Figure 5.16: R_{sh} maps obtained after annealing of (a) Ta/Al/TaN contacts at 550 °C for 3 minutes and (b) Ti/Al/Ni/Au contacts at 850 °C for 30 seconds. R_{sh} mean values are (a) 500 ± 25 Ω/sq and (b) 660 ± 40 Ω/sq, respectively. A larger R_{sh} degradation is clearly visible after the high temperature anneal of the Ti/Al/Ni/Au contacts compared to the as-grown R_{sh} of about 420 Ω/sq. White regions represent areas at the edge of the wafers that were not measured.

Previous studies on the robustness of the 2DEG of AlGaN/GaN heterostructures under thermal treatments at temperatures ranging from 500 °C to 900 °C have shown that the significant increase of the sheet resistance with the annealing temperature can be associated with a modification of the 2DEG system in terms of reduction in the sheet carrier density and/or electron mobility.[100, 154, 168, 169, 170, 171] For example, Shiojima et al. reported an increase of the sheet resistance due to a significant loss of 2DEG density after anneal up to 800 °C.[100] Roccaforte et al. found that annealing AlGaN/GaN layers at 500 °C already resulted in a decrease of the 2DEG sheet carrier density and mobility.[169] Since the 2DEG structure is extremely sensitive to the surface condition of the heterostructure, the degradation of the 2DEG system is strongly correlated to the alteration of the AlGaN surface during thermal treatments. For this reason, proper surface passivation layers on top of the AlGaN surface are commonly adopted before processing ohmic contacts in order to improve the thermal stability of AlGaN/GaN heterostructures during annealing.[11] Hashizume et al identified serious stoichiometry disorder and nitrogen deficiency at the AlGaN surfaces processed by high temperature annealing.[172] Surface defects correlated to the nitrogen deficiency were suppressed by using SiN and Al_2O_3-based passivation schemes. SiN is widely used as passivation layer.[173] The same layer has been simultaneously used as passivation layer and gate insulator in MIS-HEMT devices.[11]

In this context, another interesting aspect is the effect of using a passivation layer deposited after the ohmic contacts annealing which can alter the surface thereby affecting the sheet resistance. For this purpose, 20 nm of Al_2O_3 were deposited by ALD on the TLM structures of the annealed

Ta/Al/TaN and Ti/Al/Ni/Au contacts. Figure 5.17 summarizes the R_{sh} obtained, starting from the as-grown value and proceeding with the R_{sh} obtained after the annealing and after the ALD-Al_2O_3 deposition. As previously discussed, the R_{sh} increases due to the ohmic contacts annealing with a larger increase in the case of Ti/Al/Ni/Au contacts annealed at higher temperature. As one can see from Figure 5.17, a recovery of the sheet resistance, much stronger in the case of Ti/Al/Ni/Au contacts, is instead obtained for both metal schemes after the Al_2O_3 passivation which results in a comparable value of R_{sh} with passivation for both samples. This result indicates that the thermal degradation of the sheet resistance during annealing is mostly related to surface effects on the unpassivated surface between the metal pads. A possible reason can be the creation of surface states during annealing which affect the 2DEG carrier concentration and whose net surface charge is later neutralized by the passivation layer, thereby restoring the 2DEG structure and the sheet resistance of the AlGaN/GaN heterostructure. This effect will be taken into account in Chapter 7 when discussing the integration of the two different types of contact schemes in MIS-HEMT devices using the ALD-Al_2O_3 layer as gate dielectric as well as passivation layer.

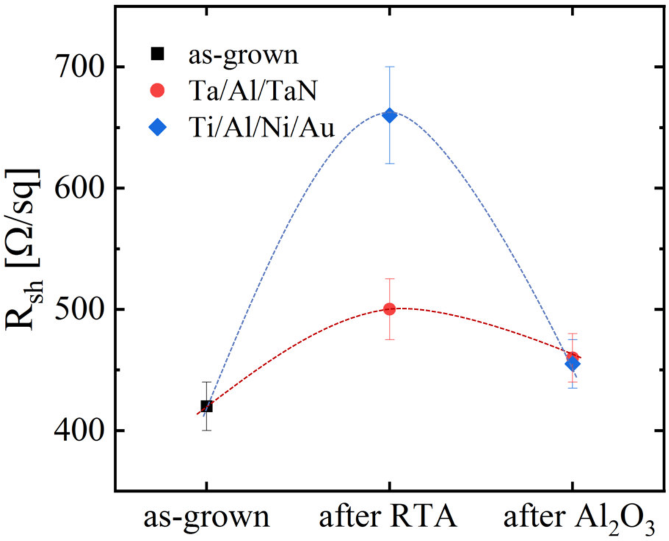


Figure 5.17: R_{sh} change of Ta/Al/TaN and Ti/Al/Ni/Au contacts after RTA (mean values taken from Figure 5.16) and after ALD-Al_2O_3 passivation. The as-grown R_{sh} value is about 420 Ω/sq for both epitaxial materials used. A recovery of R_{sh} towards the as-grown value can be seen in both cases. The dashed lines are only guides to the eye.

In conclusion, despite of the effectiveness of using a passivation layer before or after annealing, the low temperatures used for annealing Au-free Ta/Al-based contacts are beneficial to reduce the thermal impact on the AlGaN/GaN heterostructure without passivation. The latter is an important factor because, although the sheet resistance recovers after passivation this parameter mainly affects the DC performance of the device. Conversely, the surface structure could be still modified by the anneal at high temperatures in a way to detrimentally impact the dynamic behavior of the device by enhancing the vulnerability to trapping phenomena and transient behaviors. Finally, the lower thermal budget would beneficially add flexibility and opportunities in the fabrication process when a passivation layer is employed before ohmic contacts annealing but degrades with temperatures above 700 °C, for example by crystallization of an amorphous dielectric.[68]

5.2.4 Mechanism of current transport

In this section, the temperature dependence of the sheet resistance and of the contact resistance obtained from low-temperature annealed Au-free Ta/Al-based contacts and high-temperature annealed Au-containing Ti/Al-based contacts are compared in order to obtain additional insights into the transport mechanisms governing these two different metallization schemes.

The temperature measurements were performed on Ta/Al/TaN and Ti/Al/Ni/Au metal stacks annealed at 550 °C for 3 minutes and 850 °C for 30 seconds, respectively, and subsequently passivated with 20 nm of ALD-Al_2O_3. Temperature dependent measurements were performed in a range from room temperature (RT) to 200 °C. Figure 5.18 shows the R_{sh} and R_c values obtained for both metallization schemes as a function of the measurement temperature.

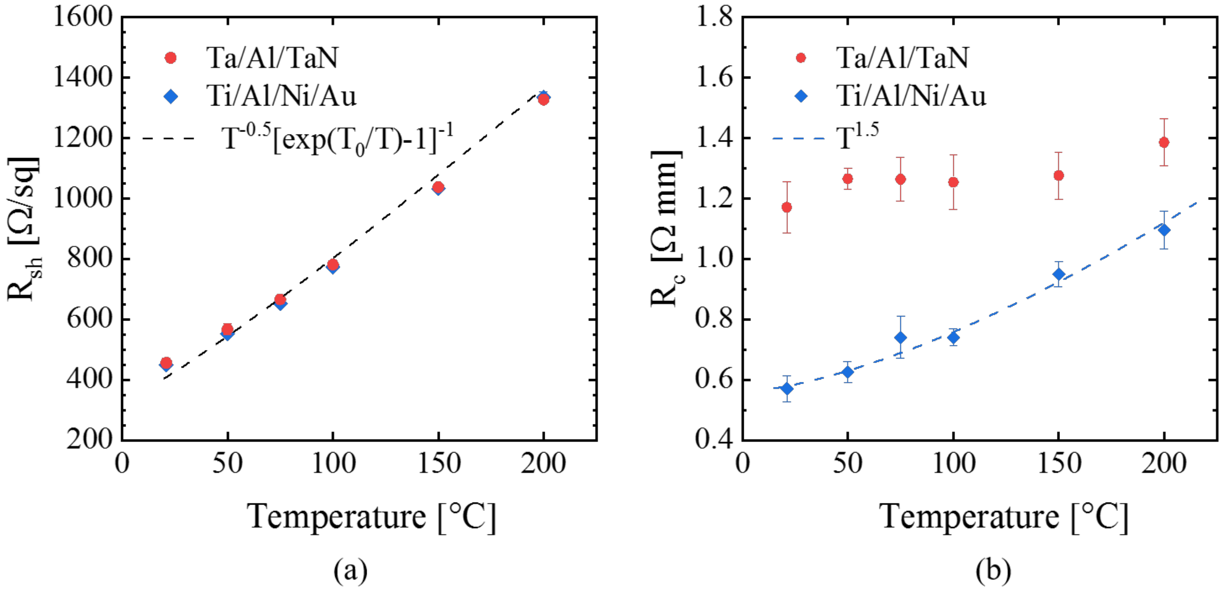


Figure 5.18: (a) R_{sh} and (b) R_c as a function of the temperature for Ta/Al/TaN and Ti/Al/Ni/Au metal stacks annealed at 550 °C for 3 minutes and 850 °C for 30 seconds, respectively, and subsequently passivated with 20 nm of ALD-Al_2O_3. The dashed line in (a) shows the fit of the experimental data with the temperature dependence $T^{-0.5} \times [\exp(T_0/T)-1]^{-1}$ in accordance with the mobility reduction due to phonon scattering, while the line in (b) shows the fit of the experimental data with the temperature dependence T^{α} with $\alpha = 1.5$ only for Ti/Al/Ni/Au ohmic contacts.

In accordance with the results obtained in Section 5.1.3, the temperature behavior of R_{sh} of both contacts is again following the mobility reduction due to increased optical phonon scattering, described by the temperature dependence of Equation 5.1 with a phonon energy $\hbar\omega_{LO} = 90$ meV corresponding to the phonon temperature $T_0 = 1070$ K, as shown in Figure 5.18a. Differently, two different temperature behaviors of the R_c were found for the two metallization schemes, as shown in Figure 5.18b. While for the Ta/Al/TaN contacts R_c slightly increases with temperature, in the case of Ti/Al/Ni/Au contacts R_c increases stronger with a temperature dependence of T^{α} with $\alpha = 1.5$. Such "metallic-like" behavior has been reported for similar contacts [13, 91] and refers to metallic systems where the resistance varies following a power law T^{α} with $1 < \alpha < 5$.[174]

For Ta/Al-based ohmic contacts, a similar temperature dependent study showing comparable trends for both R_{sh} and R_c was performed in Section 5.1.3. The resulting specific contact resistivity ρ_c, calculated by Equation 4.4, was well described with charge current transport through the AlGaN barrier by thermionic field emission tunneling, also supported by the evidence of a non-distorted AlGaN barrier beneath the metal electrode. As shown in Figure 5.19, the same interpretation of a 2DEG-semiconductor-metal contact governed by a thermionic field emission model is also confirmed with the present data with comparable values of Φ_b and N_D of 0.80 ± 0.05 eV and $4.0 \times 10^{19} \pm 0.5 \times 10^{19}$ cm^{-3}, respectively.

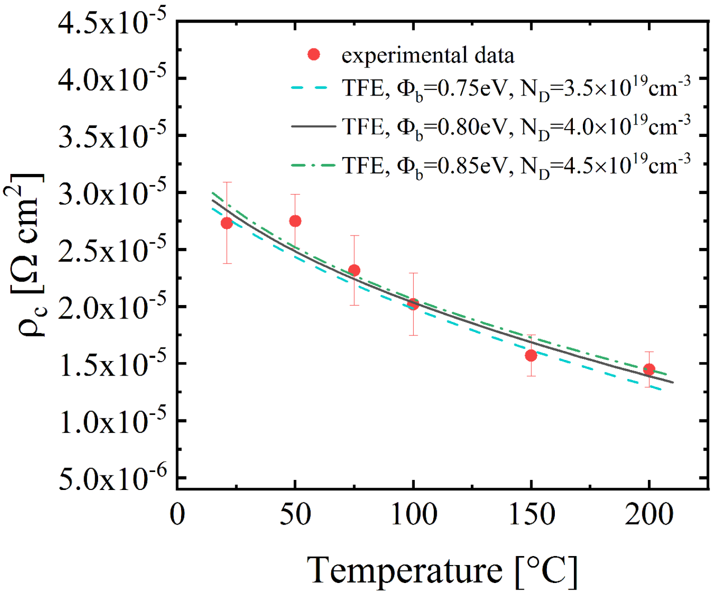


Figure 5.19: Temperature dependence of specific contact resistivity ρ_c for the Ta/Al/TaN metal stack annealed at 550 °C for a measurement temperature ranging from RT to 200 °C. The lines represent the fits obtained using the TFE model with $\Phi_b = 0.80 \pm 0.05$ eV and $N_D = 4.0 \times 10^{19} \pm 0.5 \times 10^{19}$ cm^{-3}.

Differently, for Au-containing Ti/Al-based contacts annealed at high temperatures, where the contact is most likely defined by localized metal protrusions through the AlGaN barrier directly in contact with the 2DEG, the concept of specific contact resistivity defined by the TLM model is instead not applicable.[80, 86] In fact, in this case the contact is better represented by a sidewall contact between the metal and the 2DEG rather than a metal/semiconductor interface represented by an areal stripe given by the transfer length L_T, as assumed in the TLM model (see Section 4.3.1). As a consequence, the actual contact consists more of line segments with horizontal current flow instead of a vertical current spreading at the edge of the contact. Figure 5.20 shows a schematic illustration of the contact geometries comparing the case of a 2DEG-semiconductor-metal connection in line with the TLM model with the case of a direct 2DEG-metal connection.

In the case of a direct 2DEG-metal connection, due to the horizontal current flow and assuming that the area/width of this type of contact is not changing with temperature, the temperature dependence of R_c should be rather analyzed. In this sense, the "metallic-like" temperature behavior of R_c of the Ti/Al/Ni/Au contacts shown in Figure 5.18b supports the ohmic contact mechanism based on a direct 2DEG-metal connection, most likely attributed to the direct sideway contact of the metal protrusions to the 2DEG. Similar results have been reported by Iucolano et al.[91]

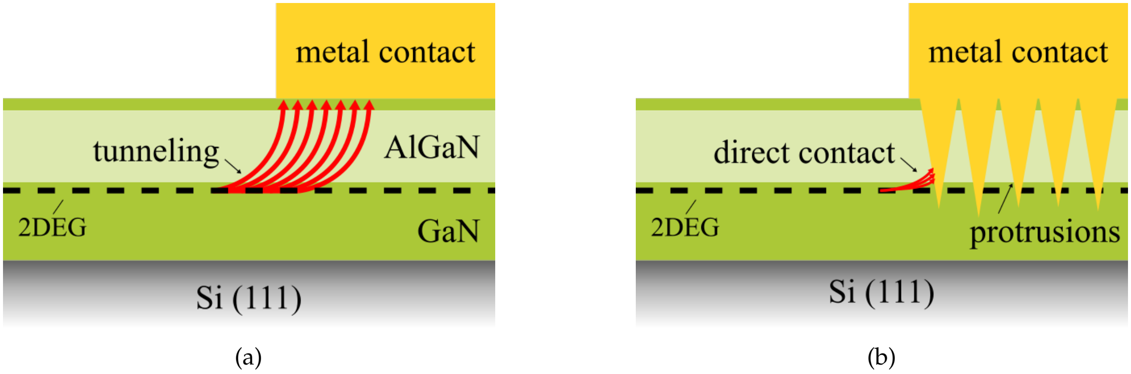


Figure 5.20: Schematic illustration of physical models of (a) a 2DEG-semiconductor-metal connection governed by tunneling in line with the TLM model and (b) a direct sideway 2DEG-metal connection due to metal protrusions into the AlGaN barrier.

In conclusion, even though the direct 2DEG-metal contact in the case of Ti/Al-based ohmic contacts prevents the calculation of the specific contact resistivity, the different temperature behavior of the contact resistance demonstrates that different transport mechanisms are involved in the two types of metallization schemes. Moreover, even though an "intimate" contact 2DEG-metal is often reported to be more efficient in terms of conduction and specific contact resistivity than tunneling through the AlGaN barrier,[13, 175] the comparison of the temperature behavior of the contact resistance also suggests that a 2DEG-semiconductor-metal connection by tunneling can be preferable for devices operating at high temperatures, as it will be discussed in Chapter 7.

5.3 Summary

In summary, low-resistive and low-temperature Au-free ohmic contacts to 2DEG-containing AlGaN/GaN heterostructures have been achieved using Ta/Al-based metal stacks fabricated by sputtering. Contact resistance values lower than 1 Ω mm at annealing temperatures below 600 °C could be obtained without AlGaN barrier recess. For higher annealing temperatures the stability of the entire metal stack resulted to degrade when using a Ta cap layer due to strong Ta–Al alloying, which was circumvented by utilizing the compound materials of TiN and TaN as capping layer. Moreover, even though the contact properties could not be uniquely attributed to the thickness of the Ta bottom layer or to the Ta/Al thickness ratio, a dependency of the ohmic behavior from these contact features was also identified. The optimal Ta/Al thickness ratio was estimated to be at about 1:25 Ta/Al thickness ratio. The ohmic contact formation has been also shown to be sensitive to the presence of a thin AlN spacer layer at the AlGaN/GaN interface, which can be understood for a contact transport mechanism from the 2DEG through the AlGaN barrier to the metal governed by tunneling rather than for a direct 2DEG-metal connection. The former interpretation of the contact mechanism was supported by TEM investigations showing an undistorted and well-defined AlGaN barrier layer as well as by the decrease of the specific contact resistivity with increasing temperature well described by the thermionic field emission model. Also, presence of nitrogen in the metal stack was revealed by EELS analysis indicating the out-diffusion of nitrogen from the AlGaN barrier initiated by the contact annealing as potential n-type doping source of the AlGaN barrier. Based on this interpretation of contact formation, even lower values of the contact resistance might be realized by the utilization of an AlGaN barrier recess etch within the contact process.

The low-temperature and Au-free Ta/Al-based ohmic contacts were also demonstrated on 150 mm GaN-on-Si substrates. In particular, the Au-free manufacturing process of Ta/Al-based ohmic contacts implemented by sputtering on large area substrates was shown to give comparable results to conventional Au-containing Ti/Al-based ohmic contacts and therefore to be suitable for the integration of GaN-based devices in Si platforms. Homogeneous R_c values as low as 1.2 ± 0.1 Ω mm could be obtained over the entire substrate using Ta/Al/TaN metal stacks annealed at 550 °C. Also, the low annealing temperature used for Ta/Al-based contacts resulted to be beneficial in reducing the impact of the annealing on the thermal stability in terms of sheet resistance of the heterostructure without passivation. Moreover, the contact resistance for low-temperature annealed Au-free Ta/Al-based contacts showed a weaker increase with temperature compared to high-temperature annealed Au-containing Ti/Al-based ohmic contacts. The different behavior was attributed to the different contact type based on a direct metal-2DEG connection in the case of high-temperature annealed Au-containing Ti/Al-based contacts, compared to a 2DEG-semiconductor-metal connection governed by tunneling for Ta/Al-based ohmic contacts. Due to the weaker increase with temperature of the contact resistance for the Ta/Al-based contact scheme, the latter was also indicated as more suitable candidate for (MIS-)HEMT devices operating at high temperatures, as it will be discussed in Chapter 7.

6 Engineering and optimization of MIS-gate module

The employment of an insulator in MIS-HEMTs compared to Schottky-gate HEMTs gives the additional advantage of significant gate leakage reduction, enabling larger gate bias swing and better immunity to gate breakdown.[9, 53, 176] However, the insertion of a gate dielectric can cause operational instability due to the presence of high-density trap states located at the dielectric/III-nitride interface or within the dielectric.[11, 140, 141] This chapter investigates the dielectric/III-nitride interface and dielectric bulk properties using MISH capacitor structures where ALD-Al_2O_3 is used as insulator because of its promising properties as gate dielectric in MIS-HEMT devices. In particular, the effects on the ALD-Al_2O_3/III-nitride interface of the O_2 plasma-based surface preconditioning applied before the Al_2O_3 deposition and of the N_2 annealing after gate metallization are investigated in order to minimize the trap states at the interface. The influence of the annealing temperature of the postmetallization treatment on the gate leakage currents is also discussed. Finally, since the annealing for the ohmic contacts formation is a crucial processing step during the MIS-HEMT fabrication, the impact on the Al_2O_3/III-nitride interface of the low annealing temperature employed for the formation of Ta/Al-based ohmic contacts is discussed and compared to the impact of Ti/Al-based contacts annealed at high temperature. This chapter is based on the results published in Ref. [177].

Table 6.1: List of MISH capacitor structures highlighting the processing conditions which are compared and investigated in this chapter. Refer to Section 4.2 for more details about the fabrication process conditions and to Table 4.1 for specifications on the epitaxial materials indicated in the column "Epi".

Sample	**Epi**	**Ohmic contacts**	**SPC** (optional)	**Dielectric**	**Gate electrode**	**PMA** (optional)
E.I	IV	Ti/Al/Ni/Au 850 °C, 30 sec, N_2		16 nm ALD-Al_2O_3	100/150 nm Ti/Au	
E.II	IV	Ti/Al/Ni/Au 850 °C, 30 sec, N_2	x	16 nm ALD-Al_2O_3	100/150 nm Ti/Au	
E.III	IV	Ti/Al/Ni/Au 850 °C, 30 sec, N_2	x	16 nm ALD-Al_2O_3	100/150 nm Ti/Au	N_2, 10 min 300/350/400 °C
F.I	III	Ta/Al/TaN 550 °C, 3 min, N_2	x	16 nm ALD-Al_2O_3	100/150 nm Ti/Au	
F.II	III	Ti/Al/Ni/Au 850 °C, 30 sec, N_2	x	16 nm ALD-Al_2O_3	100/150 nm Ti/Au	

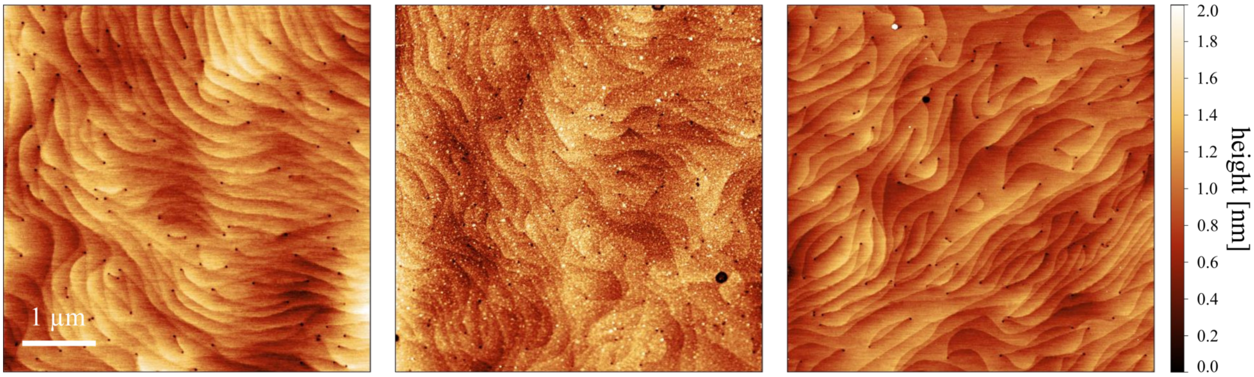
The detailed processing steps of the MISH capacitor structures investigated throughout this chapter are summarized in Table 6.1. For simplicity, the samples are arranged in two groups named as E and F. Specifically, samples of the group E were used to investigate the influence on the ALD-Al_2O_3/III-nitride interface and on the gate leakage currents of the SPC treatment before the gate dielectric Al_2O_3 deposition and of the PMA treatment after gate metallization. Lastly, samples of group F were instead employed to evaluate the impact on the quality of the Al_2O_3/III-nitride interface of the annealing process used for the ohmic contacts formation.

6.1 Surface preconditioning

The quality of the dielectric/III-nitride interface largely depends on the condition of the GaN surface prior to the dielectric deposition.[10] In particular, surface contaminations and morphology degradation of the GaN surface, caused by the fabrication processes preceding the dielectric deposition, can affect the dielectric/III-nitride interface and eventually deteriorate the performance of the MIS-gate module and of resulting MIS-HEMT devices.[178] For this reason, it is essential to obtain a clean GaN surface before the dielectric deposition by removing contaminants without however damaging the crystal order or introducing additional defect states. Based on this, the following section investigates the ALD-Al_2O_3/III-nitride interface using MISH capacitors where the SPC treatment is employed prior to the Al_2O_3 deposition. In particular, the effectiveness of this O_2 plasma-based treatment is first evaluated by investigating its influence on the GaN surface morphology, which is primarily affected by the ohmic contacts processing before the gate dielectric deposition. Afterwards, the impact of the SPC on the electrical properties of the Al_2O_3/III-nitride interface in MISH capacitors is investigated by using multifrequency C-V measurements from which the interface state density D_{it} is determined.

6.1.1 GaN surface morphology

Figure 6.1a shows the atomic force microscopy (AFM) image of an as-grown MOCVD GaN-capped AlGaN/GaN heterostructure surface which shows the typical smooth surface with terraces of mono- or bi-layer high step edges.[68] Small pits are also visible at the termination of step edges, which are associated to the endpoints of dislocations with a screw component running vertically through the epitaxial material. As comparison, a GaN surface before the gate dielectric deposition but after Ti/Al/Ni/Au ohmic contacts patterning, organic wet cleaning and subsequent annealing at 850 °C for 30 seconds is shown in Figure 6.1b. As one can see, the surface morphology appears rough and covered by nanosized particles which is attributed to a partial surface contamination and decomposition after lift-off and the high temperature annealing for the ohmic contact formation. In order to clean and restore the morphology of the GaN surface affected by these fabrication processes, the SPC treatment consisting of a partial surface oxidation by O_2 plasma and a subsequent wet cleaning by HCl is applied to the GaN surface after ohmic contact formation (see Section 6.1). As shown from the AFM image of a GaN surface after applying the SPC treatment in Figure 6.1c, the SPC is indeed effective in removing contaminants and restoring the flat step-like terrace structure of the surface resulting in a template similar to the usual as-grown GaN surface of Figure 6.1a. In the next section, the impact of the SPC on the electrical properties of the Al_2O_3/III-nitride interface of MISH capacitors is investigated.



(a) (b) (c)

Figure 6.1: AFM images showing the surface morphology of a MOCVD GaN/AlGaN/GaN surface (a) as-grown, (b) before SPC and (c) after SPC. The SPC treatment is effective in removing contaminants and restoring the surface morphology resulting in a flat step-like terrace structure similarly to the as-grown GaN surface.

6.1.2 Influence on ALD-Al_2O_3/III-nitride interface

The experimental C–V characteristics of MISH capacitors with 16 nm thick ALD-Al_2O_3 fabricated without (Sample E.I) and with (Sample E.II) SPC treatment are shown in Figure 6.2. The voltage was swept from -10 V to 4 V and then back to -10 V. The measurement frequency was 1 kHz. The capacitance of the first flat part of the two characteristics, for both the up-sweep and the down-sweep curves, is given by the series capacitance of the AlGaN, GaN-cap and Al_2O_3 layers of 22 nm, 2 nm and 16 nm, respectively, in accordance with the capacitance model described in Section 4.3.2. However, the double-step C-V curve which is peculiar of a MISH capacitor with a double-interface structure, given by the Al_2O_3/GaN and AlGaN/GaN interfaces in this case, was only obtained for the MISH capacitor treated by SPC. In fact, in the case no SPC treatment was applied, the second step was instead not visible in the voltage range considered because the amount of interface traps was probably so large that the second step was already shifted beyond 4 V during the up-sweep measurement, after which the leakage currents became too large to perform accurate C-V measurements. Conversely, the typical double-step C–V curve was observed for the MISH capacitor treated by SPC treatment. The presence of the second step already indicated a reduced amount of interface states compared with the untreated case. Nevertheless, the ideal value of $C_{Al_2O_3}$ corresponding to the 16 nm thick Al_2O_3 was not reached by the second step during the up-sweep measurement because a significant amount of traps was probably still present at the Al_2O_3/GaN interface causing a stretch out of the C-V curve.

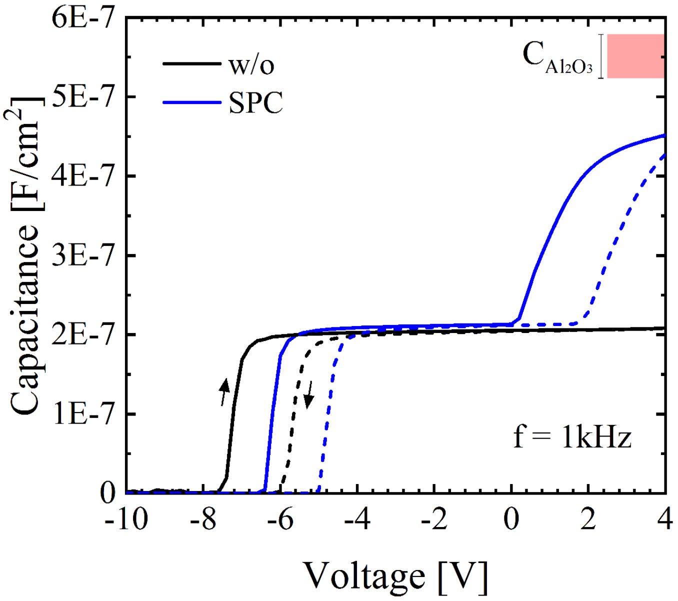
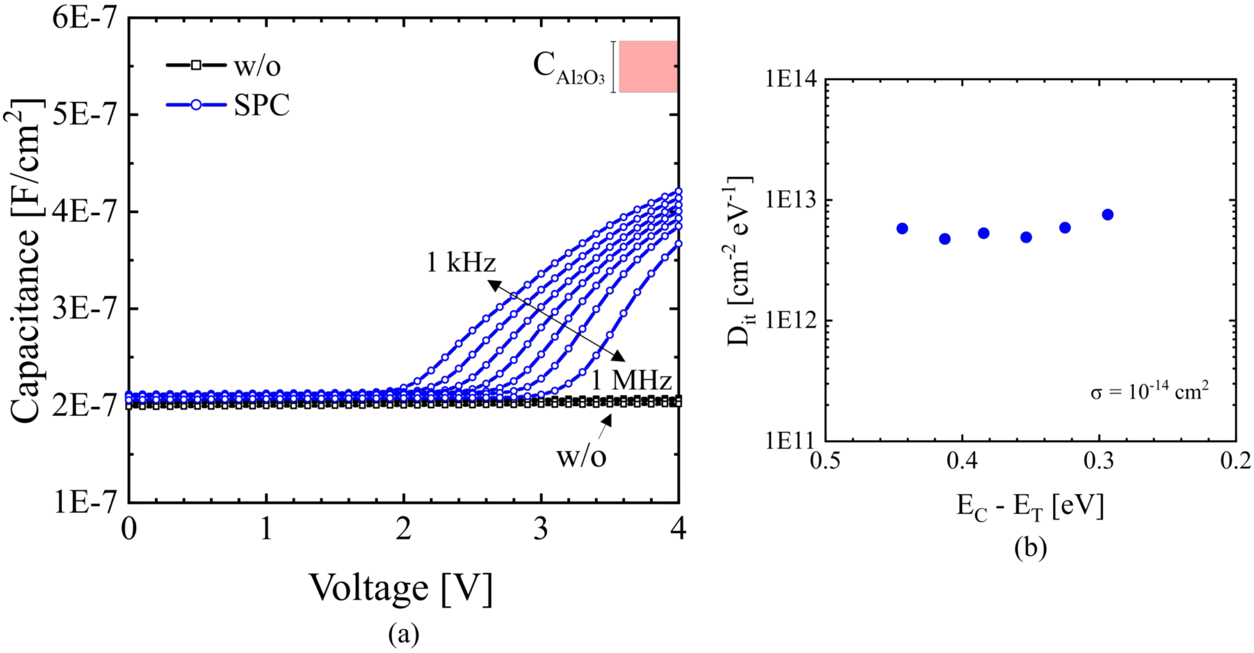


Figure 6.2: C–V characteristics of Al_2O_3/GaN/AlGaN/GaN capacitors having 16 nm thick Al_2O_3 without (Sample E.I) and with (Sample E.II) SPC treatment applied. The DC voltage sweep starts at -10 V. The AC signal frequency is 1 kHz with 30 mV amplitude. Down-sweep curves are indicated by dashed lines in both cases. The ideal range of values of $C_{Al_2O_3}$ calculated from 16 nm thick Al_2O_3 considering a deviation from the nominal value of 0.5 nm is also indicated, in accordance with the series capacitance model.

Looking at Figure 6.2, another important aspect is that during the down-sweep measurement a significant C-V hysteresis was obtained for both MISH capacitors without and with SPC treatment applied. In particular, for both samples the down-sweep measurement resulted in a positive rigid shift of the complete C-V curve compared to the up-sweep curve. The latter is due to electrons which are trapped in deep interface traps or border traps by applying positive voltages during the up-sweep measurement, for which electrons start to overcome the AlGaN barrier layer and accumulate at the Al_2O_3/GaN interface (spill-over region), and are not re-emitted during the following down-sweep measurement. Note that, border traps refer to bulk traps typically located near the dielectric/III-nitride interface for which the detrapping process is still strongly limited by the very long emission time. Although in the untreated case only a shift of V_{th} was visible, the latter is comparable to the one obtained in the MISH capacitor treated by SPC. Therefore, although the presence of the second step in the SPC treated case indicates a better Al_2O_3/GaN interface, the similar C-V hysteresis seems to indicate a comparable behavior in terms of deeper interface traps or border traps in both MISH capacitors without and with SPC applied. This result will be taken into account in Chapter 7 when discussing MIS-HEMTs with ALD-Al_2O_3 as gate dielectric subjected to positive gate bias stress, where both interface traps and border traps contribute to the resulting V_{th} instability of the device.

The detailed analysis of the interface trap states is performed using the frequency dispersion of the C-V characteristics in the spill-over region of the ALD-Al_2O_3/GaN/AlGaN/GaN structure of MISH capacitors (see Section 4.3.2). Figure 6.3a shows the C–V curves obtained for frequencies ranging from 1 kHz to 1 MHz for both samples without (Sample E.I) and with (Sample E.II) SPC treatment applied. The bias voltage is swept from positive to negative direction to initiate each measurement in a defined state of maximum electron trapping. Note that, resembling the hysteresis of the down-sweep curve of the C–V characteristics of Figure 6.2, this condition leads to an initial rigid shift toward positive direction of the overall C–V curve due to electrons trapped in deep energy states which are not re-emitted during the measurement time. Most importantly, Figure 6.3a shows that, although in the untreated case the second step is still not visible at all frequencies due to a probable large amount of interface trap states, a certain frequency dispersion is instead obtained for the sample treated by SPC. Figure 6.3b shows the D_{it}-E_T energy map extracted from the frequency dispersion of Figure 6.3a for the MISH capacitor fabricated with SPC which was determined accordingly to Equations 4.8 and 4.7, assuming a capture cross-section $\sigma = 10^{-14}$ cm^2. The employment of the SPC treatment gives a first improvement of the Al_2O_3/GaN interface in terms of interface states compared to the untreated case and results in an interface trap density D_{it} in the order of 7×10^{12} cm^{-2} eV^{-1} near the conduction band edge. In the next section, the Al_2O_3/GaN interface will be further improved by using the SPC treatment in combination with a postmetallization annealing process.



(a)

(b)

Figure 6.3: (a) Frequency dispersion in forward bias region of the C–V characteristics of Al_2O_3/GaN/AlGaN/GaN capacitors having 16 nm-thick Al_2O_3 without treatment applied (Sample E.I in black rectangles) and after SPC (Sample E.II in blue circles). The frequency ranges from 1 kHz to 1 MHz, e.g. [1, 3, 10, 30, 100, 300, 1000 kHz]. The ideal range of values of $C_{Al_2O_3}$ is indicated. In (b) the corresponding D_{it}-E_T mapping for the Al_2O_3/GaN/AlGaN/GaN capacitor after SPC treatment.

6.2 Postmetallization annealing

Postmetallization and postdeposition annealing treatments have been demonstrated to effectively improve GaN-based device performance by reducing interface states or deep-level traps both at the dielectric/III-nitride interface and within the dielectric.[10, 179, 180, 181, 182] In particular, while the specific mechanisms are yet unclear, postmetallization treatments in N_2 atmosphere have been shown particularly effective at reducing interface trap states and increasing the device performance.[179, 183, 184, 185, 186] In the following, the effects on the ALD-Al_2O_3/III-nitride interface of an N_2 annealing applied after gate metallization are investigated in MISH capacitors by frequency-dependent C-V method. The impact of the postmetallization annealing temperature on the Al_2O_3/III-nitride interface and on the gate leakage currents is also discussed.

6.2.1 Effects on ALD-Al_2O_3/III-nitride interface

Figure 6.4 shows the C–V characteristic obtained for the MISH capacitor fabricated by applying the SPC treatment prior to the ALD-Al_2O_3 dielectric deposition and an additional PMA process at 300 °C for 10 minutes in N_2 ambient after gate metallization (Sample E.III). For comparison, the C-V characteristics discussed in previous section, which were obtained for capacitors without treatment (Sample E.I) or only with SPC treatment (Sample E.II) applied, are also shown in the graph. The voltage was swept from -10 V to 4 V and then back to -10 V at the measurement frequency of 1 kHz.

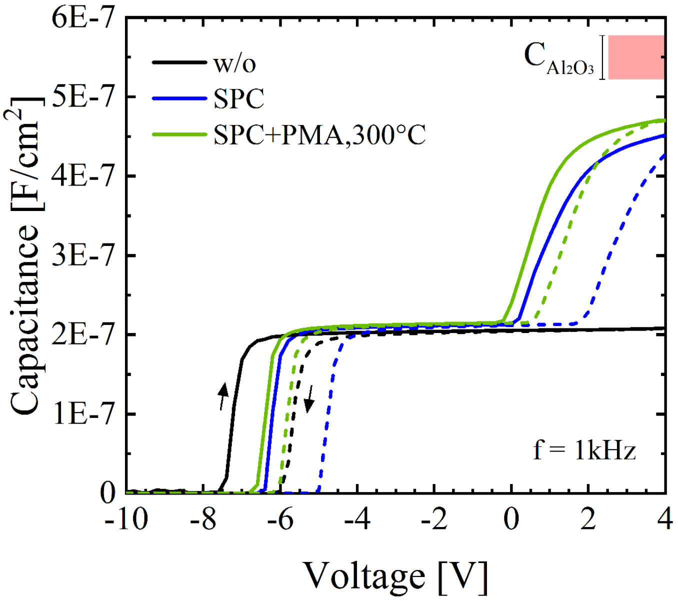
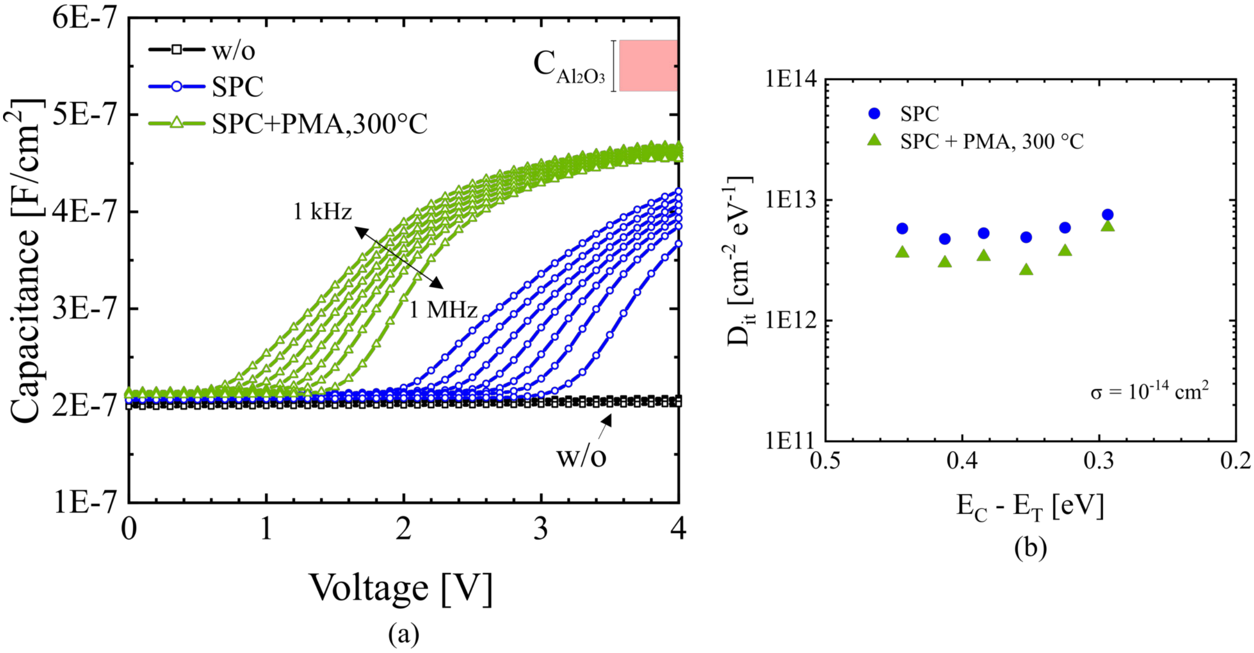


Figure 6.4: C–V characteristics of 16 nm Al_2O_3/GaN/AlGaN/GaN capacitors fabricated without (Sample E.I) and with (Sample E.II) SPC treatment and with SPC treatment combined with the PMA process at 300 °C for 10 minutes in N_2 ambient (Sample E.III). The DC voltage sweep starts at -10 V. The AC signal frequency is 1 kHz with 30 mV amplitude. Down-sweep curves are indicated by dashed lines in all cases. The ideal range of values of $C_{Al_2O_3}$ is also indicated, in accordance with the series capacitance model.

As one can see, same as in the case of the MISH capacitor subjected to the only SPC treatment, the typical double-step C–V curve was also observed for the sample which was treated by SPC combined with the PMA treatment. Note that, in the latter case, the value of the capacitance of the first flat part of the characteristic is still in accordance with the series capacitance model considering the thicknesses of the AlGaN, GaN-cap and Al_2O_3 layers of 22 nm, 2 nm and 16 nm, respectively. However, when the PMA is applied in combination with the SPC treatment, the change of the capacitance of the second step becomes steeper by reaching a larger capacitance value closer to the ideal value of $C_{Al_2O_3}$. A slight shift of $V_{\text{spill-over}}$ toward 0 V is also visible. These are qualitative indications of the effectiveness of SPC combined with PMA at further improving the interface quality with respect to the only SPC case, by reducing the amount of traps at the Al_2O_3/GaN interface. Furthermore, a smaller C-V hysteresis is also visible in the case of SPC combined with PMA. This suggests a significant influence of the PMA also on deeper interface traps or border traps with emission time longer than the period of the AC signal applied during the C-V measurement.



(a) (b)

Figure 6.5: (a) Frequency dispersion in forward bias region of the C–V characteristics of Al_2O_3/GaN/AlGaN/GaN capacitors without treatment applied (Sample E.I in black rectangles), after SPC (Sample E.II in blue circles) and SPC combined with PMA at 300 °C for 10 minutes in N_2 (Sample E.III in green triangles). The frequency ranges from 1 kHz to 1 MHz, e.g. [1, 3, 10, 30, 100, 300, 1000 kHz]. The ideal range of values of $C_{Al_2O_3}$ is indicated. In (b) the corresponding D_{it}-E_T maps extracted from the frequency dispersion only in the cases of capacitors treated with SPC and SPC combined with PMA.

The frequency dispersion of the C-V characteristics in the spill-over region of the investigated MISH capacitors are shown and compared in Figure 6.5a. The frequencies of the C-V curves range from 1 kHz to 1 MHz. Looking at these curves, a smaller frequency dispersion for the sample fabricated by combining the SPC and PMA treatments is clearly visible. The latter, together with the smaller $V_{\text{spill-over}}$ and the steeper C–V slope, reveal an effective reduction of trap states at the

Al_2O_3/GaN interface. The mapping of the interface trap densities extracted from the frequency dispersions of Figure 6.5a, according to Equations 4.8 and 4.7 and assuming a capture cross-section $\sigma = 10^{-14}$ cm^2, are reported in Figure 6.5b. The combination of the SPC and PMA treatments further improves the Al_2O_3/GaN interface compared to the capacitor where only SPC is used by further reducing the D_{it} to a value in the order of 5×10^{12} cm^{-2} eV^{-1} near the conduction band edge. In the next section, the impact of different annealing temperatures employed for the PMA treatment on the Al_2O_3/III-nitride interface and on the gate leakage currents is investigated.

6.2.2 Impact of annealing temperature

The postmetallization annealing treatment effectively reduces the interface trap states and border traps as revealed by the smaller frequency dispersion and hysteresis of the C-V characteristics obtained in the previous section. To obtain further insights into the topic, the influence of the postmetallization annealing on the electrical properties of MISH capacitors was also investigated by capacitance-voltage measurements for various annealing temperatures.

Figure 6.6 shows the C-V characteristics of MISH capacitors subjected to the SPC treatment in combination with the PMA treatment performed at the annealing temperatures of 300 °C, 350 °C and 400 °C for 10 minutes in N_2 atmosphere (Samples E.III). Note that, the C-V characteristic obtained for the sample treated by PMA at 300 °C was already discussed in the previous section and it is reported in the graph only for comparison.

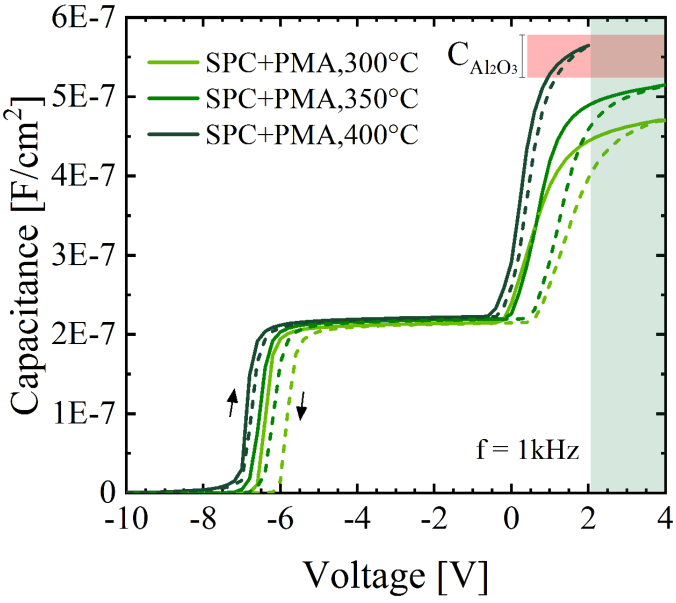


Figure 6.6: C–V characteristics of Al_2O_3/GaN/AlGaN/GaN capacitors where the SPC treatment is combined with the PMA treatment performed at the annealing temperatures of 300 °C, 350 °C and 400 °C for 10 minutes in N_2 ambient (Samples E.III). The DC voltage sweep starts at -10 V and the AC signal frequency is 1 kHz with 30 mV amplitude. Down-sweep curves are illustrated by dashed lines and the ideal range of values of $C_{Al_2O_3}$ is indicated. The green shadow area indicates the voltage measurement limit for the sample treated by PMA at 400 °C due to leakage currents preventing the C-V measurement beyond 2 V.

As one can see, compared to the sample treated by PMA at 300 °C, the MISH capacitor annealed at 350 °C reveals a steeper change of the capacitance in correspondence to the second step of the C-V curve, leading to a capacitance value of the second flat part even closer to the ideal value $C_{Al_2O_3}$. Furthermore, a smaller C-V hysteresis of the overall C-V curve is also obtained. As explained in previous section, the latter is related to slow border traps or deep-level interface states with an emission time constant longer than the period of the AC signal used for the C-V measurement. In fact, electrons trapped in these trap states cannot respond to the AC signal. Therefore, the increase of the annealing temperature to 350 °C results in a further reduction of the interface trap states as well as border traps compared to the sample treated by PMA at 300 °C.

By increasing the PMA temperature to 400 °C, the shape of the C-V characteristic is further affected, as can be seen from Figure 6.6. In particular, the C-V slope of the second step results to be very steep. Additionally, the capacitance of the second flat part saturates at a value which is in the range of the expected ideal $C_{Al_2O_3}$, calculated according to the Al_2O_3 layer thickness and also indicated in Figure 6.6. However, differently from the other MISH capacitors, for the sample annealed at 400 °C the measurement of the capacitance could not be performed beyond the voltage of 2 V due to large leakage currents resulting in a large increase of the dissipation factor and therefore limiting the measurement accuracy.[80]

In relation to this, Figure 6.7 shows the gate leakage currents of the MISH capacitors under investigation having 16 nm thick ALD-Al_2O_3 as gate dielectric and annealed at the PMA temperatures of 300 °C, 350 °C and 400 °C. As one can see, the gate leakage currents increase drastically with rising

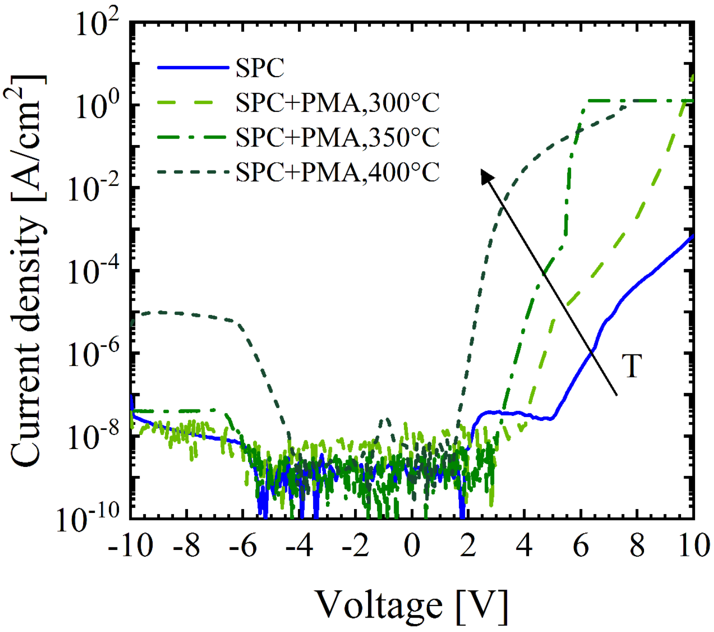


Figure 6.7: Impact of the PMA temperature on the leakage current density of MISH capacitors having 16 nm ALD-Al_2O_3 as gate dielectric subjected to PMA treatment at the annealing temperatures of 300 °C, 350 °C and 400 °C for 10 minutes in N_2 atmosphere (Samples E.III). Each measurement was performed on a fresh device from 0 V to -10 V and from 0 V to +10 V, respectively.

the annealing temperature above 350 °C. In particular, for the sample which received the PMA at 400 °C, a strong increase in the leakage currents for voltages higher than 2 V is clearly visible, supporting the previous argument related to the limitation occured during the C-V measurement. The increase of the leakage currents of ALD-grown Al_2O_3 films deposited on GaN has already been reported for MISH capacitors subjected to an N_2 postdeposition anneal at a relatively low thermal budget. In particular, this effect has been related to reactions of the underlaying GaN layer with the Al_2O_3 layer during annealing, which change the chemical bonding and stoichiometry of the insulator.[184, 187]

Another aspect of the C-V characteristic of the MISH capacitor annealed at 400 °C is that a smaller hysteresis is obtained compared to the other samples. However, due to the mentioned limitation of the C-V measurement at a voltage range up to 2 V caused by the leakage currents, this hysteresis is not comparable to the one obtained for the other samples, where a larger maximum voltage is applied as starting voltage for the down-sweep measurement. In fact, the hysteresis and the resulting shift of the C-V curve obtained during the down-sweep measurement are related to the maximum voltage applied.[70, 141, 188] Nevertheless, the C-V slope in correspondence of the second step of the C-V curve and the resulting saturation value of the capacitance are not affected by the maximum voltage applied during the up-sweep measurement. For this reason, the steeper C-V slope of the second step and the larger saturation value of the capacitance resulting from the up-sweep measurement of the sample annealed at 400 °C, still confirm an improvement of the Al_2O_3/GaN interface with the increase of the annealing temperature. However, since the key aspect of inserting a dielectric material into MIS-HEMTs is the reduction of the gate leakage currents, the larger gate leakage currents obtained with the increasing of the annealing temperature still remain an important aspect when employing the PMA treatment in MIS-HEMT devices.

The frequency dispersion in forward bias region of the C–V characteristics obtained for the MISH capacitors under investigation are shown in Figure 6.8. The frequency ranges from 1 kHz to 1 MHz and the bias voltage is swept from positive to negative direction to initiate each measurement in a defined state of maximum electron trapping. However, while for the samples treated by PMA at 300 °C and 350 °C a maximum voltage of 4 V was applied, for the sample annealed at 400 °C a maximum voltage of 2 V was used because of the measurement limitation given by the leakage currents. Note that, the frequency dispersion obtained for the sample treated by PMA at 300 °C was already discussed in the previous section and it is reported in the graph only for comparison. In the case of PMA at 350 °C, a reduction of the frequency dispersion is revealed with respect to the case of annealing at 300 °C. In particular, in the first case a voltage shift of about 250 mV is obtained between the C–V curves at frequencies of 1 kHz and 1 MHz in correspondence of the midpoint, compared to the one of about 500 mV for the sample treated at 300 °C. The situation even improves with the PMA temperature of 400 °C with a resulting voltage shift of about 90 mV.

Despite the use of a lower starting voltage in the case of PMA at 400 °C, the saturation of the capacitance of the second step in the C-V curve ensures the population of a second channel at

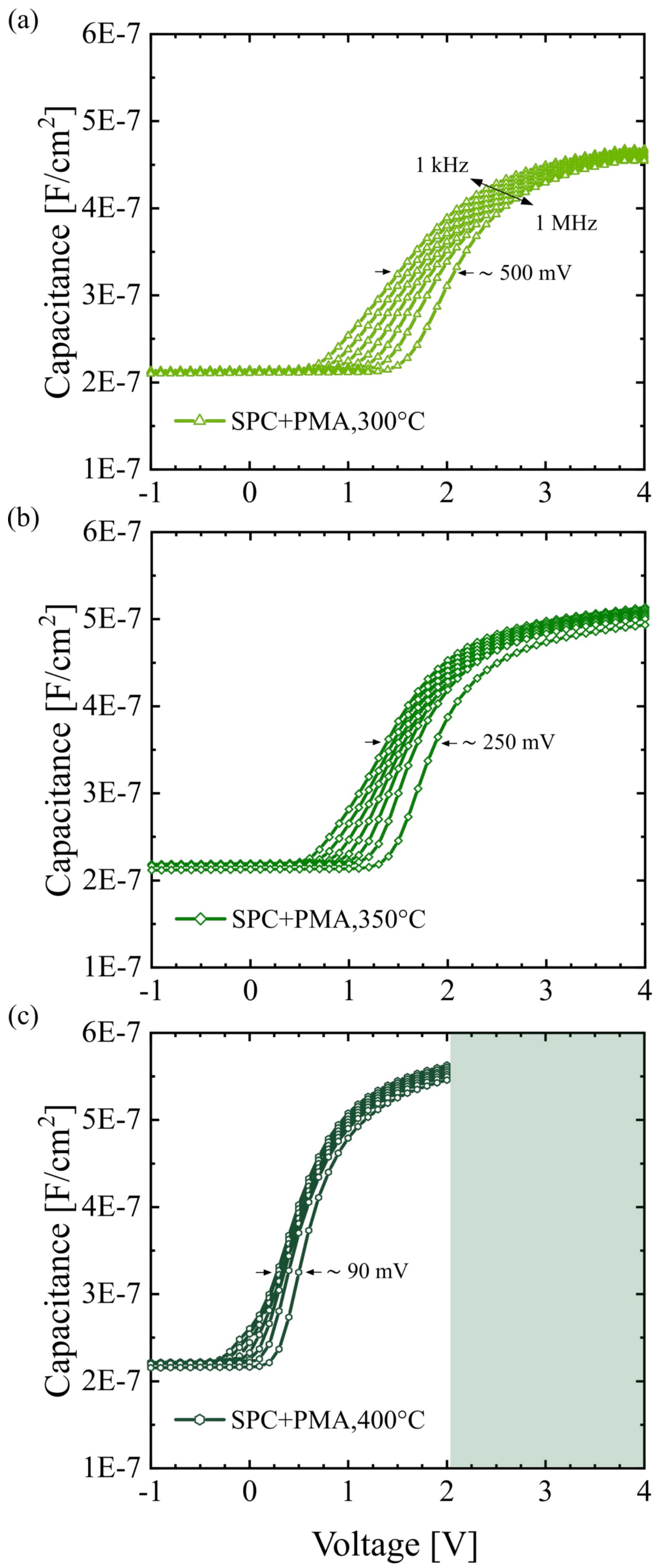


Figure 6.8: Frequency dispersion in forward bias region of the C–V characteristics of MISH capacitors with 16 nm ALD-Al_2O_3 treated by SPC combined with PMA (Samples E.III) at (a) 300 °C (b) 350 °C and (c) 400 °C for 10 minutes in N_2. The frequency ranges from 1 kHz to 1 MHz. The voltage shifts between C–V curves at the frequencies of 1 kHz and 1 MHz are indicated. The green shadow area in (c) indicates the voltage measurement limit for the sample treated by PMA at 400 °C due to large leakage currents beyond 2 V.

the Al_2O_3/GaN interface (spill-over region) and the filling condition of the interface trap states. The initial rigid shift towards positive direction of the overall C–V curve might depend on the maximum starting voltage used, as previously discussed, but here the frequency dispersion is assumed to be independent on the starting voltage as long as the capacitance shows a saturation. Based on this assumption, the D_{it}-E_T energy maps extracted from the frequency dispersions of Figure 6.8 for all MISH capacitors, according to the method explained in Section 4.3.2, are reported in Figure 6.9. A clear reduction of D_{it} is obtained with the increase of the annealing temperature. A D_{it} in the range of 2×10^{12} cm^{-2} eV^{-1} and 1×10^{12} cm^{-2} eV^{-1} near the conduction band edge is extracted for the annealing temperatures of 350 °C and 400 °C, respectively.

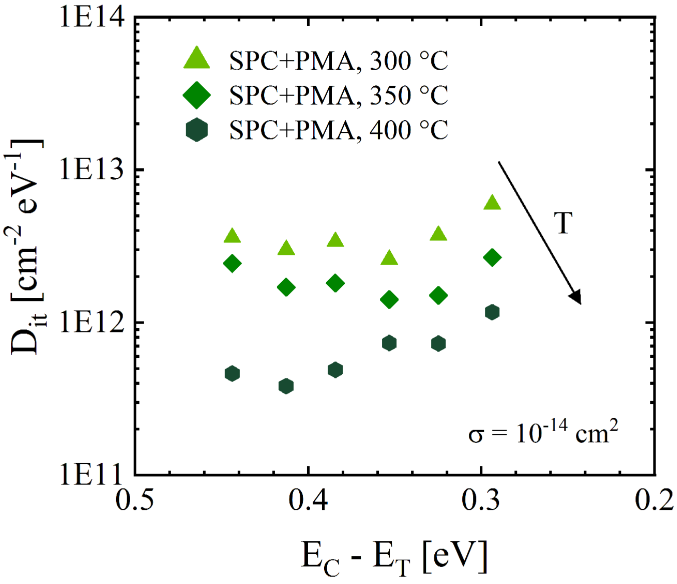


Figure 6.9: Interface trap density versus trap energy from the conduction band, extracted from the frequency dispersions of Figure 6.8 for MISH capacitors subjected to SPC combined with PMA at the annealing temperatures of 300 °C (b) 350 °C and (c) 400 °C for 10 minutes in N_2 ambient. A reduction of the D_{it} with the increase of the PMA temperature is clearly visible.

In conclusion, even though higher annealing temperatures seem beneficial in terms of Al_2O_3/GaN interface quality, the annealing temperature employed for the PMA treatment is limited by the increase of the gate leakage current. For this reason, the PMA at the annealing temperature of 350 °C will be used in Chapter 7 for the optimization of the MIS-gate module of MIS-HEMT devices, as a trade-off between the quality of the Al_2O_3/GaN interface and the gate leakage current in the considered voltage range of operation.

6.3 Influence of ohmic contacts annealing

The processing steps for the fabrication of ohmic contacts can affect the dielectric/III-nitride interface of the MIS-gate structure of GaN-based MIS-HEMTs. During the anneal at high temperature applied for conventional ohmic contacts, the (Al)GaN surface has been demonstrated to be chemically deteriorated prior to the gate dielectric deposition (ohmic-first approach), which can cause serious reliability issues in AlGaN/GaN MIS-HEMTs.[61, 172] In Section 6.1.1, a degraded GaN surface with a rough morphology was also observed after the lift-off and the high temperature anneal at 850 °C applied for the formation of Ti/Al-based ohmic contacts. From this perspective, the use of a low annealing temperature for the ohmic contact formation could be also beneficial to optimize the performance of MIS-gate modules in MIS-HEMT devices. In the following, the dielectric/III-nitride interface of MISH capacitors using the developed low-temperature annealed Ta/Al-based ohmic contacts is compared to the one of capacitors using conventional Ti/Al-based contacts annealed at high temperature.

Figure 6.10 shows the C-V characteristics of the MISH capacitors fabricated using Ta/Al/TaN (Sample F.I) and Ti/Al/Ni/Au (Sample F.II) ohmic contacts, which were formed by thermal annealing at 550 °C for 3 minutes and at 850 °C for 30 seconds, respectively, followed by the deposition of 16 nm of ALD-Al_2O_3 as gate insulator. Note that, both samples were treated by SPC to ensure a better Al_2O_3/GaN interface quality, as discussed in previous sections. The voltage was swept from -10 V to 4 V and then back to -10 V at the measurement frequency of 1 kHz.

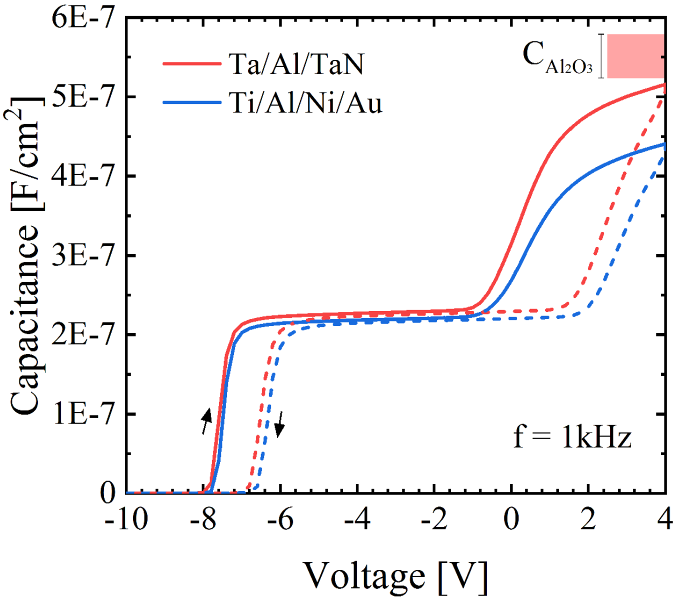


Figure 6.10: C–V characteristics of Al_2O_3/GaN/AlGaN/GaN capacitors having 16 nm-thick Al_2O_3 fabricated with Ta/Al/TaN (Sample F.I) and Ti/Al/Ni/Au (Sample F.II) ohmic contacts annealed at 550 °C for 3 minutes and at 850 °C for 30 seconds, respectively. The SPC treatment was applied for both samples prior to the Al_2O_3 gate dielectric deposition. The DC voltage sweep starts at -10 V and the AC signal frequency is 1 kHz with 30 mV amplitude. Down-sweep curves are indicated by dashed lines in both cases. The ideal range of values of $C_{Al_2O_3}$ is also indicated, in accordance with the series capacitance model.

The capacitance of the first flat part of both characteristics is in accordance with the series capacitance model considering the thicknesses of the AlGaN, GaN-cap and Al_2O_3 layers of 25 nm, 2 nm and 16 nm, respectively. Most importantly, the typical double-step shape of the C-V curve is clearly visible for both samples, in line with the results obtained in the previous sections for MISH test structures treated by SPC. However, the MISH capacitor with Ta/Al/TaN ohmic contacts revealed a steeper change of the capacitance at the second step by reaching a larger capacitance value closer to the ideal value of $C_{Al_2O_3}$. Therefore, the lower annealing temperature used for Ta/Al-based ohmic contacts seems to provide a better Al_2O_3/GaN interface. On the other hand, no significant difference was visible in terms of C-V hysteresis. Since the C-V hysteresis is largely dependent on border traps inside the dielectric, it is reasonable that those traps are not affected when using an ohmic-first fabrication approach where the ohmic contacts annealing is performed prior to the dielectric deposition.

The C–V characteristics in forward bias region of the MISH capacitors under investigation at frequencies from 1 kHz to 1 MHz are shown in Figure 6.11a and 6.11b. The corresponding D_{it}-E_T

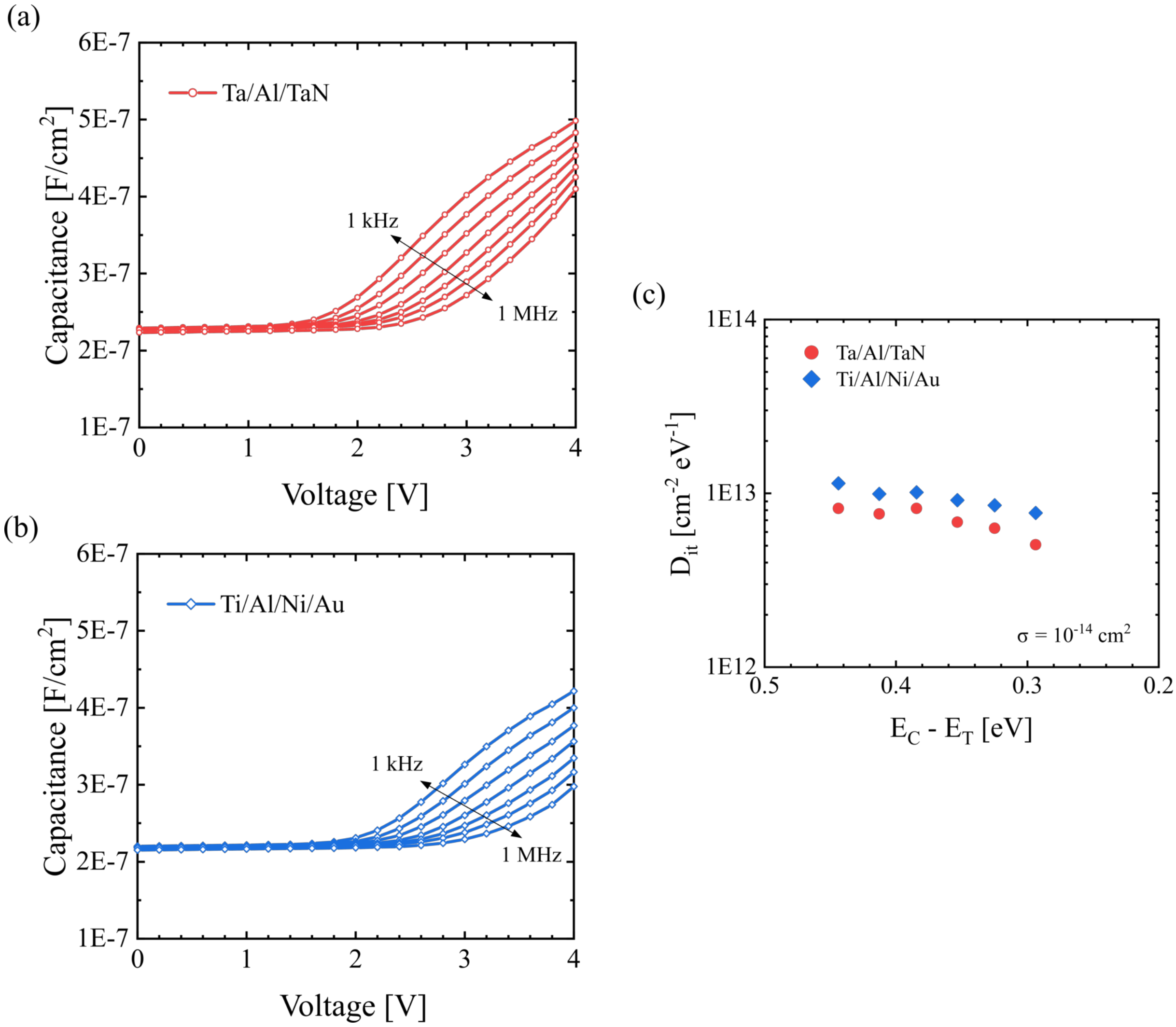


Figure 6.11: Frequency dispersion in forward bias region of the C–V characteristics of Al_2O_3/GaN/AlGaN/GaN capacitors using (a) Ta/Al/TaN (Sample F.I) and (b) Ti/Al/Ni/Au (Sample F.II) ohmic contacts annealed at 550 °C for 3 minutes and 850 °C for 30 seconds, respectively. In (c) the corresponding D_{it}-E_T maps extracted from the frequency dispersion for both samples.

energy maps extracted from the obtained frequency dispersions (see Section 4.3.2) are shown in Figure 6.11c. A reduction of D_{it} is obtained for the MISH capacitor with Ta/Al/TaN ohmic contacts annealed at the lower temperature of 550 °C compared to the capacitor with Ti/Al/Ni/Au contacts annealed at 850 °C, with a larger discrepancy in D_{it} closer to the conduction band edge.

Therefore, using lower annealing temperatures for the formation of ohmic contacts improves the quality of the ALD-Al_2O_3/GaN interface in terms of interface trap density, making the low-temperature Ta/Al-based ohmic contacts also beneficial for optimizing the MIS-gate module of AlGaN/GaN MIS-HEMTs.

6.4 Summary

In summary, a high-quality interface in terms of interface trap states between ALD-Al_2O_3 and GaN-capped AlGaN/GaN heterostructures has been achieved by the combination of an O_2 plasma-based surface preconditioning and an N_2 postmetallization anneal. Particularly, the O_2 plasma-based treatment has been shown to be effective at removing contaminants and restoring the morphology of the GaN surface which was observed to be affected by the fabrication processes before the Al_2O_3 deposition. Moreover, MISH capacitors treated by SPC combined to PMA showed a reduced frequency dispersion and a smaller hysteresis in the C-V characteristics than capacitors without treatment or with only SPC applied, demonstrating a reduction of interface states as well as deep-level traps both at the ALD-Al_2O_3/GaN interface and within the dielectric. Furthermore, a clear reduction of the interface trap density with the increase of the PMA temperature was obtained, with a value of D_{it} of about 1×10^{12} cm^{-2} eV^{-1} near the conduction band edge achieved for the annealing temperature of 400 °C. However, the PMA at temperatures above 350 °C was also found to be detrimental in terms of leakage currents through the ALD-Al_2O_3 gate dielectric. Therefore, the increase of gate leakage currents with the PMA temperature must be also taken into account when optimizing the performance of the MIS-gate module in MIS-HEMT devices. Based on these insights, in the following chapter the effectiveness of both SPC and PMA on the ALD-Al_2O_3/GaN interface is investigated by monitoring the threshold voltage stability of Al_2O_3-AlGaN/GaN MIS-HEMT devices subjected to these treatments by positive gate stress pulsed sweep measurements.

Lastly, the annealing temperature for the ohmic contacts formation has been shown to influence the ALD-Al_2O_3/GaN interface when using an ohmic-first fabrication approach where the ohmic contacts are processed before the gate dielectric deposition. Particularly, the low annealing temperature used for Ta/Al-based contacts has been shown to be beneficial in terms of D_{it} at the ALD-Al_2O_3/GaN interface compared to the high annealing temperature applied for conventional Au-containing Ti/Al-based ohmic contacts, representing a step forward towards the optimization of the MIS-gate module in MIS-HEMT devices.

7 Performance of AlGaN/GaN MIS-HEMTs

In the first part of this chapter, AlGaN/GaN MIS-HEMTs fabricated on a 150 mm GaN-on-Si substrate using low-temperature and Au-free Ta/Al-based ohmic contacts are presented. In particular, the device characteristics of MIS-HEMTs integrating Ta/Al-based ohmic contacts are first compared to the ones of devices using conventional Au-containing Ti/Al-based contacts. Afterwards, novel reliability aspects related to the employment of these two different contact schemes in devices operating at high temperature are discussed. In the second part, based on the previous experimental results, the influence of the SPC and PMA treatments on the threshold voltage stability of AlGaN/GaN MIS-HEMTs using ALD-Al_2O_3 as gate dielectric is investigated by pulsed measurements under positive gate bias stress condition.

7.1 Au-free Ta/Al-based ohmic contacts in MIS-HEMTs

The use of a Au-free ohmic contacts technology to AlGaN/GaN on large GaN-on-Si substrates is suitable for the cost-effective large-scale production of AlGaN/GaN devices in the standard Si technology production lines. In Chapter 5, the Au-free manufacturing process of Ta/Al-based ohmic contacts was shown to give comparable results to conventional Ti/Al-based contacts and to be suitable for large area substrates. For this reason, in the following AlGaN/GaN MIS-HEMTs integrated on a 150 mm GaN-on-Si substrate using the developed Au-free Ta/Al-based ohmic contacts are presented, demonstrating that the Au-free Ta/Al-based ohmic contact technology represents a very promising Si CMOS-compatible alternative to conventional Au-containing Ti/Al-based contacts for AlGaN/GaN devices. The device characteristics of AlGaN/GaN MIS-HEMTs with Au-free Ta/Al-based ohmic contacts are compared to MIS-HEMTs fabricated using Au-containing Ti/Al-based ohmic contacts. Finally, the different temperature behavior of the contact resistance obtained using the two metallization schemes and discussed in Section 5.2.4, is shown to introduce novel aspects regarding the performance degradation of AlGaN/GaN devices operating at high temperature.

The detailed processing steps conditions of the fabricated MIS-HEMTs which are compared throughout this section are summarized in Table 7.1.

Table 7.1: MIS-HEMTs processing conditions applied to the fabricated samples of this section. Refer to Table 4.1 for specifications on the epitaxial materials indicated in the column "Epi" and to Section 4.2 for more details on the fabrication process.

	Epi	S/D ohmic contacts	SPC	Gate dielectric	Gate electrode
Ta/Al- MIS-HEMTs	III	Ta/Al/TaN, 10/240/20 nm, 550 °C, 3 min, N_2	x	ALD-Al_2O_3 16 nm	Ti/Au 100/150 nm
Ti/Al- MIS-HEMTs	III	Ti/Al/Ni/Au, 35/200/40/100 nm, 850 °C, 30 sec, N_2	x	ALD-Al_2O_3 16 nm	Ti/Au 100/150 nm

7.1.1 DC characteristics

The DC transfer (I_{DS}-V_{GS} and I_{GS}-V_{GS}) and transconductance (g_m-V_{GS}) characteristics of the AlGaN/GaN MIS-HEMT with Au-free Ta/Al/TaN ohmic contacts are shown in Figure 7.1. The device has a gate-to-source distance L_{GS} = 3 µm, a gate length L_G = 3 µm and a gate-to-drain distance L_{GD} = 14 µm. The gate voltage was swept from -10 V to 0 V and then back to -10 V.

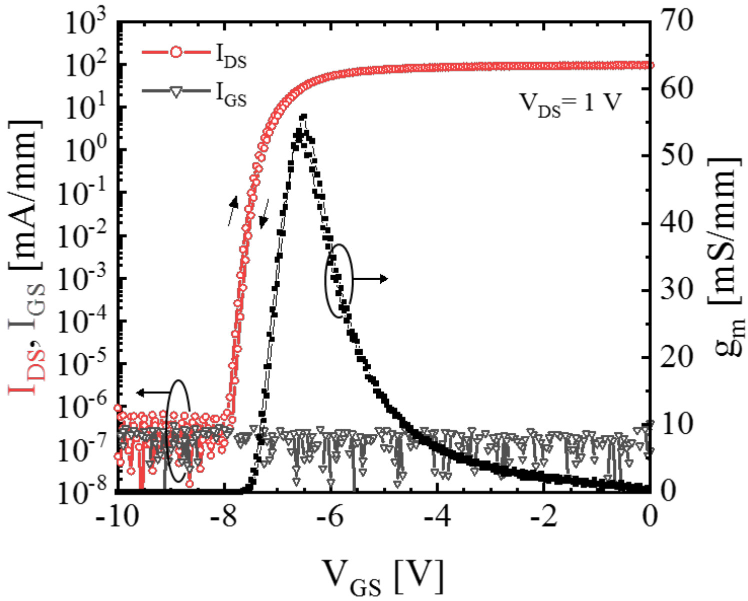


Figure 7.1: DC transfer (logarithmic scale) and transconductance characteristics of AlGaN/GaN MIS-HEMT with 16 nm-thick ALD-Al_2O_3 as gate insulator and Ta/Al/TaN ohmic contacts, for V_{DS} = 1 V. The V_{GS} is swept from -10 V to 0 V and then back to -10 V. The device has L_{GS} = 3 µm, L_G = 3 µm and L_{GD} = 14 µm. The threshold voltage V_{th} is -6.5 V, subthreshold swing SS is 75 mV/dec and the peak g_m is 56 mS/mm.

The threshold voltage is about -6.5 V using the peak g_m extrapolation method. The subthreshold swing SS and the peak of the transconductance g_m (V_{DS} = 1 V) are 75 mV/dec and 56 mS/mm, respectively. The MIS-gate module with 16 nm of ALD-Al_2O_3 efficiently suppresses the gate leakage current to a value in the range of 10^{-7} mA/mm, implicating the large on/off current ratio of about 5×10^{10}. Almost no hysteresis was observed between the up- and the down-sweep transfer curves, indicating negligible trapping at the Al_2O_3/GaN interface or within the dielectric in the negative voltage region. No considerable difference was revealed between the DC characteristics of MIS-HEMTs using the Ta/Al/TaN ohmic contacts in Figure 7.1 and the ones obtained using Ti/Al/Ni/Au contacts (not shown here). The DC transfer and transconductance characteristics of the MIS-HEMT are fundamentally related to the gate-to-channel coupling ascribed to the MIS-gate module. Variations of the interface trap density at the dielectric/III-nitride interface of the MIS-gate structure has only a minor influence on the DC performance of MIS-HEMTs in the negative voltage region.[143] Particularly, in this region interface traps act as fixed charge shifting the V_{th} of the device. The V_{th} shift caused exclusively by interface traps is difficult to detect. For this reason, even though in Section 6.3 a different interface trap density was observed in MISH capacitors with Ta/Al/TaN and Ti/Al/Ni/Au contacts, the DC characteristics of the corresponding MIS-HEMTs are not affected and their similarity is due to the comparable MIS-gate structures (see Table 7.1).

The output characteristics of the MIS-HEMTs fabricated with Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts measured up to V_{DS} = 10 V are compared in Figure 7.2. The gate voltage V_{GS} was varied from 0 V to -10 V in steps of 2 V. Note that, in order to avoid detrimental degradation of the static on-state resistance and of the saturation current in the corresponding output characteristic caused by V_{th} instabilities, positive values of V_{GS} were not applied in the present measurement.[71]

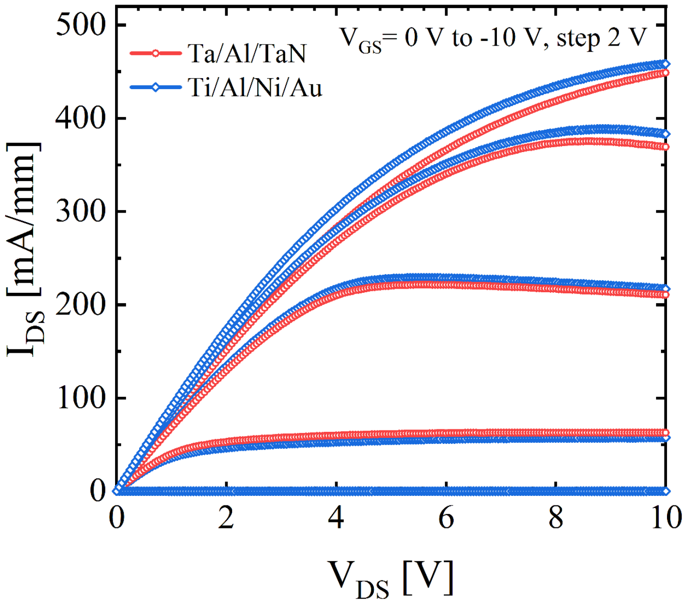


Figure 7.2: DC output characteristics of AlGaN/GaN MIS-HEMTs fabricated with 16 nm-thick ALD-Al_2O_3 as gate insulator and Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts. Design parameters of measured devices are L_{GS} = 3 µm, L_G = 3 µm and L_{GD} = 14 µm.

The maximum saturation drain-to-source current ($I_{DS,max}$) of about 445 mA/mm and 460 mA/mm at V_{GS} = 0 V was achieved for the MIS-HEMTs with Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts, respectively. In both cases, the drain current starts to decrease slightly with the increase of the drain voltage due to self-heating effects. The different values obtained for $I_{DS,max}$ are related to the different on-state drain-to-source resistance $R_{DS,on}$. The static $R_{DS,on}$ can be extracted from the inverse slope of the linear region of the output characteristic and it is directly related to the source/drain contact resistance and to the sheet resistance of the 2DEG, as discussed in Section 2.3. The $R_{DS,on}$ values of 12.2 Ω mm and 10.9 Ω mm were extracted at V_{GS} = 0 V for the MIS-HEMTs using Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts, respectively. As a consistency check, the extracted $R_{DS,on}$ value can be compared to the value of $R_{DS,on}$ calculated using Equation 2.9. The input values for the calculation are the design parameter of the total source-to-drain distance L_{SD} = L_{GS} + L_G + L_{GD} = 20 µm, the source/drain contact resistance $R_c{}^{S/D}$ and the sheet resistance R_{sh} of the 2DEG. The $R_c{}^{S/D}$ and R_{sh} were obtained in Section 5.2 from TLM structures of the Ta/Al/TaN and Ti/Al/Ni/Au contacts fabricated on the same substrate as the MIS-HEMTs under investigation. Note that, in the present MIS-HEMT design, the Al_2O_3 layer acts also as passivation layer between the gate and S/D ohmic contacts. Therefore, the input value of R_{sh} takes into account its strong recovery after the Al_2O_3 deposition, as discussed in Section 5.2.3. Moreover, the R_{sh} value is assumed to be the same beneath the gate electrode and between the gate and S/D contacts when V_{GS} = 0 V. Table 7.2 shows the overall comparison for the respective devices.

Table 7.2: Comparison of the calculated and measured on-state drain-to-source resistance $R_{DS,on}$ of MIS-HEMTs with Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts. The input parameters of $R_c{}^{S/D}$ and R_{sh} for the calculation were obtained in Section 5.2 taking into account the Al_2O_3 passivation layer.

L_{SD} = 20 µm V_{GS} = 0 V	$R_c{}^{S/D}$ [Ω mm]	R_{sh} [Ω sq^{-1}]	$R_{DS,on}$ (calc.) [Ω mm]	$R_{DS,on}$ (meas.) [Ω mm]
Ta/Al- MIS-HEMTs	1.2	465	11.7	12.2
Ti/Al- MIS-HEMTs	0.7	460	10.6	10.9

As one can see, the results obtained for the calculated $R_{DS,on}$ are in accordance with the measured values. Due to similar values of R_{sh}, the lower value of $R_{DS,on}$ obtained for the MIS-HEMT with Ti/Al/Ni/Au contacts is caused by the slightly lower contact resistance with respect to the MIS-HEMT with Ta/Al/TaN contacts. This difference could be further reduced by precisely controlling the thickness of the metal stack used for the Ta/Al-based ohmic contacts, as discussed in Section 5.1. Therefore, Ta/Al-based ohmic contacts annealed at low temperature represent a valid solution as Au-free ohmic contact technology to AlGaN/GaN on large GaN-on-Si substrates, showing comparable DC performance to devices fabricated using conventional Ti/Al-based ohmic contacts.

7.1.2 Influence of ohmic contacts at high-temperature operation

The different temperature behavior of the contact resistance of Ta/Al-based and Ti/Al-based contacts demonstrated in Section 5.2, poses novel aspects in terms of reliability when employing these ohmic contact schemes in MIS-HEMT devices that are operating at high temperatures. Particularly, it was observed that while for Ta/Al/TaN contacts R_c slightly increases with temperature, for Ti/Al/Ni/Au contacts R_c increases with a dependence T^{α} with $\alpha = 1.5$ similarly to a "metallic-like" behavior. The latter behavior was attributed to a different ohmic contact mechanism better described by a direct 2DEG-metal contact in case of Au-containing Ti/Al-based contacts rather than a 2DEG-semiconductor-metal contact governed by tunneling in the case of Ta/Al-based ohmic contacts. The different temperature behavior of R_c can have a different impact on the DC performance in terms of $R_{DS,on}$ of AlGaN/GaN devices operating at high temperature.

The effect of the temperature behavior of R_c on the $R_{DS,on}$ was evaluated by monitoring the change of the $R_{DS,on}$ of AlGaN/GaN MIS-HEMTs at elevated temperature. Figure 7.3 shows the output characteristics at $V_{GS} = 0$ V of MIS-HEMTs fabricated with Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts at operation temperatures ranging between 25 °C and 200 °C.

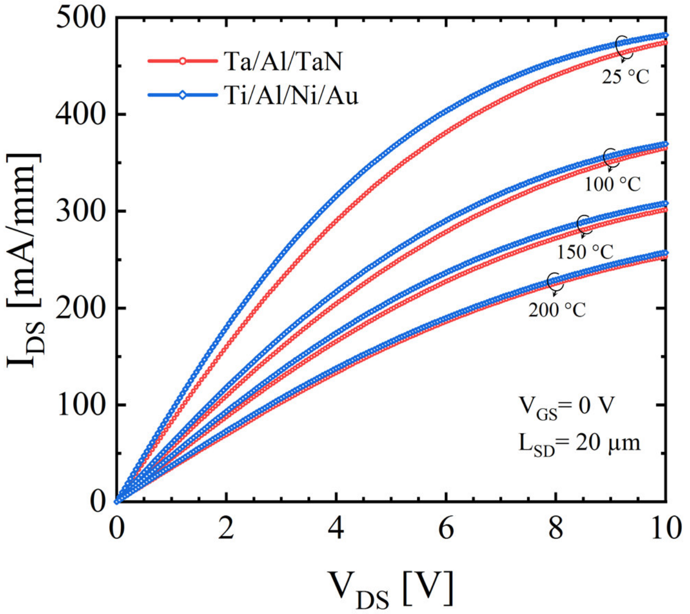


Figure 7.3: Output characteristics at $V_{GS} = 0$ V of MIS-HEMTs using Ta/Al/TaN and Ti/Al/Ni/Au ohmic contacts measured at 25 °C, 100 °C, 150 °C and 200 °C. A larger degradation of $R_{DS,on}$ for higher temperatures is obtained using Ti/Al/Ni/Au contacts due to the stronger increase of R_c with increasing temperature. Design parameters of measured devices are $L_{GS} = 3$ µm, $L_G = 3$ µm and $L_{GD} = 14$ µm.

As one can see, a larger degradation of the $R_{DS,on}$ is obtained with increasing temperature in the case of the MIS-HEMT fabricated with Ti/Al/Ni/Au contacts. In fact, the output characteristic of this device tends to merge together with the one obtained using Ta/Al/TaN contacts by increasing the operation temperature. To better visualize this effect, Figure 7.4 shows the relative degradation of $R_{DS,on}$ with respect to the value of $R_{DS,on}$ measured at 25 °C for both devices. In both cases, a large increase of the $R_{DS,on}$ is clearly visible. The latter is largely attributed to the sheet resistance increase with temperature as R_{sh} is the major contribution to the $R_{DS,on}$ for devices with a long source-to-drain distance. For example, looking at Table 7.2 of the previous section, for L_{SD} = 20 µm the contribution of R_{sh} is about 85 % of the overall $R_{DS,on}$. However, a larger degradation with increasing temperature is clearly visible in the case of Ti/Al/Ni/Au contacts. As shown in Section 5.2, the R_{sh} degradation is independent from the type of contact scheme and it is related to the increase of phonon scattering in the heterostructure. Therefore, given the same behavior of R_{sh} with temperature for both types of device, the different behavior of the $R_{DS,on}$ degradation must be attributed to the different behavior of the R_c with increasing temperature (see Figure 5.18).

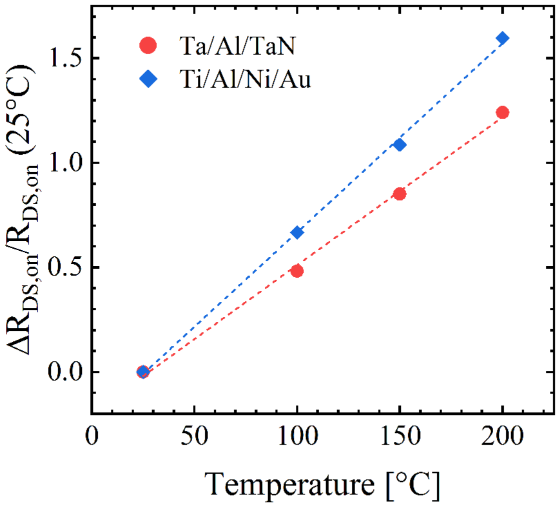


Figure 7.4: Relative $R_{DS,on}$ degradation with respect to the $R_{DS,on}$ value at 25 °C of MIS-HEMTs using Ta/Al/TaN and Ti/Al/Ni/Au contacts extracted from Figure 7.3. The temperature dependence of R_c (see Figure 5.18) of Ti/Al/Ni/Au ohmic contacts results in a more pronounced $R_{DS,on}$ degradation.

The effect of the $R_{DS,on}$ degradation ascribed to the different temperature behavior of the contact resistance is only minor in the investigated case due to the long source-to-drain distance L_{SD} = 20 µm, which is typical for MIS-HEMTs used for power applications. However, this effect can be of critical importance for shorter distance devices as for example in the case of devices used for RF applications and operating at high temperature. Therefore, another interesting aspect is that even though the direct 2DEG-metal contact is typically beneficial in terms of reproducibility in achieving ohmic behavior, this type of contact mechanism can have detrimental effects for short devices when operating at high temperature. On the other hand, for Ta/Al-based ohmic contacts with a metal-semiconductor-2DEG connection this degradation is minimized, since R_c is almost independent on the operation temperature.

7.2 MIS-HEMTs with optimized ALD-Al_2O_3/III-nitride interface

The insertion of a dielectric layer in MIS-HEMTs is especially attractive to power switching applications due to the suppressed gate leakage and large gate voltage swing. However, the MIS-gate structure incorporates trap states at the dielectric/III-nitride interface and inside the dielectric which introduce new reliability problems. Particularly, MIS-HEMTs suffer from serious threshold voltage drifts induced by forward gate bias stress which are mainly attributed to electron trapping at the dielectric/III-N interface. This is considered one of the major concern in terms of device reliability as it can affect the circuit stability during switching operation.[71, 72, 73, 74, 189]

In the previous chapter, surface preconditioning and postmetallization annealing treatments have been observed to reduce interface states or deep-level traps at the dielectric/III-nitride interface and within the dielectric of MISH capacitors. In this section, the influence of these treatments on the V_{th} stability of AlGaN/GaN MIS-HEMTs is investigated by pulsed I-V measurements under positive gate stress condition. Although a reduction of the interface trap density after various surface treatments and postdeposition annealing has been already reported,[10, 65, 140, 142, 178, 179, 190, 191] still few reports dealt with the effects of surface and postdeposition treatments in terms of interface trap density and their related implications on the V_{th} stability of the device.

The investigation of the V_{th} instability under positive gate stress condition was performed by pulsed I_{DS}-V_{GS} measurements (see Section 4.3.3) on AlGaN/GaN MIS-HEMTs fabricated on the same samples as the MISH capacitive test structures presented in the previous chapter (Samples of

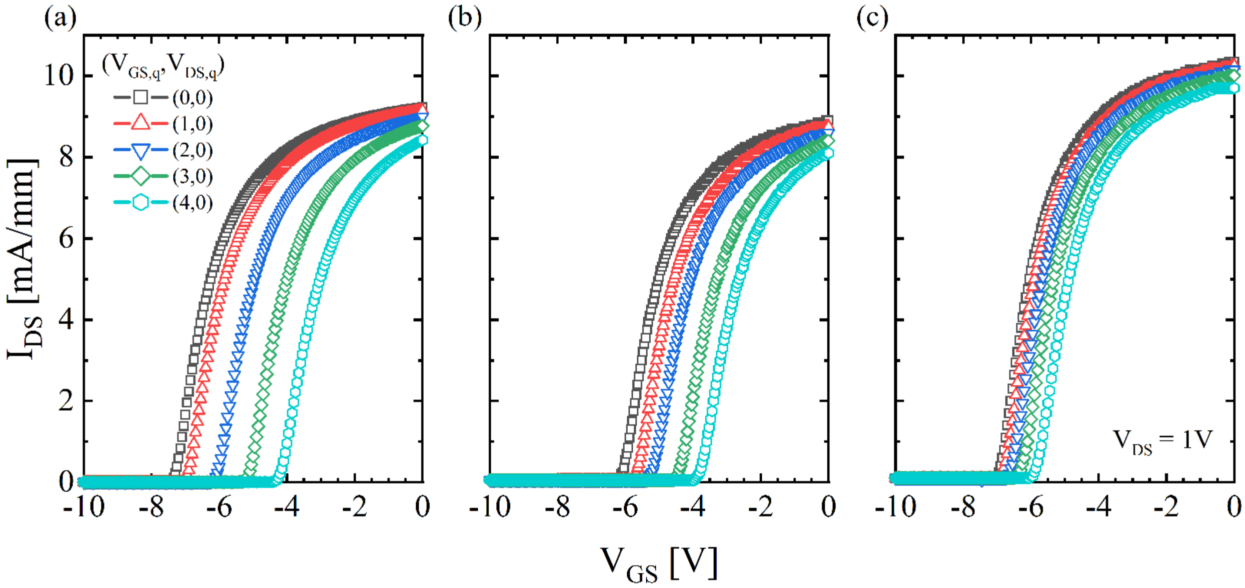


Figure 7.5: Pulsed I_{DS}-V_{GS} characteristics of GaN-capped AlGaN/GaN MIS-HEMTs with 16 nm ALD-Al_2O_3 as gate dielectric performed for different gate stress voltages $V_{GS,q}$ in the range of 0-4 V a) without treatment applied, b) after SPC and c) after SPC combined with PMA at 350 °C for 10 minutes in N_2 ambient. The $V_{GS,m}$ is swept from -10 V to 0 V. The devices have L_{GS} = 3 µm, L_G = 3 µm and L_{GD} = 14 µm.

group E of Table 6.1). Specifically, the devices under test consist of AlGaN/GaN MIS-HEMTs with 16 nm ALD-Al_2O_3 as gate dielectric which were fabricated, in line with previous investigations, without and with SPC, and with SPC combined with PMA applied at the optimal annealing temperature of 350 °C for 10 minutes in N_2 atmosphere. The measurements were carried out by sweeping $V_{GS,m}$ from -10 V to 0 V at $V_{DS,m}$ = 1 V for the gate stress voltages $V_{GS,q}$ from 0 V to 4 V and $V_{DS,q}$ = 0 V (to avoid any contribution from trapping mechanisms in the epitaxial layers). The pulse period and pulse width were 50 ms and 1 ms, respectively, with 1 ms being the time limit of the measurement system. Figure 7.5 shows the obtained pulsed transfer characteristics of the ALD-Al_2O_3/GaN/AlGaN/GaN MIS-HEMTs fabricated without and with SPC and PMA. In Figure 7.5a, the characteristics of the MIS-HEMT without treatment applied show a remarkable positive V_{th} shift triggered by gate stress voltages $V_{GS,q} > 0$ V. On the other hand, while the V_{th} shift is slightly improved for the MIS-HEMT treated only by SPC, the combination of the SPC and PMA treatments greatly reduces the V_{th} shift after stress.

To better visualize the effectiveness of these treatments, Figure 7.6 shows the threshold voltage shift ΔV_{th} extrapolated from Figure 7.5 as a function of the gate bias stress applied $V_{GS,q}$. Although the V_{th} drifts in the positive direction for larger positive gate bias stress in all samples, a larger V_{th} shift of about 3.5 V for $V_{GS,q}$ = 4 V is obtained for the MIS-HEMT without treatment applied. The amplitude of the V_{th} shift is instead significantly reduced to approximately 1 V in the case of the MIS-HEMT treated by SPC combined to the PMA treatment. Note that, the large values of V_{th} shifts obtained are caused by the harsh stress conditions applied to the devices under investigation ($V_{GS,q}$ up to 4 V with pulse width of 50 ms). As first rough estimation, a V_{th} shift of about 1 V would already cause a degradation of the maximum drain-to-source current of about 10-15 %.

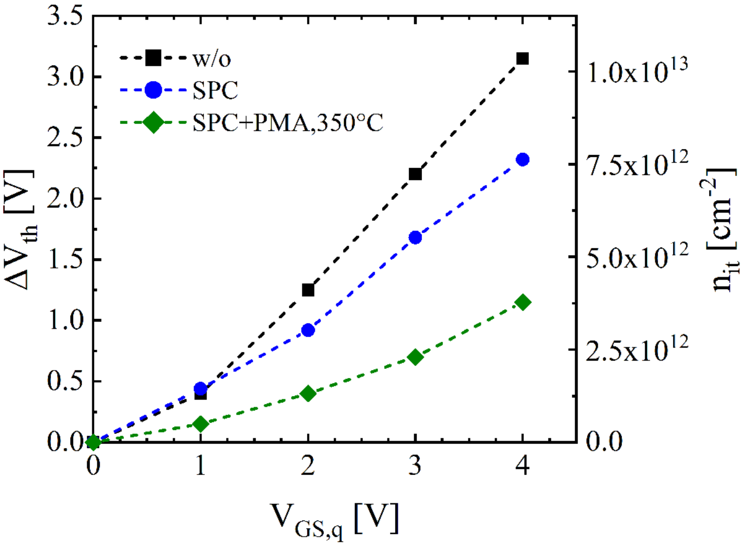


Figure 7.6: V_{th} shift extrapolated from the pulsed I_{DS}-V_{GS} characteristics of AlGaN/GaN MIS-HEMTs without treatment applied, after SPC and after SPC combined with PMA at 350 °C for 10 minutes in N_2 shown in Figure 7.5. The corresponding effective interface charge density n_{it} calculated using Equation 4.5 is also illustrated. The dashed lines are only guides to the eye.

It is important to note that the contribution of the interface traps to the V_{th} shift obtained using pulsed I_{DS}-V_{GS} sweep measurements only reflects the occupancy of traps with an emission time longer than the measurement pulse width. Interface traps with emission time constants shorter than the pulse width are able to emit electrons before the sampling and cannot be detected using this method. The upper energy range limit which is detectable can be deduced from Equation 4.6 by considering the measurement pulse width of 1 ms and it is calculated to be E_C-E_T = 0.5 eV. Therefore, the obtained pulsed I_{DS}-V_{GS} measurements are sensitive to deeper interface states in energy compared with the frequency-dependent C–V method applied in the previous chapter. In addition, as already explained in Section 4.3.3, the charge trapping promoting the V_{th} shift during forward bias stress is most likely correlated not only to interface states but also to border traps distributed within the dielectric.[192] Despite the separate contributions of border and interface traps cannot be disentangled, an effective interface charge density n_{it} accounting for D_{it} and border traps can be determined by Equation 4.11.

The extracted n_{it} as a function of the gate stress voltage is shown in Figure 7.6. According to the V_{th} shift, the interface states located in the described energy range limits and border traps are reduced for the samples fabricated by SPC or by combining the SPC and PMA treatments. Specifically, the resulting n_{it} is less reduced in the case where only the SPC was applied with respect to the case treated by SPC and PMA. This result is in line with the observation in Section 6.1 where a comparable hysteresis in the C-V characteristics of MISH capacitors without treatment and with only SPC applied was observed, as the C-V hysteresis is also related to deep interface traps or border traps which are not emitted during sampling. Therefore, the reduced V_{th} shift in the SPC case is mostly related to the reduction of interface traps rather than border traps. On the other hand, the larger reduction of V_{th} shift in the case of the MIS-HEMT subjected to SPC and PMA is both due to the reduction of interface states as well as deep-level traps both at the ALD-Al_2O_3/GaN interface and within the dielectric, in accordance with the results obtained in Section 6.2. Although interface traps and border traps cannot be distinguished with the pulse I-V method in the latter case, the reduction of the D_{it} distribution revealed by frequency-dependent C–V method is also contributing to the smaller relative change with increasing gate bias stress in the pulsed I_{DS}–V_{GS} measurement. Therefore, the effectiveness of the SPC and PMA treatments to reduce interface states at the Al_2O_3/III-nitride interface is also demonstrated to contribute to the improvement of the electrical properties of the GaN-based MIS-HEMTs under forward gate bias stress.

7.3 Summary

In summary, low-temperature and Au-free Ta/Al-based ohmic contacts fabricated by sputtering on AlGaN/GaN heterostructures have been integrated in MIS-HEMTs on a 150 mm GaN-on-Si substrate. Comparable DC performance between AlGaN/GaN MIS-HEMTs using Ta/Al-based ohmic contacts annealed at low temperature and devices with conventional Ti/Al-based contacts annealed at high temperature have been demonstrated. Additionally, since Ta/Al-based ohmic contacts showed a weaker increase of the contact resistance with temperature compared to high-temperature annealed Au-containing Ti/Al-based ohmic contacts, the contact scheme of the Ta/Al-based ohmic contacts resulted superior for (MIS-)HEMTs operating at high temperature as it reduces the $R_{DS,on}$ degradation caused by the increase in contact resistance. Therefore, the Au-free ohmic contacts technology to AlGaN/GaN on large GaN-on-Si substrates based on the Ta/Al-based contact scheme represents a potential solution for the cooperative manufacturing of GaN-based devices in standard Si fabs.

The high-quality dielectric/III-nitride interface obtained by surface preconditioning and post-metallization annealing treatments was demonstrated to also improve the electrical properties of AlGaN/GaN MIS-HEMTs with ALD-Al_2O_3 as gate insulator by pulsed I_{DS}–V_{GS} measurements under positive gate bias stress condition. Particularly, since the SPC acts mostly on the interface traps at the ALD-Al_2O_3/GaN interface, a smaller improvement in terms of V_{th} stability was obtained with respect to the combination of SPC and PMA. In the latter case, the reduction of interface states as well as deep-level traps both at the ALD-Al_2O_3/GaN interface and within the dielectric greatly improves the V_{th} stability of MIS-HEMTs, representing a promising solution to enhance the robustness of the MIS-gate structure under forward gate bias stress as required for power switching applications.

8 Conclusions

AlGaN/GaN high electron mobility transistors are promising candidates for next generation high-frequency and high-power applications due to the excellent physical properties of wide bandgap GaN-based materials. Additionally, the high charge carrier density and high mobility two-dimensional electron gas confined at the AlGaN/GaN heterostructure interface enables the achievement of low on-state resistance minimizing power losses and self-heating of the device. However, many challenges still need to be faced in order to enable the massive introduction of AlGaN/GaN devices into the electronic market. Among them, the development of a Au-free ohmic contacts technology is still demanded for the large-scale and cost-effective manufacturing of GaN-based devices into standard silicon fabs and existing production lines. Moreover, trap states at the dielectric/III-nitride interface and inside the dielectric of the MIS-gate structure of AlGaN/GaN MIS-HEMTs represent a bottleneck in terms of gate reliability. Therefore, this work focused on the fabrication, characterization and optimization of the AlGaN/GaN MIS-HEMT mainly targeting high-power applications. A low-resistive and Au-free ohmic contacts technology to AlGaN/GaN was developed using Ta/Al-based contacts annealed at low temperature. Regarding the MIS-gate structure, processing treatments were investigated to deliver a robust MIS-gate module with low interface and bulk trap states improving the device reliability under forward bias device operation.

In the first part of this thesis (Chapters 2 and 3), the basic characteristics of heterostructure field-effect transistors were introduced and the operation principles of AlGaN/GaN HEMTs with a Schottky-gate were presented. Moreover, the properties of the epitaxial materials and of the device modules of gate and ohmic contacts which are critical to obtain high performance devices for high-power applications were highlighted. Particularly, the employment of an insulator to implement a MIS-gate structure in MIS-HEMTs compared to Schottky-gate HEMTs was discussed and the fundamentals and requirements of ohmic contacts to AlGaN/GaN heterostructures were reviewed and described.

In Chapter 4, the experimental methods applied in this work were presented. First, the technological processes and fabrication steps involved in the fabrication of the various test structures were illustrated. Afterwards, the different techniques applied for the electrical characterization of the samples and the resulting electrical parameters were explained and discussed in terms of their applicability and limitations.

In Chapter 5, low-temperature and Au-free ohmic contacts to AlGaN/GaN heterostructures using sputtered Ta/Al-based metal stacks were experimentally investigated. Low-resistive Ta/Al-based ohmic contacts with R_c values lower than 1 Ω mm at annealing temperatures below 600 °C could be achieved without AlGaN barrier recess. The Ta/Al-based metal stack was optimized in terms of thermal stability and metal stack conductivity. In fact, for annealing temperatures higher than 550 °C the stability of the entire metal stack degraded when using a Ta cap layer due to strong

Ta–Al alloying. This issue was circumvented by utilizing the compound materials of TiN and TaN as cap layer. TaN was considered as alternative compound material to TiN as it still prevents a strong intermixing with the underlying metals but it also improves the overall contact resistance due to a lower resistivity compared to TiN. TaN was also tested to be thermally stable up to 700 °C. Also, the ohmic behavior and the contact properties of contact resistance and optimum annealing temperature of Ta/Al-based contacts were found to depend on the thickness of the Ta bottom layer and on the Ta/Al thickness ratio. Even though clear dependencies between these contact features could not be fully identified, general trends were extracted and an optimal Ta/Al thickness ratio of about 1:25 was found. Regarding the contact mechanism of Ta/Al-based ohmic contacts, due to TEM investigations showing an undistorted and well-defined AlGaN barrier layer as well as the decrease of the specific contact resistivity with increasing temperature, the nature of current transport pointed towards a current path from the metal through the AlGaN barrier to the 2DEG channel by thermionic field emission. Also, in line with several reports indicating the out-diffusion of nitrogen from the AlGaN barrier to the metal contact initiated by the contact annealing as potential n-type doping source of the AlGaN barrier, presence of nitrogen in the metal stack after annealing was revealed by EELS analysis. N vacancies acting as n-type donors in AlGaN pull down the conduction band towards the Fermi level and enhance the electron tunneling through the AlGaN barrier. In line with the former interpretation, the contact formation was found to be sensitive to the presence of a thin AlN spacer layer at the AlGaN/GaN interface. The large band discontinuity between AlN and GaN represents a high energy barrier in the vicinity of the 2DEG channel which, following the interpretation of charge carrier transport through the AlGaN barrier dominated by tunneling, impedes the carrier conduction from the metal through the AlGaN barrier to the 2DEG. Based on this interpretation of contact formation, even lower values of the contact resistance might be realized by the utilization of a recess etch of the AlGaN barrier within the contact fabrication process.

Furthermore, the developed low-temperature and Au-free Ta/Al-based ohmic contacts were demonstrated on 150 mm GaN-on-Si substrates and compared to high-temperature annealed Au-containing Ti/Al-based ohmic contacts. The manufacturing process of Au-free Ta/Al-based ohmic contacts based on sputtering was shown to give comparable results in terms of homogeneity and contact resistance to conventional Ti/Al-based contacts, being therefore suitable for production on large area substrates as required for the integration of GaN-based devices in Si platforms. Moreover, Ta/Al-based contacts showed very smooth surface morphology and excellent edge acuity, which also facilitates the down scaling of the device. Also, the low temperature employed for the annealing of Ta/Al-based contacts revealed to reduce the impact on the sheet resistance of the heterostructure without passivation compared to Ti/Al-based contacts annealed at high temperature. Finally, the temperature dependence of the contact resistance obtained for Ta/Al-based and Ti/Al-based contacts was compared. While a weaker increase of the contact resistance was observed for low-temperature annealed Au-free Ta/Al-based contacts, an increase of the contact resistance similarly to a "metallic-like" behavior was revealed by Ti/Al-based contacts. This difference was attributed to the different mechanism of current transport for the two metallization schemes, the 2DEG-semiconductor-metal connection governed by tunneling for Ta/Al-based ohmic contacts rather than a direct metal-2DEG contact type in the case of high-temperature annealed Au-containing Ti/Al-based contacts.

In Chapter 6, the MIS-gate structure of GaN-capped AlGaN/GaN heterostructure capacitors using ALD-Al_2O_3 as gate insulator was investigated and optimized in terms of trap states at the dielectric/III-nitride interface and inside the dielectric. First, the O_2 plasma-based SPC treatment was shown to effectively restore the morphology of the GaN surface which was affected by the fabrication processes before the ALD-Al_2O_3 deposition. Afterwards, the combination of the O_2 plasma-based surface preconditioning and an N_2 postmetallization anneal was revealed to reduce the interface states and border traps by resulting in smaller hysteresis and frequency dispersion of the C-V characteristics. Moreover, despite the improvement of the Al_2O_3/GaN interface quality for higher annealing temperature employed for the PMA treatment, the annealing temperature used resulted to be limited by the increase of the gate leakage currents. As a conclusion, a trade-off must be considered when using the PMA treatment between the quality of the Al_2O_3/GaN interface and the gate leakage currents in a certain voltage range of operation. The optimal annealing temperature of 350 °C applied for 10 minutes in N_2 was established. Finally, the impact of the annealing temperature used for the formation of ohmic contacts on the ALD-Al_2O_3/GaN interface was briefly introduced and investigated. The latter represents a new aspect to be considered when using an ohmic first fabrication approach, where ohmic contacts are processed before the gate dielectric deposition. Even though a more systematic study is required, first frequency-dependent capacitance voltage measurements demonstrated that the low annealing temperature employed for Ta/Al-based contacts is beneficial in terms of trap states at the ALD-Al_2O_3/GaN interface.

In Chapter 7, AlGaN/GaN MIS-HEMTs using the developed low-temperature and Au-free Ta/Al-based ohmic contacts fabricated by sputtering were demonstrated on a 150 mm GaN-on-Si substrate. The MIS-HEMT showed comparable DC performance to devices using Ti/Al-based ohmic contacts annealed at high temperature. Moreover, Ta/Al-based contacts showed to improve the robustness in terms of $R_{DS,on}$ of devices operating at high temperature, due to the weaker increase of the contact resistance with temperature with respect to Au-containing Ti/Al-based contacts annealed at high temperature. Overall, the developed Au-free Ta/Al-based ohmic contacts technology represents a very promising alternative to conventional Au-containing Ti/Al-based contacts for AlGaN/GaN (MIS)-HEMT devices for high-frequency, high-power and high-temperature applications and it is suitable for the cooperative manufacturing of GaN-based devices in standard Si fabs.

Moreover, the SPC and PMA treatments were demonstrated to effectively improve the V_{th} stability of AlGaN/GaN MIS-HEMTs using ALD-Al_2O_3 as gate insulator by pulsed I-V measurements under positive gate bias stress. In particular, the combination of the SPC and PMA treatments resulted to be the most effective solution due to the reduction of both interface states as well as deep-level traps both at the ALD-Al_2O_3/GaN interface and within the dielectric. From this perspective, this work contributed to the development of a more robust MIS-gate module which is especially demanded in forward bias operation, one of the most critical concern in terms of gate reliability in power switching applications.

In conclusion, this work contributed to the advance of the current technology of Au-free ohmic contacts to AlGaN/GaN heterostructures grown on large area Si substrates, which is a key step for the integration of GaN-based devices into Si device fabs. However, while the state of the art is already very promising, there is still no full understanding of the mechanism of contact formation and current transport. Moreover, additional research should be also devoted to ohmic contacts fabricated with AlGaN barrier recess which can further lower the contact resistance and may require even lower annealing temperature for the contact formation. Lastly, progress in gate dielectric technology of AlGaN/GaN MIS-HEMTs using ALD-Al_2O_3 as gate insulator were made in terms of dielectric/III-nitride interface and dielectric properties affecting the threshold voltage stability of the device under forward bias stress condition. However, the current state of the art still requires remarkable progress in terms of interface control technology, gate dielectric and gate stack engineering and focused efforts are still needed in order to ensure low interface and bulk trap density and robust reliability under stringent and dynamic electrical stresses. Further advance in the ohmic contact and gate dielectric technologies are necessary to overcome these obstacles and to pave the way for the massive advent of the GaN-based technology in the electronic market.

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List of symbols

Symbol	Description	Units
A	contact area	m^2
A^*	effective Richardson constant	$\mathrm{A\,m^{-2}\,K^{-2}}$
A^{**}	modified Richardson constant	$\mathrm{A\,m^{-2}\,K^{-2}}$
A_{eff}	effective contact area	m^2
α	coefficient of temperature dependence of contact resistance	1
c	equation parameter for in FE model	eV^{-1}
C	capacitance per unit area	$\mathrm{F\,m^{-2}}$
C_{AlGaN}	AlGaN capacitance per unit area	$\mathrm{F\,m^{-2}}$
$C_{Al_2O_3}$	Al_2O_3 capacitance per unit area	$\mathrm{F\,m^{-2}}$
$C_{dielectric}$	dielectric capacitance per unit area	$\mathrm{F\,m^{-2}}$
C_G	gate-to-channel capacitance per unit area	$\mathrm{F\,m^{-2}}$
$C_{GaN-cap}$	GaN-cap capacitance per unit area	$\mathrm{F\,m^{-2}}$
$C_{GaN,depl}$	depleted GaN buffer layer capacitance per unit area	$\mathrm{F\,m^{-2}}$
C_{ins}	insulator capacitance per unit area	$\mathrm{F\,m^{-2}}$
d	layer thickness	m
d_{AlGaN}	AlGaN barrier thickness	m
d_C	contact spacing	m
$d_{GaN-cap}$	GaN-cap thickness	m
d_{ins}	insulator thickness	m
D_{it}	interface trap density	$\mathrm{m^{-2}\,eV^{-1}}$
ΔE_C	conduction band offset	eV
ΔE_V	valence band offset	eV
$\Delta R_{DS,on}$	difference in on-state drain-to-source resistance	Ω m
$\Delta V_{f_1,f_2}$	voltage shift in 2nd step of C-V characteristics	V
$\Delta V'_{f_1,f_2}$	equation parameter for interface trap density calculation	V
ΔV_{th}	threshold voltage shift	V
E	energy	eV
E_0	equation parameter for in TFE model	eV
E_{00}	characteristics energy	eV
E_C	conduction band minimum	eV
E_F	Fermi level	eV
E_{Fm}	metal Fermi level	eV
E_{Fs}	semiconductor Fermi level	eV
E_G	energy bandgap	eV
$E_{T,f}$	trap energy probed at frequency f	eV
E_T	trap energy	eV
E_V	valence band maximum	eV
ε	relative permittivity	1
ε_0	vacuum permittivity	$\mathrm{F\,m^{-1}}$

Symbol	**Description**	**Units**
ε_{AlGaN}	relative AlGaN permittivity	1
$\varepsilon_{GaN-cap}$	relative GaN-cap permittivity	1
ε_{ins}	relative insulator permittivity	1
f	frequency	Hz
g_m	transconductance	$\mathrm{S\,m^{-1}}$
h	Planck's constant	J s
$\hbar$	reduced Planck's constant	J s
I	electrical current	A
I_{DS}	drain-to-source current	A
$I_{DS,max}$	maximum saturation drain-to-source current	A
$I_{DS,sat}$	saturation drain-to-source current	A
I_{GS}	gate-to-source current	A
J	current density	$\mathrm{A\,m^{-2}}$
J_{DS}	drain-to-source current density	$\mathrm{A\,m^{-2}}$
k_B	Boltzmann constant	$\mathrm{eV\,K^{-1}}$
L	contact length	m
L_G	gate length	m
L_{GD}	gate-to-drain distance	m
L_{GS}	gate-to-source distance	m
L_{SD}	source-to-drain distance	m
L_T	transfer length	m
m^*	effective electron mass	g
μ	2DEG mobility	$\mathrm{m^{-2}\,V^{-1}\,s^{-1}}$
n_{it}	effective interface charge density	$\mathrm{m^{-2}}$
n_s	sheet carrier density	$\mathrm{m^{-2}}$
N_c	effective density of states in the conduction band	$\mathrm{m^{-3}}$
N_D	semiconductor doping	$\mathrm{m^{-3}}$
ω_{LO}	LO-phonon frequency	$\mathrm{rad\,s^{-1}}$
P	total polarization	$\mathrm{C\,m^{-2}}$
P_{PE}	piezoelectric polarization	$\mathrm{C\,m^{-2}}$
P_{SP}	spontaneous polarization	$\mathrm{C\,m^{-2}}$
q	elementary charge	C
R_c	contact resistance	Ω m
$R_c^{S/D}$	source/drain contact resistance	Ω m
$R_{DS,on}$	on-state drain-to-source resistance	Ω m
R_m	metal pad resistance	Ω m
R_{sh}	sheet resistance	$\Omega\,\mathrm{sq^{-1}}$
R_T	total resistance	Ω
ρ_c	specific contact resistivity	$\Omega\,\mathrm{m^2}$
SS	subthreshold swing	$\mathrm{V\,decade^{1}}$
σ	capture cross-section of a trap	$\mathrm{m^2}$

Symbol	Description	Units
σ_P	polarization sheet charge density	C m^{-2}
t_{Al}	thickness of Al layer	m
t_{Ta}	thickness of Ta layer	m
T	absolute temperature	K
T_0	phonon temperature	K
τ	period AC signal	s
τ_e	trap emission time constant	s
u_F	Fermi level position with respect conduction band	eV
v	thermal velocity	m s^{-1}
V	voltage	V
V_{DS}	drain-to-source voltage	V
$V_{DS,m}$	non-quiescent point drain-to-source voltage	V
$V_{DS,q}$	quiescent point drain-to-source voltage	V
$V_{DS,sat}$	saturation drain-to-source voltage	V
V_G	gate voltage	V
V_{GS}	gate-to-source voltage	V
$V_{GS,m}$	non-quiescent point gate-to-source voltage	V
$V_{GS,q}$	quiescent point gate-to-source voltage	V
$V_{spill-over}$	spill-over voltage	V
V_{th}	threshold voltage	V
Φ_b	Schottky barrier height	eV
W	contact width	m
W_G	gate width	m
x	Aluminium content	1

List of abbreviations

Abbreviation	Description
2DEG	two-dimensional electron gas
AC	alternating current
AFM	atomic force microscopy
ALD	atomic layer deposition
CMOS	complementary metal-oxide-semiconductor
D	drain electrode
DC	direct current
EDX	energy dispersive X-ray spectroscopy
EELS	electron energy loss spectroscopy
Epi	epitaxial heterostructure
FE	field emission
G	gate electrode
HEMT	high electron mobility transistor
HFET	heterostructure field-effect transistor
ICP	inductively coupled plasma
LO	longitudinal-optical
LPCVD	low-pressure chemical vapor deposition
MIS	metal-insulator-semiconductor
MISH	metal-insulator-semiconductor heterostructure
MIS-HEMT	metal-insulator-semiconductor high electron mobility transistor
MOCVD	metal organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field-effect-transistor
PDA	postdeposition annealing
PMA	postmetallization annealing
PVD	physical vapor deposition
RF	radio frequency
RIE	reactive ion etching
RT	room temperature
RTA	rapid thermal annealing
S	source electrode
SEM	scanning electron microscopy
SPC	surface preconditioning
STEM	scanning transmission electron microscopy
TE	thermionic emission
TEM	transmission electron microscopy
TFE	thermionic field emission
TLM	transfer length method
TMA	trimethylaluminium

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2017/11 - 2018/04	Research Assistant at NaMLab gGmbH, Dresden, Germany Si power MOSFET gate stack reliability and modeling
2016/03 - 2016/11 (M.Sc. Thesis)	Research Scientist at imec, Leuven, Belgium Boron-doped diamond films for diamond probe fabrication
2013 - 2014 (250 hours project)	Internship at Microla Optoelectronics srl, Chivasso, Italy Investigation of biosensor based on photonic crystals

List of publications

A. Journal articles

1. **A. Calzolaro**, R. Hentschel, I. F. Edokam, V. Sizov, T. Mikolajick and A. Wachowiak. Material investigations for improving stability of Au free Ta/Al-based ohmic contacts annealed at low temperature for AlGaN/GaN heterostructures. *Semicond. Sci. Technol.*, 35: 075011, 2020.
2. **A. Calzolaro**, N. Szabó, A. Großer, J. Gärtner, T. Mikolajick and A. Wachowiak. Surface Preconditioning and Postmetallization Anneal Improving Interface Properties and V_{th} Stability under Positive Gate Bias Stress in AlGaN/GaN MIS-HEMTs. *Physica Status Solidi A*, 218: 2000585, 2021.

B. Conference articles

1. **A. Calzolaro**, T. Mikolajick and A. Wachowiak. Integration and Reliability Aspects of Low-Temperature and Au-free Ta/Al-based Ohmic Contacts for AlGaN/GaN MIS-HEMTs. *European Solid-State Device Research Conference (ESSDERC)*, Grenoble, France, September 2021.

B. Conference contributions

1. **A. Calzolaro**, T. Mikolajick and A. Wachowiak. (Talk) Integration and Reliability Aspects of Low-Temperature and Au-free Ta/Al-based Ohmic Contacts for AlGaN/GaN MIS-HEMTs. *European Solid-State Device Research Conference (ESSDERC)*, Grenoble, France, September 2021.
2. **A. Calzolaro**, R. Hentschel, N. Szabó, A. Großer, J. Gärtner, A. Wachowiak and T. Mikolajick. (Poster) Influence of surface pre-conditioning and post-deposition annealing on V_{th} instability under positive gate bias operation in AlGaN/GaN MIS-HEMTs. *Semiconductor Interface Specialists Conference (SISC)*, San Diego, CA, USA, December 2019.
3. **A. Calzolaro**, R. Hentschel, N. Szabó, A. Großer, A. Wachowiak and T. Mikolajick. (Invited Talk) ALD Al_2O_3 dielectric for AlGaN/GaN MIS-HEMT gate module. *Novel High-k Application Workshop*, Dresden, Germany, June 2019.
4. **A. Calzolaro**, R. Hentschel, A. Wachowiak and T. Mikolajick. (Talk) Performance degradation of AlGaN/GaN MIS-HEMTs under different operational stress-conditions. *DPG Spring Meeting*, Regensburg, Germany, April 2019.

Declaration of Authorship

I, the undersigned .... hereby declare that I am the sole author of this thesis. To the best of my knowledge this thesis contains no material previously published by any other person except where due acknowledgement has been made. This thesis contains no material which has been accepted as part of the requirements of any other academic degree or non-degree program, in English or in any other language.

Place, Date:

Name (printed letters):

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