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Erstveröffentlichung in / First published in:

Ultramicroscopy. 2018, 193, S. 24-32 [Zugriff am: 11.10.2022]. Elsevier. ISSN 1879-2723.

DOI: <https://doi.org/10.1016/j.ultramic.2018.05.011>

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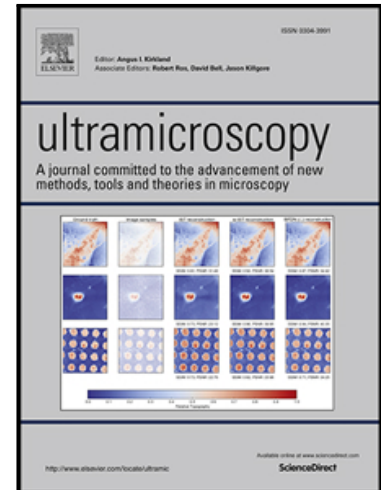
PII: S0304-3991(16)30202-9
DOI: [10.1016/j.ultramic.2018.05.011](https://doi.org/10.1016/j.ultramic.2018.05.011)
Reference: ULTRAM 12586

To appear in: *Ultramicroscopy*

Received date: 20 September 2016
Revised date: 26 November 2017
Accepted date: 29 May 2018

Please cite this article as: Stefan Doering , Andre Wachowiak , Hagen Roetz , Stefan Eckl , Thomas Mikolajick , SDVSRM - a new SSRM based technique featuring dynamically adjusted, scanner synchronized sample voltages for measurement of actively operated devices, *Ultramicroscopy* (2018), doi: [10.1016/j.ultramic.2018.05.011](https://doi.org/10.1016/j.ultramic.2018.05.011)

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Highlights

- SDVSRM, a new SSRM based two pass SPM mode is introduced.
- The new method combines SVM and SSRM in a two pass measurement.
- SDVSRM enables two-dimensional dopant characterization of actively operated devices with high spatial resolution and high dynamic range.
- Several proof of concept measurements are successfully demonstrated using the example of a well-known photo diode test device.

ACCEPTED MANUSCRIPT

SDVSRM - a new SSRM based technique featuring dynamically adjusted, scanner synchronized sample voltages for measurement of actively operated devices

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Abstract:

Scanning spreading resistance microscopy (SSRM) with its high spatial resolution and high dynamic signal range is a powerful tool for two-dimensional characterization of semiconductor dopant areas. However, the application of the method is limited to devices in equilibrium condition, as the investigation of actively operated devices would imply potential differences within the device, whereas SSRM relies on a constant voltage difference between sample surface and probe tip. Furthermore, the standard preparation includes short circuiting of all device components, limiting applications to devices in equilibrium condition. In this work scanning dynamic voltage spreading resistance microscopy (SDVSRM), a new SSRM based two pass atomic force microscopy (AFM) technique is introduced, overcoming these limitations. Instead of short circuiting the samples during preparation, wire bond devices are used allowing for active control of the individual device components. SDVSRM consists of two passes. In the first pass the local sample surface voltage dependent on the dc biases applied to the components of the actively driven device is measured as in scanning voltage microscopy (SVM). The local spreading resistance is measured within the second pass, in which the afore obtained local surface voltage is used to dynamically adjust the terminal voltages of the device under test. This is done in a way that the local potential difference across the nano-electrical contact matches the software set SSRM measurement voltage, and at the same time, the internal voltage differences within the device under test are maintained. In this work the proof of the concept could be demonstrated by obtaining spreading resistance data of an actively driven photodiode test device. SDVSRM adds a higher level of flexibility in general to SSRM, as occurring differences in cross section surface voltage are taken into account. These differences are immanent for actively driven devices, but can also be present at standard, short circuited samples. Therefore, SDVSRM could improve the characterization under equilibrium conditions as well.

1. Introduction

1.1. Standard SSRM

Scanning spreading resistance microscopy (SSRM) is a secondary imaging mode derived from contact mode atomic force microscopy (AFM) using conductive probes [1]. A specific, constant dc sample bias (V_{dc}) is applied to the device under test (DUT) while scanning the sample with a probe at ground potential. The local current flow is measured by a logarithmic current amplifier to ensure a high dynamic range and the resistance output is calculated as a function of V_{dc} . As all series resistances within the measurement path contribute to the measurement signal, SSRM strongly relies on the spreading resistance at the nano-electric point contact to be the dominant resistance contribution. For Si samples the very interface resistance of the nano-contact from the probe to the semiconductor is much smaller than the spreading resistance, since a phase transformation to a

metallic state of the silicon right beneath the probe tip is achieved by the high contact forces [2, 3]. Under these conditions, the measured resistance can be described in first approximation and referring to the classical Maxwell ohmic nanocontact model as a function of sample resistivity (ρ_{sample}) and the contact area (a):

$$R_{\text{meas}} \sim R_{\text{nano-el. contact}} = \rho_{\text{sample}}/4a$$

If the contact area (a) remains constant during SSRM measurement, the measurement signal corresponds to the local sample resistivity that is linked to the local free carrier concentration. Therefore, SSRM is used for two-dimensional semiconductor dopant characterization. Beside the local current flow through the probe tip, the DUT is in equilibrium condition under ideal SSRM operation, as all dopant areas and device components are intentionally short circuited by the back contact. The wide acceptance of SSRM as a method for semiconductor dopant characterization [4, 5, 6] and failure analysis [7, 8] proves this approach to be reasonable. In fact, the equilibrium condition of the DUT guarantees the measured local resistivity (as a function of the local free charge carrier density) to correlate with the activated dopant concentration, which is usually the desired result.

1.2. Motivation for the Introduction of Dynamic, Scanner Synchronized Voltage Adjustment

Electron devices and their dopant distribution are designed for electrical operation. In case of a metal oxide semiconductor field effect transistor (MOSFET) this includes switching between on- and off-state with significantly different electrical properties of the device. The field effect transistor (FET) channel resistance, for example, decreases more than six orders of magnitude from off- to on-state. Commonly used methods for active device characterization are I - V - or C - V -measurements, both being electrical methods showing the response of the complete device. From this integral electrical response, deductions on the dopant distribution can be made by so called inverse modeling techniques [9]. On the contrary, SSRM assesses the free charge carrier distribution of a device in equilibrium state. The obtained local data can be used to derive predictions on the integral electrical behavior of the actively driven device. On the other hand deriving predictions is not as good as really measuring the free charge carrier distribution in the actual active state of the device. This is something standard SSRM is not capable of. As stated in the section above standard SSRM relies on the short circuiting of all device components, and therefore, is only capable of characterization of the device in equilibrium state. As soon as non-negligible internal potential differences within the DUT are present, a measurement using standard SSRM would lead to significant measurement errors of the local spreading resistance, and hence, free carrier distribution. Figure 1 shows a theoretical example of a device or part of a device not being in equilibrium condition. The materials spreading resistance is assumed to have a constant value of $1\text{M}\Omega$ at every position. A linear potential increase from -1V to $+1\text{V}$ over a distance of $10\mu\text{m}$ is present at the sample surface. It is notable that only at position $x=-2.5\mu\text{m}$ the sample surface voltage (V_S) equals the software set dc voltage $V_{\text{dc-sw}}$, and therefore, only at this position the correct spreading resistance is obtained. As the measured resistance R_{meas} is calculated by the AFM using $V_{\text{dc-sw}}$ divided by the measured current, positions exhibiting lower surface potential V_S than $V_{\text{dc-sw}}$ ($x < -2.5\mu\text{m}$) will result in too low spreading resistance values, whereas for $V_S > V_{\text{dc-sw}}$ ($x > -2.5\mu\text{m}$) the output results in too high spreading resistance values. In case of different polarity between $V_S(x)$ and $V_{\text{dc-sw}}$ no reasonable output is generated at all ($x > 0\mu\text{m}$).

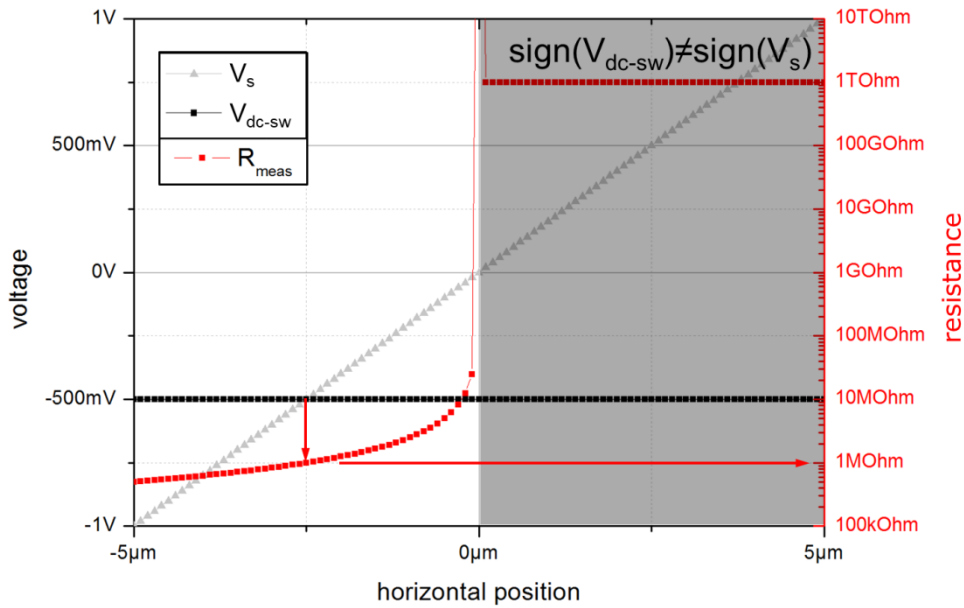


Figure 1. Correlation of measured resistance R_{meas} at a constant $V_{\text{dc-sw}}$ in case V_s is increasing linear as a function of the horizontal position. In this model a sample having a constant local spreading resistance of $1\text{M}\Omega$ is assumed.

However, the combination of both, electrically functional devices, that can be actively driven and a simultaneous visualization and characterization of the free charge carrier distribution has the potential for a better understanding of device functionality. This applies for all areas of application of SSRM. In device development, the simulation results might fit the actual carrier distribution for the equilibrium case, but exhibit differences under certain modes of operation. Direct assessment of the free carrier distribution in the specific mode would be of great benefit. Another possible application case would be in failure analysis. It is perfectly conceivable to increase the fingerprint of a defect by switching from equilibrium state to some actively driven mode of operation. Physical analysis of a FET exhibiting, for example, punch through behavior in I - V -characterization would drastically benefit from the possibility, to set the device into off-state during analysis. For a better demonstration and verification of the method, a rather simple sample exhibiting laterally constant dopant distribution is used in this work.

All active biasing of devices as described within this work is of a static nature. A specific state of operation is set by biasing and then kept constant during the whole measurement. Although, dynamic voltages are applied, the potential differences between different ports of the device stay constant during the measurement while dynamic device behavior is neglected.

1.3. Alternative SPM Methods for Active Device Characterization

First attempts to apply the relatively new scanning probe microscopy (SPM) techniques to actively driven devices, were already made short after SSRM was established. A method for local potential measurements was introduced in 1995 [10] and patented in 1998 [11]. This method, dubbed nanopotentiometry is equivalent to what is referred to as scanning voltage microscopy (SVM) by other groups and in this work. Results of this method applied to a MOSFET can be found in the literature [12, 13]. SDVSRM uses the SVM methodology within its first pass of the measurement to obtain the local surface voltage of the sample.

In 2000, scanning capacitance microscopy (SCM) was successfully applied for active device characterization for the first time [14]. As a major advantage, in SCM the probe tip is not in direct contact with the semiconductor material, thus reducing the probes electrical influence on the DUT. A second example for the application of the SCM technique includes a flexible approach to combine

the sample holder and voltage application [15]. In this work, a similar setup employing packaged devices is used.

A lot of effort on characterization of active devices was put in by a group at the University of Toronto. Focus of their work was the investigation on indium phosphide (InP) heterostructure multi-quantum-well lasers. Additionally to classical SCM and SSRM measurements [16], SVM was applied on a larger scale [17, 18, 19]. The work culminated in the development of the scanning dynamic spreading resistance microscopy (SDSRM), a lock-in amplifier assisted SSRM method focusing on the characterization of active devices [20, 21].

Although, all of the above mentioned methods are able to visualize either surface potential or sample resistance in two dimensions with high spatial resolution, none of them is capable of obtaining the actual sample surface voltage distribution and the free charge carrier distribution at the same time in only one measurement.

2. Experimental Details

2.1. Measurement Principle of SDVSRM

When considering actively driven devices for SSRM measurement, measurement voltages have to be redefined. In standard SSRM the applied dc bias V_{dc} is set within the AFM control software. It is applied to the sample chuck and therefore to the bulk of the sample. Furthermore, V_{dc} is assumed to be present at the sample cross section surface, otherwise the interpretation of the measured resistance as spreading resistance becomes inaccurate. Both relations are repealed when measuring active devices. To be able to drive individual ports (i) of a DUT using different voltages, the software set SSRM measurement voltage V_{dc-sw} has to be decoupled from the DUT port voltages V_{active}^i . As a result of the DUT internal potential differences, the sample surface voltage V_s is now a function of the probe position (x), the active DUT voltages V_{active}^i and the device properties like dopant concentration.

The basic idea of SDVSRM is to obtain an SSRM image with constant potential between probe and surface equal to the software set dc bias (V_{dc-sw}), although voltage differences between different ports of the DUT cause an active static state. This is accomplished (line by line) by measuring the local cross section surface voltage $V_s(x)$ dependent on the port voltages V_{active}^i applied to the DUT in the first pass of the scan. In the second pass, the actual SSRM measurement, the voltages applied to the individual DUT ports are controlled dynamically ($V_{dynamic}^i$) in a way, the potential differences between the ports stay the same as defined by the set active state, and furthermore, the potential between probe and surface matches the software set dc bias (V_{dc-sw}) at any position of the probe during scanning. The matching of the probe to surface potential and (V_{dc-sw}) is only possible because of the data acquisition in the first pass.

Since the resulting port voltages become dynamic ($V_{dynamic}^i$) in the second pass of SSRM data acquisition, the method is called scanning *dynamic voltage* spreading resistance microscopy (SDVSRM).

In summary, SDVSRM brings the DUT in an active state first, followed by mapping the surface potential distribution caused by this active state during the first pass. In the subsequent second pass the potential distribution is shifted as a whole in a way the potential difference to the probe tip is adjusted to be V_{dc-sw} at any measurement point. The DUT itself stays in the same electrical state and has the same internal potential distribution throughout the whole measurement (first and second pass).

A theoretical example, illustrating the dynamic voltage measurement principle and the relationship between the involved voltages, is shown in figure 2.

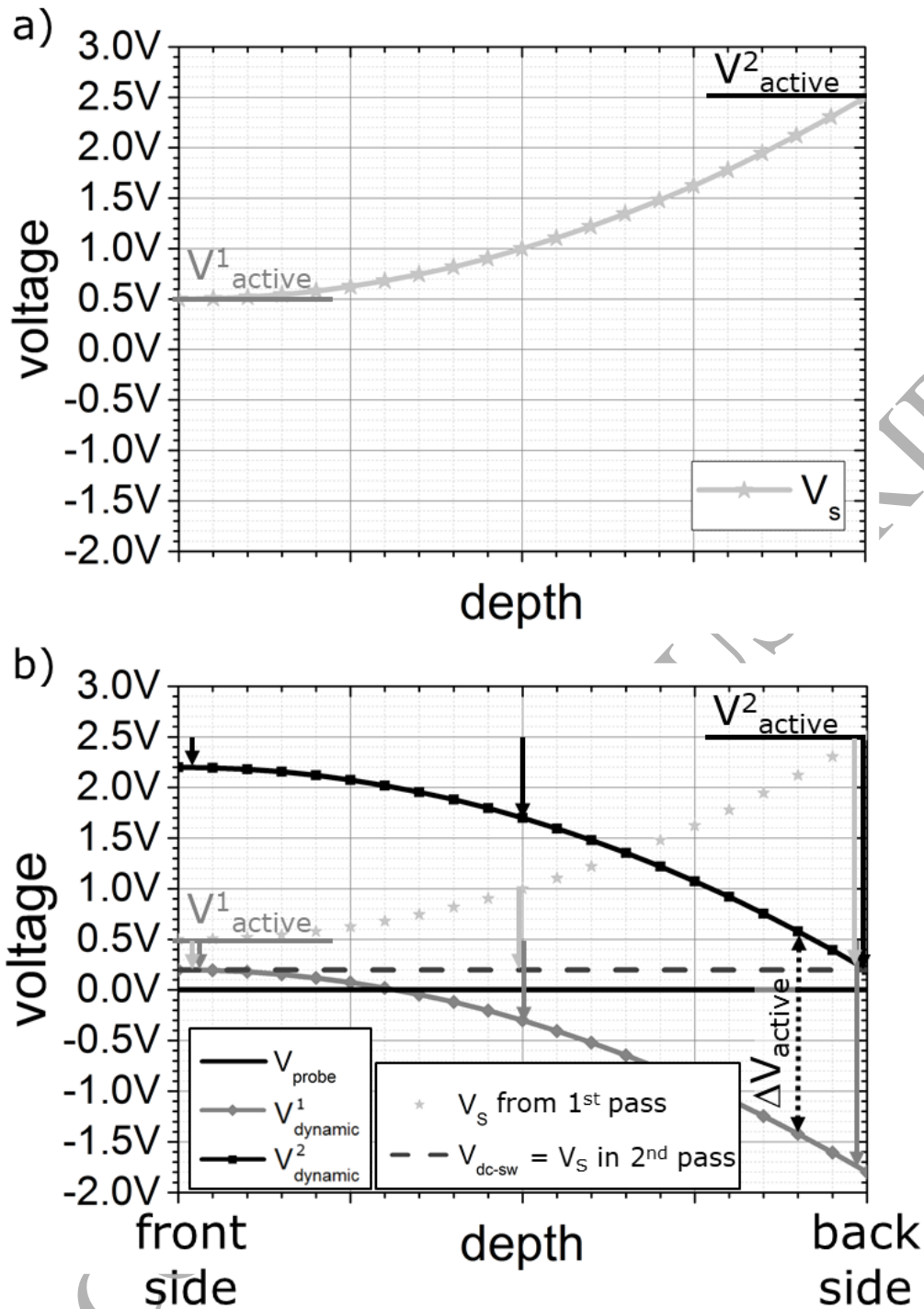


Figure 2. Example plot demonstrating the correlation of the different voltages to be considered in SDVSRM. In a) the potential profile V_s from the front- to the back-side of the sample is shown, as it is measured in the first pass (SVM) of the SDVSRM measurement. This profile is defined by the active voltages (V_{active}) applied to the front- and backside of the sample in combination with the doping profile. The dopant profile was assumed to be non-constant, in order to achieve a nonlinear potential profile. Voltages relevant in the second pass are shown in b). The intended SSRM measurement bias ($V_{\text{dc-sw}}$) is +0.2V. As the probe tip is fixed at ground potential (V_{probe} – solid black curve), the different device terminals have to be dynamically driven (V_{dynamic}) dependent on the probe tip position (depth) during the second pass SSRM data acquisition. This is mandatory in order to keep the actual sample surface potential (V_s) at every single measurement position within the second pass equal to $V_{\text{dc-sw}}$ by simultaneously maintaining the potential difference (ΔV_{active}) between the sample front- and back-

side. The arrows at the front side, back side and center position illustrate the difference between the first pass V_{active} and the second pass V_{dynamic} at these points being equivalent to the difference of V_s from the first pass to V_s in the second pass, which is in turn equivalent to $V_{\text{dc-sw}}$.

Assumed is a thin sample of p - or n -type doping exhibiting a front- and back side contact. $V_{\text{active}}^1 = +0.5\text{V}$ is applied at the front and $V_{\text{active}}^2 = +2.5\text{V}$ at the back side. The potential difference between front- and backside, thereby, is $\Delta V_{\text{active}} = 2\text{V}$. A decreasing dopant concentration from the front- to the back side is assumed to introduce a nonlinear voltage profile $V_s(x)$ to be observed by SVM in the first pass of the SDVSRM measurement (figure 2a). As the probe voltage ($V_{\text{probe}} = 0\text{V}$) is kept constant at the amplifier virtual ground potential at any time, the whole sample potential has to be adapted during the second pass SSRM measurement (figure 2b) in a way that first, the potential difference between sample front- and backside stays constant during the measurement ($\Delta V_{\text{active}} = 2\text{V} = \Delta V_{\text{dynamic}}$) and second, the potential difference between the probe tip (V_{probe}) and the local surface voltage ($V_s(x)$) is kept constant and equal to the SSRM measurement voltage ($V_{\text{dc-sw}}$). Therefore, the device bias voltages have to be dynamically controlled during SSRM data acquisition ($V_{\text{dynamic}}(x)$). The relationship is shown in the following equation for terminal number i :

$$V_{\text{dynamic}}^i(x) = V_{\text{active}}^i - V_s(x) + V_{\text{dc-sw}}$$

For the verification of the equation, the positions of front- and back side can be considered. For both positions, the according V_{active} equals the SVM measured $V_s(x)$. Therefore, V_{dynamic} of the respective location becomes $V_{\text{dc-sw}}$, the desired sample bias with respect to the probe voltage at ground.

2.2. Measurement Setup for SDVSRM

The AFM used within this work is a Bruker Dimension Icon equipped with a Nanoscope V controller. The developed setup is shown in figure 3. The first pass SVM measurement for $V_s(x)$ acquisition requires an electrometer. A Keithley 6614/E is used in the experiments described. The following SSRM measurement makes use of the standard Bruker SSRM amplifier. To be able to switch between both, a relay was included in the setup. Switching has to be synchronized with data acquisition. Therefore, a relay capable of being triggered by a transistor transistor logic (TTL) signal was used¹.

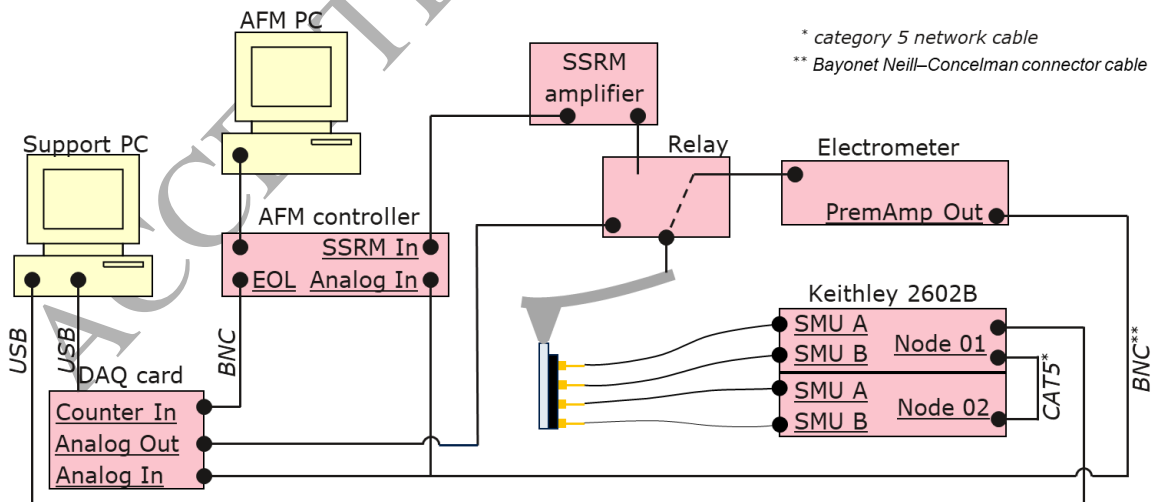


Figure 3. Setup scheme of the SDVSRM technique.

¹ Customizable relay board with latching option and active high/low option from Engineeringshock – <http://www.engineeringshock.com/custom-relay-board.html>

There are three possible synchronization options: per pixel, per line and per frame. On the one hand, per pixel synchronization places too high demands on relay switching speeds. On the other hand, synchronization per frame excessively increases the time between $V_s(x)$ measurement and the spreading resistance measurement, based on the $V_s(x)$ input. Artifacts caused by sample drift or tip wear would become more likely. Moreover, the length of the feedback loop for adjusting synchronization or imaging settings would be unacceptable. Based on these considerations, per line synchronization was realized. In addition to the standard SSRM signal routing, the electrometer pre-amplifier output is fed into the AFMs controller analog input and simultaneously into a data acquisition (DAQ) device. The employed DAQ card features digital, as well as analog in- and outputs². The acquired electrometer output data ($V_s(x)$) is processed by a support computer, adding the SSRM measurement voltage (V_{dc-sw}). The DAQ card also registers the scanner completing an individual scan line by counting the end-of-line (EOL) pulses of the AFM. The DAQ card applies the required switching signal to the relay trigger input, based on the number of EOL pulses. For DAQ card input readout and output control, the LabView visual programming environment was used. As the employed Keithley 2602B Source Measure Units (SMUs) provide LabView driver software, they could be controlled directly throughout the software via universal serial bus (USB) connection. During SVM operation, the individual SMU outputs are set to the constant dc voltages V_{active}^i , defining the DUT active state. After switching to SSRM mode, the local surface voltage ($V_s(x)$) is subtracted from and the SSRM measurement voltage (V_{dc-sw}) is added to the individual V_{active}^i . The resulting $V_{dynamic}^i$ is then applied to the SMUs in a dynamic way, synchronized with the scanner position.

2.3. Photodiode Test Device

The SDVSRM measurements presented in this work originate from a photodiode test sample. In contrast to samples including highly integrated devices, the array of photosensitive areas offers planar implant areas of several ten micrometer length. This enables decoupling of changes in free carrier concentration from changes in measurement signal due to an alteration of the driving voltages of the device. For example, in one SDVSRM 2D-scan of the cross section of the photodiode test structure, one can measure parts of the scan with different bias conditions, while the same dopant profile is present. This kind of measurement is beneficial for comparisons, since variations originating from the particular conditions of the probe tip are minimized.

² NI myDAQ from National Instruments – <http://www.ni.com/mydaq/>

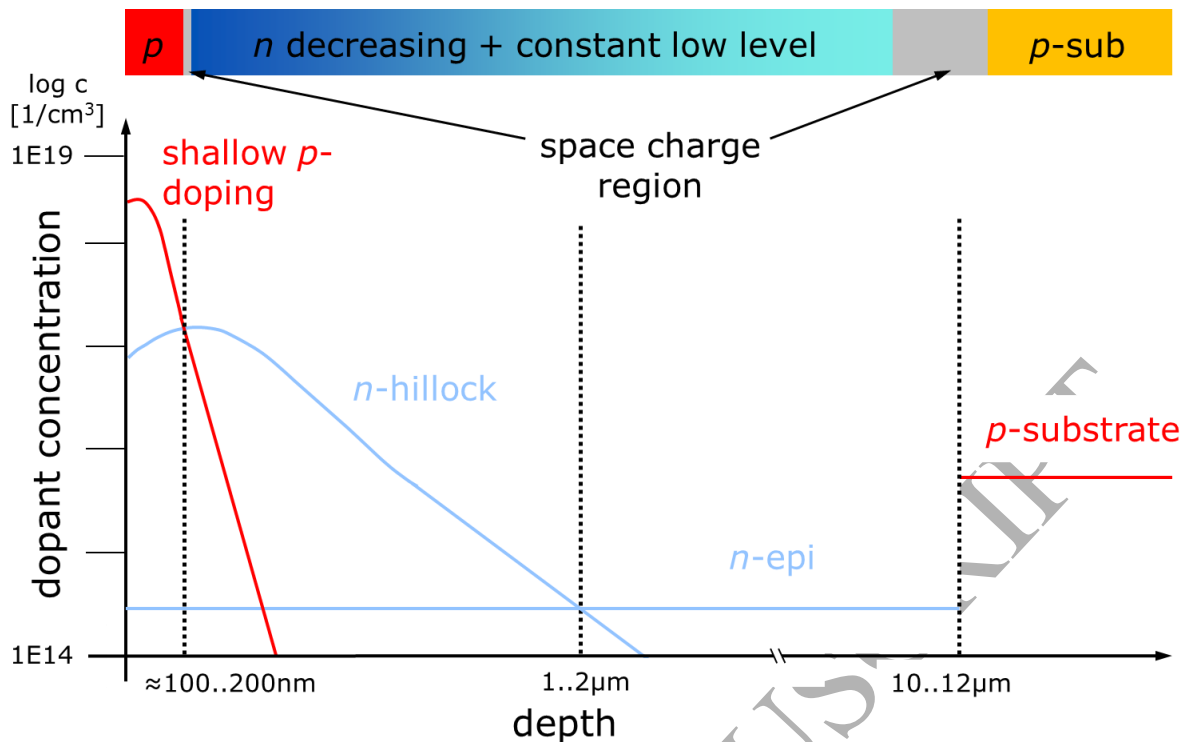


Figure 4. Schematic view (top) and doping profile (bottom) of the photodiode test sample. At the surface, there is a thin, highly p -doped layer, followed by an n -doped hillock with decreasing dopant concentration down to the low n -epi level. At the bottom the moderately p -doped substrate completes the test layer stack.

The 1-dimensional dopant profile of the photodiode sample is shown in figure 4. A shallow (approximately 100...200nm in depth), highly p -doped layer is present at the sample surface, followed by a moderately doped n -layer. The dopant concentration of this layer decreases in approximately 1 to 2 μm depth down to the constant low doping level of the n -epi. The overall depth of the n -epi is 10 to 12 μm . The underlying substrate is moderately p -doped. This layer stack includes two p - n -junctions. The one near the sample surface, between the highly p -doped layer and the moderately n -doped layer will form a narrow space charge region (SCR) under equilibrium conditions, whereas the deeper junction between the p -substrate and the lowly doped n -epi develops a wider SCR. Of particular interest in active device characterization are the observation of changes of the p - n -regions upon application of different bias potentials and how the dimensions of the associated SCRs are altered. The photodiode is a well suited test device, since much is known from CV -characterization of these broad structures [22].

2.4. Sample preparation

Mechanical grinding and polishing was used for sample preparation because of several reasons. First of all, the freedom of cross section positioning should be preserved. With possible applications in failure analysis in mind, this is a strong requirement, simultaneously ruling out sample cleaving. On the other hand, focused ion beam (FIB) with its superior accuracy, strongly limits the prepared cross section area and therefore, was not taken into account for sample preparation. By the application of grinding and polishing, large cross section areas of high quality can be achieved at user specified positions with an accuracy as low as 100nm. Another reason was that in previous studies, it has been shown that grinding and polishing delivers the most reliable results with respect to the minimization of surface leakage currents occurring at the samples cross section surface due to the preparation [12].

One major requirement for an active driving of several distinct components of a DUT is the ability to electrically contact them separately. In general, the electrical connection can be established whether

before or after the cross section preparation. Though, an additional preparation step following the final cross section preparation is not recommended, due to the sensitivity of the cross section surface. Furthermore, establishing electrical connection after the various, partly dirty, preparation steps, is difficult and might not yield in low resistance contact. Within this work, wire bond samples within a test package were used and the electrical connection of the individual device components was done before cross sectioning. By doing so, the electrical contact could be achieved at the complete, non-prepared and therefore clean chip. Furthermore, this approach offers the possibility of electrical characterization, e.g. by means of IV -characterization, before, during and after sample preparation. For protection and passivation purposes, the bond wires were coated before grinding and polishing, using an epoxy resin³.

A part of the photodiode array after sample preparation is shown in the top down optical microscopy image in figure 5 a). One single cell is approximately $40 \text{ by } 40 \mu\text{m}^2$ in size. The center contact, which connects the shallow, top, highly p -doped layer of each cell, is clearly resolved in the image. The orientation of the cross section has to be chosen in a way that this center contact and its metal connection (dark line above) are not removed by the preparation process. In between the individual cells, the metallization stack is visible. An optical microscope image of the so prepared cross section is shown in figure 5 b).

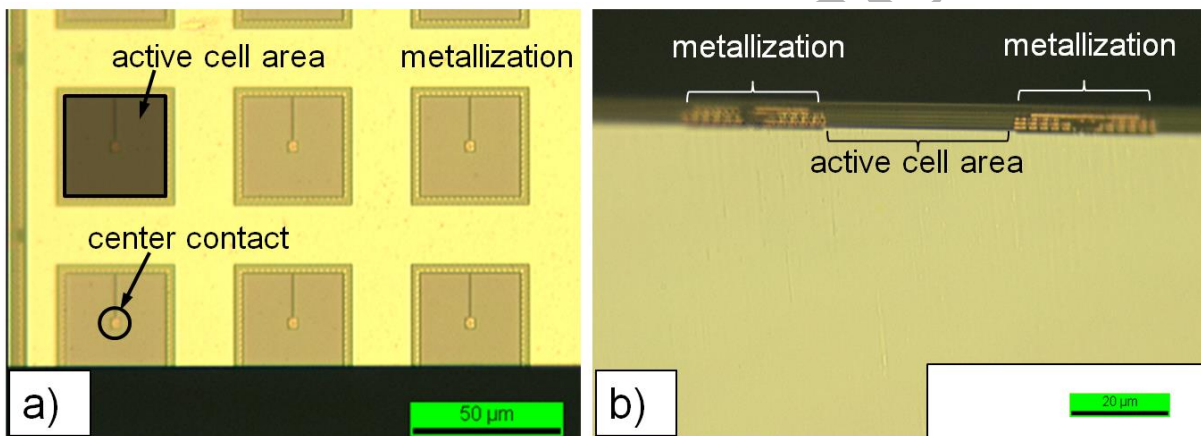


Figure 5. Top down (a) and cross section (b) optical microscope images of the photodiode test sample after preparation.

3. Results and Discussion

The experiments using the new SDVSRM technique were conducted at the above shown photodiode test sample. First, an example of SVM measurement and the resulting dynamic signals (V_{dynamic}^i) are shown in figure 6 for the scan across the upper (surface near) p - n junction of the photodiode. In the SVM measurement the n -epi and p -substrate were forced to 0V, whereas +0.3V was applied to the shallow p -region. The complete voltage drop is measured across the space charge region of the upper p - n junction as shown in the SVM data.

For the 2nd SSRM scan a target voltage of $V_{\text{dc-sw}} = 0.1\text{V}$ was intended. In addition, Figure 6 shows the synchronized dynamic voltage, which demonstrates the successful voltage adaption to generate a surface voltage of 0.1V. There are some small deviations visible for positions exhibiting steep slopes in the V_s signal. Most probably the observed deviations are caused by the slow adaption speed of the SMUs. Although measuring in contact mode at high contact forces limits the scan speed to some degree in order to prevent tip wear out, the limited SMU response time was found to be the bottleneck in our setup also limiting the maximum scan rate for a certain resolution (points per line).

³ EpoThin from Buehler

4 ms per point of a 512 points per line scan lead to a minimum scan time of approximately 2 s per line, which corresponds to a scan rate of 0.25 Hz. Future work on this new characterization method should focus, inter alia, on solving this problem, for example by replacing the rather slow SMUs. Different from what would be expected, in this example the shallow p -layer exhibits a maximum in voltage in its center. This might be a result of tip wear out. Only at the center of the layer, the probe is in full contact with the shallow p -area. More to the left and to the right, the probe tip was most probably in contact with surrounding material, affecting the measured V_S . Although tip wear out has a negative effect on measurement results in general, this example shows one of the strengths of the method. It takes probe tip and imaging conditions automatically into account. From the probe tips point of view, the obtained V_S profile is the actual potential profile at the set device active state. Exactly that V_S profile has to be matched to V_{dc-sw} in the second pass to achieve the desired result.

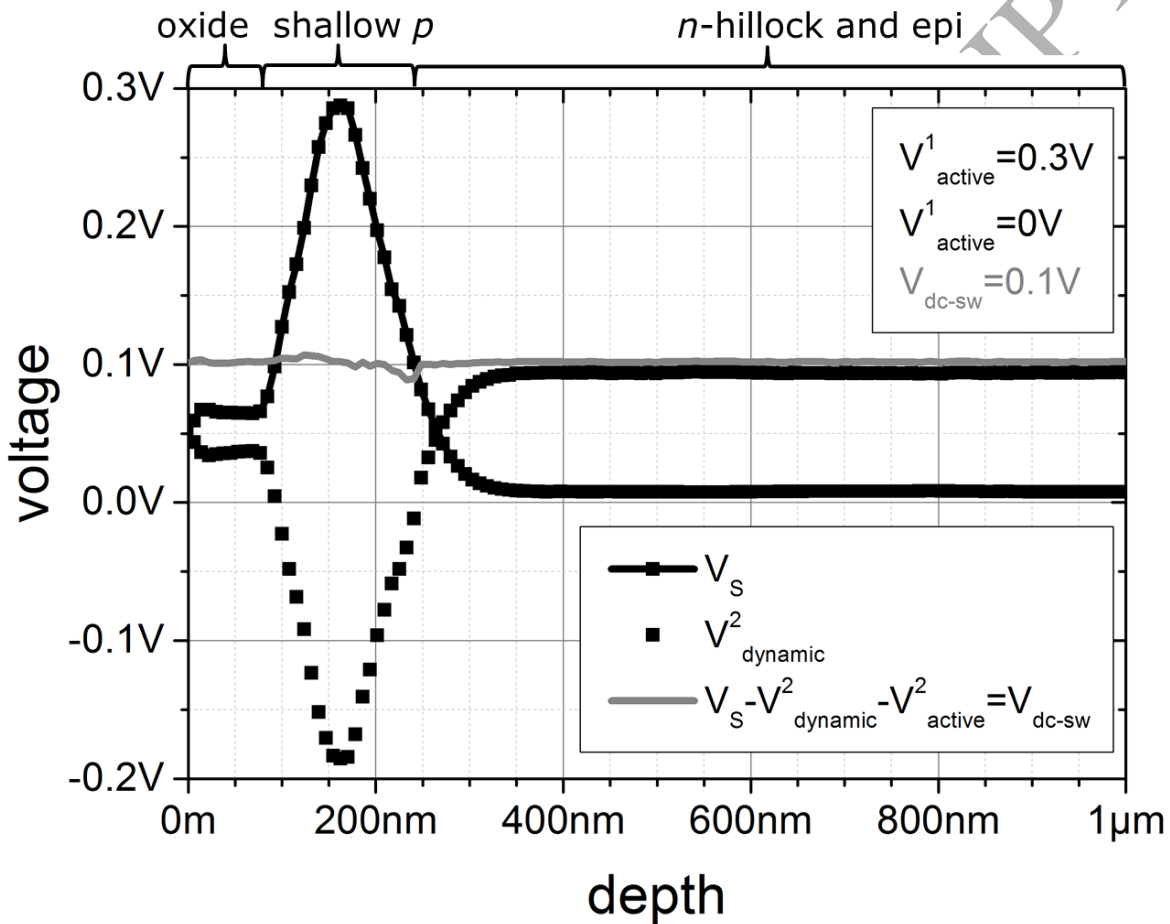


Figure 6. Shown are the first pass SVM data (black line and symbols) obtained from the photodiode test sample, the $V_{dynamic}^2$ (symbols only) applied during the second pass SSRM measurement and the effective voltage difference (grey line) between the probe tip ($V_{probe}=0V$) and the sample dependent on the scanner position. In this experiment $V_{active}^2 = 0V$ is applied to the n -epi and the substrate of the sample, while the voltage applied to the shallow p -region was set to $V_{active}^1 = +0.3V$.

SDVSRM measurements of the photodiode are shown in figure 7. Every measurement delivers SVM and SSRM data, as both methods are combined in this two pass technique. Figure 7 a) shows the SSRM data obtained at $V_{dc-sw} = -50mV$. The voltage of the n -epi and p -substrate were both set to $0V$, whereas the voltage of the shallow p -layer (V_p) was varied in a stepwise manner during scanning as noted at the left hand side of the image. Starting from the bottom of the image at the devices equilibrium state, V_p was decreased in $1V$ steps, until a minimum V_p of $-6V$ was reached. In this case, one can directly compare the data on different stripes of different active voltage, since it can be assumed that the doping profile is not changing along the vertical axis (parallel to the surface), but

only on the horizontal axis (depth scale) according to fig. 4. Hence, different bias conditions can be analyzed in one image, which drastically reduces measurement time.

The corresponding SVM and SSRM depth profiles for each bias condition are shown in figure 7b) and c) for the full depth scale, as well as in d) and e) for the first micrometer from dielectric to silicon interface. Both, SSRM image and profiles show no change in p -sub and n -epi carrier distribution for a depth $> 5 \mu\text{m}$ during the experiment. Significant changes in SSRM profiles upon different bias condition could be observed within the first $4\mu\text{m}$ of the device.

Starting the discussion with the resistance profile in equilibrium condition, a resistance maximum is observed at around 180nm between minima at about 50 and 300nm . The maximum matches well the location of the space charge region of the surface near p - n -junction and the minima at 300nm stems from the higher doped n -region of the n -hillock. The resistance value within the n -region is continuously increasing from the minima at 300nm to the n -epi value in some μm depth. In this example, a lower resistivity value is expected for the p -substrate compared to n -epi and for the shallow p -region compared to the n -hillock, but the inverse behavior is measured. Partly this effect can be attributed to the higher mobility of electrons compared to the mobility of holes. The major part of this discrepancy, however, can be attributed to the non-ohmic behavior of the probe to sample contact. As in all SSRM measurements the absolute values of resistance between n - and p -regions cannot be directly compared without any further calibration. Despite this apparent asymmetry of dopant polarity, relative signal variations within the same dopant type are still reliable.

With decreasing voltage V_p , and hence, operating the surface near junction more and more in reverse bias condition, several changes can be seen in the SSRM profiles. Before going into detail, it should be pointed out that the process of depletion can be divided into two distinctive stages. In the first stage of depletion ($0V > V_p > -3V$) the SCR grows slowly in width as on the n -side of the junction the moderately doped n -hillock has to be depleted first. In the second stage ($-3V > V_p$) the n -hillock is completely depleted and the SCR now quickly extends to greater depths into the lowly doped n -Epi. This behavior as observed by SDVSRM confirms C - V measurements on the same kind of device [22]. In the first stage of depletion starting from the equilibrium state ($V_p = 0V$) towards negative values, the resistance maximum at around 180nm , which corresponds to the center of the space charge region between shallow p - and n -hillock/epi broadens, increases in value and shifts slightly deeper. The increase in value can be attributed to further reduction of mobile charge carriers within the SCR as the reverse voltage and, hence, the width of the SCR increases. As the shallow p -layer is of rather high doping compared to the n -hillock, the broadening of the SCR occurs predominantly at the n -side of the junction. Therefore, the maximum value of resistance, which is measured in the center part of the SCR shifts in this direction as well. Also in the first stage of depletion ($0V > V_p > -3V$) the resistance minimum in the n -hillock region increases and shifts deeper, before it disappears, correlating with the complete depletion of the n -hillock. All these observations for this stage of depletion are in good agreement with the design of the photodiode and the integral C - V measurements. Only the measured decrease in resistance of the shallow p -region is not fully understood and still under discussion.

In stage two of the depletion process ($-3V > V_p$) the entire n -hillock is depleted and the SCR extends into the n -epi. From this point on, the SCR grows much deeper with increasing reverse bias voltage. This characteristic is showing up as the missing resistance minimum in the n -hillock region due to broad and deep maximum of the SCR, which is clearly observed in the resistance profiles of 7 b) or visualized in figure 7 a). Accordingly, the voltage drop of the SVM profiles extends deeper into the n -epi layer, when the SCR extends beyond the n -hillock.

When looking at the different $V_s(x)$ profiles in more detail (figure 7 e), a significant difference between the applied V_p and the observed $V_s(x)$ at the shallow p region is observed. Moreover, the SVM profiles of $V_p = -3V$ and $-5V$ do not follow the trend of lower $V_s(x)$ voltage for lower V_p values in the shallow p -region. The deviations might be caused by a sudden degradation of the electrical contact between probe and sample during the measurement. If these deviations between expected and measured $V_s(x)$ can cause the observed, but unexpected, decrease in spreading resistance of the shallow p -layer with increasing V_p could not be clarified. The data suggest a sensitive relation, since the largest differences between expected and measured voltage show up for $V_p \leq -3V$, when the

spreading resistance significantly drops and a curious shoulder in the resistance profile of the rise from the resistance minimum in the shallow p -region to the maximum in the SCR develops. In addition, it cannot be excluded that the laser light for scanning the probe tip could be another potential source for artefacts in the SSRM signals (due to charge carrier generation).

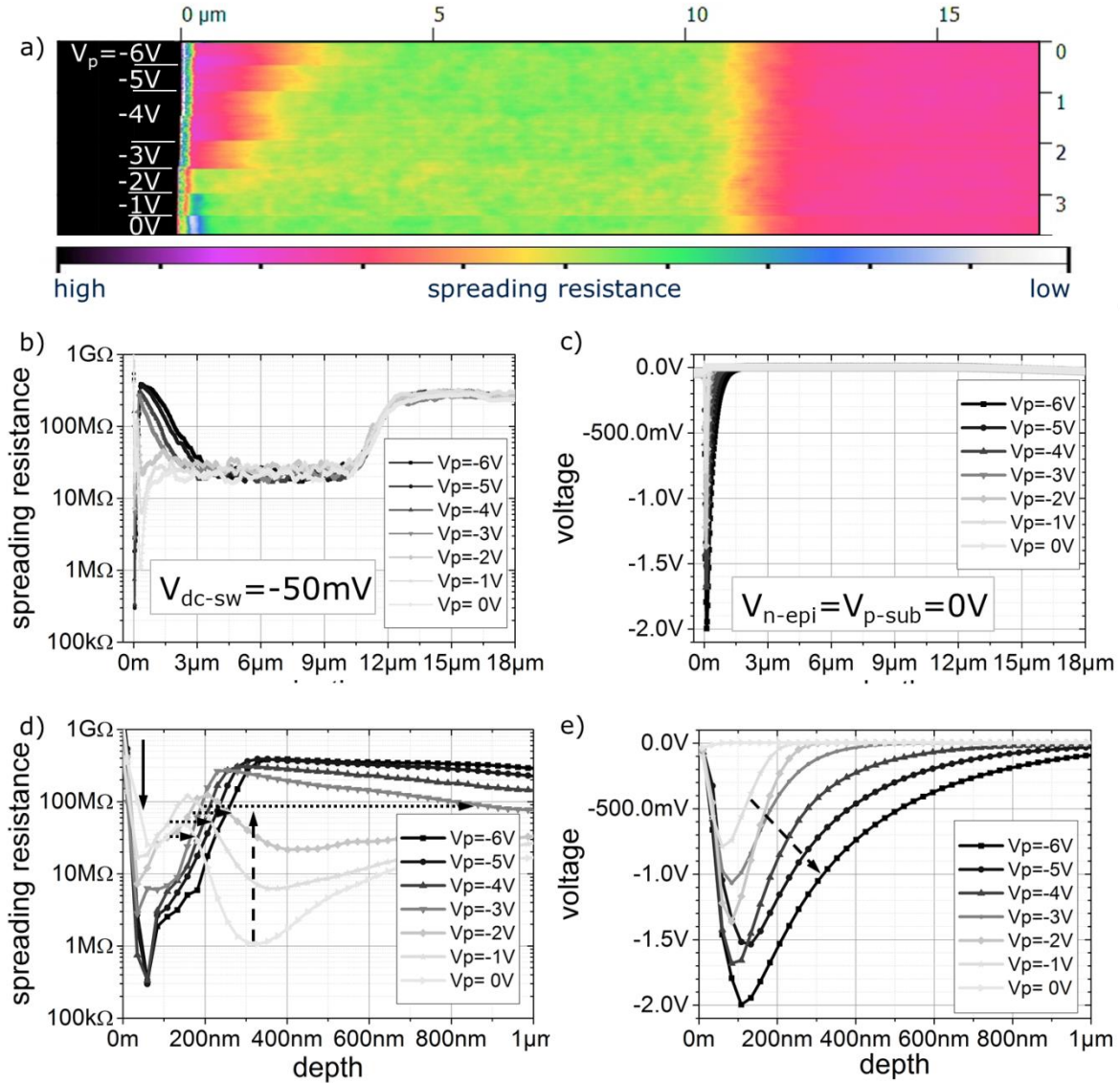


Figure 7. SDVSRM results obtained from the photodiode test structure. In a) the resulting SSRM image using $V_{dc-sw} = -50mV$ is shown. The extracted profiles for each V_p setting are shown for the full depth in b) and for the first micrometer in d). The corresponding SVM data are illustrated in c) and e), respectively.

The results of a comparable measurement when biasing the upper p - n -junction in forward bias direction are shown in figure 8. As in the previous experiment, V_{n-epi} and V_{p-sub} were kept constant at 0V and V_p was varied stepwise during scanning, starting from the devices equilibrium condition ($V_p = 0V$) up to +1V. The resulting SSRM image for V_{dc-sw} of +50mV is shown in figure 8 a), the corresponding depth profiles in b) and the corresponding SVM data in c). Up to V_p values of +0.4V only an increase in $V_s(x)$ at the shallow p -layer is observed. The resistance of the shallow p -region strongly decreases from the value at equilibrium, too. Although not fully understood, this behavior might be attributed to carrier injection caused by driving the DUT in active state. The width of the SCR between the shallow p - and the adjacent n -layers decreases significantly. Although the observed maximum resistivity shifts slightly towards greater depths (dashed line), this might be a result of the

decreased p -layer resistance. Above V_p values of +0.4V the SCR disappears and a decrease of the resistance in the lowly doped n -epi is measured as well as an increase in $V_s(x)$ for the n -epi is observed. This behavior can be attributed to the switching the p - n -junction to forward bias conditions. At this point the voltage applied to the p -shallow region directly influences the n -Epi voltage. As long as the SCR is still present, in contrast, no influence from V_p to V_s at the position of the n -Epi is visible.

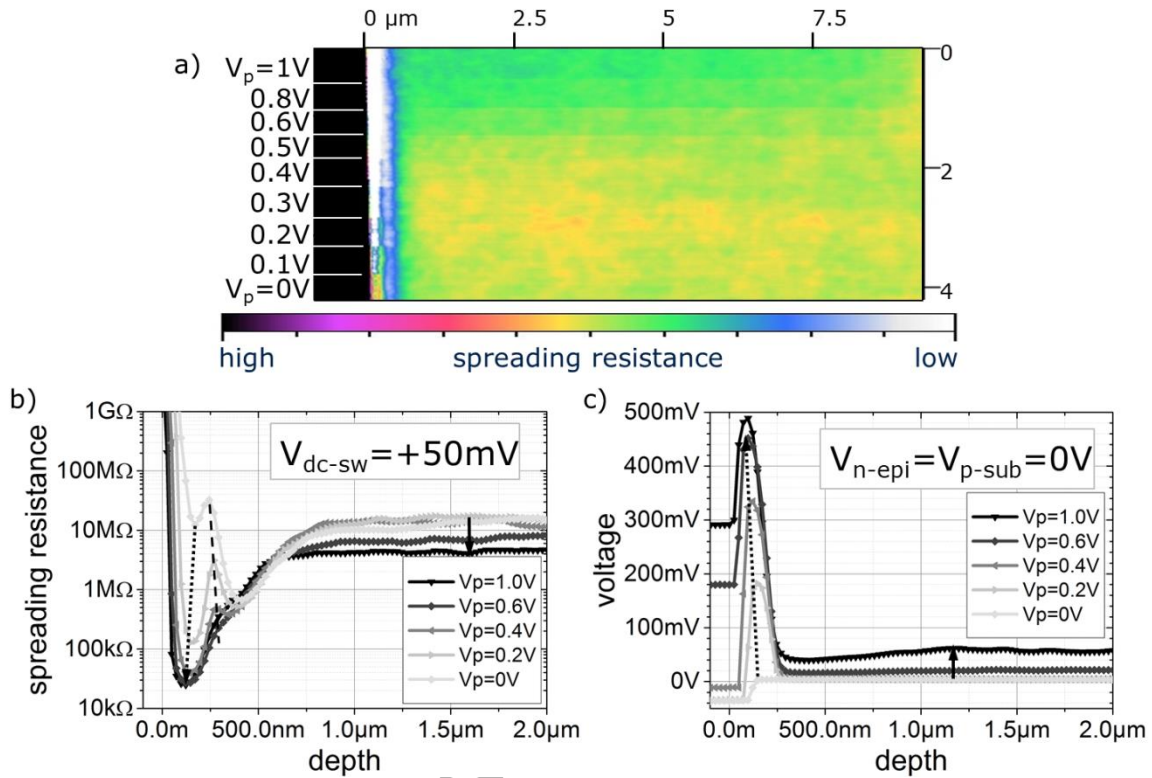


Figure 8. SDVSRM results obtained at the photodiode test structure. In a) the resulting SSRM image using $V_{dc-sw} = +50mV$ is shown. The extracted profiles for each V_p setting are shown in b) and the corresponding SVM data in c).

Another consistency check of the SDVSRM methodology was performed. In this experiment, the whole DUT potential was shifted, with respect to the probe tip. Internal potential differences were kept constant. The SSRM data of the two cases are included in figure 9. The second stripe from top corresponds to $V_p = 1V, V_{n-epi} = V_{p-sub} = 0V$. The topmost stripe exhibits the same V_p potential difference with respect to V_{n-epi} and V_{p-sub} , but this time all voltages were decreased by 1V. The resulting surface voltages V_s , shown in figure 9 a) clearly reveal the different voltage levels applied to the device. The corresponding SSRM data is shown in 9 b). The two profiles are in agreement, as expected for similar internal potential distribution. This experiment clearly demonstrates the major advantage of decoupling surface potential (V_s) and SSRM measurement voltage (V_{dc-sw}), as done by the new SDVSRM method.

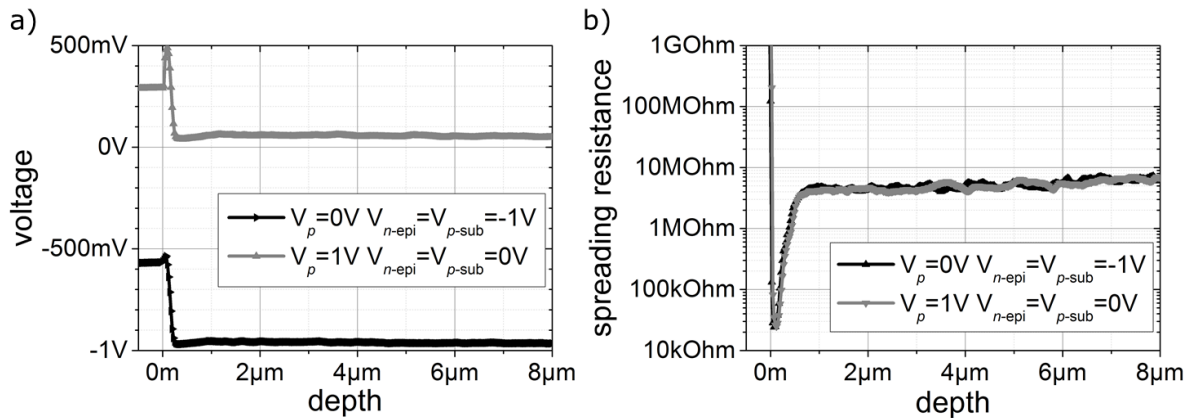


Figure 9. Device potential with respect to the probe a) and resulting SSRM data b). Although the overall device potential with respect to the probe is shifted, the same SSRM data is obtained.

4. Conclusion

SDVSRM, a new SPM technique, combining SVM and SSRM in a two pass process, was conceived and applied successfully to an integrated device for the first time within this work. SDVSRM was developed to obtain reliable SSRM data of devices under external bias condition. It delivers complementary information, by the simultaneously mapping of the local surface voltage V_s and the correlating local free carrier concentration as measured by SSRM. The local V_s dependent on the applied voltage to the device is obtained in the first SVM pass. In the second SSRM pass, the external bias voltages are dynamically adapted according to the SVM scan in order to obtain a constant surface potential at each probe position, although the potential differences between the ports of the device are maintained as in the SVM scan. SDVSRM of a special photodiode device show details of the local free charge carrier concentration under different bias condition. An accurate measurement of the surface potential in the SVM scan is important due to the sensitive relation between the SVM and the successive SSRM measurement. The results demonstrate the potential of SDVSRM as an ideal candidate for two dimensional, high spatial resolution carrier concentration mapping of actively driven devices. Furthermore, the possible deviations between V_s and V_{dc-sw} for devices under equilibrium conditions could be circumvent by the application of SDVSRM.

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