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Multi-staged deposition of trench-gate oxides for power MOSFETs

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Here, silicon oxide was formed in a U-shaped trench of a power metal-oxide semiconductor field-effect transistor device by various processes. One SiO_2 formation process was performed in multiple steps to create a low-defect Si-SiO_2 interface, where first a thin initial oxide was grown by thermal oxidation followed by the deposition of a much thicker oxide layer by chemical vapor deposition (CVD). In a second novel approach, silicon nitride CVD was combined with radical oxidation to form silicon oxide in a stepwise sequence. The resulting stack of silicon oxide films was then annealed at temperatures between 1000 and 1100 °C. All processes were executed in an industrial environment using 200 mm-diameter (100)-oriented silicon wafers. The goal was to optimize the trade-off between wafer uniformity and conformality of the trenches. The thickness of the resulting silicon oxide films was determined by ellipsometry of the wafer surface and by scanning electron microscopy of the trench cross sections. The insulation properties such as gate leakage and electrical breakdown were characterized by current–voltage profiling. The electrical breakdown was found to be highest for films treated with rapid thermal processing. The films fabricated via the introduced sequential process exhibited a breakdown behavior comparable to films deposited by the common low-pressure CVD technique, while the leakage current at electric fields higher than 5 MV/cm was significantly lower. *Published by the AVS.* https://doi.org/10.1116/1.5080527

I. INTRODUCTION

Since the 1990s, when trenches were first applied in double-diffused metal-oxide semiconductor (MOS) technologies,[1] U-shaped trenches have been commonly used in semiconductor power devices.[2] These so-called U-shaped MOS field-effect transistors (UMOSFETs) have a lower on-resistance because of their higher channel density. Moreover, the cell package density can be higher than other designs owing to the wide gate channel.[3] Although the UMOSFET possesses many benefits in terms of design and functionality, the insertion of trenches into the structure also introduces some challenges in the formation of the gate oxide. One challenge is caused by the nature of the silicon crystal, wherein the silicon oxidation rate is strongly influenced by the crystal orientation of the silicon surface. In a (100)-oriented wafer, for example, the trench sidewalls can possess various orientations depending on their alignment to the notch; namely, it exhibits a (100) orientation at 45° to the notch, (110) at 90°, and (111) at 54.74°. Owing to the higher density of silicon atoms on the (100) plane, the reaction process with oxygen is slower than that on the (110) or (111) plane. Thus, the thermal oxidation in trenches with unmatched bottom and sidewall orientations will automatically result in nonconformal growth of the silicon oxide.[2]

The trench corner is a particularly problematic region, because the reduced diffusion of oxygen in this region particularly inhibits the growth of silicon oxides. Also, the expansion of silicon during thermal oxidation is not homogenous in trenches with sharp corners, and thus thin areas are created. These effects can cause major deviations from the target thickness of the gate oxide. Studies have shown that the majority of silicon failures can be traced back to these "localized thinnings."[3,4]

The major goal of this work is the deposition of a thick gate oxide (>30 nm) that exhibits uniformity over the entire wafer, conformality in the trenches, and no sign of localized thinning in U-shaped trenches.

II. EXPERIMENT

A. Deposition and thickness measurement

Thick films of silicon oxide were deposited on 200 mm wafers with an orientation of (100), which were pre-etched with U-shaped trenches. As discussed in Sec. I, the wafers were rotated to match the crystal orientations of the trench sidewalls and bottom. The first type of silicon oxide deposition was executed in multiple steps where, first, an initial oxide layer 3–4 nm thick was formed using either wet or dry thermal oxidation or radical oxidation. Radical oxidation is a low-pressure process characterized by the combined injection of hydrogen and oxygen into a rapid thermal processing tool.[5] Second, a thick silicon oxide film was deposited by chemical vapor deposition (CVD) and annealed in a hydrogen/nitrogen environment at 1000–1100 °C, where tetraethyl orthosilicate (TEOS) and oxygen were used as CVD precursors. The thermal oxidation and the annealing processes were performed in a batch furnace. In an alternative approach, a second type of silicon oxide deposition was used where silicon nitride was

Note: This paper is part of the Conference Collection from the 20th Workshop on Dielectrics in Microelectronics Conference.

first deposited by CVD and subsequently transformed to silicon oxide using radical oxidation.

These processes were performed on unstructured surfaces and on surfaces structured with U-shaped trenches. The silicon oxide film thickness on planar wafers and test structures was determined in-line by spectral ellipsometry (KLA-Tencor Corporation). The oxides in the trenches were investigated using cross section samples with scanning electron microscopy (SEM) and transmission electron microscopy on an FEI Tecnai F20. The latter was also used to perform electron energy loss spectroscopy and investigate the elemental composition of the deposited films.

B. Electrical characterization

The leakage and breakdown behavior of the MOSFET structures herein was investigated by measuring the current–voltage (I-V) profile in a constant ramp regime. These measurements were executed on a semiautomatic probe system (PA200, Karl Suss MicroTec) in combination with a semiconductor parameter analyzer (HP4155A, Hewlett-Packard).

A fast, in-line wafer-level reliability test was performed, where the voltage was increased stepwise and then held for a defined time and the leakage current was measured at 5 V. If the current was found to significantly change from one measurement to the next, the last voltage was defined as the breakdown voltage.

In this work, only the electrical characterization of silicon oxides on planar surfaces is discussed. The results are discussed in Sec. III B.

III. RESULTS AND DISCUSSION

A. Multistage deposition of silicon oxide

While thermal oxidation forms the cleanest Si-SiO_2 interface possessing a low-defect density, earlier studies have shown that this technique is not suitable for the deposition of thick gate oxides in trench devices owing to the challenges discussed in Sec. I. Therefore, thermal oxidation was only used herein to form a thin interface, while low-pressure CVD (LPCVD) with TEOS was used to deposit the bulk of the silicon oxide film.

Figures 1(a)–1(d) show the SEM images of the sample cross sections. The LPCVD process, used herein with TEOS, ensures a conformal deposition within the trenches. Here, the trench bottoms [Figs. 1(b) and 1(d)] and sidewalls [Figs. 1(a) and 1(c)] possess the same silicon oxide thickness and the corners exhibit no localized thinning (center-to-edge thickness difference <6%).

The silicon oxide uniformity across the entire wafer, however, was not satisfactory. The silicon oxide center-to-edge thickness difference in the trenches located at the center and at the edge of the wafer was up to 20% (Table I), as illustrated in the two left columns of Fig. 2. It was determined that the combination of a heavy precursor such as TEOS (molecular mass: 208.3 g cm^{-1}) and the selected tools could not simultaneously achieve a good uniformity and conformality. The resulting trade-off between these film characteristics is not acceptable for application in power MOSFETs.

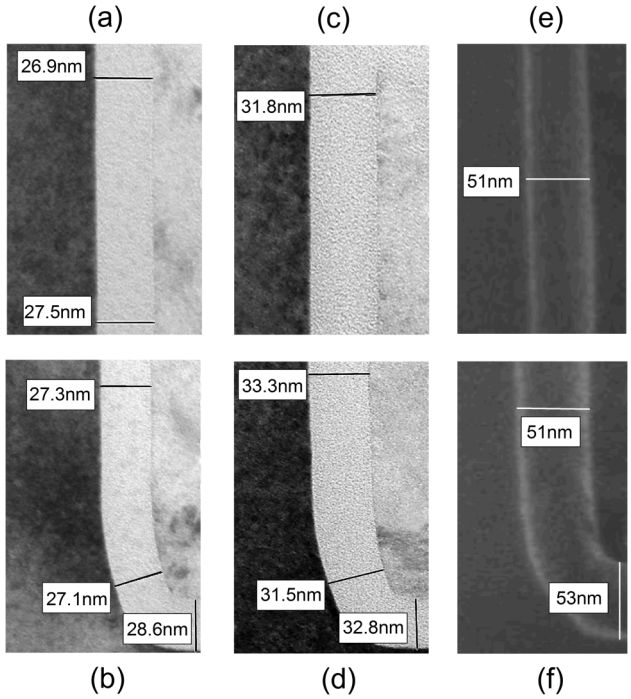

FIG. 1. Scanning and transmission electron microscope images of the cross section of the trench [(a), (c), and (e)] sidewalls and [(b), (d), and (f)] bottom corners deposited with silicon oxide via various processes: [(a) and (b)] 3 nm-thick radical oxide +33 nm-thick LPCVD oxide; [(c) and (d)] 4 nm-thick wet thermal oxide +33 nm-thick LPCVD oxide; and [(e) and (f)] 52 nm-thick reoxidizied nitride produced via sequential deposition and radical oxidation of silicon nitride. All cross section images were obtained from the wafer center.

Therefore, the second silicon oxide deposition process was applied using the sequential deposition and oxidation of silicon nitride referred to as the reoxidized nitride process (REOX). The nitride is conformally deposited into the trenches, and the subsequent oxidation uniformly transforms it into silicon oxide owing to the lack of a crystal structure in the deposited silicon nitride film. With a center-to-edge thickness difference of only 2%–6%, the REOX nitride film exhibits a much better uniformity than films deposited with TEOS LPCVD with a comparable conformality.

During this reaction, the film thickness expands by 67% as determined by Eq. (2),[6] where N is the molecular density in mol/cm^3, d is the film thickness, ρ is the film density, and

TABLE I. Thickness and electrical breakdown of various oxide films from Fig. 4.

	Species	Thickness (nm)	Electrical breakdown (V)
4(a)	50 nm TEOS (no anneal)	45.5	42.1
4(b)	4 nm wet oxide + 50 nm TEOS (no anneal)	48	45.2
4(c)	5 nm dry oxide + 50 nm TEOS (no anneal)	48.5	46.2
4(d)	4 nm wet oxide + 50 nm TEOS (anneal)	48	47.7
4(e)	5 nm dry oxide + 50 nm TEOS (anneal)	48.5	49.2
4(f)	13 nm REOX + 40 nm TEOS (anneal)	53.5	54.3

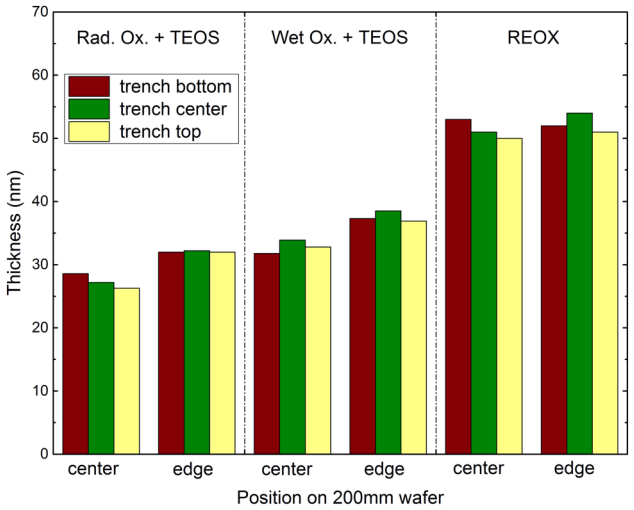

FIG. 2. Comparison of the silicon oxide thickness uniformity over the wafer and the conformality within a trench for three silicon oxide-forming combination processes: (left column) 3 nm-thick radical oxide + TEOS LPCVD, (center column) 4 nm-thick wet thermal oxide + TEOS LPCVD, and (right column) silicon nitride LPCVD + REOX.

M is the molar mass. The parameter indices Si for silicon, N for nitrogen, SiO_2 for silicon dioxide, and Si_3N_4 for silicon nitride indicate the material for which the respective parameter is valid as follows:

$$\frac{d_{SiO_2}}{d_{Si_3N_4}} = \frac{N_{SiO_2}}{N_{Si_3N_4}} = \frac{\left(M_{Si} + \frac{4}{3}M_N\right) \cdot \rho_{SiO_2}}{(M_{Si} + 2M_O) \cdot \rho_{Si_3N_4}}, \quad (1)$$

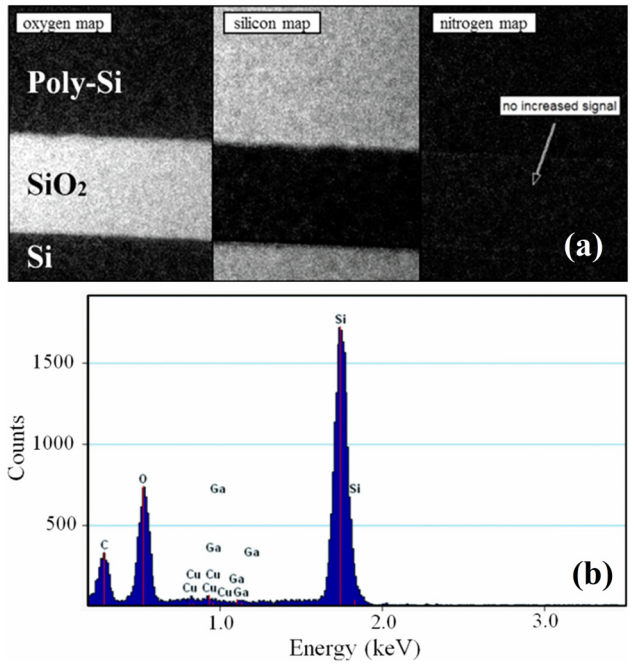

FIG. 3. (a) Electron energy loss spectra-obtained elemental maps acquired in a scanning transmission electron microscope shows the distribution of oxygen (left), silicon (center), and nitrogen (right) in the gate stack formed by radical oxidation of silicon nitride. (b) Energy dispersive x-ray spectra of the silicon oxide film in the same stack as (a).

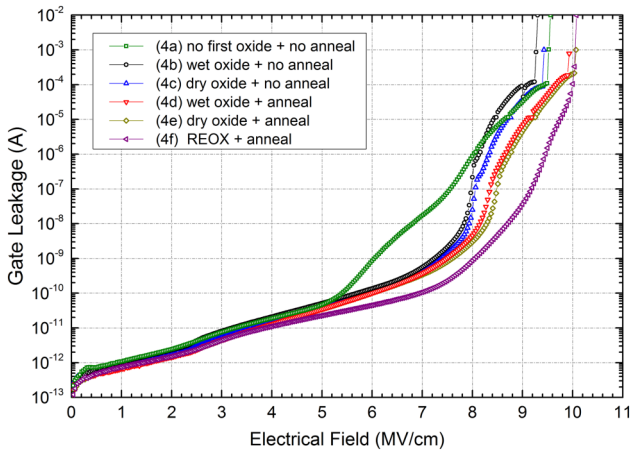

FIG. 4. Influence of the initial oxide and post-treatment on the leakage current in the gate stack as a function of electric field (up to 10 MV/cm).

$$d_{SiO_2} = \frac{\left(M_{Si} + \frac{4}{3}M_N\right) \cdot \rho_{SiO_2}}{(M_{Si} + 2M_O) \cdot \rho_{Si_3N_4}} \cdot d_{Si_3N_4} \approx 1.67 \cdot d_{Si_3N_4}. \quad (2)$$

Electron energy loss spectroscopy of the deposited stack confirmed that the silicon nitride fully reacted with the hydrogen and oxygen radicals [Fig. 3(a)], and no significant amount of silicon nitride was detected in elemental maps of the stack. Additionally, energy dispersive x-ray spectroscopy of the silicon oxide film revealed that the K_α peak of oxygen at 0.525 keV was present, but no nitrogen peak at 0.392 keV was detected [Fig. 3(b)].

B. Electrical characterization

The focus of this work is the formation of silicon oxide in gate trenches, and thus the main concern is the behavior of these films as an insulating material. The conduction mechanism in thick oxides at high electric fields, such as those presented in this work, can be Fowler–Nordheim tunneling.[7] This was investigated by using I-V measurements to determine the leakage current and electrical breakdown of the films.

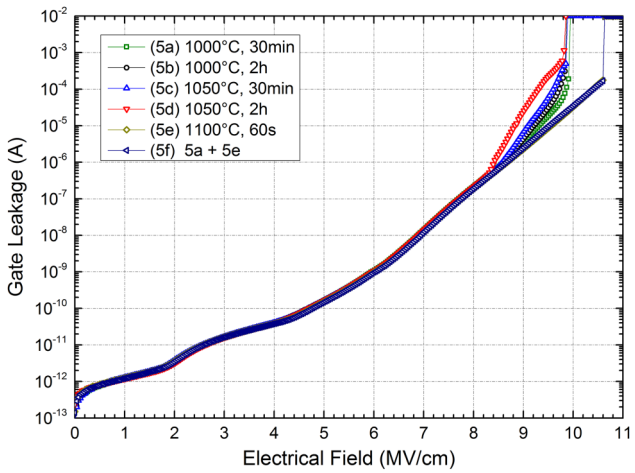

FIG. 5. Influence of various thermal treatments on the leakage current and electrical breakdown of silicon oxide deposited with LPCVD.

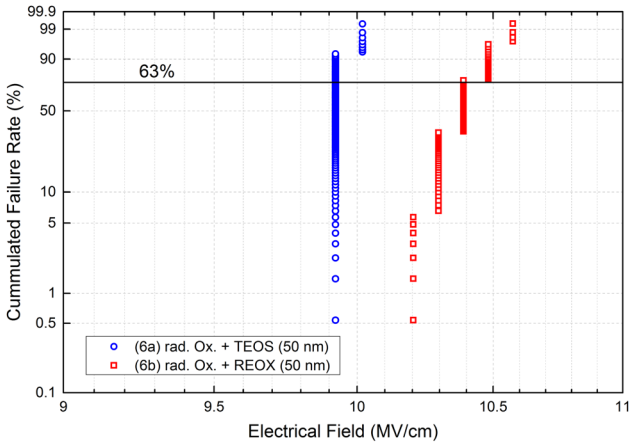

FIG. 6. Distribution of the breakdown voltage of silicon oxide films deposited by LPCVD and by the reoxidation of nitride measured using a fast wafer-level reliability technique.

First, we studied the influence that the initial oxide representing the interface had on the electrical stability of the film. Figure 4 confirms that an initial oxide is necessary, where a film deposited with no initial oxide exhibits the highest leakage at electric fields above 5 MV/cm. If a device with this oxide was operated at such high electric fields, the increased charge injection would form conductive channels in the oxide that will eventually lead to a hard breakdown.[8] It is assumed that the presence of an interface oxide can partially block the leakage.

The REOX nitride film exhibits the best insulating behavior, with a breakdown voltage comparable with the other annealed films and a leakage current that is much lower.

The LPCVD process using TEOS creates silicon oxide with a wide meshed structure containing many precursor contaminations such as hydrogen and carbon, which can be improved using a thermal annealing treatment. Figure 4 shows that the TEOS oxides without postannealing exhibited electrical breakdown at lower electric fields (9.0–9.5 MV/cm) than the annealed oxides (10 MV/cm). Therefore, various annealing recipes using the same forming gas environment were investigated. It was found that breakdown does not change for various furnace treatments, and all occur at 9.8 MV/cm. In fact, the treatment with the highest thermal budget only resulted in a higher leakage current at electric fields above 8 MV/cm. However, the rapid thermal anneals [data labeled 5(e) and 5(f) in Fig. 5] increased the electrical breakdown fields to 10.5 MV/cm.

Finally, the reliabilities of oxide films deposited by LPCVD using TEOS and by the reoxidation of silicon nitride were compared. For this, fast wafer-level reliability measurements were obtained for the films and the results are presented in a Weibull plot (Fig. 6). While most of the oxides deposited by TEOS LPCVD broke down at 9.9 MV/cm, the oxides deposited by the REOX process lasted until 10.4 MV/cm (63% line). It should also be noted that the deviation of the oxide breakdown is much higher for the REOX oxides.

IV. SUMMARY AND CONCLUSIONS

A new process of forming thick silicon oxide films in trench structures was investigated and compared to the common procedure of depositing the oxides by CVD. The new process includes the repeated process of silicon nitride deposition and radical oxidization to produce conformal and uniform films of silicon oxide. The CVD-grown films exhibited a trade-off between the film uniformity over a 200 mm wafer and the film conformality in the trenches.

The I-V characteristics showed that the reoxidized nitride breaks down at 10 MV/cm, which is comparable to the best films grown by CVD, while its gate leakage at electric fields above 5 MV/cm is much lower. For the CVD-deposited films, a thermal annealing treatment was necessary to reduce defects inside the oxide, where the best electrical behavior was shown for films treated with a rapid thermal annealing process at 1100 °C.

The fast wafer-level reliability results also favor the reoxidized nitride process over the CVD. Films formed by reoxidizing silicon nitride broke down at voltages that were 4.5 V higher than those formed by LPCVD.

Thus, combining the deposition of silicon nitride with a radical oxidation process successfully formed a thick film of silicon oxide in trench structures. Electrical characterization showed that the leakage current and electrical breakdown of these films make them a suitable choice for application in a power MOSFET.

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