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Accumulative Polarization Reversal in Nanoscale Ferroelectric Transistors

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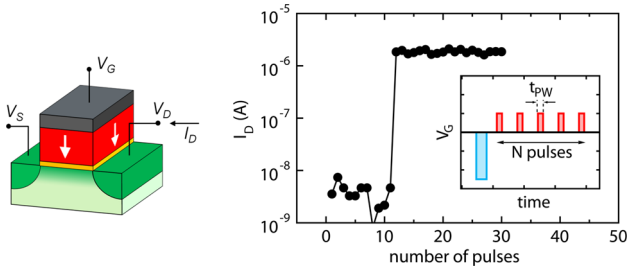
ABSTRACT: The electric field driven and reversible polarization switching in ferroelectric materials provides a promising approach for nonvolatile information storage. With the advent of ferroelectricity in hafnium oxide, it has become possible to fabricate ultrathin ferroelectric films suitable for nanoscale electronic devices. Among them, ferroelectric field effect transistors (FeFETs) emerge as attractive memory elements. While the binary switching between the two logic states, accomplished through a single voltage pulse, is mainly being investigated in FeFETs, additional and unusual switching mechanisms remain largely unexplored. In this work, we report the natural property of ferroelectric hafnium oxide, embedded within a nanoscale FeFET, to accumulate electrical excitation, followed by a sudden and complete switching. The accumulation is attributed to the progressive polarization reversal through localized ferroelectric nucleation. The electrical experiments reveal a strong field and time dependence of the phenomenon. These results not only offer novel insights that could prove critical for memory applications but also might inspire to exploit FeFETs for unconventional computing.



KEYWORDS: *ferroelectric field effect transistor (FeFET), ferroelectric switching, accumulative switching, hafnium oxide, ferroelectric memory*

1. INTRODUCTION

Achieving high density and low power nonvolatile data storage with conventional charge based memories has become a challenging task. New memory materials and concepts are currently being explored to overcome this issue.[1] Ferroelectric switching provides a promising approach in this regard.[2] Ferroelectric materials are characterized by their intrinsic lattice polarization *P*, which can be reversed through the application of an external electric field that is larger than a certain critical value (coercive field). The switching is generally reversible and gives rise to two distinct polarization states, which can be employed to store binary information. This purely electric field driven process represents an important advantage with respect to other emerging memory concepts.[3]

Among ferroelectric devices, the ferroelectric field effect transistor (FeFET) attracts strong interest due to its simple structure (one transistor memory cell), low programing voltage,[4] and fast switching.[5] Typically, the FeFET has the structure of a conventional metal oxide semiconductor field effect transistor, whose gate dielectric comprises a ferroelectric material[6] or a stack of dielectrics with one ferroelectric layer.[7] In this way, the direction of the stored polarization in the ferroelectric influences the electronic transport in the semiconductor and, hence, the value of the drain current of the transistor. The sensing of the drain current levels, used to define two logic states, is performed without disturbing the polarization, thus making the read out nondestructive. Besides the commonly used transistor channel semiconductors (e.g., silicon or germanium), alternative material systems, including two dimensional (2D) materials and strongly correlated oxides, can be employed as well, potentially offering new operation principles and device structures.[8]

Despite a long history of the FeFET device,[6] it is only the recent advent of ferroelectricity in hafnium oxide (HfO_2)[9] that has opened an unprecedented path to FeFET fabrication at the nanoscale.[10] This is primarily due to the possibility to deposit ultrathin ferroelectric HfO_2 films (<10 nm), while also being compatible with standard integration processes in the microelectronics industry.[10,11] Such an advantageous feature has rapidly allowed for demonstrating first large memory arrays fully integrated with logic transistors.[5,12] At the same time, new HfO_2 based FeFET structures, employing 2D transition metal dichalcogenides as the channel material, are being investigated for memory applications and beyond.[13,14] However, to achieve a reliable memory operation, a detailed understanding of switching processes in the scaled devices is mandatory. The recently reported novel switching phenomena, such as the abrupt and stochastic polarization reversal,[4,15] testify to the richness of electrical behaviors the FeFETs may offer. In this work, we reveal the intrinsic property of ferroelectric HfO_2,

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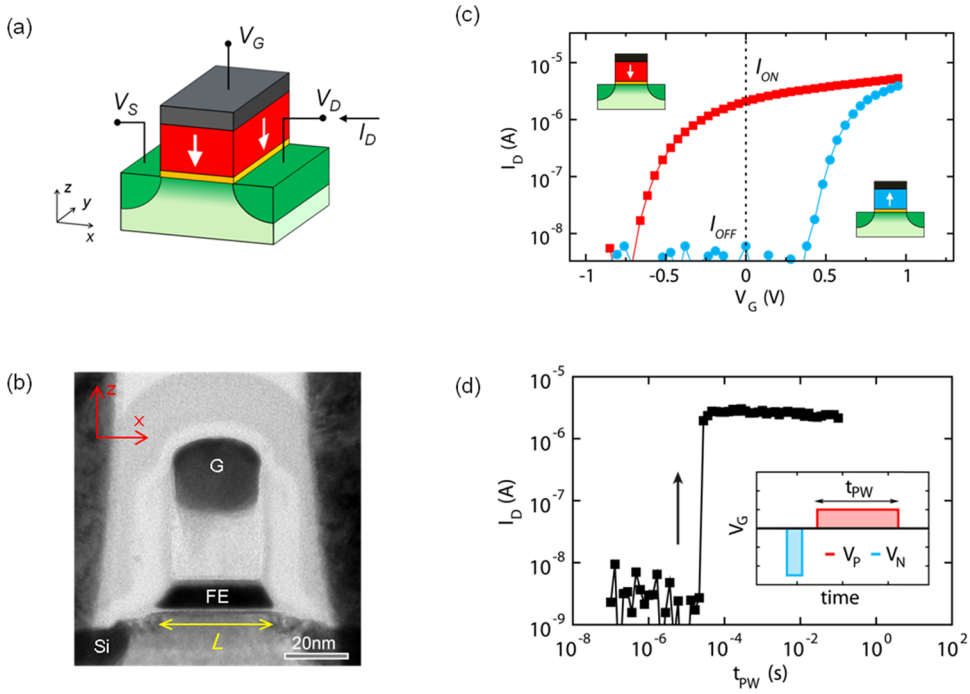

Figure 1. Structure and switching behavior of a nanoscale ferroelectric transistor. (a) Sketch of a FeFET: the ferroelectric HfO_2 film (red) is indicated by a downward pointing ferroelectric polarization and is placed within the transistor gate stack between the top gate electrode (TiN, gray) and a thin interfacial dielectric layer (SiON, yellow). V_G, V_D, and V_S indicate gate, drain, and source voltages, respectively, whereas I_D is the drain current. (b) TEM image of a device having the channel length L = 30 nm, taken along the x−z plane, indicated in (a). "G", "FE", and "Si" indicate gate contact, the ferroelectric layer, and the silicon substrate, respectively. (c) Influence of the ferroelectric polarization on the drain current: when the polarization points downward (achieved when the positive gate pulse is larger than the positive coercive voltage), electrons from the semiconductor substrate are accumulated to form the transistor channel and screen the polarization positive charge. This results in a low threshold voltage of the transistor (red I_D−V_G curve) and high conductive (ON) state at V_G = 0 V (along the vertical dashed line). When the polarization points upward (achieved when the negative gate pulse is larger in magnitude than the negative coercive voltage), the electrons are depleted from the semiconductor, inducing a high threshold voltage (blue I_D−V_G curve) and low conductive (OFF) state at V_G = 0 V. The two states are separated by orders of magnitude in current. (d) Abrupt switching of nanoscale FeFETs (W = 80 nm, L = 30 nm) in terms of a drain current I_D extracted at V_G = 0 V (as indicated in (c)) upon the gate excitation (shown in the inset): the negative gate pulse V_N = −4 V sets the starting OFF state. Then, a positive pulse having V_P = 2.2 V and a pulse width t_{PW} attempts the switching to the ON state. The sequence is repeated for increasing t_{PW}, resulting in a sharp switching at $t_{PW} \approx 15$ μs.

integrated within a nanoscale FeFET, to accumulate electrical stimuli, followed by a sudden and complete switching. This behavior contrasts the typical binary operation mode, where only one pulse is needed to accomplish switching. We attribute this integration effect of voltage pulses to the progressive polarization reversal through localized ferroelectric nucleation. Moreover, we use electrical characterization to study its specific field−time dependence and to assess the inherent stochasticity. The results provide important insights regarding the sensitivity of FeFETs to disturbs, which could limit their performance in memory arrays. On the other hand, they might inspire exploiting the accumulation property for unconven tional computing, thereby making FeFETs as building blocks for normally off logic and neuromorphic circuits.

2. RESULTS AND DISCUSSION

The ferroelectric transistors used in this study have the gate stack grown on a single crystal p doped silicon (100) substrate, which consists of the dielectric (interface) layer (1.2 nm silicon oxynitride SiON), ferroelectric layer (10 nm silicon doped HfO_2), and top gate electrode (TiN and polysilicon) (see Experimental Section and refs 4 and 16). The HfO_2 film was polycrystalline after annealing. The gate electrode patterning defined the lateral (that is, parallel to gate electrode surface) dimensions of 30 nm and 80 nm for the length and width of the transistor, respectively. A schematic illustration of the device and the transmission electron microscopy (TEM) image of its cross section are shown in Figure 1a,b.

To measure the ferroelectric properties of the transistors, the electrical excitations are applied to the gate electrode, after which the transfer characteristics are determined to assess the ferroelectric polarization state. Figure 1c shows the results obtained for two gate pulse (V_G) polarities. Upon a positive pulse, for which the voltage drop across the ferroelectric exceeds its coercive voltage V_C, the electric field orients the ferroelectric polarization toward the SiON, whereas a negative pulse orients it toward the metallic gate electrode. By means of the Coulomb coupling, the spontaneous polarization of the ferroelectric induces a charge in the semiconductor, thus modulating the conductivity of the transistor channel. Polarization down (up) then corresponds to high (low) electron concentration in the transistor channel, which can be assessed by sensing the drain current (I_D) level at a proper gate voltage (e.g., V_G = 0 V in Figure 1c). Therefore, the results in Figure 1c suggest a proper ferroelectric switching in our devices. Unlike ferroelectric capacitors or ferroelectric tunnel junctions, ferroelectric transistors present a separation between the two polarization states of several orders of magnitude in the drain current, which is due to the inherent gain of the transistor. This prominent attribute not only makes ferro

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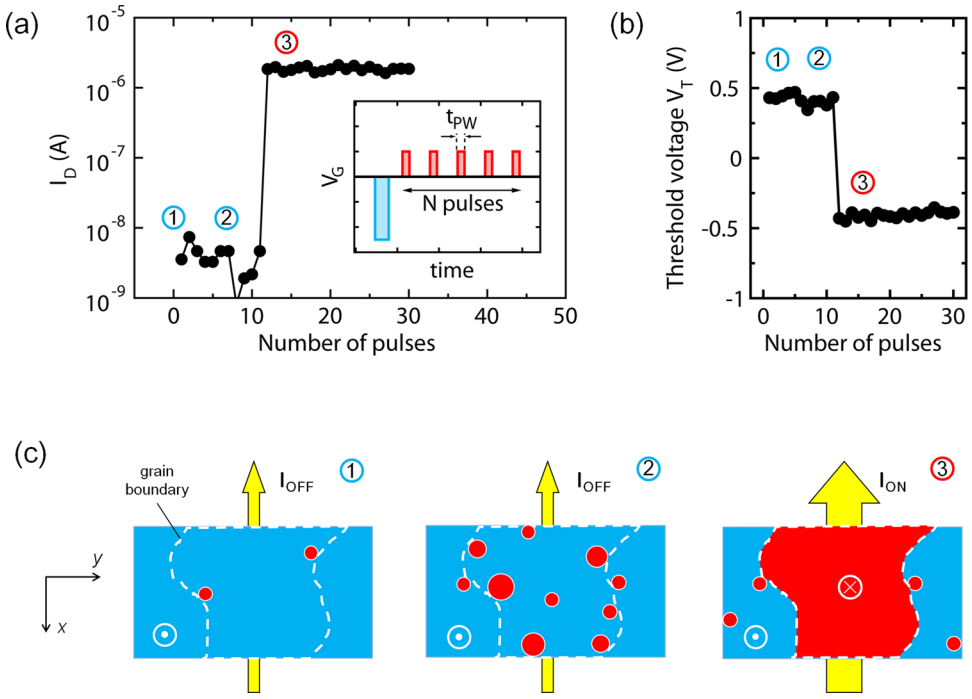

Figure 2. Accumulative polarization reversal in ferroelectric transistors. (a) Sharp switching from OFF to ON after a number of received identical pulses (V_P = 2.2 V, t_{PW} = 1 μs), as depicted in the inset. A single pulse is not sufficient to reverse the polarization, as evident from Figure 1d. The time distance between single pulses is Δt = 100 ns. The accumulative behavior is invariant with respect to Δt (see Supporting Information Figure S2); (b) the threshold voltage V_T was extracted at the drain current level I_D = 0.1 μA W/L. (c) Schematic illustration of the top down view of the ferroelectric film (plane x−y of Figure 1a) showing the formation of reverse ferroelectric domains starting from OFF state (polarization up ⊙, blue coloring). Three stages illustrate the domain evolution with increasing N as indicated in (a): (1) onset of the nucleation of the domains having polarization down (⊗) (red coloring); (2) further nucleation and domain growth upon increasing the number of pulses prior to switching; (3) polarization reversal within the entire grain between drain and source regions after a critical number of received pulses, which causes a sharp increase of the drain current (I_{ON}).

electric transistors appealing for applications but also facilitates fundamental studies of the polarization reversal processes at the nanoscale.

The ferroelectric switching in our devices, where the ferroelectric film is spatially very confined, is extremely sharp both in the time and voltage domains (see the Supporting Information Figure S1). In fact, when we apply positive gate pulses $V_G = V_P$ = 2.2 V with increasing pulse width t_{PW} (inset Figure 1d) from 100 ns to 100 ms to a transistor in the OFF state, an abrupt increase of the drain current at around t_{PW} = 15 μs is observed. Note that the relaxed pulsing time ($t_{PW} \geq$ 100 ns) was chosen to avoid extrinsic RC constant delays, originating from the test structure design[17] and unintentional voltage overshoots at the gate terminal (caused by too steep gate voltage pulse edges in combination with imbalanced impedance matching in the adopted test structures) and, hence, to ensure reliable results using the standard measurement equipment and single device structures. However, in a FeFET based integrated circuit, the switching time can be substantially reduced to the nanosecond range, as demonstrated recently.[5] Indeed, as reported in our previous work,[4] larger (lower) V_P amplitudes would result in exponentially shorter (longer) switching times, whereas the switching remains abrupt in its nature.

Furthermore, it is clear from this experiment that switching under a single pulse having t_{PW} shorter than 10 μs is precluded for V_P = 2.2 V. Interestingly, when we consecutively apply several shorter pulses, each of which is insufficient for switching (e.g., V_P = 2.2 V, t_{PW} = 1 μs; inset Figure 2a), the switching eventually takes place after a certain critical number of delivered pulses (Figure 2a). This unexpected phenomenon clearly points to a sort of accumulative polarization reversal within the ferroelectric. We argue that this occurs, most probably, through the successive formation of ferroelectric nuclei (nanodomains) with an opposite polarization orientation, which gain in their quantity and size with increasing number of electrical pulses, as schematically depicted in Figure 2c. The nuclei formation might be preferentially initiated at the defect sites,[18,19] i.e., grain boundaries (because of the polycrystalline film) and the bottom and top interfaces of the ferroelectric. Following this interpretation, the succession of gate pulses will generate nanodomains up to a critical point, at which the polarization reversal of the entire grain occurs. Consequently, this creates a uniform polarization pathway between the source and drain regions, which turns the device on. This peculiar feature of accumulation of electrical stimuli through ferroelectric nucleation can be viewed as energy accumulation within the material. To some extent, this represents an analogy to the accumulative crystallization found in phase change materials upon multiple optical[20] or electrical excitations.[21,22] Moreover, this switching mechanism contrasts the traditional binary memory operation mode, where a FeFET cell is deterministically switched using a single pulse.

It should be noted that the transition from OFF to ON state is evident only after all necessary pulses to switch are delivered to the device. This all or none behavior can be further appreciated in Figure 2b, which illustrates the evolution of

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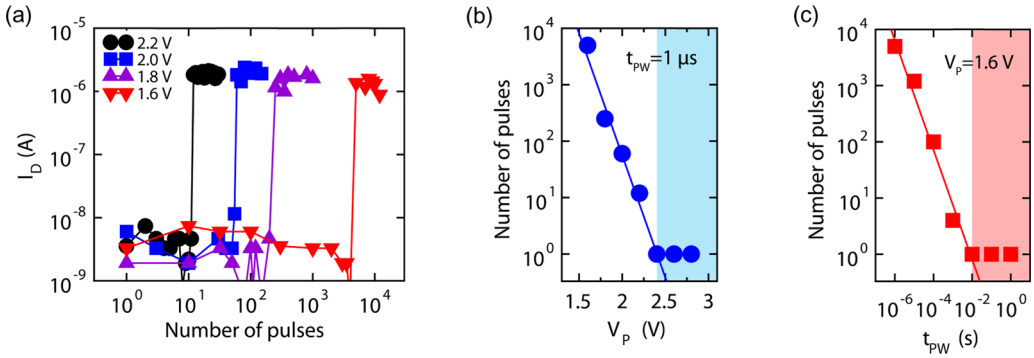

Figure 3. Dynamics of the accumulative switching. (a) Impact of gate pulse amplitude V_P: lower V_P induces a slower domain nucleation and a higher number of pulses is necessary for switching. The abrupt change in the drain current upon switching is independent of the strength or duration of the individual incoming spikes, but occurs only after all necessary pulses are delivered (all or none behavior). (b) Number of pulses to switch as a function of V_P while keeping t_{PW} = 1 μs and (c) as a function of t_{PW} while keeping V_P = 1.6 V. The shaded area represents the range of V_P (b) and t_{PW} (c) values, where the switching occurs deterministically under a single pulse, i.e., accumulative switching is absent.

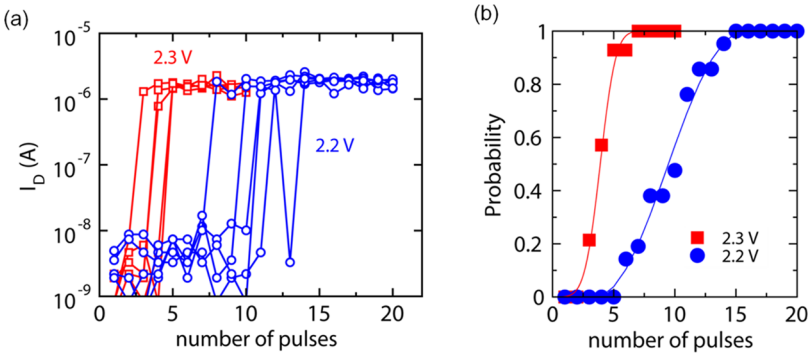

Figure 4. Stochastic accumulative switching. (a) Polarization reversal in nanoscale ferroelectric transistors is a stochastic process due to a probabilistic nucleation mechanism. This leads to a variation of the number of pulses to switch, even if the experiment of Figure 2a is repeated with an identical set of parameters. Five switching curves for each of the two values of V_P are shown. (b) Probability of switching vs a number of received pulses obtained by repeating 20 times the experiment of Figure 2a for each V_P. The solid lines are only guide to the eye.

the threshold voltage V_T with the increasing number of excitation pulses. The V_T level remains almost invariant over the first 11 pulses. Then, the 12th pulse abruptly lowers the V_T level to a value that does not change upon additional pulses. The fact that no intermediate V_T states are elicited by the incoming electrical pulses drastically distinguishes these small area ferroelectric transistors from the large area ones. In fact, the latter ones display a gradual polarization switching, which corresponds to a continuum of states between the nominal high V_T and low V_T states,[23,24] and could be potentially exploited for the multilevel information storage.

Note that the accumulation property presented here does not decay over time. In fact, the number of pulses necessary to switch does not considerably change upon increasing the pulse interarrival time from 100 ns to 1 s (see Supporting Information Figure S2). This is due to the nonvolatile nature of our devices.

To investigate the accumulation property of our devices under diverse pulse parameters, we performed the experiment (in Figure 2a) by changing V_P and t_{PW}. As expected from the theory of ferroelectric nucleation,[25,26] and confirmed by our previous reports for hafnium oxide,[4,27] the switching is both time and field dependent. This implies that longer excitation pulses and/or higher pulse amplitudes will favor switching. In fact, Figure 3 fully confirms this behavior: when increasing V_P from 1.6 to 2.2 V, while keeping t_{PW} = 1 μs, the number of pulses to switch decreases exponentially from more than 5000 to only 12. A further increase in the pulse amplitude beyond 2.4 V makes the device exit the accumulation mode and enter the binary operation mode (shaded area in Figure 3b), where a single pulse is sufficient for complete switching. Figure 3c shows that by increasing the excitation pulse width, while keeping V_P constant, the number of pulses to switch decreases almost linearly in the log−log graph. These experiments indicate that we can tailor the number of pulses to switch by appropriate choice of the amplitude and duration of pulses. Moreover, note that the all or none switching behavior is preserved regardless of the number of pulses and pulse parameters applied (Figure 3a).

Figure 4 reveals an additional property of the accumulative switching in FeFETs. When the experiment of Figure 2a is repeated several times with the unchanged set of parameters, the number of pulses to switch experiences a certain spread of values. This can be understood by considering that the ferroelectric nucleation is inherently a stochastic process. In fact, by studying the nucleation and domain wall growth in $PbTiO_3$ perovskite ferroelectrics by means of molecular dynamics simulations, it was found that nucleation behaves as a Poisson process.[28] Recently, a similar statistical evidence has been experimentally confirmed for our devices as well.[4]

Although the accumulative switching property in FeFETs described in this work represents an attractive feature, it poses constraints when it comes to the memory operation. In fact, to obtain high storage densities and compete with existing or

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emerging memory concepts, FeFETs are usually organized in memory array architectures (e.g., NAND[29] or AND arrays[5,12]), where many devices share the same gate line. If one device in a row (selected device) is being programmed, all other devices sharing the gate line (unselected devices) will experience a certain excitation. Although the impact of such disturb pulses is largely reduced by proper inhibit schemes[30] (for instance, by applying a certain voltage at the source and drain terminals to lower the overall voltage drop across the unselected gate stacks), a fraction of the total programing amplitude will, however, be delivered to unselected devices. Consequently, upon repeated programing cycles on the same gate line and due to the accumulation property, these devices could finally undergo an undesired switching. This needs to be taken into account upon analyzing the disturb effects in dense FeFET memory arrays.

On the other hand, the FeFET in the accumulation operating mode could be seen as a perfect integrator (accumulator). In fact, as the accumulated ferroelectric nuclei do not decay over time (i.e., the leakage effect is absent on typical time scales of computing operations), it counts (integrates) the incoming voltage pulses and emits a drain current spike when a certain pulse count is reached. Thus, a FeFET might be exploited as a building block in electronic circuits performing nonvolatile (normally off) arithmetic[21] or logic[31] computations, which could represent an alternative to the conventional and volatile complementary metal oxide semiconductor logic.

Moreover, the integration of incoming spikes and the subsequent drain current firing show a certain resemblance to the integrate and fire operation of a biological neuron.[32] In combination with a proper circuital environment, capable of supporting a FeFET in mimicking the basic neuronal behavior, this could open a route for exploiting this device in neuromorphic computing.

3. CONCLUSIONS

In summary, we presented the accumulative switching property of ferroelectric HfO_2 embedded within a nanoscale FeFET device. It manifests in the way that the device undergoes a complete and abrupt switching upon a train of identical incident gate voltage pulses, each of which is insufficient for switching. We attributed the phenomenon to a progressive nucleation of ferroelectric domains, which gain in their size and quantity with increasing the number of incoming pulses. Such behavior is strongly time and voltage dependent and exhibits an inherent stochasticity. The results provide important guidelines regarding the voltage disturbs in FeFETs organized in memory array architectures, where such an accumulation of disturbs must be limited to avoid undesired switching of unselected cells. On the other hand, the integration effect might open a path for exploiting the FeFET as a building block for normally off logic circuits and integrate and fire artificial neurons.

4. EXPERIMENTAL SECTION

4.1. Device Fabrication. HfO_2 based metal−ferroelectric−insulator−semiconductor field effect transistors feature a TiN/Si:HfO_2/SiON/Si gate stack fabricated in the following way: first, a 1.2 nm thick interfacial nitrided SiO_2 layer (SiON) was grown on the p doped silicon substrate, followed by a deposition of 10 nm Si:HfO_2 layer grown from $HfCl_4$ and $SiCl_4$ in a water based atomic layer deposition process at 300 °C. At this step, a 4 mol % of silicon doping was introduced to induce the ferroelectric orthorhombic phase in the film after annealing. The metal gate electrode was obtained by physical vapor deposition of TiN, which was consequently contacted with polysilicon (Figure 1b). A two step lithographic process then defined the lateral dimensions: width, 80 nm; length, 30 nm. The source and drain n^+ regions were obtained by phosphorous ion implantation, which were then activated by a rapid thermal annealing at around 1000 °C. This resulted in a polycrystalline Si:HfO_2 ferroelectric layer as well.

4.2. Electrical Characterization. All measurements were performed in a voltage pulsed approach, not to stress the device and to avoid the parasitic charge trapping. The characterization was performed with a Keithley 4200 SCS semiconductor analyzer; 4225 pulse measurement units were adopted for voltage pulsing and fast I_D−V_G characterization. The minimum pulse width that can be reliably applied to devices was 100 ns, which is the limitation of the measurement setup. I_D−V_G curves were obtained by applying a gate voltage sweep in the range from −1 to 1 V with the total sweep duration of 500 μs. Drain voltage was kept at 100 mV. Such a fast measurement limits the drain current resolution to 10 nA. The gate leakage was negligible (I_G < 2 pA) for all V_G values adopted in the manuscript.

■ ASSOCIATED CONTENT

Additional data concerning the abrupt switching and its time−voltage dependence in FeFETs as well as the dependence of the accumulative switching on the interarrival times of single electrical stimuli (PDF)

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Notes The authors declare no competing financial interest.

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