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# Reconfigurable Si Nanowire Nonvolatile Transistors

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**Reconfigurable transistors merge unipolar p- and n-type characteristics of field-effect transistors into a single programmable device. Combinational circuits have shown benefits in area and power consumption by fine-grain reconfiguration of complete logic blocks at runtime. To complement this volatile programming technology, a proof of concept for individually addressable reconfigurable nonvolatile transistors is presented. A charge-trapping stack is incorporated, and four distinct and stable states in a single device are demonstrated.**

## 1. Introduction

Future integrated circuit (IC) architectures will demand an ultradense integration of logic and memory with fine-grained connectivity to enhance performance.[1] In conventional logic circuits, the Boolean function is fixed by the original circuit design. Electrically programmable functions can be customized either in a coarse- or fine-grain approach. In the former, the signals are routed to predefined logic blocks as practiced in field programmable gate arrays. In the latter approach, reconfiguration on the function of the elementary building blocks in the circuit gives rise to distinct functions after manufacturing and even at runtime. With the rise of novel nanoelectronic devices, with the inherent property to alter switching mechanisms, the fine-grain path is enabled. For instance, as occurs in memristive circuits.[2,3] The fine-grain reconfiguration approaches aim at the reduction of routing-related delays and chip area reduction. A very interesting fine-grain approach that emerged during the last decade is based on polarity programmable or reconfigurable field-effect transistors (RFETs). RFETs have been highlighted due to their novel functionality providing both n-type and p-type field-effect transistor (FET) function in a single device selected simply by an electric signal.[4–9] Up to date, reconfigurable transistors have been limited to dynamic programming on the function, i.e., a constant program signal needs to be applied to maintain the required function.

However, a nonvolatile component that can be embedded into these reconfigurable logic devices would not only eliminate the requirement of having the configuration voltage applied continuously but would also bring additional advantages in terms of multivalent memory operation and close proximity between memory and logic. A number of demonstrations of nanowire-based nonvolatile memory cells have been reported in literature.[10–12] In these realizations, the channel polarity of the memory cell is determined by the doping type of silicon. First demonstrators of nonvolatile reconfigurable device operation were shown with the use of a common back gate electrode;[13] in the work by Schwalke et al., the charge trapping is performed using the buried oxide while a high voltage is applied to the global back gate. With this approach, it is difficult to individually address the desired device and to perform other operations in the chip, while writing/erasing some of the devices. Recently, a poly-Si reconfigurable device with a bottom gate array was also demonstrated and showed nonvolatile functionality.[14]

In this work, the first demonstration of individually addressable nonvolatile RFETs based on bottom-up grown Si nanowire is presented. **Figure 1** shows a schematic design and a cross-sectional transmission electron micrograph (TEM) image of the fabricated and measured device. We make use of charge trapping in the gate stack of a dedicated gate electrode. As a vehicle to verify our proof of principle, we integrated the technologically lean charge trapping metal–nitride-oxide–silicon (MNOS) gate stack. The validity of the MNOS stack for nonvolatile charge storage, in general, is well accepted in the memory community.[15,16] For simplicity, in demonstrating the concept, we use a rather thick $Si_3N_4$ layer of 15 nm and omit the use of a top blocking oxide. In this configuration, the top part of the thick trapping layer has the same electrostatic function as the blocking oxide in the silicon-oxide–nitride-oxide–silicon

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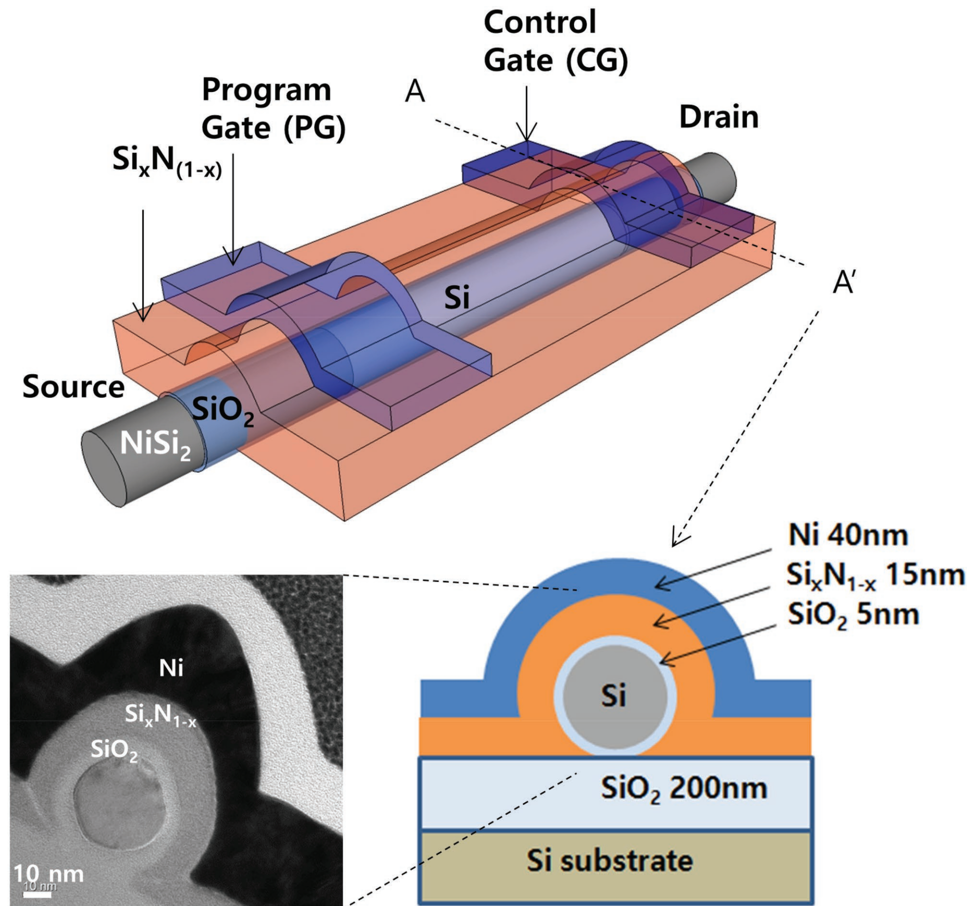


**Figure 1.** Schematic of the Si nanowire reconfigurable nonvolatile transistor. The upper drawing shows a top view and the lower a cross-sectional view along the line (A–A′) together with a TEM image of the cross-section of the transistor.

(SONOS), and therefore it enables a reasonable large memory window. However, a real blocking oxide needs to be added when optimizing the performance of the retention and erase behavior of the device.[17] We, nevertheless, note that our concept is extendable to more complex charge trapping stacks as employed in the newest memory production technologies, such as SONOS or stacks with high-*k* dielectrics and high work function electrodes like tantalumnitride–aluminiumoxide–nitride–silicon stack[17] to reduce write and erase program voltages and to improve the retention. However, to make the MNOS stack suitable for our reconfigurable approach, we apply an omega-gate geometry with a silicon nanowire channel, as this enhances the gate program electric fields at the semiconductor–oxide interface improving the programming/erasing behavior. In addition, silicon nanowires are chosen as abrupt, flat, and reproducible silicide-to-silicon junctions can be formed in them.

## 2. Results and Discussion

In order to illustrate the physical polarity control mechanism in RFETs with two independent gates, we also fabricated Schottky barrier FET with a single gate design as control devices on the same substrate. The gate electrode of the control devices is separated from the source/drain (S/D) contact leads by 200 nm and was designed to overlap the intruded $NiSi_2$–Si junctions. In **Figure 2** (inset), the optical microscopic top view for three Schottky barrier transistors fabricated on a single Si nanowire are shown. The energy bands of silicon are bent upward when negative bias is applied to the gate. Thinned Schottky barriers between both source and drain to the channel valence band result in a high injection of holes. At the same time, an increased blocking energy barrier for the electron injection occurs. In contrast, positive gate bias makes electron injection through the thinned Schottky junctions possible while blocking hole injection. Consequentially, the transfer curve of the single gate Schottky barrier FET exhibits an ambipolar characteristic since hole injection through the Schottky barrier is dominant for negative gate bias and electron injection is dominant for positive gate bias as shown in the top graph of Figure 2. The asymmetric transfer characteristic indicates superior hole conduction compared to electron conduction because the $NiSi_2$–Si contact has a lower Schottky barrier for hole injection (≈0.46 eV) than for electron injection (≈0.66 eV).[4] The transfer characteristics also confirmed that the device with silicon nitride layer works properly as a Schottky barrier transistor. The subthreshold swing is extracted to be ≈300 mV $dec^{-1}$ and the on/off ratio is $10^6$.



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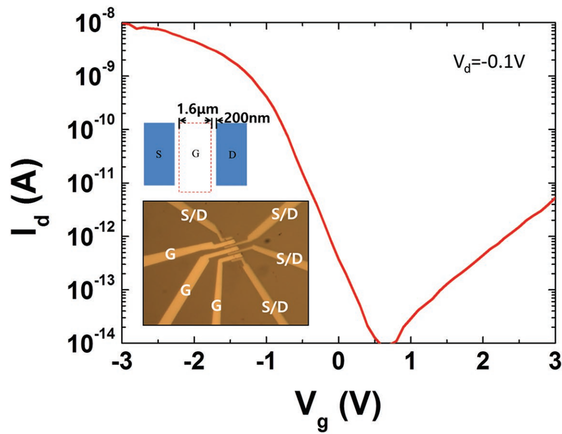


**Figure 2.** Measured transfer curve of Si nanowire Schottky barrier FET showing ambipolar characteristic. Schematic band diagram shows injection of different types of charge carrier according to the gate bias.

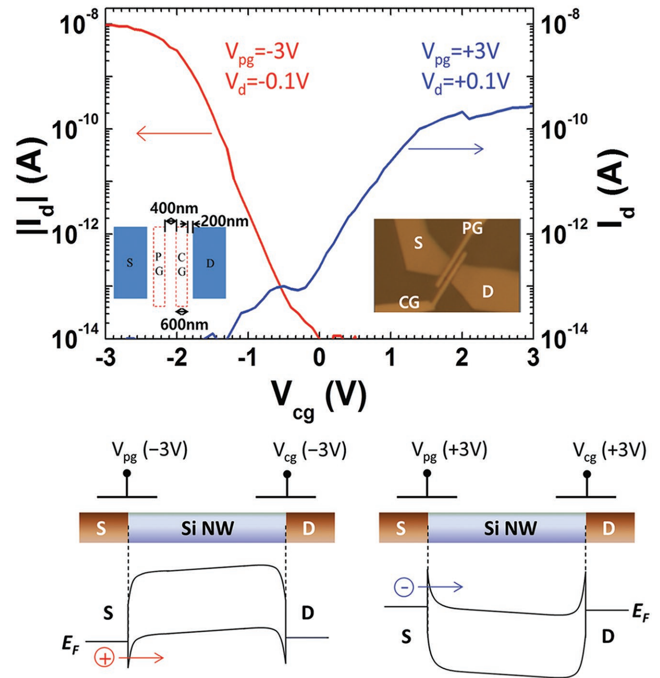


**Figure 3.** Measured transfer curve of Si nanowire reconfigurable nonvolatile transistor. The polarity of the transistor is configured by the bias on polarity gate. Schematic band diagram shows injection of different types of charge carrier according to the polarity gate bias and control gate bias.

Reconfigurable transistors are based on Schottky FETs but have the ability to filter out the undesired charge carrier type, thereby switching the polarity of the device with an electrical signal. The operation of the reconfigurable transistor is discussed in detail in ref. [4]. The reconfigurable transistor has two independent gates, the control gate (CG) and the polarity gate (PG), placed on $NiSi_2$–Si contacts. These gates are separated from each other by 400 nm distance and 200 nm from source/drain electrode to the contact openings. As the silicide is intruded into the nanowire, good electrostatic coupling between the gates and the junctions is ensured. **Figure 3** shows successful reconfigurable transistor operation with n-type transfer characteristics or p-type transfer characteristics as adjusted by the polarity gate bias. When the polarity gate bias $V_{pg} = -3$ V is continuously applied, p-type behavior is programmed in a volatile manner as shown in the red curve (left-hand side) of Figure 3. The energy bands of silicon under the polarity gate (source side in the given device structure) are bent upward blocking electron injection and only allowing hole injection through the thin Schottky barriers. The conductance of the device is controlled by the Schottky barrier thickness at the $NiSi_2$–Si contact of the other side with the control gate. On the other hand, for n-type transistor operation, the polarity gate bias $V_{pg} = +3$ V is applied. In contrast to p-type transistor operation, it creates a band structure that leads to electron-dominant conduction. With the positive polarity gate bias, the silicon energy bands under the polarity gate are bent downward and make the Schottky barrier thinner for electron injection and create a large energy barrier for hole injection. The resulting n-type transfer curve is shown in blue (right-hand side) in Figure 3. Therefore, both selective n-type and p-type volatile transistor operations are demonstrated on the single reconfigurable transistor with silicon oxide/silicon nitride double-layered dielectric.

Programming/erasing operation was characterized in the nonvolatile reconfigurable transistor by using the Fowler–Nordheim tunneling mechanism through the tunneling $SiO_2$ layer. For hole programming/erasing, a polarity gate bias of −3 V was applied while S/D was grounded. This results in p-type configuration. At the same time, a negative pulse of −13 V (corresponding to an electric field of ≈10 MV $cm^{-1}$) was applied for 10 ms to the control gate in order to perform hole programming first as shown in control gate pulse/sweep trace in **Figure 4**a. Accordingly, holes tunnel through the oxide to the $Si_xN_{(1-x)}$:H trapping layer[18–20] under the control gate by Fowler–Nordheim tunneling since a high electric field is applied through the entire dielectric stack.[21] (As we discussed in the transfer curve in Figure 3, the energy bands of the silicon channel in the polarity gate side are bent upward when the polarity gate is negatively biased, and they help hole injection while electron injection is inhibited.) To erase the hole programming, a voltage of +10 V (≈8 MV $cm^{-1}$) is applied for 10 ms to the control gate, while the device is operated in the p-type operation mode. The transfer curves in Figure 4a show the negative shift owing to trapped holes in the silicon nitride layer as well as the successful recovery with electron injection by positive bias pulse on the control gate. In the erasing operation of the p-type nonvolatile RFET, trapped holes in the silicon nitride layer are forced to be de-trapped toward the channel or compensated by electron trapping by the positive pulse gate bias. On the other hand, the programming state in the n-type nonvolatile RFET operation occurs with a positive pulse bias of +13 V and erased with



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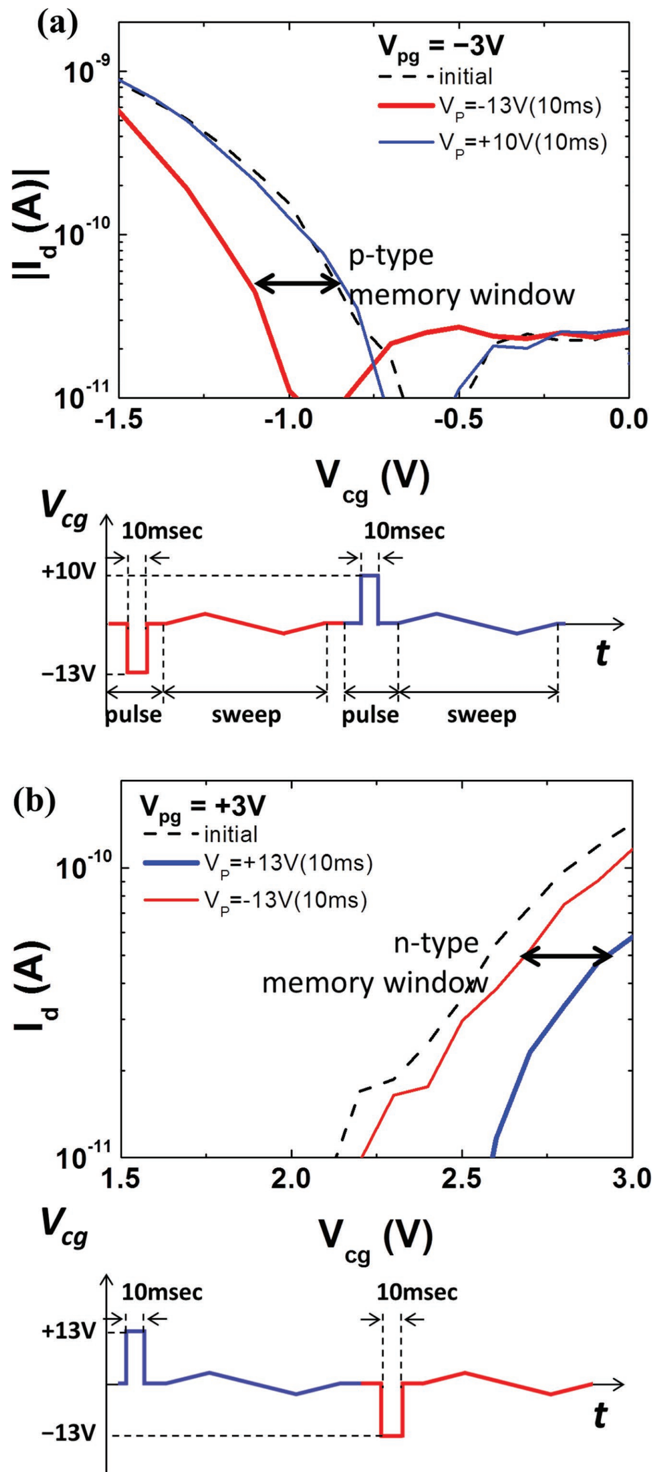


**Figure 4.** Programming/erasing characteristics of the reconfigurable nonvolatile transistor, showing nonvolatile threshold voltage shift in a) p-type and b) n-type device operation.

$V_p$ = −13 V at the control gate while keeping the polarity gate bias +3 V and S/D grounded (Figure 4b). For the n-type nonvolatile operation, electrons injected from source and drain sides are trapped in the silicon nitride layer via tunneling during the programming state and detrapped or compensated by hole injection with a negative erasing gate pulse. In the description above, we can discern between four clearly distinguishable operation states (**Figure 5**): p-type down, p-type up, n-type down, and n-type up. This unique feature gives inherently a dual-bit operation functionality. Different from conventional multibit charge trapping devices,[17,22] the additional bit storage arises from the ability to trap electrons and holes from the reconfigurable channel. Since the dual-gate RFETs are structurally completely symmetric, one can also speculate on the ability to manipulate electron/hole trapping and detrapping under the polarity gate. Potentially, this could give additional storage states, but the practical use will depend on the read/write/erase circuitry employed that goes beyond the scope of this paper. The memory window of the reconfigurable nonvolatile transistor is 0.25 and 0.35 V for p-type and n-type nonvolatile operation, respectively, at $I_d$ = 50 pA ($I_d \cdot L/W$ = 3.75 nA; $L$ = 1.5 µm; $W$ = 20 nm). The observed memory window is lower compared to the conventional nonvolatile SONOS flash memories or other nonvolatile Schottky barrier transistors using nanomaterials.[23–26] The results obtained in our reconfigurable transistor can be attributed to the thick $SiO_2$ tunnel layer and the absence of a block oxide between the silicon nitride layer and the gate metal. Much thinner tunnel oxide together with a top oxide will allow us to fully reconfigure the device in a nonvolatile fashion with smaller program and erase voltages. Also a higher memory window is expected, since the trapped charges can be located further away from the gate electrode, and parasitic charge injection from the gate electrode side is avoided. Although the data retention and long-term endurance properties are not studied in this first proof of principle, we expect that these properties behave similar to that of conventional nanowire flash cells with an equivalent charge storage stack and omega-gate geometry, for example, the results of the SONOS omega-gate cell[27] because the physical trapping and detrapping mechanisms should be identical. In this work, we have focused on verifying that it is possible to combine the RFET with a nonvolatile storage mechanism and demonstrated that it can be used for storing data or to tailor the threshold voltage of the device.

## 3. Conclusions

The individually addressable, reconfigurable, nonvolatile transistor based on bottom-up grown Si nanowire was successfully demonstrated for the first time, and it shows the potential for combining memory function with reconfigurable operation for future IC architectures demanding an ultradense integration of logic and memory and fine-grained connectivity. The unique transfer characteristic of the reconfigurable transistor, switching the polarity of the transistor by applying an electric signal, was observed by using a silicon oxide/silicon nitride double-layered dielectric. Successful programming and erasing for both p-type and n-type modes were demonstrated with the device. Further optimization of the fabrication process, i.e., thinner tunneling oxide and implementation of a blocking oxide on the device structures, will be carried out to fully unveil the potential of the utilization of nonvolatile polarity switching and to enable a detailed study of the achievable reliability.



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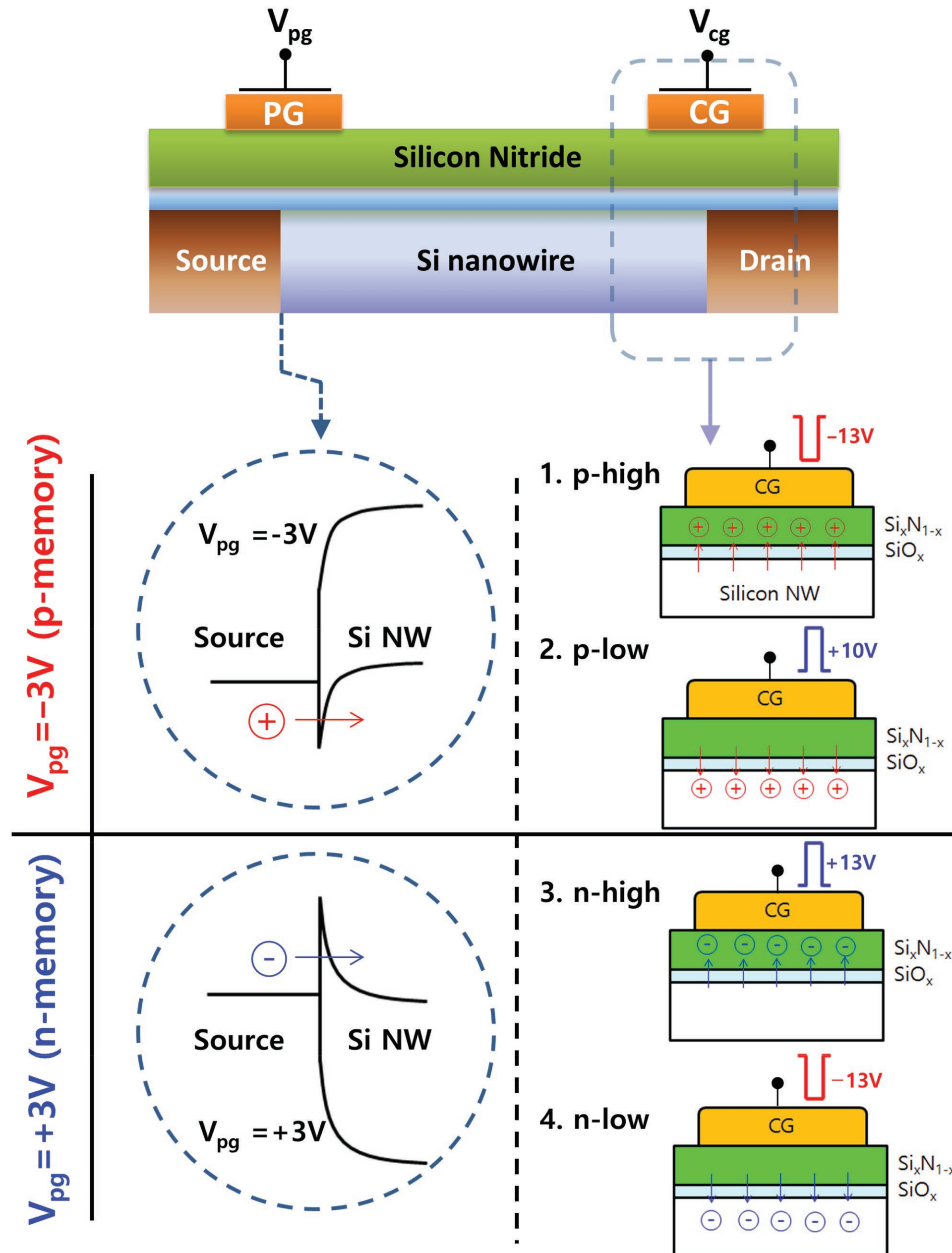


**Figure 5.** Schematic showing the four distinct memory states that can be achieved in a single device: p-high/p-low/n-high/n-low.

## 4. Experimental Section

For the fabrication of the reconfigurable nonvolatile transistor demonstrators, intrinsic silicon nanowires of ≈20 nm thickness were grown by the Au catalyst-assisted vapor–liquid–solid mechanism in predominant <112> direction. After etching the Au catalyst particles, the nanowires were suspended in isopropyl alcohol. The nanowire solution was dispersed on 200 nm thick thermally grown $SiO_2$/Si substrate. The $SiO_2$ tunneling oxide shell surrounding the Si nanowire was formed through a rapid thermal process in oxygen at 875 °C for 1 min. Forming gas annealing at 500 °C was followed to passivate nanowire/oxide interface traps. Although the thickness of the $SiO_2$ layer was measured as 2–3 nm thick in a planar reference wafer, which is processed with the same oxide growth condition of the device, the resulting oxide thickness around the mean nanowire was ≈5 nm as determined with TEM analysis due to the growth rate affected by the Si geometry and faceted initial surface.[28,29] The source/drain electrodes were patterned with electron beam lithography, and the $SiO_2$ shell under source/drain part was etched with 1% buffered hydrofluoric acid (BHF) in order to have the direct contact between Si nanowire and source/drain electrode. Deposition of 40 nm thick nickel was carried out using sputtering for the formation of source/drain electrodes. Subsequently, the silicidation process was followed with a rapid thermal process at 450 °C for 30 s in the forming gas to form $NiSi_2$ at source/drain side of the nanowire. $NiSi_2$ electrodes were used for both electron and hole conduction since the Fermi level of $NiSi_2$ aligns near the Fermi level of intrinsic Si.[30] The abrupt $NiSi_2$–Si junction was fabricated, and the length of the silicide was between 200 and 300 nm. The 15 nm thick silicon nitride $Si_xN_{(1-x)}$ trapping layer was deposited on the $SiO_2$ shell using a plasma-enhanced chemical vapor deposition process. Finally,



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electron beam lithography of the gate electrode was carried out to pattern the 40 nm thick nickel for the completion of the device.

Electric transfer curves and nonvolatile properties were measured using a Keithley 4200 semiconductor parameter analyzer in a shielded probe station.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

intrinsic silicon nanowires, nonvolatile transistors, reconfigurable field effect transistors, reconfigurable memory, Schottky barrier

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