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MoS2 based Memristive Synapses for Neuromorphic Computing

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MOS_2 BASED MEMRISTIVE SYNAPSES FOR NEUROMORPHIC COMPUTING

by

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ABSTRACT

Brain inspired computing enabled by memristors have gained prominence over the years due to its nano-scale footprint, reduced complexity for implementing synapses and neurons. Several demonstrations show two-dimensional (2D) materials as a promising platform for realization of robust and energy-efficient memristive synapses. Ideally, a synapse should exhibit low cycle-to-cycle (C-C) and device-to-device (D-D) variability along with high maximum /minimum conductance (G_{max}/G_{min}) ratio, linearity and symmetry in weight update for obtaining high learning accuracy in neural networks (NNs). However, the demonstration of neuromorphic circuits using conventional materials systems has been limited by high C-C and D-D variability and non-linearity in the weight updates. In this study, we have realized robust memristive synapses using 2D molybdenum disulfide (MoS_2) to address the concerns like high variability and non-linear weight update and asymmetry. We have utilized engineering techniques like electrode and stack engineering to realize ultra-low variability and linear weight update in MoS_2 synapses. The ultra-low C-C and D-D variability in SET voltage, RESET power and weight update is demonstrated in Au/MoS_2/Ti/Au synapses. Further, these synapses were integrated with MoS_2 leaky-integrate and fire (LIF) neurons to realize AND, OR and NOT logic gates proving the viability of these synapses for in-memory computing. However, these MoS_2 synapses suffer from low G_{max}/G_{min} ratio. We have employed stack engineering to increase G_{max}/G_{min} ratio while preserving low variability. In that regard, the active medium is modified to a heterogenous stack of MoS_2/SiO_x with Ti/Au bottom and top electrodes. We observe an increase in the G_{max}/G_{min} ratio from 2 to ~10. Further, electrode engineering is used to realize graphene/MoS_2/SiO_x/Ni to obtain linear weight update with identical pulses essential for online training of NNs. This work

substantiates the necessity of engineering techniques to implement essential synaptic characteristics like ultra-low variability and linear and symmetric weight update.

To my uncle, dad and mom

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LIST OF ACRONYMS (or) ABBREVIATIONS

2D	Two-Dimensional
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ANL	Asymmetric Non-Linearity factor
ANN	Artificial Neural Network
CC	Current compliance
C-C	Cycle-to-Cycle
CV	Coefficient of Variation
CVD	Chemical Vapor Deposition
CMOS	Complementary Metal Oxide Semiconductor
D-D	Device-to-Device
ECM	Electro-Chemical Metallization
EDS	Elemental energy Dispersive x-ray Spectroscopy
EELS	Electron Energy Loss Spectroscopy
FNT	Fowler Nordheim Tunneling
$\mathbf{G_{max}}$	Maximum conductance
$\mathbf{G_{min}}$	Minimum conductance
$\mathbf{G_{max}/G_{min}}$	Dynamic Range
hBN	Hexagonal Boron Nitride
HCS	High Conductance State
HRS	High Resistance State

HRTEM	High Resolution Transmission Electron Microscopy
IQHE	Integer Quantum Hall Effect
LCS	Low Conductance State
LIF	Leaky-Integrate and Fire
LRS	Low Resistance State
LTD	Long term depression
LTP	Long term potentiation
MAC	Multiply-Accumulate
MBE	Molecular Beam Epitaxy
MOCVD	Metal Organic Chemical Vapour Deposition
MoS_2	Molybdenum disulfide
NLF	Non-Linearity Factor
NN	Neural Networks
NVM	Non-volatile memory
PCM	Phase Change Memory
PF	Poole-Frenkel
RRAM	Resistive Random-Access Memory
SCLC	Space Charge Limited Conduction
SD	Standard Deviation
Si	Silicon
SRAM	Static Random-Access Memory
STP	Short term potentiation

STDP	Spike timing dependent plasticity
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy
TMDC	Transitional Metal Dichalcogenides
TSM	Threshold Switching Memristor
VC	Voltage Compliance
VM	Volatile Memory
VMM	Vector Matrix Multiplication
XPS	X-Ray Photoelectron Spectroscopy

CHAPTER 1 INTRODUCTION

The conventional von Neumann architecture is realized using metal oxide semiconductor (CMOS) transistors. The computers using von Neumann architecture tend to introduce latency in data intensive operations due to the physical separation between the memory and logic units. Furthermore, this architecture does not possess qualities like learning, recognition similar to the human brain. The artificial intelligence applications entail the process of learning and inference to perform a task like human brain which is also inherently energy efficient. Therefore, new approach emulating human brain's information processing behavior is implemented which is known as "neuromorphic computing". Neuromorphic computing is an attractive alternative because of the co-location of memory and processing units resulting in a distributed computing scheme, made plausible by the interconnection of neurons and synapses. The neurons behave as the computing units and synapses are local storage elements.[1] This paradigm shift is shown in **Figure 1 (a-b)**. Artificial intelligence applications, such as voice recognition, image recognition, motion tracking and gesture recognition has been typically realized using artificial neural networks (ANNs). Neural networks involve layers of neurons connecting to each other through synaptic weights, requiring the multiplication of the input neuron matrix with the synaptic weight matrix (**Figure 1 (c)**). Thus, a multi-layered neural network necessitates multiple such vector matrix multiplication (VMM) or multiply-accumulate (MAC) operations. Additionally, the neural network requires several epochs of training, which demands the repeat of the MAC operations. Conventionally, these algorithms are run on CMOS hardware, which brings about a complexity of $O(N^2)$ for each MAC operation, where N is the number of inputs. Thus, it is fathomable that a complex multi-level neural network for a single artificial intelligence task requires multiple days of training. Therefore, for energy-

efficient and fast realization of ANNs, it is necessary to have parallel computing systems at the fundamental device level. The emerging non-volatile memory devices prove to be promising for implementing these brain-inspired algorithms. Here, the synapses are realized using analog non-volatile memories, such as resistive memory and flash memory (floating gate transistors, charge trapping devices). By replacing the present day static random-access memory (SRAM) devices with crossbar arrays of the emerging analog memory devices, the computation will be more efficient. In a cross bar, as shown in **Figure 1(d)**, the analog memory cell is present at each cross point. The conductance of the memory cell is equivalent to the weight (w_{ij})of the neural network. The current through a single cross point is the product of the voltage (V_i) and the conductance (w_{ij}), $V_i \times w_{ij}$, simply by Ohm's law. The current drawn through the j^{th} vertical line, I_j in the crossbar array is the sum of the currents through each cross point, $I_j = \sum_{i=1}^{N} V_i \times w_{ij}$ by following Kirchoff's law. Thus, it can be seen that by simply extracting the current through a vertical line on the crossbar, one performs the complex task of multiplying the two vector matrices ([V] and [w]) instantaneously. Additionally, in an SRAM array, a binary SRAM cell consists of six or eight transistors. In contrast, an emerging non-volatile memory cell, comprising a single cross-point device with nanoscale lateral dimensions, has decreased foot-print and exhibits analog memory states. This increases the integration density which in turn can support a large dataset. This facility of storing all the weights on the chip decreases off-chip memory access which, in turn, increases the computational speed and decreases the energy consumption of the system. Further, these devices do not suffer from stand-by leakage due to their non-volatility. It is estimated that the neural networks realized using resistive memories increase the energy efficiency by orders of magnitude when compared to the conventional CMOS hardware platforms.[2]

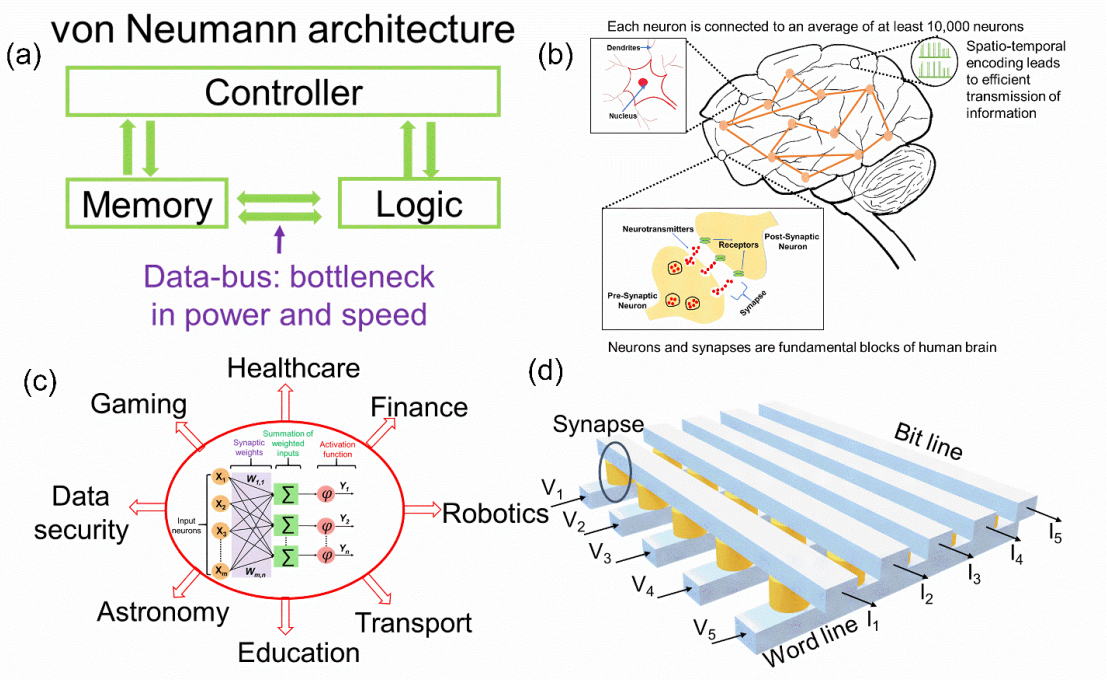

Figure 1: (a): Schematic showing the conventional von Neumann architecture where the memory and logic units are physically separated. (b): Paradigm shift in the computing architectures for artificial intelligence applications, inspired by the parallel computing observed in human brain. (c): NN schematic and artificial intelligence applications. (d): Cross-bar array architecture for implementing NNs with a synaptic device (analog memory) at each cross-point.

1.1 Introduction to 2D materials

The scaling of silicon (Si) has arguably reached its saturation. This saturation makes the traditional definition of Moore's law obsolete. Transistor scaling refers to shrinking the transistor size where the distance between source and drain is decreased, or the gate length is decreased, which leads to increase in the packing density on the chip. However, this scaling comes at a price of short channel effects which lead to increase in the leakage current, higher static power dissipation etc.[3] Due to these reasons, substitutes for conventional channel materials are explored. After the isolation of graphene in 2004, 2D materials or layered materials have garnered significant interest for low power electronics, optoelectronics, catalysis and quantum applications.

2D materials are crystalline solids consisting of single layers of atoms. The atoms are covalently or ionically bonded within the same plane of the material. The individual layers are bonded to each other by out-of-plane van der Waals interactions. [4] Thus, these materials can be thinned down to a single layer without any dangling bond.[5] Contrast this with conventional semiconductors, such as Si. Though Si and other conventional semiconductors can be etched down to the nanometer-scale thicknesses, due to the very nature of atomic bonding in these materials, there will be out-of-plane bonds which will lead to the deleterious effects of surface states. Due to the absence of dangling bonds, the mobility of the 2D materials does not degrade due to surface and interface roughness scattering.[6]

The library of 2D materials offers an extensive array of electronic materials, ranging from metals, semi-metals, insulators, semiconductors, ferroelectric and ferromagnetic materials to superconductors. The library of 2D materials is shown in **Figure 2**. [7]

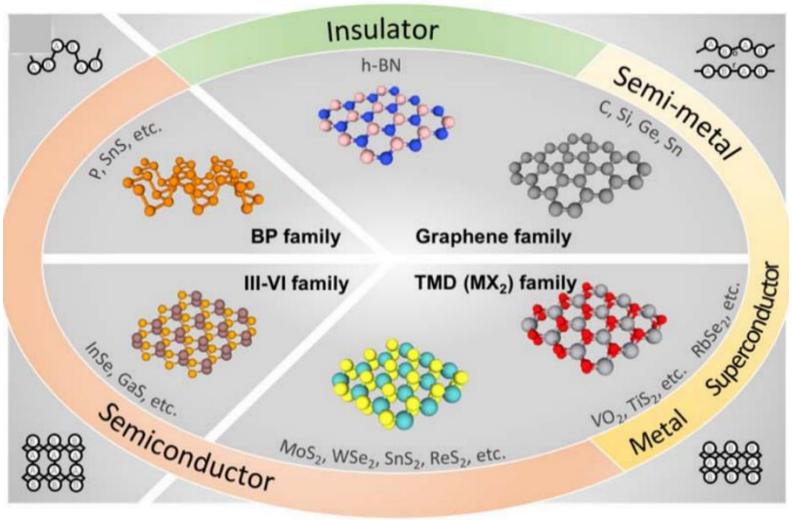

Figure 2: 2D materials family. Reprinted with permission from the reference [7] © 2018 IEEE.

Graphene is a semi-metallic 2D material which has ambipolar behavior at room temperature. Due to ballistic transport, the material shows carrier mobility in excess of 10^5 cm^2/V-s at low temperatures.[8] Graphene exhibits integer quantum hall effect (IQHE) at room temperature due to its massless Dirac fermions that move relatively unscattered in the presence of a magnetic field.[9] Further, graphene has exceptional mechanical properties, such as a high Young's modulus of ~0.5 -1 TPa (compared to steel's ~200 GPa) , a high spring constant of ~ 1-5 N/m and a tensile strength of~ 130 GPa (compared to steel's ~400-800 MPa).[10-13] The absorption spectrum of graphene is in the range of 300 nm – 1400 nm, showing transparency of 97% in the visible region of the spectrum. Despite these attractive qualities, the zero bandgap of graphene limits its utilization for digital logic operations. Graphene led to emergence of the field of 2D materials and inspired the quest for materials with a bandgap for electronic applications.

Transitional metal dichalcogenides (TMDCs) are a versatile family of 2D materials. These materials have a finite bandgap. They have the formula MX_2, where 'M' represents the transition metal – Mo, W, Hf, Re etc., and 'X' represents the chalcogen – S, Se, Te as shown in **Figure 3**.[14] Similar to graphene, the M and X atoms are arranged in a honeycomb structure where M is stacked between two X atoms to form X-M-X. Most of these semiconducting TMDCs show a direct bandgap at monolayer thickness, and transition to indirect bandgap when the thickness increases. The tunability of bandgap with material thickness expands on the versatility of these materials for the realization of diodes, transistors and other optoelectronic devices. Further, due to the ease of fabrication of heterostructures due to the van der Waals bonding, TMDCs have become an attractive choice for emerging devices, such as sensors for internet of things, neuromorphic devices for pattern recognition, and energy harvesting devices. The library of 2D materials also consists of insulating materials, such as hexagonal boron nitride

(hBN), superconducting materials, such as $NbSe_2$, X-enes, which are the layered form of Group IV elements, Si, Ge called as silicene and germanene, black phosphorus and Group IIIA chalcogenides, such as GaS and GaSe.

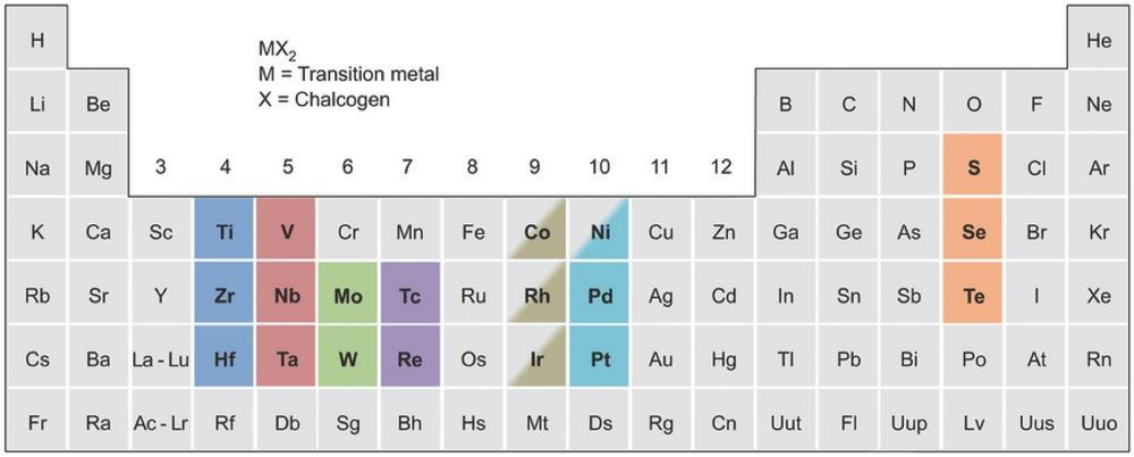

Figure 3: Periodic table showing various possible TMDCs where the highlighted sections represent metal and chalcogen atoms. Reprinted with permission from the reference [14] © 2013 Springer Nature.

The synthesis of 2D materials can be classified into two approaches. The top-down approach involves mechanical and chemical exfoliation, and the bottom-up approach involves direct synthesis, for example, chemical vapor deposition (CVD). Initial studies on proof-of-concept devices with exfoliated 2D materials unraveled the extraordinary potential of the materials system.[6, 15-24] Since then, large scale synthesis of 2D materials have been explored for integrating 2D materials in digital electronics, photovoltaics and battery technologies. Metal-Organic Chemical Vapor Deposition (MOCVD), molecular beam epitaxy (MBE) and atomic layer deposition (ALD) have facilitated the large-scale growth of TMDCs. The wafer scale realization of 2D materials has proved to be advantageous for high density circuits which are capable of performing complex computing tasks. Due to the possibility of realizing a variety of devices, such

as transistors, diodes, memristors, and other types of memory devices, 2D materials are promising candidates for neuromorphic computing applications, too.

1.2 Characteristics of artificial synapses

1.2.1 Power consumption

The power consumed to change the conductance state upon the application of a stimulus pulse plays a critical role in online training of the ANNs. In biological synapses, energy per synaptic event is ~ 10 fJ.[25] The power consumption is dependent on the amplitude and width of the applied stimulus pulses, and the current flowing through the synapse. The width and amplitude of the pulses are dependent on the power requirement and speed of the ANN's training. It is necessary to have synaptic devices that operate at programming voltages of <1 V for μs-long pulses. These parameters will increase the energy efficiency and decrease the latency of the ANN. Further, the programming voltages should be compatible with the supply voltage of the peripheral circuitry which is comprised of conventional CMOS devices. In general, programming current, programming voltage and pulse duration should be as low as possible.

1.2.2 Device dimensions

The implementation of complex, large scale neuromorphic circuits require synaptic devices with the smallest device footprint. The device area determines the packing density and the area overhead. Therefore, it is necessary to realize synapses in the sub-10-nm regime. Intuitively, area

scaling leads to the improvement of operating voltage, current and speed of the network while there will be trade-offs in the minimum to maximum conductance ratio of the device.

1.2.3 Dynamic range

The dynamic range of a synaptic device is defined as the ratio between the maximum conductance (G_{max}) and the minimum conductance (G_{min}). Most synaptic devices have a dynamic range between 2 and 100. It is essential to exhibit a higher dynamic range because this allows better mapping of weights in the algorithm to conductance of the devices. However, the requirement of dynamic range depends strongly on the application, *i.e.* training or inference. A high dynamic range accounts for a higher learning accuracy of the neural network.

1.2.4 Weight update precision

The weight update characteristics of an artificial synapse. Similar to biological synapses, artificial synapses in neural networks should exhibit analog-like multi-level weight states. Upon the application of the positive stimulus pulses, the synaptic weight should increase in gradual steps, and when stimulus pulses of opposite polarity are applied, the weight should decrease gradually. These weight update characteristics are used during the training of the neural network, where the weights of each synapse are adjusted to the appropriate values corresponding to the input image (for image identification). In an artificial synapse, weight update is the process of tuning the conductance of the synapse by the application of electrical pulses. Here, these conductance states refer to the weights in the NN. The presence of many synaptic levels ensures better learning

capability. In general, online training requires a greater number of states compared to inference applications.

1.2.5 Non linearity factor (NLF)

The linearity of the trajectory of the weight update characteristics plays a significant role in determining the online training accuracy of the ANN. The NLF are extracted for both long term potentiation (LTP) (NLF_{Pot}) and long term depression (LTD) (NLF_{Dep}), and the asymmetry is obtained as $ANL = |NLF_{Pot} - NLF_{Dep}|$. For a linear weight update, NLF<1 which provides a high online training accuracy. Perfectly symmetric characteristics impose asymmetric non-linearity factor (ANL) equal to 0. This implies that the trajectory of the weight increase (potentiation) is identical to that of weight decrease (depression). A symmetric weight update ensures that, during the training, the same number of applied pulses that increase the weight by a definite amount can also decrease the weight by exactly the same amount. This factor eases the training process and increases the training accuracy. ANL is particularly important to ANN online training because of the frequent weight updates required in synaptic devices. This feature becomes critical because linear and symmetric update allows direct mapping of weights in the algorithms to the conductance of the synapses. The non-linearity decreases the learning accuracy. Another important factor is the type of programming pulses that are applied to the devices to perform weight updates. It is essential to obtain linear and symmetric weight update using identical pulses. However, it is observed that most of the synaptic devices suffer from non-linear and asymmetric weight update with identical pulses, because of the mechanism of conduction in these devices. In that case, several strategies can be used to obtain linear and symmetric weight update. One of the commonly used strategies is

the application of non-identical LTP/LTD pulses. However, this method is not recommended because it necessitates the use of additional pulse generation circuitry which becomes impractical for on-chip implementations. Therefore, it is preferred to obtain linear and symmetric weight update with identical pulses.

1.2.6 D-D variability

The D-D variation is defined as the random variation in conductance that is observed in various synapse devices as a response to a single LTP/LTD pulse, which in turn affects the whole weight update trajectory. Additionally, the amplitude and duration of the programming pulse required for the weight update can vary from device to device. This tends to become a significant factor while implementing the NN. The D-D variation plays a more significant role in training in comparison to the inference process of the ANN.

1.2.7 C-C variability

The C-C variation refers to the variation in the conductance state within the same device when applying the same voltage pulse. This results in variability in weight update characteristics over subsequent cycles. The C-C variation observed in synapses decreases the training and inference accuracy of the ANN.

1.2.8 Endurance

Endurance refers to the ability of the device to sustain its characteristics for multiple cycles of applied stimulus pulses. It should be noted that the need for high endurance is dependent on the application. A high cycling endurance is necessary during the training process of the ANN. In general, a small task like training for MNIST handwritten digit recognition (60,000 images, with 50 training epochs) requires a maximum of 3×10^6 updates.[25] For each training epoch, during the weight update phase, all the synapses are not activated. Despite that it is necessary to have an endurance of at least 10^4 cycles for MNIST data set recognition tasks. This indicates that endurance requirements will increase as the complexity of the task increases. Usually, in the weight update phase, the update is a miniscule change in the conductance which can be the result of single or a few LTP/LTD pulses. This change does not cover the entire dynamic range of the device. Therefore, the application of 10^4 or 10^6 pulsed cycles does not indicate that the device has been stressed completely. In that case subjecting the device to DC cycling, where the device repeatedly goes from its OFF state to the highest ON state, can help evaluate the endurance.

1.2.9 Retention

The retention property is not critical when it comes to the online training of ANN since the weights of the synapses are usually updated. But this quality becomes critical in the inference process. Theoretically, the devices should have retention or behave like long term memory for at least 10 years. This retention should be at the maximum chip operating temperature of 85 °C.

1.3 Objectives

The main objectives of the dissertation are as follows:

1. Fabrication of proof-of-concept device. Here, graphene is used as the bottom electrode and MoS_2 as the switching medium. Ni is used as the electrodes for both graphene and MoS_2.
2. Preliminary results to demonstrate non-volatile resistive switching and synaptic behavior in 2D materials.
3. To develop ultra-low variability memristive device by implementing electrode engineering and device engineering using MoS_2.
4. To study ultra-low variability in synaptic characteristics.
5. To study the switching mechanism in ultra-low variability synapses.
6. To implement Boolean logic using MoS_2 synapses and MoS_2 leaky integrate and fire neurons.
7. To develop ultra-low variability synapse with high dynamic range by implementing stack engineering.
8. To demonstrate linear weight update in MoS_2 synapses by implementing electrode engineering.
9. To study the switching mechanism in linear weight update synapses.
10. To implement integration of linear weight update synapses and MoS_2 LIF neuron to study the spiking.

1.4 Dissertation Overview

Chapter 2 gives an overview of the types of artificial synapses that have been realized using 2D materials. It provides review of memristive synapses that have realized using insulating, semiconducting 2D materials to demonstrate low power consumption and high endurance. This chapter also introduces dominant mechanisms that are observed in resistive switching devices.

Chapter 3 presents the proof-of-concept demonstration of memristive synapses using MoS_2 as the switching medium, graphene as the bottom electrode and Ni as the top electrode. The fabrication, synaptic characterization are explored in detail. In the experimental section, near-linear weight update is demonstrated for multiple cycles.

Chapter 4 explores the fabrication and experimental details of ultra-low variability synapses realized using device engineering. The statistical analysis with respect to SET voltage distribution, RESET power distribution, ANL variation over at least 10 devices is provided. Additionally, this chapter also covers the experimental results pertaining to mechanism study.

Chapter 5 provides insight into the material characterization performed on ultra-low variability synapses. Material realizations like TEM show the robustness of the device stack post biasing. XPS and EELS spectra results show the role played by the top electrode Ti.

Chapter 6 demonstrates the Boolean logic implementation using robust synapses and MoS_2 LIF neurons. The results include the AND, OR and NOT gate implementations using MoS_2 synapses and neurons

Chapter 7 covers the stack engineering technique employed on ultra-low variability synapses to increase G_{max}/G_{min} ratio while keeping low variability intact. The chapter includes device fabrication where the active stack is modified to MoS_2/SiO_x and the results are compared

with MoS_2 device. The experimental section includes DC and pulsed measurements and their comparison with MoS_2 devices.

Chapter 8 presents the results pertaining to linear weight update synapses. The fabrication section entails the electrode engineering on MoS_2/SiO_x stack where bottom electrode is replaced by graphene and top electrode by Ni. The experimental section has the results of DC potentiation and depression, retention and mechanism studies. The linear weight update is explored by varying the pulse parameters. Finally, the efficacy of circuit implementation is explored by integrating MoS_2 synapses and neurons.

Chapter 9 provides the conclusion of this dissertation and discusses the future perspectives MoS_2 based synapses. It also discusses the challenges that needs to be addressed to realize high-density neuromorphic circuits using 2D materials.

CHAPTER 2 TYPES OF ARTIFICIAL SYNAPSES

2.1 Resistive memory

With the proposal of the fourth circuit element called memristor by L. Chua et al., followed by the demonstration of memristance in a metal/oxide/metal structure, a new field of resistive random access memory (RRAM) was unraveled.[26, 27] RRAMs promise to bridge the "memory wall" because of their high speed of switching. With their nanoscale footprint, they offer to pack more bits in a smaller area compared to the conventional SRAM devices. In a typical RRAM device, the switching medium is sandwiched between top and bottom electrodes, where the active area of the device is defined by the area of the junction between the bottom and top electrodes. The resistance of the device transitions from high resistance state (HRS) to low resistance state (LRS) and vice versa. The process of transition from HRS to LRS is called as SET and the transition from LRS to HRS is called RESET. Depending on the type of switching, these devices can be utilized to realize a synapse or a neuron. For implementing a synapse, it is necessary for the device to exhibit non-volatile memory (NVM) and neuron can be utilized using a volatile memory (VM) device.

2.1.1 2D Materials as electrodes in RRAM

Resistive memories (NVMs/VMs) have been realized using insulators like TiO_2[27], HfO_2[28], TaO_x[29] and bilayer stacks like HfO_x/AlO_x.[30] The presence of analog-like multilevel states led to the use of oxide-based RRAM devices as synapses in neural networks. Of late, various 2D materials have been used to demonstrate RRAM devices followed by their realization as

synapses. The incorporation of 2D materials for neuromorphic computing started with the introduction of graphene as an interfacial layer between the active oxide and electrode.[31] The reset current is reduced by ~10× in the device where a single layer graphene is sandwiched between the active HfO_x and the top electrode. Graphene is shown to act as a barrier to oxygen movement from the oxide to the electrode. Tian *et al.*, used bilayer graphene as the bottom electrode to realize a synaptic device with AlO_x as the active switching medium.[32] Graphene offers a high out-of-plane resistance in comparison to the conventional metal electrodes, due to its van der Waals bonding with the active medium. This is hypothesized to substantially reduce the programming currents in devices with graphene electrodes.[33-35] Chakrabarti *et al.*, demonstrated resistive switching in $TiO_x/Al_2O_3/TiO_2$ stacks using top and bottom graphene electrodes, with sub-μA programming currents and sub-nW reset power.[34] In the work of Lee *et al.*, graphene edge electrodes are used to in HfO_x RRAM devices.[33] These devices operate at considerably lower SET/RESET voltages than HfO_x RRAM devices with Pt bias electrode. Further, owing to the lower programming current and voltages, graphene also assists in the reduction of overall power consumption of the device. The authors observed a 300× reduction in the power consumption of devices with graphene electrodes compared to the devices with Pt electrode. While these initial efforts deal with demonstrating improved performance of RRAM devices by the inclusion of graphene, these do not shed light on the analog memory capabilities. In a graphene/2D-perovskite/Au stack, synaptic characteristics of LTP and STP were demonstrated with an energy consumption of 400 fJ/spike, with an ultra-low operating current of only 10 pA Here, the resistive switching is facilitated by bromide ion migration in the perovskite layers.[36] A synapse showing low operating currents and near-linear weight update curves, repeatable over 15 cycles was demonstrated with graphene as an electrode and MoS_2 as the switching medium.[37]

These demonstrations of devices elucidate the role played by graphene electrode in making the memristive synapses energy-efficient. Further, the transparency of graphene was tapped to perform in-situ X-ray photoelectron spectroscopy (XPS) analysis of the Pt/TiO_2/TiO_x/monolayer graphene(bottom to top) to observe the oxygen vacancy drift through the changes in binding energies.[38] However, the absence of a bandgap in graphene confines its role to that of an electrode in multiple demonstrations of RRAMs and other synaptic devices.

2.1.2 Insulating 2D materials RRAM

With oxides being used as the most prominent medium for memristive switching, it is natural to consider insulating 2D materials for the same. By using exfoliated h-BN, which was treated with oxygen plasma to form BNO_x as the switching medium, ultra-low energy consumption of ~1 fJ was reported for the resultant graphene/BNO_x/Ag device.[18] The device exhibits an ultra-low operating current, with an off-state of several fA and an ON state of less than 10 pA. A flexible resistive memory device was demonstrated with CVD-grown h-BN, facilitated by the use of Ag electrode.[39] Memristive switching in CVD h-BN through conducting nanofilaments was used to demonstrate synaptic behavior.[40] An exhaustive study on h-BN-based memristive devices revealed two major defect groups that affect the device properties: (a) wrinkles, polymer residues and other fabrication-related defects that increase the local out-of-plane resistance, but does not affect the breakdown voltage or resistive switching, and (b) crystallographic defects which reduce the out-of-plane resistance, affect the breakdown voltage, hence the resistive switching behavior.[41] Over 100 devices were characterized over 100 cycles

to show low C-C variability of 1.53% and low D-D variability of 5.74% in h-BN memristive crossbar arrays.[42]

2.1.3 Semiconducting 2D materials (active layer) RRAM

Semiconducting 2D materials, such as TMDCs, have found their use as the active layer in several demonstrations of synaptic devices. Memristive phenomenon is exhibited in devices with MoS_2-graphene oxide composite structure. [43, 44] 2D heterostructures hold immense promise for neuromorphic applications due to their pristine 2D/2D interface. In such devices we observe high retention, endurance and other synaptic characteristics like STP and LTP. The property of flexibility in 2D materials is necessary for smart wearable electronics. An $Ag/MoO_x/MoS_2/Ag$ stack was utilized to realize a memristive and memcapacitive switch on flexible substrates with an ultra-low operating voltage of 0.1 V enabling energy efficient neuromorphic operation along with STP and LTP [45]. Similarly, a graphene/$MoS_{2-x}O_x$/graphene device exhibits a high retention ($>10^4$ s), high pulsed endurance (10^7 cycles), high switching speed (~ 100 ns) and maintains its performance over 1200 bending cycles.[20] Various 2D materials like WS_2 [46, 47] and WSe_2 [23] have exhibited memristive behavior, which is then used to emulate a synapse. The aforementioned synaptic devices are realized with exfoliated 2D materials. For a neuromorphic hardware capable of practical implementation, it is essential to realize synapses on a wafer scale. This affirms the significance of the large-scale synthesis of 2D materials. Non-volatile switching in CVD MoS_2 was reported by Sangwan *et al.* [48] Here, the sulfur vacancies in the MoS_2 are accumulated near the abundant grain boundaries in CVD grown MoS_2. The modulation of the concentration of sulfur vacancies in the adjacent regions of the grain boundaries due to the application of an electric field

causes the resistive switching. In addition to MoS_2, non-volatile resistive switching is observed in other CVD-grown 2D materials like $MoSe_2$, WS_2, and WSe_2.[49] Recently, several demonstrations of synaptic behavior have been made with devices on CVD-grown MoS_2.[49-51] Bilayer MoS_2 grown by MOCVD was used in a Cu/MoS_2/Au device and a memristive synapse was demonstrated. These devices exhibit extremely low switching voltage of 0.1 V, high retention and synaptic characteristics such as spike timing dependent plasticity (STDP).[51] As mentioned earlier, near-linear weight update was accomplished in synapses with CVD-grown MoS_2 with graphene electrode.

2.2 Phase change memory

TMDCs exhibit different structural phases with distinct physical properties. MoS_2 has two distinct phases: 2H phase with a trigonal prismatic structure is semiconducting, and 1T phase with an octahedral structure is metallic. The transition from 2H to 1T and from 1T to 2H can be realized by various approaches including chemical and electrostatic doping, laser/electron irradiation and thermal annealing. The 1T phase of MoS_2 shows memristive behavior as a result of lattice distortions induced by the application of an electric field, while the 2H phase exhibits ohmic characteristics.[52] Another demonstration of phase change memory (PCM) is in a MoS_2 device where the phase of is changed from 2H to 1T' by Li^+ ion intercalation.[53] Li+ ions are attracted towards electrode A when a negative voltage is applied, resulting in an increase in Li+ ion concentration. This charge accumulation induces the 1T' (metallic) phase transition. A positive voltage applied to electrode A does the opposite and induces the 2H (semiconducting) phase

transition. The device also exhibits synaptic behavior as indicated by the repeatable weight update characteristics.

Non-volatile switching is also observed in $MoTe_2$ as the material transitions from semiconducting 2H phase to a distorted $2H_d$ phase when an electric field is applied.[54] The devices are realized using exfoliated 2D $MoTe_2$ with Ti/Au bottom electrode and Ti/Ni top electrode. The $2H_d$ phase is a transient state between 2H and the metallic 1T' phases. The applied bias causes the formation of the more conducting $2H_d$ phase, which forms the filament. High-angle annular dark field scanning tunneling electron microscopy (HAADF-STEM) reveals that the matrix is composed of 2H phase while the filaments consist of the transient $2H_d$ phase. These devices exhibit an endurance of 600 DC cycles and a retention of 10^5 s at both HRS and LRS.

2.3 Switching mechanisms

Resistive switching in 2D materials can be explained by two dominant switching mechanisms. Resistive switching in 2D materials by the formation of conductive filaments under bias is either due to the movement of oxygen vacancies present in the switching 2D layer or due to the migration of constituent ions.[20, 23, 45, 55] Non-volatile resistive switching is also facilitated by using a low-diffusivity metal as an electrode in a metal/2D/metal structure. In these devices, a voltage bias causes ions from one electrode to diffuse into the 2D material, forming a conductive filament. The filament ruptures upon the application of an opposite bias.[24, 56-58] In these devices, the transition from the HRS to LRS is abrupt due to the formation of conductive paths in the form of filaments. These filaments in the active layer are localized. Since the lateral dimension of each filament is in the order of the dimension of an atom, the resistance of the LRS

does not scale with device area for filamentary switching. Hence, a simple study of the scaling of LRS current with device area is evidence of the filamentary conduction, in comparison with complex and strenuous microscopy techniques to visualize the nanoscale filaments. Another dominant mechanism is due to the unique interface between the electrode and the switching medium. In these devices the transition from HRS to LRS is not abrupt, rather it is gradual. These devices have a tendency to exhibit low variability. In contrast to the filamentary devices, interface mediated RRAM exhibits area dependent resistance scaling in both HRS and LRS regions.

CHAPTER 3 PROOF-OF-CONCEPT DEVICE

The contents of this have been published in: Krishnaprasad, A., Choudhary, N., Das, S., Dev, D., Kalita, H., Chung, H.S., Aina, O., Jung, Y., and Roy, T., 2019. Electronic synapses with near-linear weight update using MoS_2/graphene memristors. Applied Physics Letters, 115(10), p.103104.

3.1 Introduction

In this chapter, we demonstrate a memristive synapse using CVD (MoS_2) as the switching medium and large area CVD grown monolayer graphene as the bottom electrode. The synaptic devices exhibit gradual potentiation and depression, with near-linear and symmetric weight update when symmetric input voltage pulses are applied. They display excellent retention characteristics of 10^4 s at 1 nA operating current, demonstrating their applicability in low-power neuromorphic systems. They also exhibit the essential synaptic characteristics of STP and LTP in the same device, and spike timing dependent plasticity (STDP).

3.2 Device schematic

Figure 4a shows the schematic of a single MoS_2/graphene device, with a large array of ~2000 devices shown in **Figure 4(a)**. CVD-grown monolayer graphene was wet-transferred[59] on p^+-Si/SiO_2. The graphene layer was patterned using photolithography and etched in oxygen plasma to form the bottom electrode of the device. Mo films (3 nm) were patterned using photolithography and e-beam evaporated on the etched graphene strips. The Mo films were sulfurized to form layered MoS_2 in a low-pressure CVD furnace at 200 mTorr and a substrate

temperature of 770 ^{0}C in an inert environment. Top contacts on MoS_2 and bonding pads on graphene were patterned using photolithography, followed by e-beam evaporation of Ni/Au (30 nm/30 nm) and lift-off. The region where MoS_2 overlaps graphene forms the active area (24-36 μm^2) for switching. The large-scale growth of graphene and MoS_2 enables the fabrication of multiple arrays of 2000 MoS_2/graphene devices as shown in the **Figure 4(b)**.

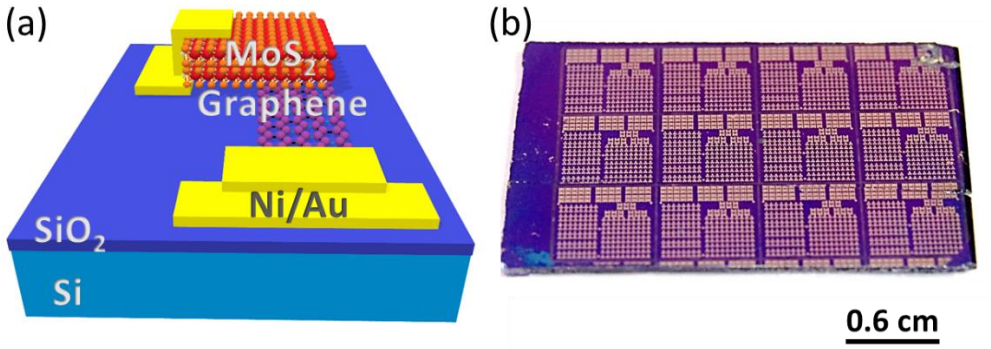

Figure 4: (a) MoS_2/graphene device schematic (not to scale) (b) Optical image of fabricated chip with MoS_2/graphene memristors.

3.3 Material Characterization

Figure 5(a)(i) shows the Raman spectra of as-deposited MoS_2 film on graphene. The presence of high intensity characteristic Raman peaks at 386 cm^{-1} and 410 cm^{-1}, corresponding to in-plane (E^1_{2g}) and out-of-plane (A_{1g}) lattice vibrations, indicates the growth of high-quality MoS_2 layers on graphene. We also studied the influence of Mo sulfurization on the quality of graphene. The Raman spectra of pristine graphene shows atypical lattice vibrations from G and 2D bands with a 2D:G peak intensity ratio of 2:1, confirming high quality single layer graphene on Si/SiO_2 substrate (**Figure 5(a)(ii)**). However, a substantial evolution of G and D peak with a suppressed 2D:G ratio is noticed after the sulfurization process, which could be due to the presence of defects in graphene layer introduced by sulfur (**Figure 5(a)(iii)**). The formation of high intensity D peak

is also noticed, which is in agreement with the literature.[60] The resistance posed by graphene after sulfurization is ~120 kΩ. The thickness of MoS_2 present in the MoS_2/graphene stack was determined by Atomic Force Microscopy (AFM) to be ~8 nm, as shown in **Figure 5(b)**. To further assess the quality and number of MoS_2 atomic layers, a cross-sectional high-resolution transmission electron microscopy (HRTEM) analysis was performed. It is evident from the **Figure 5(c)(i)** that MoS_2 film consists of horizontally grown ~9-10 atomic layers, which is consistent with the results from the Raman and AFM characterizations. The chemical composition of the MoS_2 film was further investigated by the energy dispersive x-ray spectroscopy (EDS). The EDS scanning transmission electron microscopy (STEM) image provides the elemental mapping as shown in the **Figure 5(c)(ii)**, and reveals a localized spatial distribution of Mo and S, indicative of highly stoichiometric and uniform 2D MoS_2 layers.

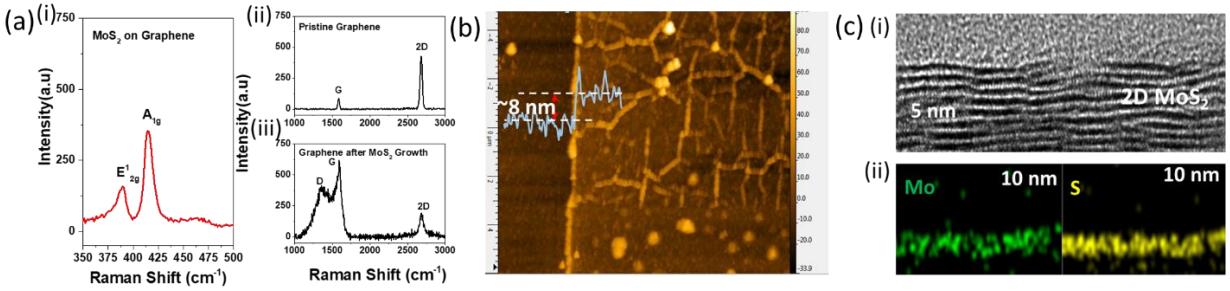

Figure 5: (a) Raman spectra of (i) CVD-grown MoS_2 on graphene, (ii) pristine graphene, and (iii) graphene after the growth of MoS_2. (b) AFM height profile of MoS_2 on graphene, indicating the thickness of MoS_2 to be ~8 nm. (c) (i) Cross-sectional HRTEM image of MoS_2 atomic layers grown on graphene. (ii) EDS-STEM elemental mapping image of MoS_2 on graphene.

3.4 Electrical Characterization

3.4.1 DC characterization

We examine the response of the MoS_2/graphene device to a sinusoidally varying input voltage, as shown in **Figure 6(a)**. The inset in the figure shows the sinusoidally varying input applied for the measurements. The MoS_2/graphene device exhibits a pinched hysteresis loop, confirming that this two-terminal device is a memristor.[61] Additionally, the width of the hysteresis loop decreases with increasing frequency of the input signal, which is a characteristic feature of a memristor.[61]

Figure 6(b) shows the DC switching characteristics of a pristine MoS_2/graphene device for two consecutive SET-RESET cycles. During the DC characterization of these devices, the voltage on the top electrode (Ni/Au) is held constant at 0 V, while the voltage on the bottom graphene electrode is swept. The SET voltage for the first cycle is similar to the SET voltage of the second cycle, indicating that a high electroforming voltage is not required for this device. A possible cause for this "forming-free" behavior could be due to the high series resistance of graphene after the sulfurization step. We observe that the graphene resistance is ~120 kΩ, with a maximum ON state resistance for the MoS_2/graphene device being 1.5 MΩ. Thus, the series resistance of the graphene electrode might play a significant role in preventing accidental breakdown of the heterostructure device. The device also exhibits non-linear IV characteristics and low reset current of 192 pA The OFF state resistance varies significantly across the two consecutive cycles, from 50 GΩ in the first cycle to ~12.5 GΩ in the second cycle. The cycle-to-C-C variations need to be eliminated for practical realization of these devices in memory/neuromorphic applications.

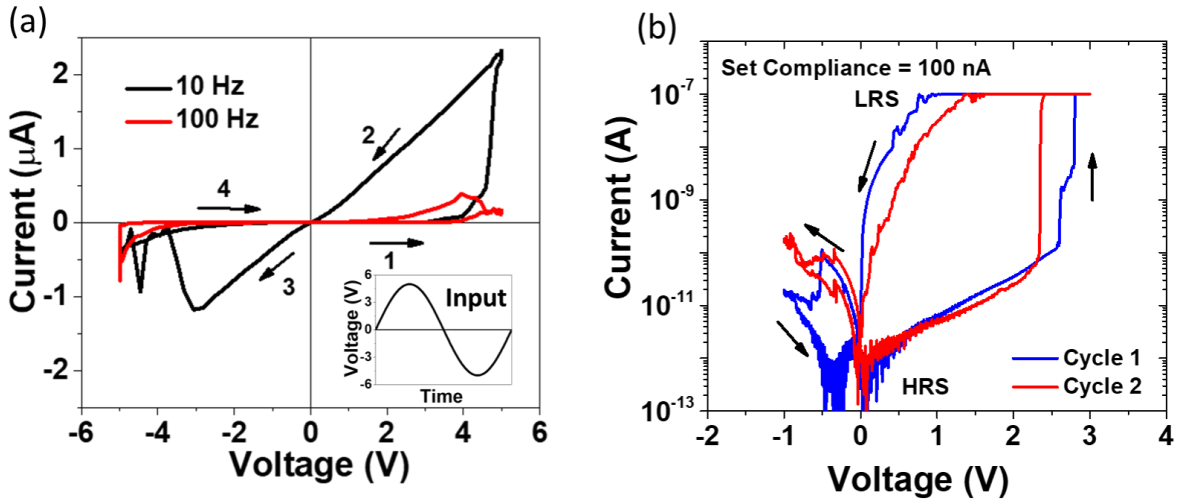

Figure 6: (a) Pinched hysteresis loop in I-V for sinusoidally varying input voltage of amplitude 5 V peak-to-peak, and frequency of 10 Hz and 100 Hz, confirming memristive behavior of the MoS_2/graphene device. (Inset: The input waveform) (b) Non-linear IV characteristics of MoS_2/graphene memristors at 100 nA current compliance showing that a high electroforming voltage is not required by the device.

A continuous SET process is performed by increasing the SET current compliance from 1 nA to 1 μA, immediately followed by a continuous RESET by increasing the magnitude of the negative reset stop voltage from -0.2 V to -1 V. **Figure 7** shows that five distinct states are obtained during the continuous DC SET and RESET processes. This demonstrates the potential of the MoS_2/graphene devices to display gradual change in conductance both in the low resistance and high resistance regimes, which is mandatory for emulating potentiation and depression of a synapse.

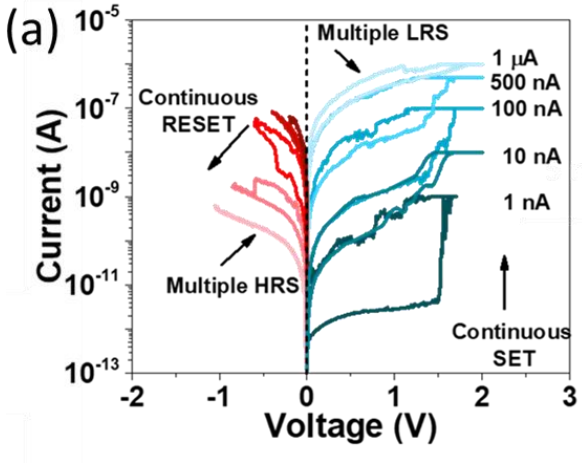

Figure 7: DC potentiation and depression with continuous SET at 1 nA, 10 nA, 100 nA, 500 nA, and 1 μA, followed by continuous RESET using negative reset stop voltages with increasing magnitude from -0.2 V to -1 V.

3.4.2 Retention Measurements

The MoS_2/graphene devices also exhibit excellent retention characteristics for ~10^4 s at 1 nA and 1 μA current compliances as shown in **Figure 8(a)**. The retention of data is tested for the lowest (1 nA) and the highest (1 μA) programming currents. First the device is set at 1 nA current compliance. Then read voltage pulses (amplitude 100 mV, duration 5 ms) are applied to measure the current through the synapse. The MoS_2/graphene memristor exhibits ~ 4 nA of current consistently for 6700 s as shown in **Figure 8(a)**. Then the same device is set at 1 μA, and read voltage pulses are applied. The current through the device is 58 nA, which matches with the DC characteristics at the same read voltage. The current remains at 58 nA consistently for 10^4 s. The SET characteristics of MoS_2/graphene memristors at 1 nA and 1 μA current compliances prior to applying voltage pulses (100 mV, 5 ms) for data retention measurements are shown in the **Figures 8(b-c)**. The variation in the SET voltages for 1 nA and 1 μA current compliances is due to the C-C variability observed in these devices. The SET voltage varies between 1 V and 2 V.

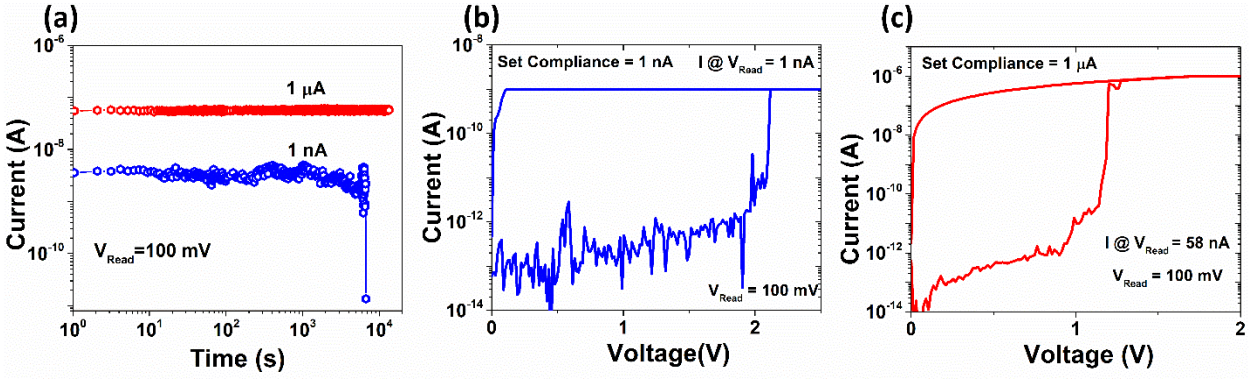

Figure 8: (a) Data retention of MoS_2/graphene memristors at 1 nA and 1 µA current compliances for 10^4 s. (b) Set characteristics of MoS_2/graphene memristor at 1 nA current compliance for retention. (c) The SET characteristics of MoS_2/graphene memristors at 1 µA current compliance prior to applying pulses (100 mV, 5 ms) for data retention measurements.

3.4.3 DC Endurance

Figure 9(a) shows sustained switching of a typical MoS_2/graphene device for 100 DC cycles at both 1 nA and 100 nA current compliances. The I_{ON}/I_{OFF} for SET current compliance of 1 nA is ~10^2 throughout the 100 DC cycles. The endurance of 100 DC cycles at 1 nA and at 100 nA by the same device establishes the robustness of the memristive switching process. **Figure 9(b)** shows the logarithmic distribution of the HRS and the two LRS (1 nA and 100 nA) for these 100 cycles. The low variation in the HRS and LRS currents are evident here. The maximum reset current and power of the MoS_2/graphene device for the SET current compliance of 1 nA is plotted in **Figure 9(c)**. The reset current varies between 10 pA and 1 nA over the 100 DC cycles. The device exhibits sub-nW reset power throughout the 100 DC cycles, with a minimum reset power of 10 pW. The reset power required by the MoS_2/graphene devices is 6 orders of magnitude lower than the reset power of metal oxide RRAMs.[30]

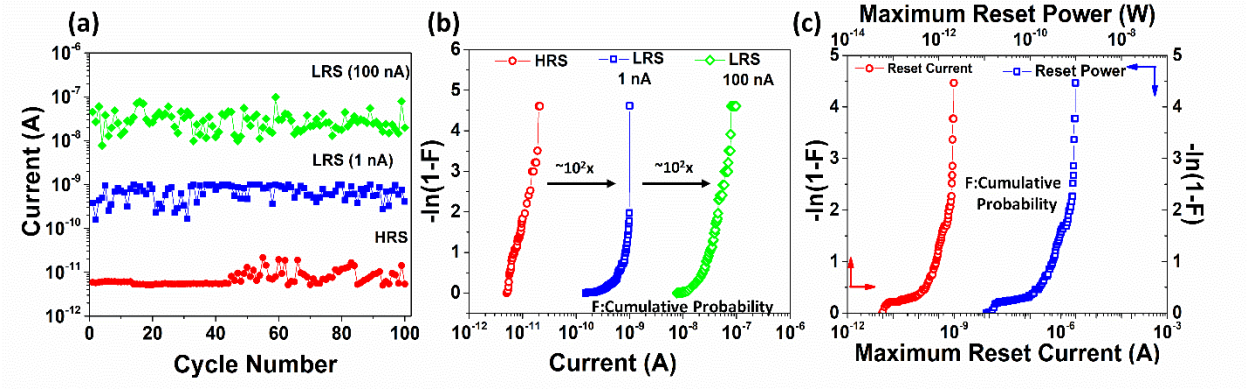

Figure 9: Endurance characteristics of MoS_2/graphene memristor. (a) Evolution of HRS and multi-level LRS at 1 nA and 100 nA for 100 DC cycles at V_{Read} = 2 V. The SET voltages for 1 nA and 100 nA current compliances are 3.5 V and 4.5 V respectively. (b) Logarithmic distribution of the 2 LRS's and HRS at V_{Read} = 2 V. (c) Logarithmic distribution of maximum reset current and power for LRS of 1 nA.

3.4.4 Pulsed I-V measurements

Pulsed I-V measurements are performed to determine the synaptic behavior of these devices. The current flowing through the memristive synapse as a response to the incoming voltage pulses is defined as the post-synaptic current (PSC). The device conducts current when the voltage pulse is ON, and the short pulse duration restricts the abrupt formation of the conducting channel. This facilitates the gradual formation of the conduction path during the pulsing intervals.[30, 32] Because of this gradual formation of the channel, the device exhibits a higher number of conductance states during pulsed measurements than during a continuous DC SET process.[32] This process of conductance tuning is characteristic of a biological synapse, and is termed as synaptic weight update.[25] A hundred pulses with a pulse-width of 100 µs and an amplitude of 5 V are applied to cause potentiation, immediately followed by another 100 pulses with width of 100 µs and amplitude of -4 V to cause depression. A total of 15 pairs of such identical positive-negative voltage pulse trains are applied to an MoS_2/graphene device, as shown in the **Figure**

10(a). The corresponding conductance is plotted against the pulse number in **Figure 10(b)**. We observe distinct conductance states with pulsed voltage input. The MoS_2/graphene device exhibits an almost linear weight update with identical input voltage pulses. We calculate the NLF for the potentiation and depression regimes using a behavioral model described by Chen et al.[62] Our MoS_2/graphene device exhibits an exceptional NLF of 0.276 in the potentiation regime, with an NLF of 0 indicating a completely linear weight update.[62] The weight update during depression exhibits an NLF of ~5. The near-linear weight update observed in the MoS_2/graphene synapse holds potential for unsupervised learning applications.[25] Although ~100 distinct conductance states during potentiation and depression are observed for all 15 pulse trains, we note that the instability of the lower conductance states would result in significant write noise for system level applications, thus reducing the number of resolvable conductance states. This issue can be circumvented using a write/verify algorithm, which is costly from the standpoint of power consumption.

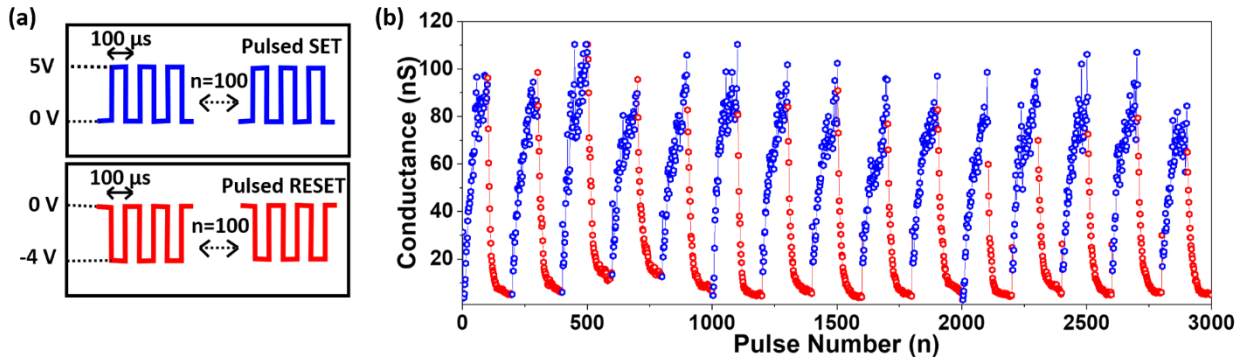

Figure 10: (a) Pulsing scheme: 15 pulse trains, with each pulse train comprising 100 identical positive pulses and 100 identical negative pulses. (b) Near-linear weight update observed in MoS_2/graphene synapse with the application of symmetric voltage pulses shown in (a).

The MoS_2/graphene memristors are also tested for essential characteristics of a biological synapse, such as short-term potentiation (STP), LTP and LTD. **Figure 11(a)** shows the STP

characteristics of a typical MoS_2/graphene synaptic device. Here, note that we use a different measurement protocol than that for retention measurements of Figure S3a. Six identical voltage pulses of 5 ms pulse width and amplitude of 3 V are applied to the bottom graphene electrode. The PSC through the synapse increases to 300 nA as the train of voltage pulses are applied. Following the train of 6 pulses, a read voltage of 0.2 V is applied to record the PSC. The PSC decreases to ~100 pA approximately 100 s after the withdrawal of the pulse train, indicating STP of the synaptic device. In **Figure 11(b)**, 18 identical voltage pulses (pulse width 5 ms, amplitude 3 V) are applied to the same MoS_2/graphene synaptic device after it exhibits STP. The PSC again increases to 300 nA during the pulsing period. After the pulsing period, a constant read voltage of 0.2 V is applied to record a PSC of ~5 nA for 10^4 s. This indicates the stabilization of the conduction path in the MoS_2/graphene device, inducing LTP. The synaptic weight update due to LTP is irreversible unless the device is RESET to its original state. This measurement also indicates that the synaptic device can retain its weight for > 10^4 s. The observation of LTP and STP in the same device by modulating the strength of the stimulus has been already reported in other memristive devices.[63],[64] Now we study LTD in a different device. Initially, the device is SET at 300 nA (Figure S5). Six identical pulses of amplitude -2.5 V and duration of 5 ms are applied. The PSC reduces from 209 nA to 13 nA as shown in the **Figure 11(c)**. After the withdrawal of the negative voltage pulses, a constant read voltage of 0.2 V is applied to record the PSC. The PSC is 500 pA (HRS), indicating that the device was reset by the applied pulses and continues to be in the HRS for at least 10^4 s.

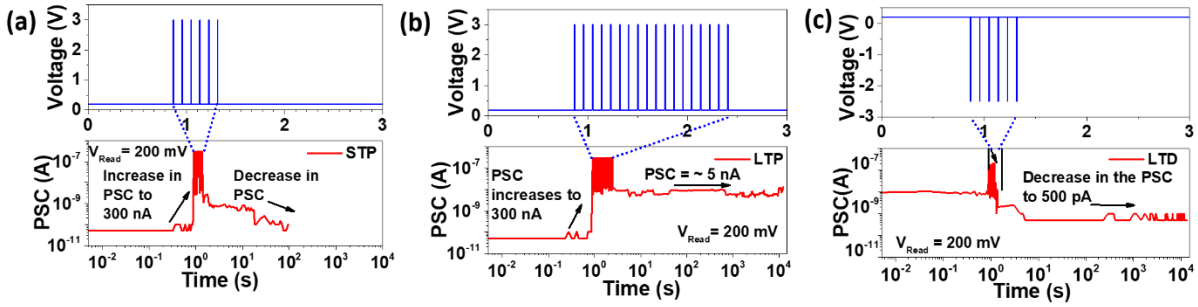

Figure 11: (a) STP of MoS_2/graphene synapse with input pulsing scheme (top) and PSC as a function of time (bottom). (b) LTP of the same device for 10^4 s with input pulsing scheme (top) and PSC as a function of time (bottom). (c) LTD of MoS_2/graphene synapse for 10^4 s with pulsing scheme (top) and PSC as a function of time (bottom).

Spike timing dependent plasticity (STDP) as the biological rule of Hebbian learning can be implemented in a hardware neural network for unsupervised learning.[25] The Hebbian learning rule attributes the temporal correlation between the pre-spike and the post-spike signals as the cause for the synaptic weight modulation. As the timing between the firing of the pre-spike and the post-spike signals increases, the synaptic efficacy decreases. If the pre-spike signal precedes the post-spike signal, the synapse potentiates, and for the reverse, the synapse undergoes depression.[30, 65]

We now demonstrate the STDP of the MoS_2/graphene memristive synapse. The pulse scheme is designed such that the overlap of the pre-spike and the post-spike signals happens only at one instant of time. A train of voltage pulses with decreasing amplitude is applied as the pre-spike and post-spike signals. The resultant voltage across the synapse is the difference between the pre-spike and the post-spike voltage amplitudes. In **Figure 12(a)**, the resultant pulse when the pre-spike signal fires at time Δt before the post-spike is shown in blue, while the resultant pulse when the post-spike signal fires before the pre-spike, with time difference $-\Delta t$, is shown in red. The first pulse of the train is a negative voltage pulse of width 300 ms and amplitude -1 V. It is

followed by positive pulses of decreasing amplitude with 150 ms pulse width. The negative pulse is wider than other pulses to compensate for the interconnect delay of the instrumentation used and to provide stabilization time for the device response. The normalized synaptic weight change, Δw (%) is calculated as the ratio of conductance at that overlap interval Δt to the maximum conductance observed.[66] The weight change Δw (%) is plotted against Δt to obtain the STDP response curve as shown in **Figure 12(b)**. The MoS_2/graphene synaptic device obeys the asymmetric Hebbian learning rule where the synaptic weight change decreases as the time between the firing of pre-spike and post-spike signals increases.

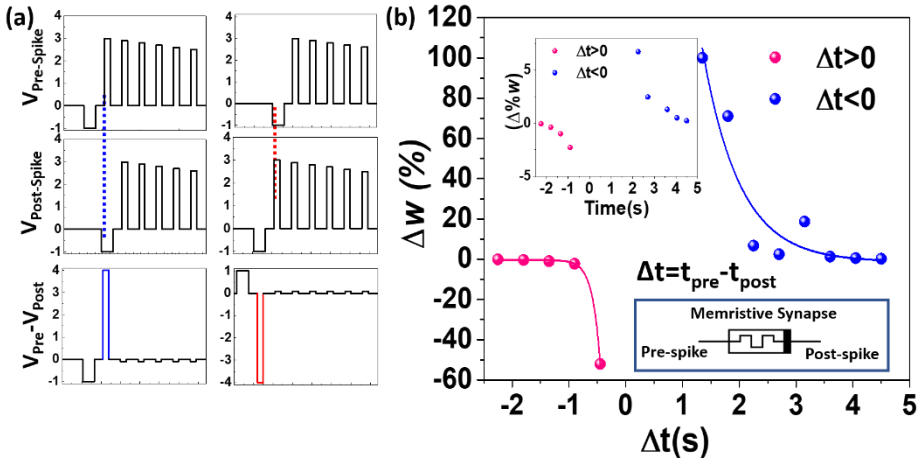

Figure 12: (a) Pulsing scheme for the STDP characterization. (b) Synaptic weight change as a function of timing difference of the pre-spike and the post-spike signals. Inset: the same plot zoomed-in from -5 Δw (%) to 8 Δw (%).

Generally, the switching mechanism can either be attributed to the formation of conductive filament through the memristive material or due to trapping/detrapping of carriers at the interface of the memristive material and the electrode. Memristive switching observed in 2D materials has been associated with the formation of a conductive filament.[32, 36, 49] In ultra-thin switching media, such as in monolayer MoS_2, the evidence of filamentary switching is noted from

the fact that the SET current does not increase with increasing area of the memristive device.[49] However, we cannot rule out the influence of the Schottky barrier between graphene and MoS_2 from playing a major role in the resistive switching observed in our devices. The linearity observed in the weight update of the MoS_2/graphene memristive synapses could be attributed to the interface mediated switching. This proof-of-concept devices was one of the first few works which reported that active 2D medium exhibits memristive behavior.

3.5 Conclusion

In conclusion, we have fabricated MoS_2/graphene memristors using large area CVD-grown MoS_2 and graphene. These memristive devices are non-volatile and exhibit multiple conductance levels, which cause them to behave as synapses. Also, these devices exhibit near linear weight update with identical input pulses, and obey asymmetric Hebbian learning rule, which is advantageous for their applications in unsupervised learning. The devices exhibit excellent room temperature data retention for ~10^4 s. Additionally, the devices exhibit STP, and undergo LTP and LTD for > 10^4 s. These MoS_2/graphene memristive devices show the necessary characteristics of a biological synapse, making them perfect for implementation in neuromorphic hardware for machine learning applications.

CHAPTER 4 ULTRA-LOW VARIABILITY MoS_2 SYNAPSES

The contents of this have been published in: Krishnaprasad, A., Dev, D., Han, S.S., Shen, Y., Chung, H.S., Bae, T.S., Yoo, C., Jung, Y., Lanza, M., and Roy, T., 2022. MoS_2 Synapses with Ultra-low Variability and Their Implementation in Boolean Logic. ACS Nano, 16(2), p.2866-2876.

4.1 Introduction

The proof-of-concept device configuration is modified to a cross-point Ti/Au/MoS_2/Ti/Au device stack. In this chapter, we demonstrate MoS_2 based synapses with Ti/Au as the bottom and top electrodes. These devices exhibit ultra-low C-C and D-D variability in SET voltage and RESET power distributions. The synapses exhibit low C-C and D-D variability in weight update characteristics as well, comparable with the industry compatible a-Si based synapses.[67] We demonstrate the existence of 26 distinct conductance states in these devices, with a retention of at least 300 s for each of these states. These devices exhibit excellent endurance by maintaining a consistent ON/OFF ratio for 1000 DC SET-RESET cycles. These exemplary characteristics observed in MoS_2 based devices can be attributed to the underlying switching mechanism which is mediated by the interface between MoS_2 and Ti, corroborated by their area-dependent resistance scaling. Further, temperature dependent I-V measurements confirm space charge limited current (SCLC) to be the dominant transport mechanism.

4.2 Device schematic

The device schematic is shown in **Figure 13(a)**. The device stack consists of Ti/Au bottom electrodes (5 nm/ 100 nm). The active medium is 2D MoS_2 of thickness of ~ 10 nm. Finally, the

top electrode is comprised of Ti/Au of thickness (10 nm/50 nm). The active area of the fabricated devices is systematically varied from 2×2 μm^2 to 50×50 μm^2. The optical microscope image of the device is shown in **Figure 13(b)**. We perform the electrical characterization of the MoS_2/SiO_x devices using Keysight B1500A Semiconductor Device Analyzer in a Janis Cryogenic probe station. The devices are characterized in vacuum (1×10^{-4} mbar).

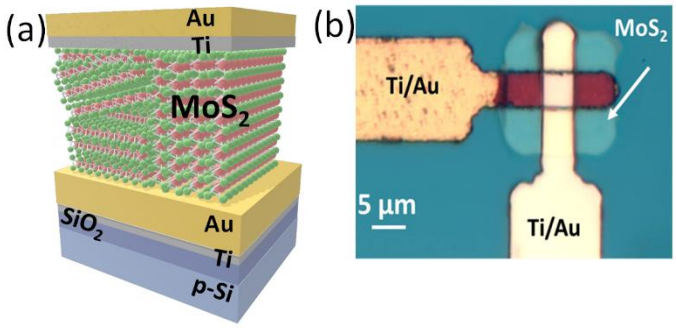

Figure 13: (a) Device schematic of ultra-low variability memristive synapse. (b) Optical microscope image of the Ti/Au/MoS_2/Ti/Au device.

4.3 DC characterization

4.3.1 I-V cycling experiments

The devices are probed in vacuum at a base pressure of 10^{-4} mbar for electrical characterization. **Figure 14** shows the DC I-V characteristics, demonstrating the non-volatile switching of the MoS_2 devices with Ti/Au electrodes. Here the I-V characterization is executed on device of area 5×5 μm^2. To perform this experiment, we apply the bias voltage to the bottom electrode while keeping the top electrode at 0 V during these measurements. These devices do not exhibit abrupt transition from the HRS to LRS, unlike filamentary memristive devices.[18, 30, 32, 33, 39, 40, 68-71] Instead, the devices exhibit a smooth transition from HRS to LRS, hinting at the

role played by the interface in the non-volatile switching behavior. Therefore, we apply a voltage compliance (VC) of 2.5 V for SET and -3 V for RESET, in contrast with the current compliance (CC) applied in filamentary memristive devices during SET, to test the endurance of the device through 1000 DC cycles.

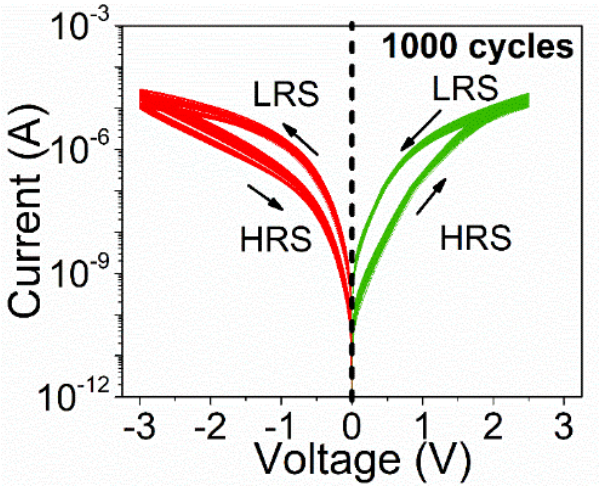

Figure 14: DC cycling: 1000 cycles indicating the low C-C variability and endurance of MoS_2 devices.

4.3.2 Endurance

Further, we extract the OFF and ON state resistance variation to demonstrate the C-C variability as shown in **Figure 15**. The OFF and ON state variation is extracted from the DC *I-V* cycling experiments performed for 1000 times (**Figure 14**). From **Figure 15**, it is evident that the MoS_2 exhibit consistent OFF and ON state resistance for 1000 DC cycles indicating the excellent endurance characteristics.

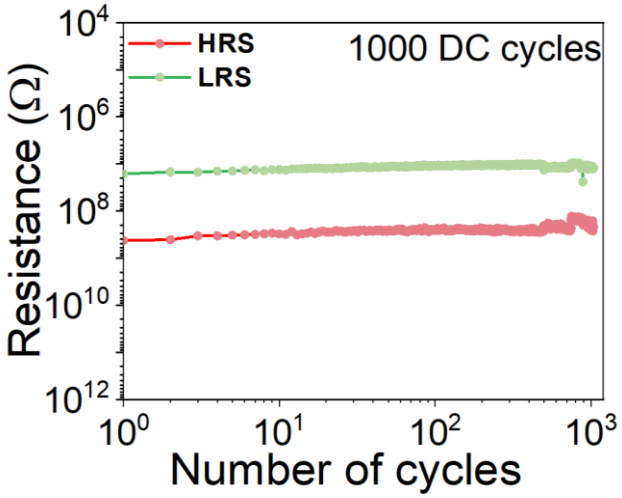

Figure 15: DC endurance of MoS_2 device extracted for 1000 DC cycles. The OFF and ON state resistance of the device were extracted at 0.25 V to investigate the OFF and ON state variation.

4.3.3 Necessity of MoS_2 layer for resistive switching

We designed test structures by patterning and depositing Ti/Au top electrode on the bottom Ti/Au electrode. These test structures went through the exact same processing steps as the MoS_2 devices, including sulfurization at 780 ^oC. The schematic of the test structure (without MoS_2) and the I-V characteristics are shown in Figure **16(a-b)**.

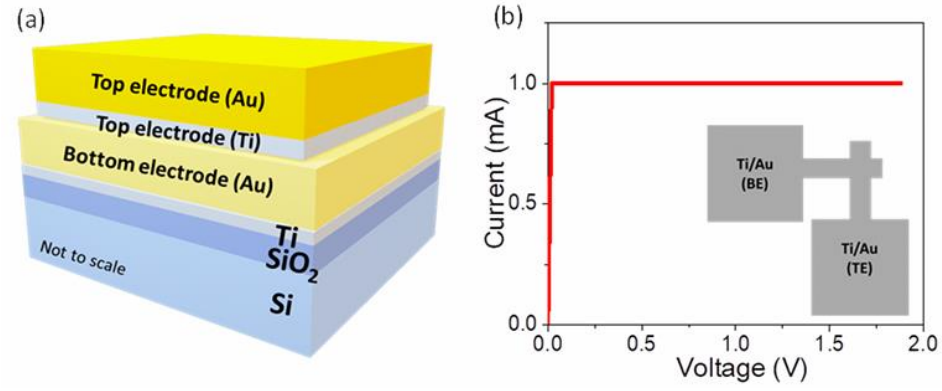

Figure 16: (a) Schematic of test structure with Ti/Au/Ti/Au. (b) I-V characteristics showing a short between the top and bottom electrode, indicating that MoS_2 is required for resistive switching. Inset: Layout schematic of the structure.

4.3.4 Role of Ti (top electrode) in resistive switching

We set out to confirm if Ti is necessary for the low C-C variability observed in the resistive switching. Hence, we fabricated test devices with Au top electrode while keeping Ti/Au (bottom electrode) same as the main device and measured their DC switching characteristics for multiple cycles. The DC cycling was performed on 6 different devices of area 5×5 μm^2. The resistive switching observed in these devices indicate high variability from one cycle to another and is consistent over multiple devices, as shown in **Figure 17(a-b)**.

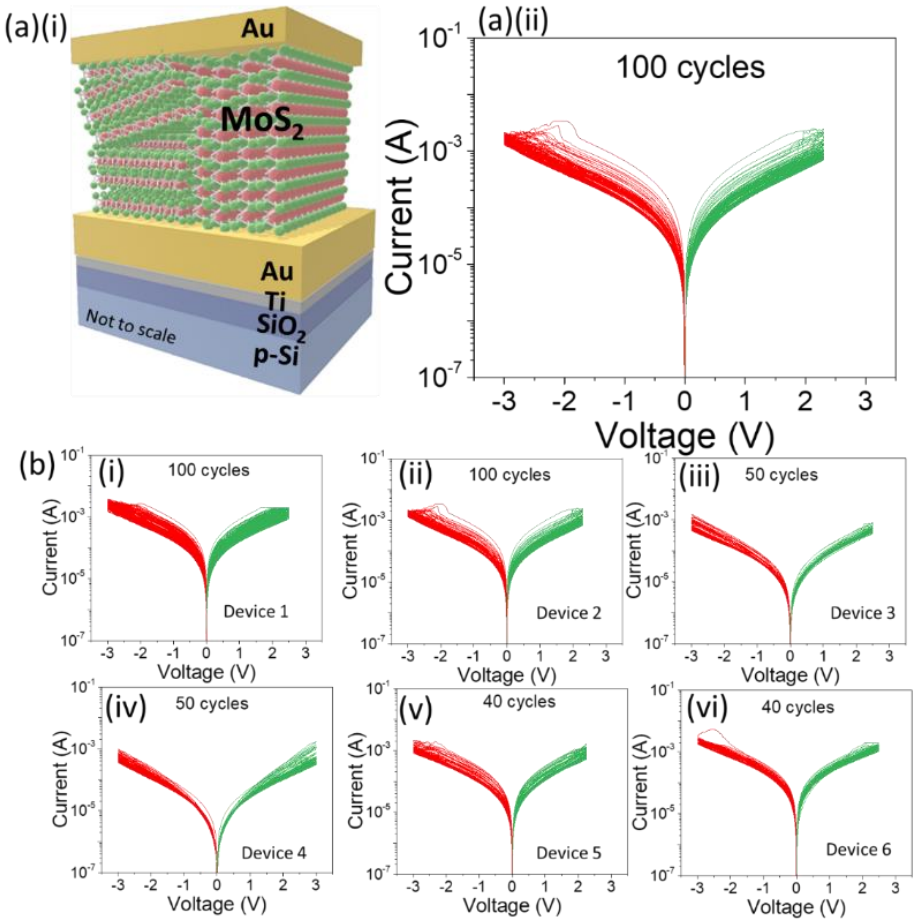

Figure 17: (a)(i) Ti/Au/MoS_2/Au (bottom to top) device schematic. (ii) DC characteristics of Ti/Au/MoS_2/Au device for 100 DC cycles showing high C-C variability. (b)(i-vi) DC characteristics of 6 Ti/Au/MoS_2/Au device exhibiting high C-C variability indicating that Ti is necessary for obtaining low C-C variability.

4.3.5 C-C variability in SET voltage and RESET Power distribution

To evaluate the variation in the SET voltage and RESET power, our MoS_2 device is cycled for 100 times by enforcing a CC keeping the maximum current density at 40 A/cm^2. The voltage at which the current through the device reaches this maximum current density is considered to be the SET voltage. Devices of area 2 × 2 µm^2 are probed for comparing the device performance with industry compatible a-Si/Ag-Cu devices, reported by Yeon *et al*, [67] for SET voltage and RESET power variation. The SET voltage distribution comparison is show in **Figure 18**. The histogram of the SET voltage variation of our MoS_2 device is shown in **Figure 18(i)**. The device exhibits a narrow distribution in the SET voltage with a range of only 0.04 V. In contrast, the histogram of SET voltage variation in a-Si/Ag-Cu device (**Figure 18(ii)**) exhibits a range of 0.45 V, confirming the exemplary ultra-low C-C variability of MoS_2 based devices.

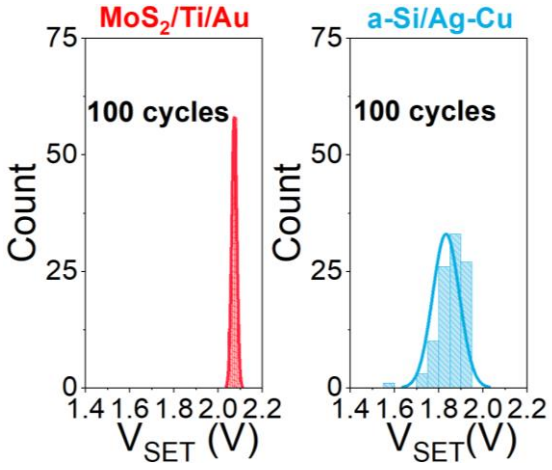

Figure 18: SET voltage comparison of (i) MoS_2/Ti/Au and (ii) a-Si/Ag-Cu based device where MoS_2 device exhibits a tight distribution of 0.04 V for 100 cycles.

The RESET power is calculated using the formula $P = V \times I$, where I is the maximum RESET current, and V is the maximum RESET voltage applied. The RESET power distribution comparison is shown in **Figure 19**.

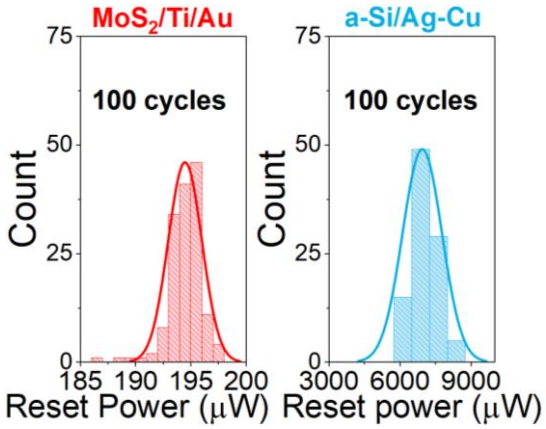

Figure 19: RESET power distribution of (i) MoS_2/Ti/Au device and (ii) a-Si/Ag-Cu device.

4.3.6 D-D variability in SET voltage and RESET Power distribution

It is essential to investigate if the narrow distribution in SET voltages and RESET power is consistent over multiple devices. Therefore, a statistical analysis is performed over 12 different devices of areas 2×2 μm^2, 5×5 μm^2 and 20×20 μm^2. Four devices of each area are measured to obtain the SET voltage and RESET power variation. The SET voltage distribution is obtained by enforcing CC that corresponds to a maximum current density of 40 A/cm^2. Therefore, for the devices with area of 4 μm^2, 25 μm^2 and 400 μm^2, a CC of 1.6 μA, 10 μA and 160 μA is enforced respectively. The individual DC characteristics of these devices are shown in **Figure 20**. From this plot the SET voltage and RESET power distribution are extracted to estimate the D-D variability.

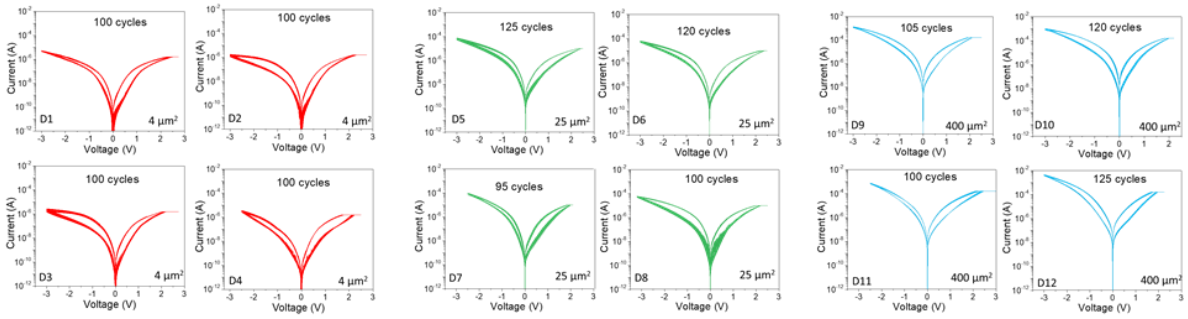

Figure 20:Individual DC characteristics of MoS_2 devices for >100 cycles from which the SET voltage and RESET power distribution is extracted to evaluate the D-D variability.

The SET voltage distribution in 12 different devices for variable areas is shown **Figure 21**. All the devices exhibited tight scatter in the variation indicating that C-C variability is observed over multiple devices. Similarly, the RESET power variation for variable areas is shown in **Figure 22**. All the devices exhibited tight scatter in the variation indicating that C-C variability is observed over multiple devices.

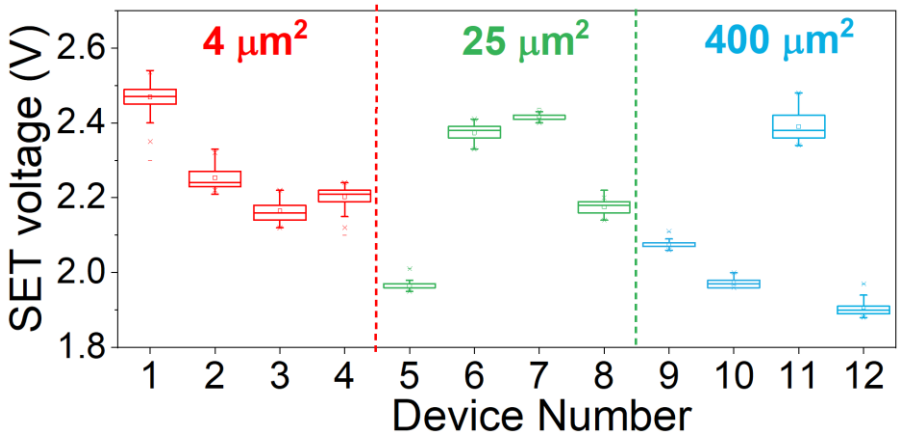

Figure 21: SET voltage distribution observed in 12 MoS_2/Ti/Au devices for >100 cycles.

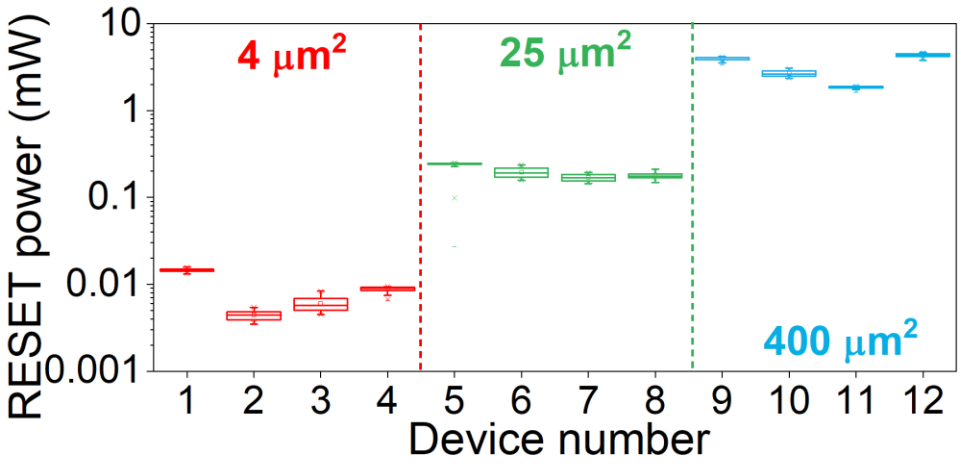

Figure 22: RESET power distribution observed in 12 MoS_2/Ti/Au devices for >100 cycles.

The D-D variability is assessed by extracting the coefficient of variation ($CV = standard\ deviation\ (SD)/mean\ (\mu)$)[72] for both SET voltage and RESET power distribution over 12 different devices. The SET voltage distribution for each device is plotted in **Figure 23**. Similarly, the RESET powers of the 12 devices are plotted in **Figure 24**. Extracting CV over the entire sample set elucidates the low D-D variability observed in MoS_2 devices. The D-D variability increases to only 1.7% in SET voltage variation over the 12 devices. It is worth noting that the CV in SET voltage variation does not exceed 2% indicating the low D-D variability of MoS_2 devices.

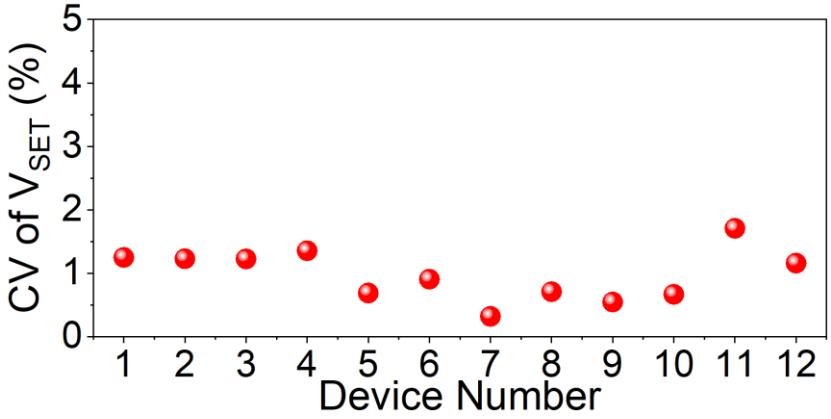

Figure 23: Coefficient of variation (CV) in the SET voltages in MoS_2 based devices.

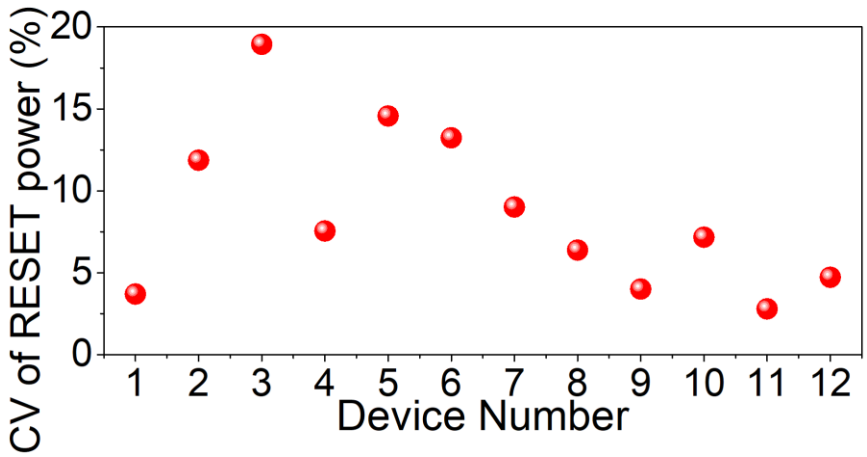

Figure 24: Coefficient of variation (CV) in the RESET power in MoS_2 devices.

4.4 Mechanism

4.4.1 Area dependent resistance scaling

It is necessary to understand the underlying mechanism in MoS_2 synapses responsible for the low C-C variability. The scaling of resistance with respect to area is considered as a clear indication of the switching mechanism in memristive devices. MoS_2 synapses of area 2×2 μm^2, $5 \times 5 \mu m^2$, 10×10 μm^2 and 20×20 μm^2 are probed for DC I-V characteristics as shown in **Figure 25**. Here, each device is measured for 50 DC cycles. From the figure, it is evident that both HRS and LRS scale proportionately to the device area.

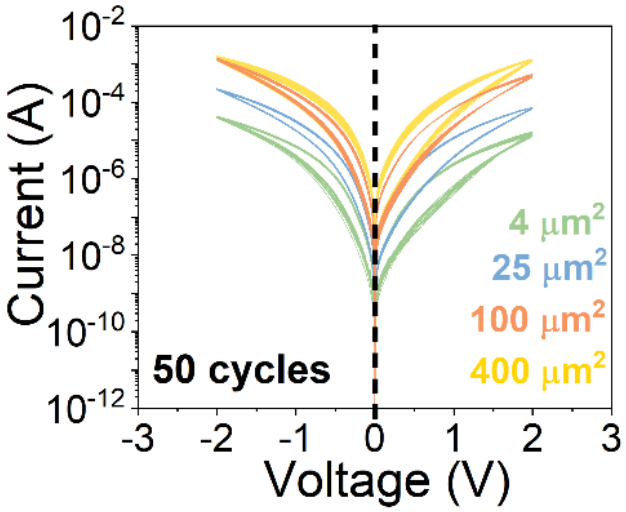

Figure 25: Area-dependent current scaling in MoS_2 devices of 4 different areas measured for ~50 cycles in each case.

The HRS and LRS are extracted at V_{Read}=0.2 V for 50 cycles and the scatter in the resistance values is represented through box plots for each device area in **Figure 26**. Clearly, the HRS and LRS scale linearly with the area insinuating that the dominant switching mechanism is not due to the formation of a conductive filament which is independent of device area.[49]

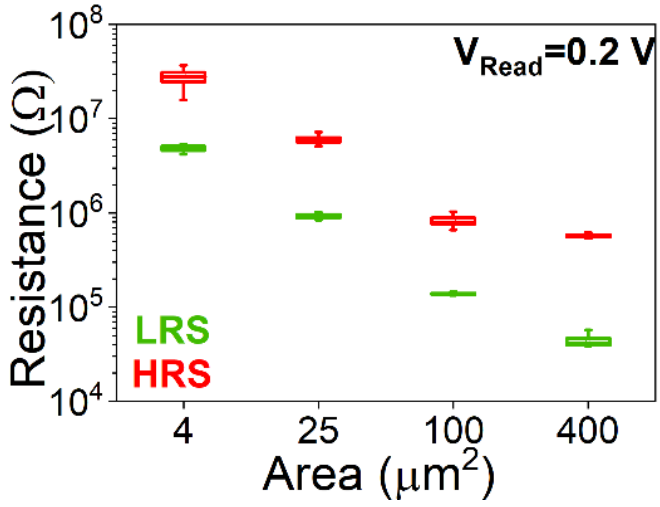

Figure 26: HRS and LRS scaling for the 4 different areas, indicating the role played by the interface at MoS_2/Ti top electrode. The error bars represent data for 50 cycles.

To exhibit the D-D variability in the area dependent resistance scaling characterization, 5 devices of area (25 µm^2, 100 µm2 and 400 µm^2) are characterized for one SET-RESET cycle by enforcing VC of 2.5 V during set and -2.5 V during reset. The OFF and ON state resistances are extracted at V_{Read}= 0.1 V. From **Figure 27**, it is evident that the OFF and ON state resistance varies linearly with the area consistently over multiple device samples, indicating the underlying switching mechanism to be non-filamentary. Further, the devices of each area exhibit tight distribution in OFF and ON states indicating low D-D variability as well.

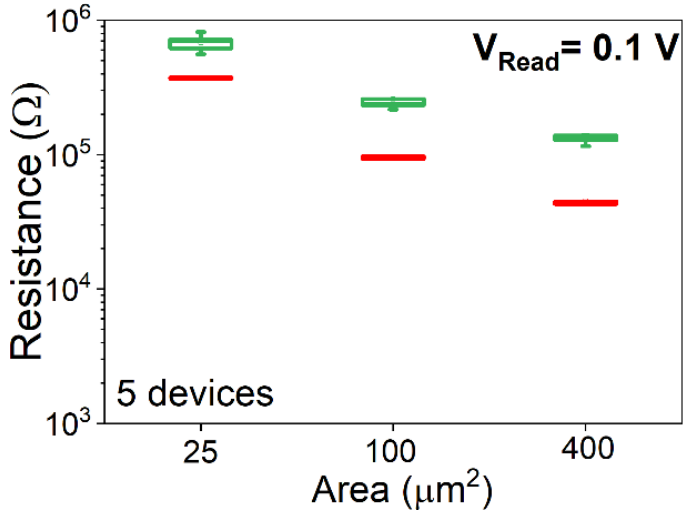

Figure 27: Area-dependent resistance scaling observed in MoS_2 device indicating the switching mechanism is non-filamentary. 5 devices of different areas are characterized for one SET-RESET cycle to extract the OFF and ON state resistance at V_{Read}= 0.1 V indicating low D-D variability.

4.4.2 Temperature dependent I-V measurements

I-V measurements are performed on 4 distinct Ti/Au/MoS_2/Ti/Au devices as a function of temperature which is varied from 300 K to 370 K. The I-V characteristics of a device, with an area of 5 × 5 µm^2, at both HRS and LRS regions as a function of temperature are shown in **Figure**

28(a-b). The current in the HRS and LRS increases as the temperature increases for both bottom electrode injection (positive bias on bottom Au electrode) and top electrode injection (negative bias on bottom Au electrode) conditions.

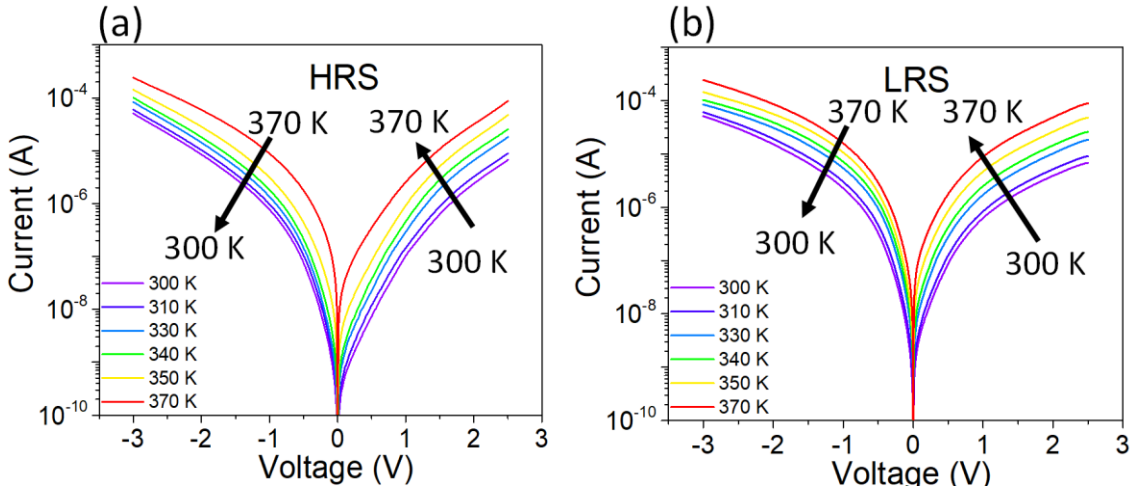

Figure 28: (a): The I-V characteristics of the MoS_2 device in HRS where the temperature dependence is observed. (b): The I-V characteristics of MoS_2 device in LRS where the temperature dependence is observed.

From the figure, it is evident that the I-V characteristics of the MoS_2 device are symmetric in spite of the dissimilar work-functions of the top Ti and bottom Au electrodes.[68] This indicates that the conduction in the HRS is not limited by the Schottky barrier at the electrodes. Among various mechanisms suggested to explain interface mediated switching, space charge limited conduction (SCLC) mechanism has been one of the strongest contenders.[73] The I-V curves obtained for various temperatures are fitted to explain the SCLC theory.[73, 74] The current through the device is given by $I \propto V^{\alpha}$ where α is the slope extracted by plotting I-V in double logarithmic scale. The conduction in the devices that follow the SCLC theory has three distinct regions which can be distinguished by the extracted slopes. The devices where the transport is dominated by SCLC have an initial ohmic region at low voltages. The MoS_2 devices exhibit ohmic

conduction at voltages <0.3 V, indicated by α= 1. At voltages >0.3 V, shallow trap SCLC dominates the conduction indicated by $\alpha \approx 2$. The transition voltage at which the current follows a higher than quadratic relationship is called V_{TFL} where the shallow traps get filled causing the current to increase. The slope at voltages higher than V_{TFL} (0.6 V) is observed to be >>2. The fitting data in both HRS and LRS regions are shown in **Figure 29(a-b)**.

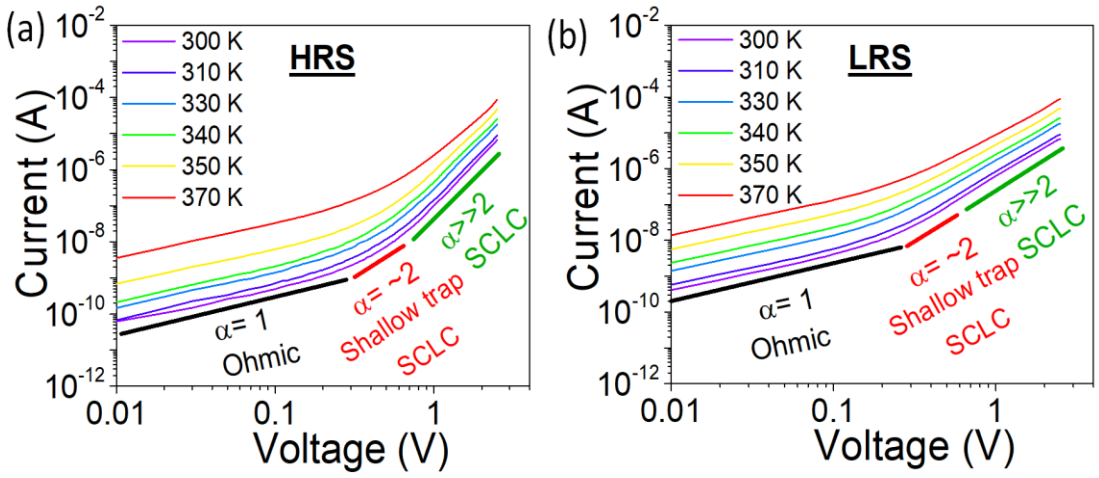

Figure 29: (a): Temperature-dependent I-V at HRS state showing the increase in OFF current with increasing temperature. Ohmic conduction in lower voltage regimes of the HRS states. Shallow trap SCLC, and SCLC conduction mechanisms at higher voltages in HRS. (b): Temperature-dependent I-V at LRS state where the ON current increases with increasing temperature. Ohmic conduction in lower voltage regimes of the LRS states and shallow trap SCLC, and SCLC conduction mechanisms at higher voltages in LRS.

The evolution of the slopes in 3 operating regimes at variable regimes is shown in **Figure 30(a-f)**.

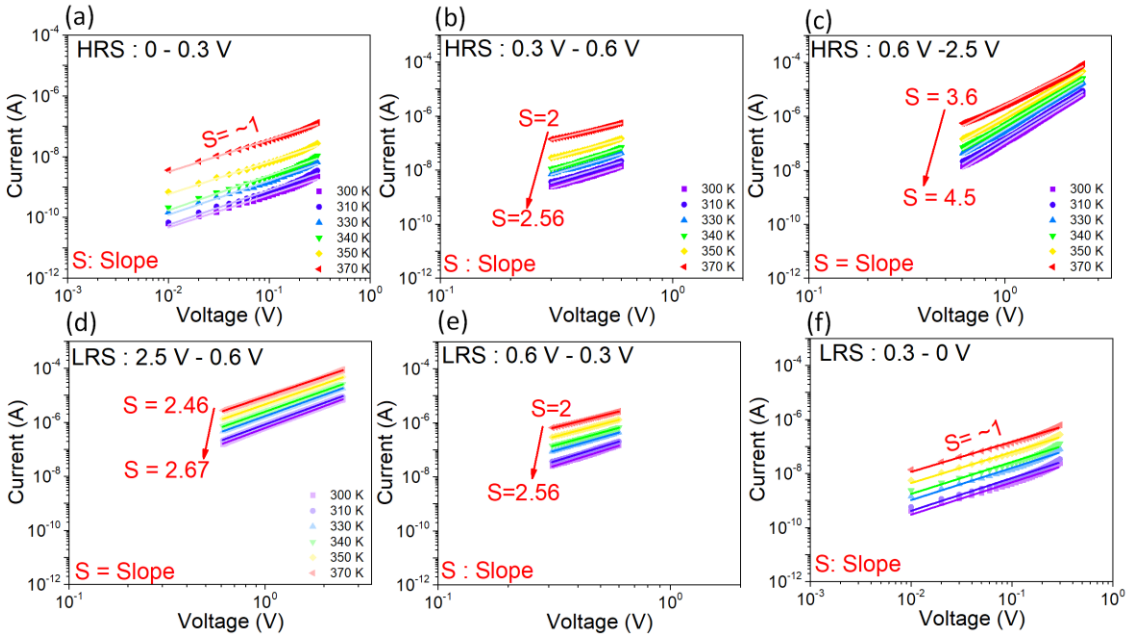

Figure 30: (a): Double logarithmic plot showing ohmic conduction in HRS at voltages <0.3 V. (b): Double logarithmic plot showing shallow trap SCLC in HRS where the current follows a near-quadratic relation with the applied voltage. (c): Double logarithmic plot showing SCLC in HRS where the current follows a higher than quadratic relationship with the applied voltage. (d): Double logarithmic plot showing SCLC in LRS where the current follows a higher than quadratic relationship with the applied voltage. (e): Double logarithmic plot showing shallow trap SCLC in LRS where the current follows a near-quadratic relation with the applied voltage. (f): Double logarithmic plot showing ohmic conduction in LRS at voltages <0.3 V.

The device characteristics at variable temperatures are then fitted with other transport mechanisms like Poole-Frenkel (PF) conduction, Schottky emission and Fowler-Nordheim Tunneling (FNT) to confirm the mechanism in Ti/Au/MoS_2/Ti/Au device is governed by the SCLC theory.

PF conduction: The current density J due to PF emission is governed by the equation[68]

$$J = J_0 \exp\left(\frac{\beta_{PF} E^{1/2} - \emptyset_t}{kT}\right) \quad \text{.....(1)}$$

where J_0 is the low-field current density, $\beta_{PF} = (\frac{q^3}{\pi\varepsilon_0\varepsilon})^{1/2}$, q is the electronic charge, ε_0 is the dielectric constant of the free space, ε is the high frequency dielectric constant, T is the temperature, k is the Boltzmann constant, and $\emptyset_t$ is the trap energy level with respect to the conduction band. To verify the temperature dependence as predicted from the equation defining the PF model, we plot $\ln(J/E)$ as a function of 1000/T as shown in the **Figure 31**. We observe that ln (J/E) does not vary linearly with 1000/T, indicating the transport mechanism does not follow the P-F model.

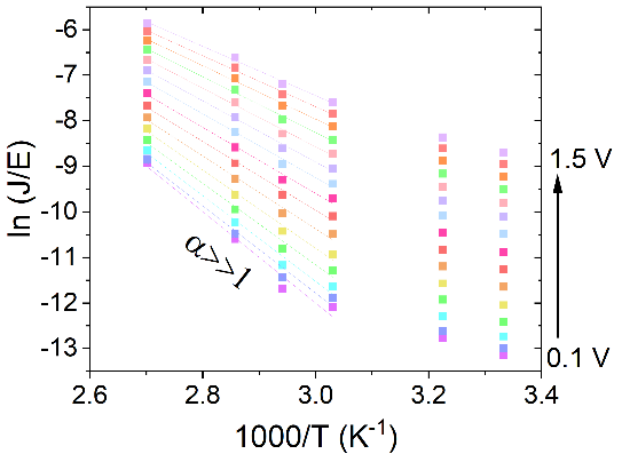

Figure 31: I-V fitting using PF model.

Schottky emission: Schottky emission is one of the key transport mechanisms in interface mediated switching memristors. Schottky emission is described by the equation.[75]

$$I = AT^2 e^{-\frac{q(\phi_{B0} - a\sqrt{V})}{KT}} \quad \text{.....(2)}$$

where A= (area × Richardson constant), a is the barrier lowering factor, T is the absolute temperature, K the Boltzmann constant, q the electron charge, ϕ_{B0} the potential barrier at the interface under zero applied bias. Therefore, ln(I/T^2) is plotted against 1000/T. Under non-

switching regime, linear slope is expected which corresponds to the apparent effective barrier given by $\phi_{B0} - a\sqrt{V}$ under each electric field. From **Figure 32**, we do not observe unit slope indicating that Schottky emission is not the underlying transport mechanism for voltages lower than 0.3 V.

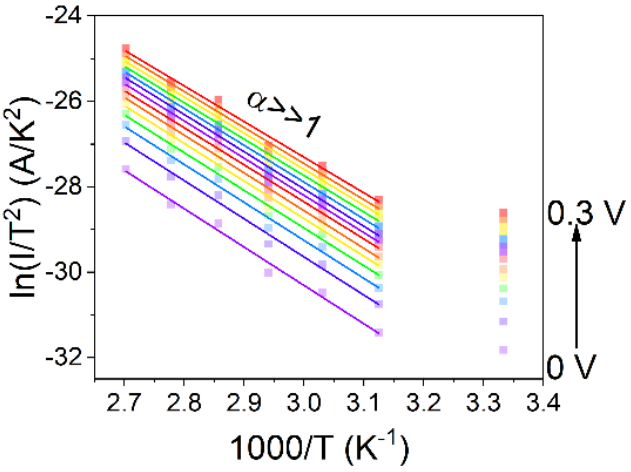

Figure 32: I-V fitting using Schottky emission model.

FNT conduction: The tunneling current through the device is given by the equation[76]:

$$J = CE^2 e^{-\frac{E_0}{E}} \quad \text{.....(3)}$$

where *J* is the tunneling current, and *C* and E_0 are the constants related to the effective electron mass and barrier height. At every temperature, log(J/E^2) is plotted against ($1/E$). If the transport is governed by FNT, log(J/E^2) should vary linearly with ($1/E$). From **Figure 33**, it is observed that there is no evident linear relationship. This proves that FNT is not the dominant transport mechanism at higher electric fields.

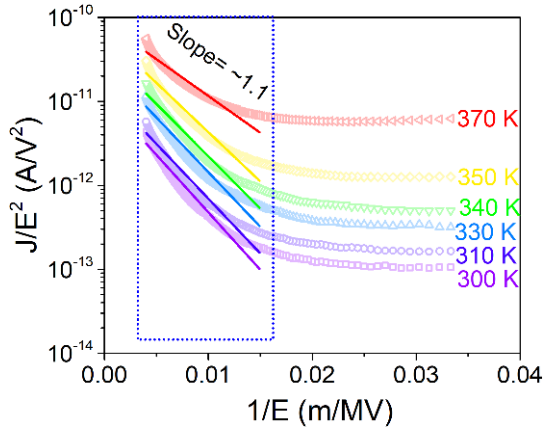

Figure 33: I-V fitting using FNT model.

4.5 Synaptic Characteristics

4.5.1 DC potentiation and depression

The ultra-low variability MoS_2 devices are further characterized as synapses suitable for use in neural network training. DC potentiation and depression measurements are performed by enforcing VC. The MoS_2 devices exhibit 4 distinct potentiation states and 5 different depression states, shown in **Figure 34** rendering preliminary indication of the ability of MoS_2 device to behave like an analog memory.

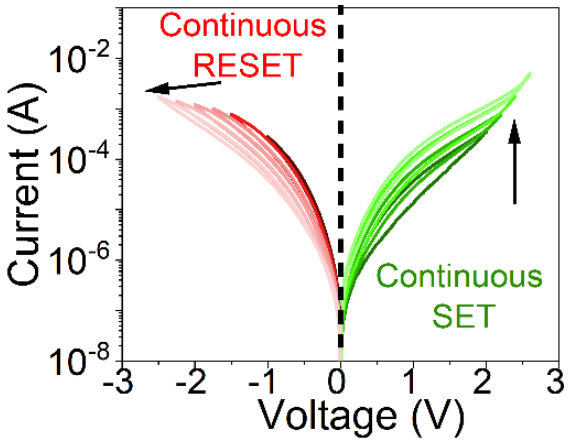

Figure 34: DC potentiation and depression.

4.5.2 Retention

Additionally, the synapse should exhibit substantial retention for at least ~ 300 s which is critical for inference when the synapse is used in a cross bar. The MoS_2 synapse exhibits excellent retention of >300 s for 26 distinct conductance states, as shown in **Figure 35.**

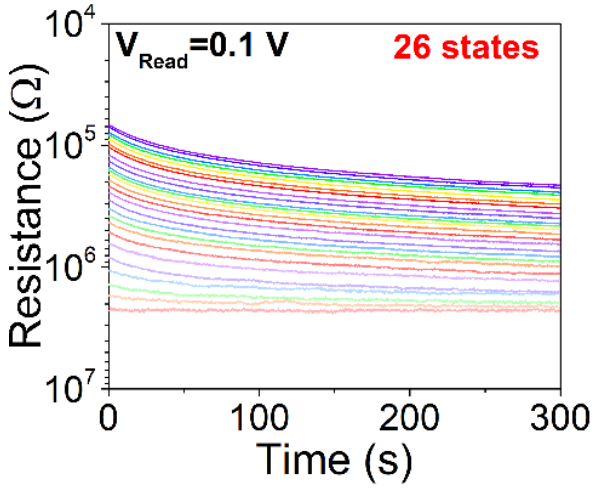

Figure 35: Retention of ~300 s for 26 distinct states.

4.5.3 Pulsed measurements

The conductance weight update is measured on 10 synaptic devices and is compared with the a-Si synapses reported by Yeon et al.[67] for C-C and D-D variability. For obtaining potentiation, 512 identical voltage pulses of duration 1 ms and amplitude 2 V are applied. To induce pulsed depression, 512 identical voltage pulses of 1 ms duration and amplitude -2.25 V are applied. The train of potentiation and depression pulses are repeated for 100 cycles, write current is measured, and write conductance is extracted for both potentiation and depression. The write conductance, normalized to the maximum conductance obtained, is plotted as a function of the

pulse number (n), as shown in the weight update curve in **Figure 36** for all 100 cycles, showing extremely low C-C variability. The pulsing scheme is shown as the inset of **Figure 36**.

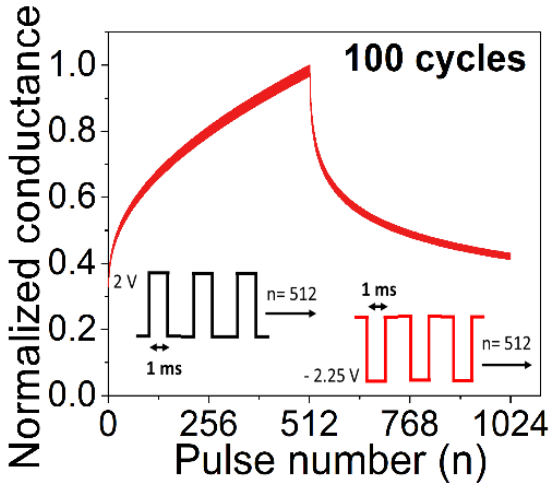

Figure 36: Weight update characteristics repeated 100 times. Inset: Pulsing scheme for each cycle.

To assess the C-C variability, ANL is extracted by the following equation.[67]

$$ANL = \frac{G_P(\frac{n}{2}) - G_D(\frac{n}{2})}{G_{max} - G_{min}} \quad \text{.....(4)}$$

where $G_P(\frac{n}{2})$ and $G_D(\frac{n}{2})$ are the median conductance values along potentiation and depression respectively; G_{max} and G_{min} are the maximum and minimum conductances, respectively. The ANL variation of 100 cycles in MoS_2 synapse is compared with ANL of 10 cycles in the a-Si/Ag-Cu synapse[67] as shown in **Figure 37(a)**. The MoS_2 synapse exhibits a tighter distribution in the ANL over 100 cycles in comparison to the modest 10 cycles observed in a-Si/Ag-Cu synapses. The weight update measurements are repeated on 10 distinct synaptic devices for 50 cycles each and the mean ANL is extracted for each device. The mean ANL over 50 cycles for 10 MoS_2 synapses is plotted and compared with the mean ANL obtained for 10 a-Si/Ag-Cu[67] synapses cycled only for 5 times as shown in **Figure 37(b)**. The extraction of SD in ANL over multiple

cycles provides the precise estimation of the C-C variability in the devices. Therefore, the SD in ANL is extracted for each synapse over 50 cycles. The extracted SD of the MoS_2 synapses (10 devices, 50 cycles each) is then compared to the SD of the a-Si/Ag-Cu[67] synapses (10 devices, 5 cycles each) as shown in **Figure 37(c)**. The MoS_2 synapses exhibit compact distribution in SD with a range of 0.02 which is superior to the SD distribution observed in a-Si/Ag-Cu[67] synapses where the range is 0.08.

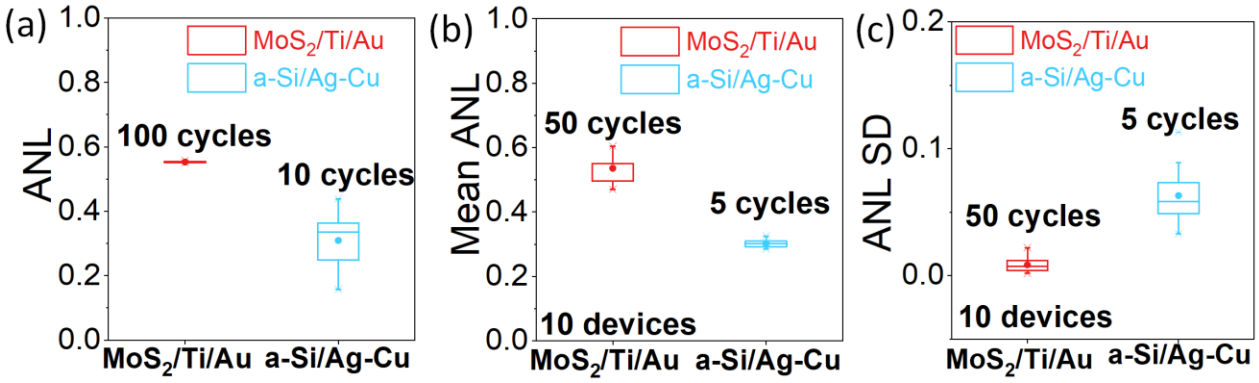

Figure 37: (a) ANL comparison of MoS_2 synapse (over 100 cycles) with a-Si synapse (over 10 cycles). MoS_2 synapses exhibit a tighter distribution in the ANL over the entire 100 cycles. (b) Mean of the ANL extracted for 50 cycles plotted for 10 MoS_2 devices shows low variation. This is compared with the mean of the ANL extracted for 5 cycles plotted for 10 a-Si devices. (c) The standard deviation (SD) of ANL for 50 cycles in MoS_2 devices is compared with the SD of ANL for 5 cycles in a-Si based devices for 10 devices in each case.

4.6 Conclusion

In conclusion, we have demonstrated ultra-low variability synapses using MoS_2 as the switching medium, and Ti/Au as the bottom and top electrodes. These devices exhibit excellent DC endurance characteristics while maintaining low cycle-to-cycle variability. Additionally, a comparison of MoS_2 synapses with a-Si/Ag-Cu synapses establishes even lower C-C variability in their weight update characteristics. The switching is facilitated by the interface between MoS_2 and Ti (top electrode) indicated by the area dependent resistance scaling and the temperature dependent

I-V measurements. From the experimental results, the dominant conduction mechanism is observed to be SCLC. Further, the results obtained by MoS_2 devices with pristine Au electrodes corroborate the necessity of Ti as the top electrode to obtain ultra-low variability.

CHAPTER 5 MATERIAL CHARACTERIZATION

The contents of this have been published in: Krishnaprasad, A., Dev, D., Han, S.S., Shen, Y., Chung, H.S., Bae, T.S., Yoo, C., Jung, Y., Lanza, M., and Roy, T., 2022. MoS_2 Synapses with Ultra-low Variability and Their Implementation in Boolean Logic. ACS Nano, 16(2), p.2866-2876.

5.1 Introduction

Material characterization techniques like TEM, EELS and XPS are employed on ultra-low variability synapses to verify the robustness of the device stack and to understand the underlying switching mechanism. The TEM results indicate that the devices are robust post biasing. The EELS and XPS exhibit the composition of the device stack to corroborate the ultra-low variability behavior.

5.2 TEM characterization

5.2.1 TEM and EDS

Cross-sectional TEM is utilized to assess the device stack as shown in **Figure 38(a)**. The TEM image shows the layered growth of MoS_2 of thickness ~10 nm. Further, the chemical composition of the device stack is analyzed by the elemental energy dispersive X-ray spectroscopy (EDS). The EDS maps clearly reveal the presence of MoS_2, bottom electrode (Au) and top electrode (Ti/Au) as shown in **Figure 38(b)**.

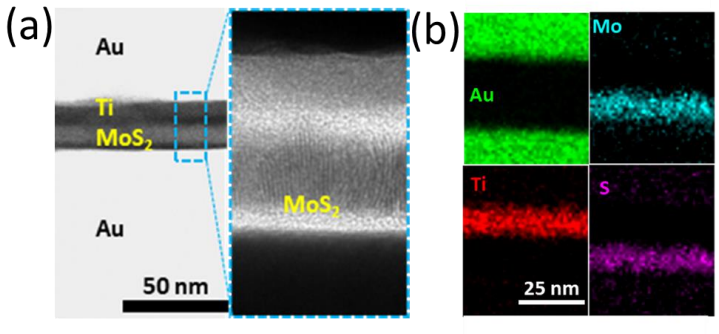

Figure 38: (a) Cross-sectional TEM of the device. (b) EDS spectra showing the signature of MoS_2 and the electrodes; Au (bottom) and Ti/Au (top).

5.2.2 TEM and EELS characterization

To confirm the layer structure of MoS_2 and analyze the chemical composition of the sample before and after biasing, high resolution cross-sectional TEM was used. One biased device (100 DC cycles) and one pristine device from the same Ti/Au/MoS_2/Ti/Au sample with the lateral size of 4×4 μm^2 were analyzed. **Figure 39(a)** shows the top-view Scanning Electron Microscope (SEM) image of the pristine device; the location at which the FIB cut was done is marked with a black rectangle (*i.e.*, the protective Cr/C film deposited before the FIB cut). From the cross-sectional TEM image and the Electron Energy Loss Spectroscopy (EELS) profiles obtained in the pristine device (**Figures 39(b)** and **39(c)**) it is concluded that the structure of the fabricated device is Au/Ti/Si/MoS_2/Au (from up to down). From **Figure 39** two unexpected and critical observations are made. First, there is an ultra-thin layer of Si in between the MoS_2 and the Ti layer, which most probably migrated from the Si/SiO_2 substrate due to the ~780 ºC applied during the sulfurization step adopted for MoS_2 growth. Secondly, while the structure of the MoS_2 is clearly layered, the orientation of its individual 2D layers varies from 0º to 90º with respect to the horizontal substrate plane (**Figures 39(b)** and **39(e)**). Statistically, we find that this structure remains unaltered for the

biased device (**Figures 39(d-e)),** indicating that the Au/Ti/Si/MoS_2/Au (up to down) stack is stable to the electrical stresses applied. It is worth noting that, as the switching mechanism is distributed (*i.e.*, shows area dependence and is analog, meaning that it is not based on the formation of local filaments), the observations in **Figure 39(e)** correspond to the switching regions. Most memristors employing MoS_2 as the switching medium[20, 77] were based on multilayer stacks of horizontally-aligned 2D MoS_2 planes, and in all cases the switching was filamentary and resulted in high C-C and D-D variability. On the contrary, the unconventional structure of our devices (based on a Si-rich highly crystalline MoS_2 of varying layer orientation) promotes smooth ion migration across it and results in analog resistive switching with ultra-low C-C and D-D variability. Among all mobile species within this Au/Ti/Si/MoS_2/Au structure, most probably the migration of O is the one responsible for the switching. The reasons that support this claim are: i) the signals of Mo, S, Si and Ti in the EELS profiles do not show significant changes, while the O profile does; ii) the MoS_2 is highly crystalline, meaning that forming S vacancies would require the applications of voltages much higher than those applied in our experiments (*i.e.*, up to 2 V in Figure 2);[78] iii) multiple studies have reported the formation of O-vacancies in memristive devices at low electrical fields;[79] and iv) the low variability is not observed without the Ti film which is known to be a very good O adsorber.

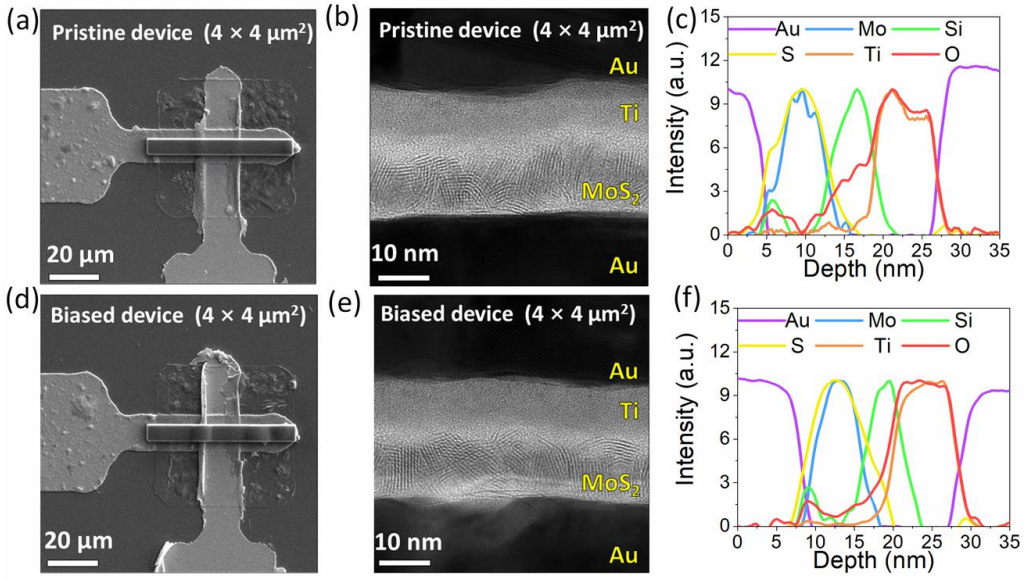

Figure 39: (a) SEM image of the pristine device with the FIB cutting location marked. (b) Cross-sectional TEM image of the lateral structure of the same pristine device in (a). (c) EELS map of the pristine device. (d) SEM image of the biased device (cycled 100 times) with the FIB cutting location marked. (e) Cross-sectional TEM image of the lateral structure of the same biased device in (d). (f) EELS map of the biased device. Scale in (a) and (d): 5 μm, scale in (b) and (e): 10 nm.

5.3 XPS Characterization

X-ray Photoelectron Spectroscopy (XPS) measurements were performed on a film of Au/Ti/MoS_2 (up to down) deposited using the same process used for the device fabrication. The XPS depth profiling is performed at 10 s intervals on the stacked film, and elemental spectra for Ti (2p), Mo (3d) and S (2p) were obtained after each etch step. From **Figure 40(a)**, clear signatures of TiS_2, TiOS and TiO are observed at 456.2 eV, 457.6 eV and 455.1 eV respectively.[80, 81]The presence of TiS_2 and TiOS indicate the migration of sulfur ions from the underlying MoS_2 layer post top electrode deposition. Furthermore, XPS spectra **Figure 40(a)** on pristine film reveals the formation TiO and TiOS, indicating the reservoir of 'O' vacancies is due to the presence of Ti contact metal. **Figure 40(b)** shows the XPS spectra of Mo (3d) where the binding energy peaks at

228.7 eV, 227.3 eV and 233.1 eV correspond to MoS_2, $MoSi_2$ and MoO_3 respectively.[82-84] The presence of $MoSi_2$ peak corroborates the observation by TEM and EELS. **Figure 40(c)** shows the XPS spectra of S (2p) where the peak binding energy at 162.4 eV signifies the presence of MoS_2, the peak at 161.09 eV corresponds to TiS_2, and the peak at 163.4 eV corresponds to TiOS.[80, 85]

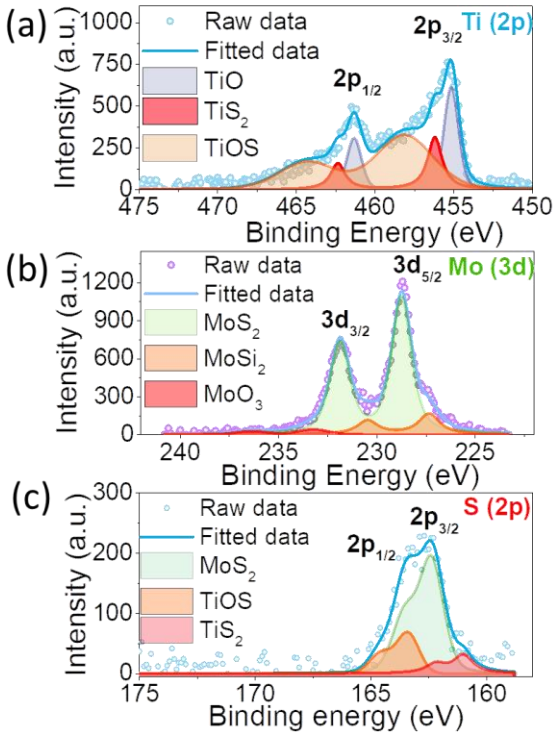

Figure 40: XPS spectra of Ti (2p), Mo (3d) and S(2p). (a) The binding energies of the $2p_{3/2}$ peaks are found at 455.1 eV, 456.2 eV and 457.6 eV correspond to the presence of TiO, TiS_2 and TiOS. (b) Mo ($3d_{5/2}$) peaks at 228.7 eV, 227.3 eV and 233.1 eV correspond to the presence of MoS_2, $MoSi_2$ and MoO_3. (c) S (2p) spectra indicating the formation of MoS_2, TiS_2 and TiOS due to the presence of peak binding energies at 162.4 eV, 161.09 eV and 163.4 eV.

5.4 Conclusion

In conclusion, this chapter reveals the robustness of the devices through the TEM characterizations performed on the pristine and biased devices. The images of pristine and biased devices confirm no physical degradation in the devices after cycling. The ultra-low variability is

enabled by the interface rendered by Ti/Au top contact on the Si-rich MoS_2 layers of mixed orientation is further corroborated by EELS and XPS characterization.

CHAPTER 6 LOGIC GATE IMPLEMENTATION

The contents of this have been published in: Krishnaprasad, A., Dev, D., Han, S.S., Shen, Y., Chung, H.S., Bae, T.S., Yoo, C., Jung, Y., Lanza, M., and Roy, T., 2022. MoS_2 Synapses with Ultra-low Variability and Their Implementation in Boolean Logic. ACS Nano, 16(2), p.2866-2876.

6.1 Introduction

To establish the viability of these ultra-low variability synapses for circuit implementations, we proceed to connect multiple such synapses to demonstrate Boolean logic gate functionalities through vector matrix multiplication. Recently, we demonstrated LIF neurons using MoS_2 as the switching medium and Ag as the top electrode in a Au/MoS_2/Ag heterostructure.[86] Here, we integrate the MoS_2 synapses with those MoS_2 LIF neurons. The connection of MoS_2 synapses with MoS_2 neurons highlights the possibility of obtaining a monolithically integrated circuit of synapses and neurons. Typically, for the applications requiring the integration of neurons and synapses, these elements are realized with dissimilar materials necessitating heterogeneous integration. This process is wrought with issues in substrate incompatibility, cost and thermal budget. For the realization of large-scale circuitry, such as deep neural networks, monolithic integration of synapses and neurons is helpful. The integration of MoS_2 synapses and neurons to realize AND, OR and NOT logic gates is shown in **Figures 42-44**. MoS_2 synapses and an external bias resistor are connected to one MoS_2 neuron. For enabling "integrate and fire" behavior of the neuron, a capacitor (C_0 = 100 nF) is connected as an integrator in parallel with the neuron. For the implementation of logic gates, voltage pulse trains of amplitude V_i are applied as input to the i^{th} synapse bearing a certain weight (conductance) W_i, which results in current flowing through the

path as $I_i = V_i \times W_i$ by Ohm's law. Thus, the current through all 'N-1' synapses and the external bias resistor add up by Kirchoff's law to $I = \sum_{i=1}^{N} V_i W_i$ which essentially is the vector matrix product of the input voltage and weight matrix. This total current at node 'B' (shown in **Figure 42(a)**) builds the potential across the capacitor C_0, charging it up. When V_B (shown **Figure 42(a)**) exceeds the threshold voltage of the threshold switching memristor (TSM), the TSM switches on, allowing the capacitor C_0 to discharge through it. This causes V_B to reduce, which in turn switches the TSM back to its HRS. The process of charging and discharging of the capacitor continues, resulting in current spikes at the output of the circuit. To realize AND and OR logic gates, an input of '0' is represented by a train of low voltage pulses (amplitude 0.01 V, pulse width 1 ms), and '1' is represented by a train of high voltage pulses (amplitude 0.7 V, pulse width 1 ms). Similarly, for NOT gate implementation, an input of '0' is represented by a train of low voltage pulses (amplitude -0.01 V, pulse width 1 ms), and '1' is represented by a train of high voltage pulses (amplitude -0.7 V, pulse width 1 ms). However, the input to bias resistor is varied since it is behaves like a differential resistor. For the bias resistor, a constant voltage of -0.7 V (AND and OR gate) and +0.7 V (NOT gate) is applied. The bias resistance is adjusted for the realization of each logic operation. If the circuit parameters determined by the synapse resistances allows the neuron to fire, the output is recorded as '1', else if the neuron does not fire, the output is considered as '0'. The voltage pulse trains are applied for 5 s.

6.2 Ti/Au/MoS_2/Ti/Au synapses retention

The MoS_2 synapse utilized for the logic gate implementation are set at a particular conductance state (weight of the synapse). The MoS_2 synapse replaces the resistor in the R-C

circuit required for obtaining the neuronal characteristics using MoS_2 TSM device. The individual device resistances of the MoS_2 device used in AND, OR and NOT gate is shown in **Figure 41(a)**. The retention of >100 s is observed in MoS_2 synapses used for AND gate implementation as shown in **Figure 41(b)**. Similarly, the retention for >100 s is measured for the synapses used for OR gate (**Figure 41(c)**) and NOT gate (**Figure 41(d)**).

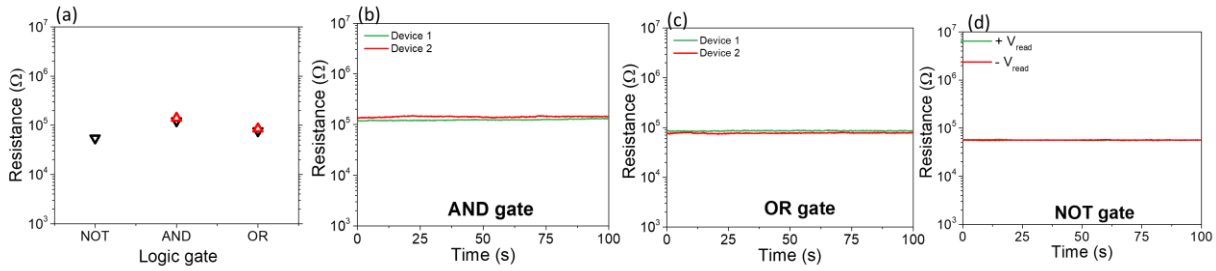

Figure 41: (a): Individual synapse resistance prior to the logic gate implementation. (b): Retention of >100 s observed in MoS_2 synapses prior to the AND gate implementation. (c): Retention of >100 s observed in MoS_2 synapses utilized for OR gate implementation. (d). Retention of >100 s observed in MoS_2 synapses at V_{Read}= ± 0.7 V utilized for NOT gate implementation.

6.3 AND gate

The circuit used for the two-input AND gate realization is shown in **Figure 42(a)**. A bias resistor (R_O) of 100 kΩ is connected to the MoS_2 synapses S1 and S2. The input pulsing scheme and the spiking output from the MoS_2 neurons for 1 s time period for various input combinations is shown in **Figure 42(b)**. The voltage pulse trains are applied for 5 s and the number of spikes is extracted and plotted as a function of inputs and time duration as shown in **Figure 42(c)**. The figure shows the implementation of AND gate where spikes are obtained for input (1 1) and the absence of spikes is observed for the other input combinations, *viz.* of (0 0), (0 1) and (1 0).

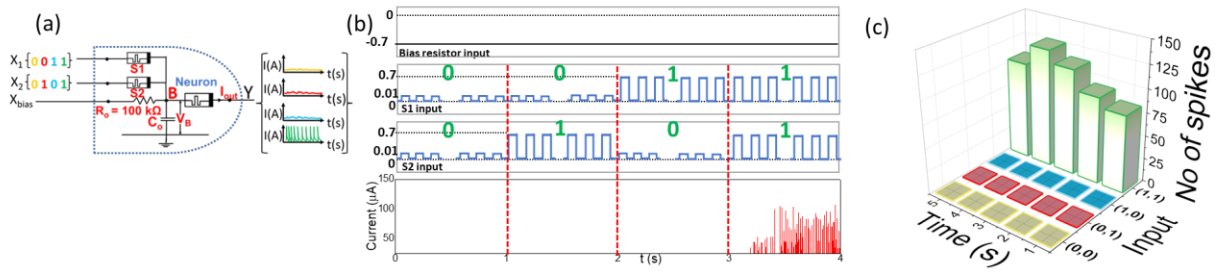

Figure 42: (a): Schematic of two-input AND gate implementation. b: Spiking output with corresponding inputs applied to the circuit. (c): Number of current spikes obtained from MoS_2 neuron as a function of time for (0,0), (0,1), (1,0) and (1,1) conditions.

6.4 OR gate

For the implementation of OR gate, the same measurement methodology as AND is used. The input pulse parameters are the same as those for the AND gate. However, we change the bias resistor (R_O) to a higher resistance of 470 kΩ. The use of a higher resistance effectively reduces the equivalent resistance of the RC circuit, which is necessary to obtain spiking in (0 1), (1 0) and (1 1) conditions. The schematic of the OR gate indicating the various input combinations and their corresponding outputs are shown in **Figure 43(a)**. Similar to the AND gate, the input pulsing scheme and spiking output for 1 s is shown in **Figure 43(b)**. The response of the OR gate for 5 s and the spiking output as a function of the input combination and time duration is shown in **Figure 43(c)**. The figure depicts the implementation of OR gate where output spikes are observed for (0 1), (1 0) and (1 1) input combinations and no spikes are observed for (0 0) condition. The number of spikes is higher for the (1 1) combination in comparison to the (0 1) and (1 0) combinations due to decreased equivalent resistance of the RC circuit.

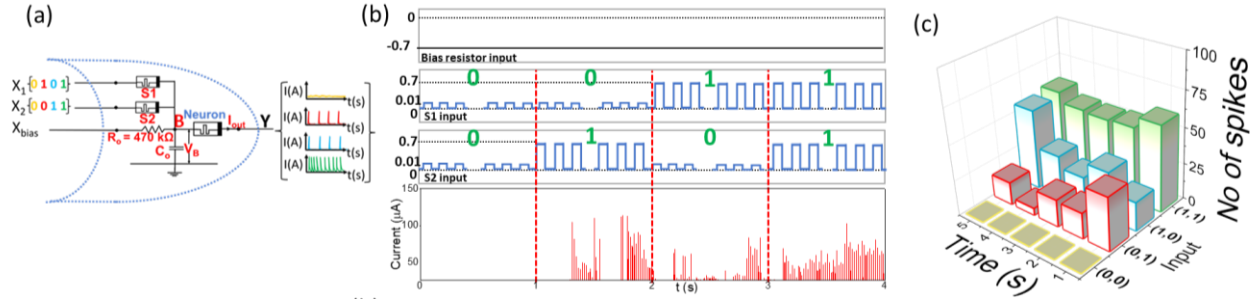

Figure 43: (a)Schematic of two-input OR gate implementation. b: Spiking output with corresponding inputs applied to the circuit. (c): Number of current spikes obtained from MoS_2 neuron as a function of time for (0,0), (0,1), (1,0) and (1,1) conditions.

6.5 NOT gate

The NOT gate is implemented using one MoS_2 synapse and a bias resistor (R_O) of resistance 47 kΩ. The schematic of the NOT gate is shown in **Figure 44(a)**. The input pulses corresponding to '0' and '1' states are applied to the MoS_2 synapse. It should be noted that for implementing the NOT gate, the MoS_2 synapse plays the role of a differential resistor. A constant voltage of 0.7 V is applied to the bias resistor. The input pulsing scheme and spiking output is shown in **Figure 44(b)**. Further, the number of spikes is plotted as a function of time duration and inputs as shown in **Figure 44(c)**.

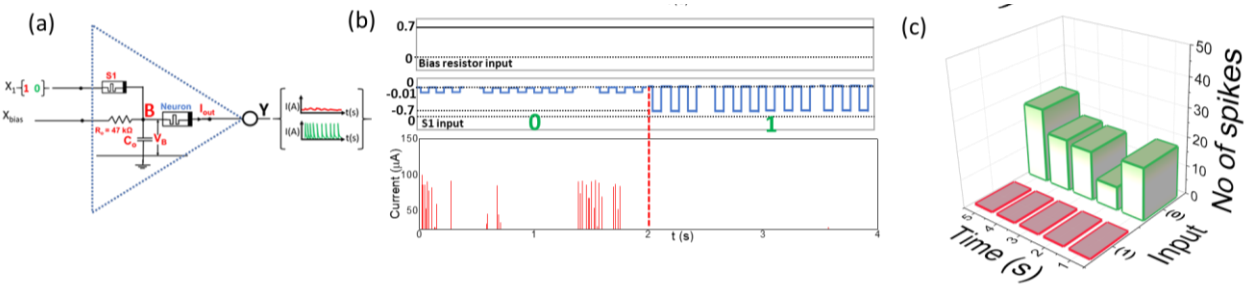

Figure 44: Schematic of NOT gate implementation. b: Spiking output with corresponding inputs applied to the circuit. (c): Number of current spikes obtained from MoS_2 neuron as a function of time for (0) and (1) input conditions.

6.6 Conclusion

In conclusion, the ultra-low variability synapses are integrated with LIF neurons based on the same materials system, *viz.* MoS_2, to implement Boolean logic. Here, memristive AND, OR and NOT logic gates are realized using MoS_2 based synapses and neurons. This study clarifies the viability of these devices for future neuromorphic applications and edge computing.

CHAPTER 7 STACK ENGINEERING in MoS_2 SYNAPSES

7.1 Introduction

In this chapter, we present the results obtained from stack engineered MoS_2 synapses on low C-C variability. The MoS_2 synapses with Ti/Au electrodes exhibit ultra-low C-C variability in SET voltage(maximum coefficient of variation (CV)=1.79 %), RESET power and weight update characteristics.[87] The low variability is attributed to the presence of Ti which creates a special interface between the top electrode and the poly-crystalline MoS_2 film with grains of mixed layer orientation. However, these devices suffer from a low dynamic range (G_{max}/G_{min}) of 2. A larger dynamic range allows improved mapping capability of the weights to the algorithms.[25] Therefore, the development of synaptic devices with high G_{max}/G_{min} ratio and low C-C variability is highly desired. In that regard, we have used stack engineering to change the switching medium from MoS_2 to MoS_2/SiO_x while retaining Ti/Au as the top and bottom electrodes.

7.2 Device schematic

The schematic of the MoS_2/SiO_x device is shown in **Figure 45(a)**. The bottom, Ti/Au (5 nm/100 nm) electrode is patterned and deposited on a p-Si/SiO_2 (280 nm) substrate using conventional photolithography, e-beam evaporation and lift-off processes. A Mo film of ~3 nm thickness is patterned and deposited followed by lift-off. The switching medium MoS_2 (~ 10 nm) is obtained by the sulfurization of Mo. SiO_x (~20 nm) is deposited, followed by the deposition of the top Ti/Au (30 nm/30 nm) electrode using e-beam evaporation without breaking vacuum. The cross-sectional TEM of the active area of $4 \times 4\ \mu m^2$ is performed to prove the stack composition

as shown in **Figure 45(b)**. We observe CVD MoS_2 layers of mixed orientation. The layers are oriented from 0° to 90 ° with respect to the basal plane. We perform the electrical characterization of the MoS_2/SiO_x devices using Keysight B1500A Semiconductor Device Analyzer in a Janis Cryogenic probe station. The devices are characterized in vacuum (1×10^{-4} mbar).

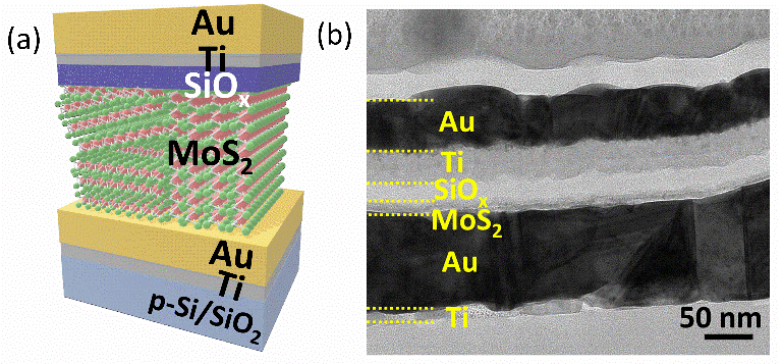

Figure 45: (a) Device schematic. (b) Cross-sectional TEM image of the MoS_2 device along the active area, indicating the configuration of the device stack.

7.3 Device Characterization

7.3.1 DC characterization and mechanism

The devices are probed by sweeping the bottom electrode while keeping the top electrode at 0 V. The device exhibits non-volatile resistive switching mediated by the interface, evident from the absence of the abrupt transition of HRS to LRS observed in filamentary memristors.[18, 40, 49, 51] In **Figure 46(a)**, the current through the device is normalized to the device area (green) and is compared with the normalized current of MoS_2/Ti/Au (pristine MoS_2 device) device[87] (red). Here, the comparison of 2 types of devices is executed by DC cycling experiments over 100 DC cycles. This comparison yields two distinct observations which supports the necessity of device engineering in MoS_2 based synapses while maintaining low C-C variability: (i) the decrease

in the programming current through the device with widened memory window, indicative of a higher number of available conductance states which will be further explored in weight update characterizations; and (ii) the increase in the ON/OFF ratio. The underlying transport mechanism is observed to be space charge limited conduction (SCLC) mechanism similar to pristine MoS_2 devices.[87] The SCLC mechanism can be inferred by the slopes (slope : α) obtained from current versus voltage (I-V) curves plotted in double log scale. The SCLC mechanism consists of an initial ohmic region (α=~1), followed by shallow trap SCLC (α=~2) and SCLC (α>>2) once the trap gets filled where the cross-over voltage is known as trap-filled limit voltage (VTFL). We have extracted slopes from the I-V characteristics of the device in both HRS and LRS regions as shown in **Figures 46(b-c)**. From **Figure 46(b)**, we observe non-ohmic conduction indicated by α<1 due to the insertion of insulating SiO_x between MoS_2 and Ti. The slope for non-ohmic conduction is extracted for voltages between 0 V−0.7 V. For the voltage range of 0.7 V – 1.9 V, α= ~2.1 is obtained, corresponding to shallow trap SCLC. Here, 1.9 V is the VTFL, where the traps get filled and the conduction is predominantly SCLC, indicated by α= ~8. Once the device switches from HRS to LRS, we observe SCLC (α= ~3) as shown in **Figure 46(c)**.

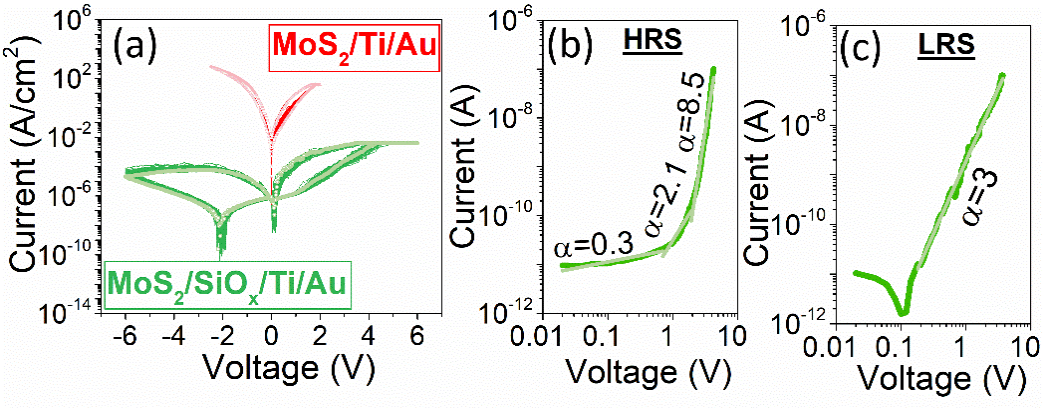

Figure 46: (a) Current through the device measured for MoS_2 device without SiO_x (Red) and with SiO_x (Green). Inclusion of SiO_x decreases the current through the device. (b)SCLC conduction mechanism in HRS indicated by the slopes obtained from double log I-V plot. (c) SCLC conduction mechanism observed in LRS.

7.3.2 SET voltage and RESET power distribution

The MoS_2/SiO_x/Ti/Au device performance is analyzed in terms of SET voltage and RESET power variation to evaluate C-C variability as shown in **Figure 47**. The SET voltage and RESET powers are extracted for 100 DC cycles. **Figure 47(a)** shows the SET voltage variation of MoS_2/SiO_x device. The SET voltage range is 0.5 V which is comparable to the range of 0.2 V observed in pristine MoS_2 devices[87]. Further the CV of SET voltage in MoS_2/SiO_x device is observed to be 1.5 % in contrast to pristine MoS_2 device where the maximum CV was 1.79 %. By the inclusion of the SiO_x layer, we observe a ~10^4 × decrease in the RESET power compared to the pristine MoS_2 device (60 µW – 80 µW) and the RESET power distribution is shown in **Figure 47(b)**. The decrease in RESET current is critical in reducing sneak current paths in cross bar architectures.[34]

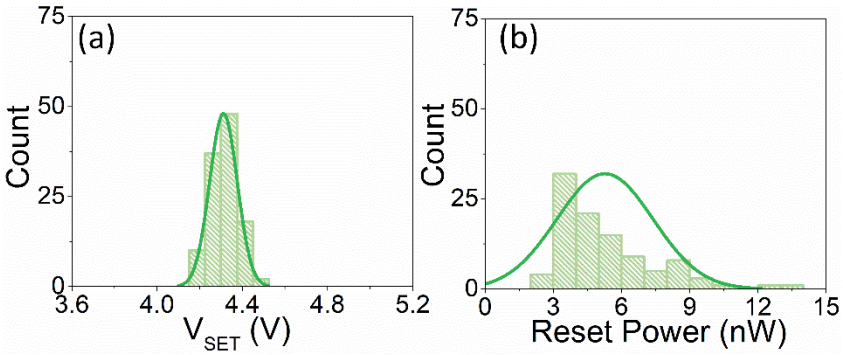

Figure 47: (a) V_{SET} distribution in $MoS_2/SiO_x/Ti/Au$ device. The device maintains low C-C variability in V_{SET} with a range of 0.5 V. (b) Histogram of RESET power distribution. MoS_2 device with SiO_x layer exhibits ~ 10^4 order decrease in the RESET power.

7.3.3 Synaptic measurements

The ultra-low variability MoS_2 devices are further characterized as synapses suitable for use in neural network training. DC potentiation and depression measurements are performed by enforcing CC. The MoS_2 devices exhibit 4 distinct potentiation states and 5 different depression states, shown in **Figure 48** rendering preliminary indication of the ability of MoS_2 device to behave like an analog memory.

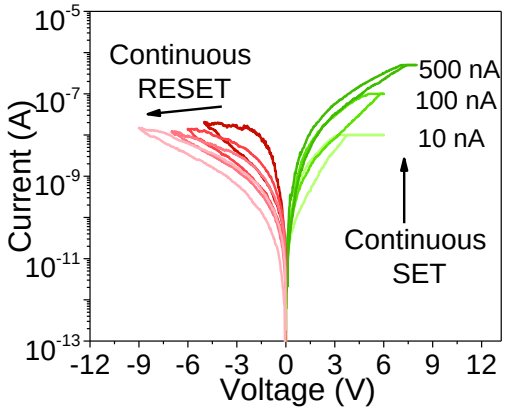

Figure 48: DC potentiation and depression

Pulsed I-V measurements are performed to evaluate the C-C variability in weight update characteristics. To induce pulsed potentiation (depression), 128 identical pulses of amplitude 5 V (-5 V) and duration 50 ms are applied. The write current corresponding to the applied pulse is recorded and the write conductance is estimated. The aforementioned potentiation/depression cycle is repeated for 100 times as shown in **Figure 49(a)**. From the figure, we observe low C-C variability in weight update characteristics. The inset of **Figure 49(a)** shows the pulsing scheme utilized for characterizing these synapses. For evaluating the retention, the device is initially SET at a particular conductance state by performing a DC sweep, and the conductance of the device is extracted by the current through the device which is read at a voltage (V_{Read}) of 1.5 V. The device exhibits a retention of >100 s for at least 14 distinct states as shown in **Figure 49(b)**. **Figure 49(c)** shows the variation in the G_{max}/G_{min} ratio (100 cycles) of MoS_2/SiO_x synapse. From the figure, it is evident that G_{max}/G_{min} increases by ~10 with the inclusion of SiO_x in contrast to pristine MoS_2 synapse[87] (G_{max}/G_{min} = 2).To investigate the low C-C variability in weight update characteristics, the ANL is extracted for each cycle over 100 weight update cycles. The ANL variation in MoS_2/SiO_x synapse is shown in **Figure 49(d)**. We observe an SD of 0.019 and CV of 2.5 % in ANL indicative of low C-C variability in weight update. The results indicate that the low C-C variability is preserved in MoS_2/SiO_x synapse and is comparable to the pristine MoS_2 synapse (SD= 0.01, CV= 2.12 %).[87]

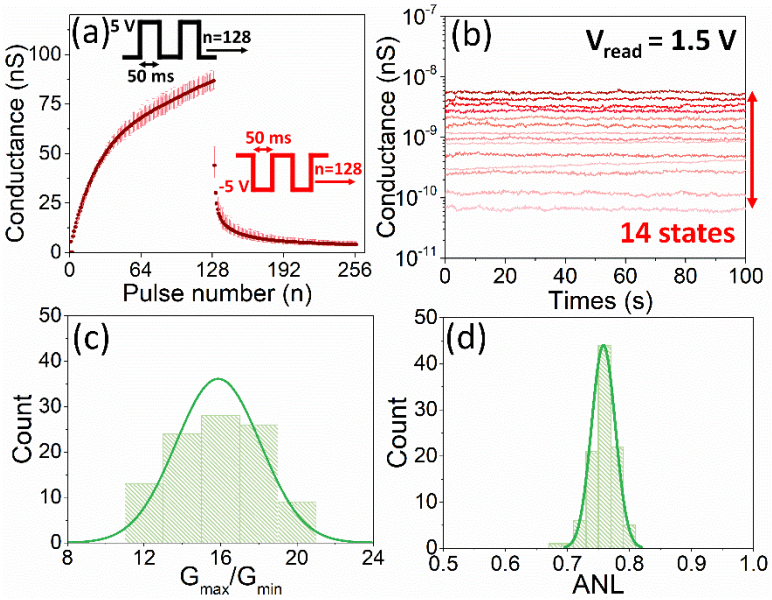

Figure 49: (a) Weight update variation observed in MoS_2 synapse for 100 cycles showing the mean weight update trajectory. Inset:Pulsing scheme. (b) Retention of >100 s at 14 distinct states. (c) The variation of G_{max}/G_{min} for the $MoS_2/SiO_x/Ti/Au$ synapse. The MoS_2 with SiO_x layer exhibits enhancement in G_{max}/G_{min}. (d) ANL variation observed in $MoS_2/SiO_x/Ti/Au$ synapse indicating the preservation of low C-C variability with the incorporation of SiO_x layer.

7.4 Conclusion

In conclusion, the MoS_2/ devices with Ti/Au electrodes have been engineered by including a thin SiO_x layer (~20 nm) to improve the G_{max}/G_{min} ratio while sustaining low C-C variability. The inclusion of SiO_x layer lowers the programming current and increases the G_{max}/G_{min} ratio by ~10. The MoS_2/SiO_x devices maintain low C-C variability in various performance metrics like SET voltage, RESET power, mean ANL and SD, and are comparable to the original MoS_2 devices. Further, the inclusion of SiO_x layer reduces the RESET power from µW to nW. The engineering technique utilized demonstrates the inherent nature of 2D materials to exhibit low C-C variability. This demonstrates the versatility of 2D based synapses for next generation neuromorphic devices.

CHAPTER 8 LINEAR UPDATE MoS_2 SYNAPSES

8.1 Introduction

In this chapter we present memristive devices using MoS_2/SiO_x active medium, with graphene as bottom electrode and Ni as top electrode, as synapses with ideal linearity and symmetry in their weight update. We explore the role of graphene and other elemental metals as electrodes to MoS_2/SiO_x and optimize the MoS_2 thickness for linear, symmetric conductance update. We report the variation of nonlinearity in weight update with varying number of pulses, pulse amplitude and pulse width. We investigate the mechanism of resistive switching in graphene/MoS_2/SiO_x/Ni devices using temperature-dependent current-voltage measurements. We observe PF emission as the primary mechanism of switching in these devices. Our group reported the first MoS_2-based LIF neurons using Ag electrode.[86] We develop an integrated synapse-neuron circuit where the synaptic conductances modulate the frequency of spiking of the MoS_2-based LIF neuron. A spiking neural network simulated with these neurons and synapses exhibits a classification accuracy of 89% on hand-written digits from the MNIST dataset.

8.2 Device schematic

Figure 50(a) shows the schematic of a typical graphene/MoS_2/SiO_x/Ni cross-point device These devices are realized using CVD MoS_2 and graphene. It should be noted that SiO_x is deposited using e-beam evaporation prior to the deposition of Ni contact metal in the same deposition step. The devices fabricated have area in the range of 5×5 μm^2 to 50×50 μm^2. The scanning electron microscope (SEM) image of the device is shown in **Figure 50(b)**.

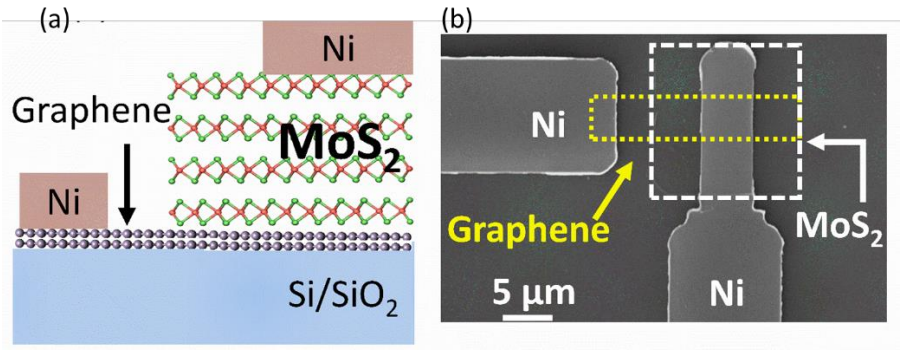

Figure 50: (a) Device schematic of graphene/MoS_2/SiO_x synapse. (b) SEM image of the graphene/MoS_2/SiO_x synapse.

8.3 Material characterization

Figure 51(a) shows the presence of high intensity characteristic Raman modes at 386 cm^{-1} and 410 cm^{-1}, corresponding to in-plane (E^1_{2g}) and out-of-plane (A_{1g}) lattice vibrations indicating the growth of high-quality MoS_2 layers on graphene. **Figure 51(b)** shows the AFM image with a height profile, indicating a thickness of 8.8 nm of the as-grown MoS_2 film. It is worth noting that the height profile obtained from the area where SiO_x is not present. The thickness of the deposited SiO_x is obtained by performing HRTEM at the active area of the device as shown in the **Figure 51(c)**. From the figure the thickness of the e-beam evaporated SiO_x is observed to be ~10 nm. The chemical composition of the stack at the active area is obtained by elemental energy dispersive X-ray spectroscopy (EDS). The EDS spectra shown in the **Figure 51(d)** reveal the presence of MoS_2, SiO_x and top contact Ni.

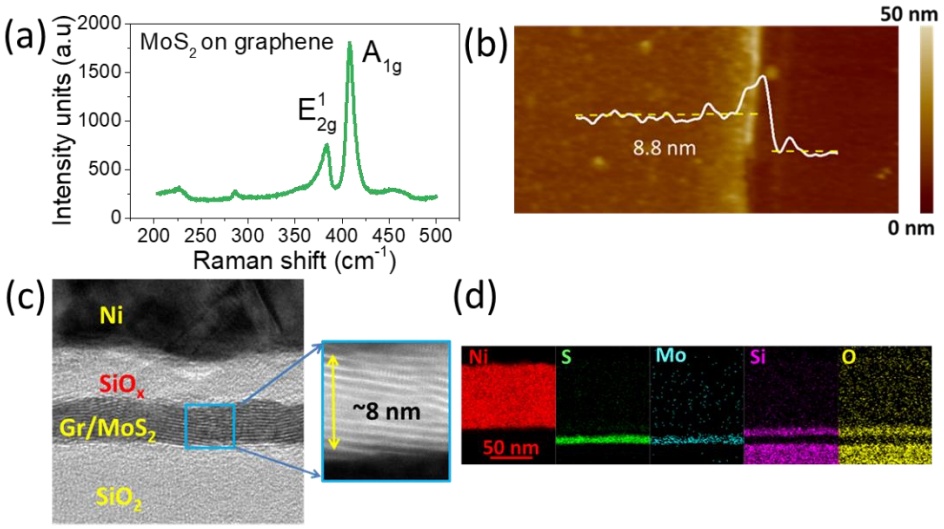

Figure 51: (a) Raman spectrum of MoS_2 grown directly on graphene. (b) AFM height profile of the MoS_2 film. (c) Cross-sectional TEM at the active area indicating the presence of MoS_2 and SiO_x. (d) EDS spectra showing the configuration of the device stack.

8.4 DC characterization

8.4.1 Comparison between CVD and exfoliated MoS_2

The DC I-V characteristics of a typical graphene/MoS_2/SiO_x/Ni device when the bias voltage is applied to the bottom graphene electrode, while the top electrode is kept at 0 V. The graphene/MoS_2/SiO_x/Ni device exhibits forming-free resistive switching since the first SET does not require a higher voltage than subsequent SET processes. To evaluate the role played by the SiO_x in the device stack, we fabricate graphene/CVD-MoS_2/Ni devices. The device schematic is as shown in the inset of the **Figure 52(a)**. The DC I-V characteristics of the device is presented in the **Figure 52(a)**. From the figure, we observe non-volatile resistive switching where the transition is gradual from HRS to LRS. This non-volatile switching is similar to that of interface-mediated switching as opposed to abrupt switching observed in graphene/MoS_2/SiO_x/Ni devices which resembles that of non-volatile switching due to the formation of conductive filaments. Further we

also examine the role of crystallinity of MoS_2. In that regard we replace CVD MoS_2 by exfoliated MoS_2. MoS_2 (~13-15 layers) thick is mechanically exfoliated and transferred on etched CVD graphene. After this, contact metal, Ni (60 nm) is deposited on both graphene and exfoliated MoS_2. The device schematic is shown in the inset of the **Figure 52(b). Figure 52(b)** shows the DC I-V of these devices which is similar to that of interface mediated switching.[75] This indicates that crystallinity of MoS_2 does not play a role in filamentary switching observed in graphene/MoS_2/SiO_x/Ni due to decreased OFF state.

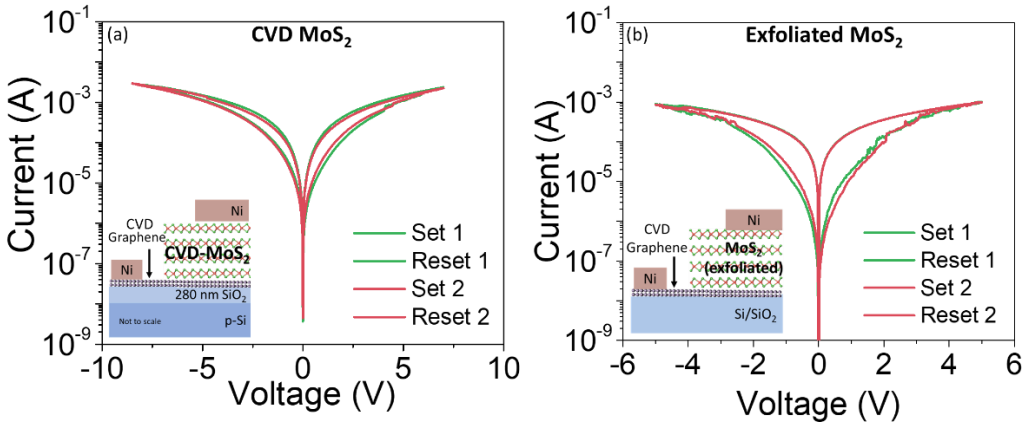

Figure 52: (a) DC cycling of graphene/MoS_2/Ni device fabricated using CVD MoS_2. Inset: Device schematic. (b) DC cycling of graphene/MoS_2/Ni device using exfoliated MoS_2. Inset: Device schematic.

8.4.2 Role of SiO_x

From the above results it is evident that the presence of SiO_x comes with two distinct advantages *viz.*, i.) by the inclusion of SiO_x the ON/OFF ratio can be increased and ii.) the programming voltage can be reduced. Further, it is also essential to investigate the role played by MoS_2 in memristive characteristics. In that regard, we have fabricated graphene/SiO_x/Ni devices. The pristine SiO_x devices are characterized by DC cycling experiments. Three devices were characterized for 50 DC cycles each by enforcing current compliance of 10 µA. Similar

measurement protocol is enforced on graphene/MoS_2/SiO_x/Ni devices. For each cycle, the OFF (HRS) and ON (LRS) state resistances are extracted at V_{Read}=0.5 V and the scatter in the resistance is plotted as shown in **Figure 53**. From the figure, it is evident that MoS_2/SiO_x is critical for obtaining low C-C variability and decreased operating current.

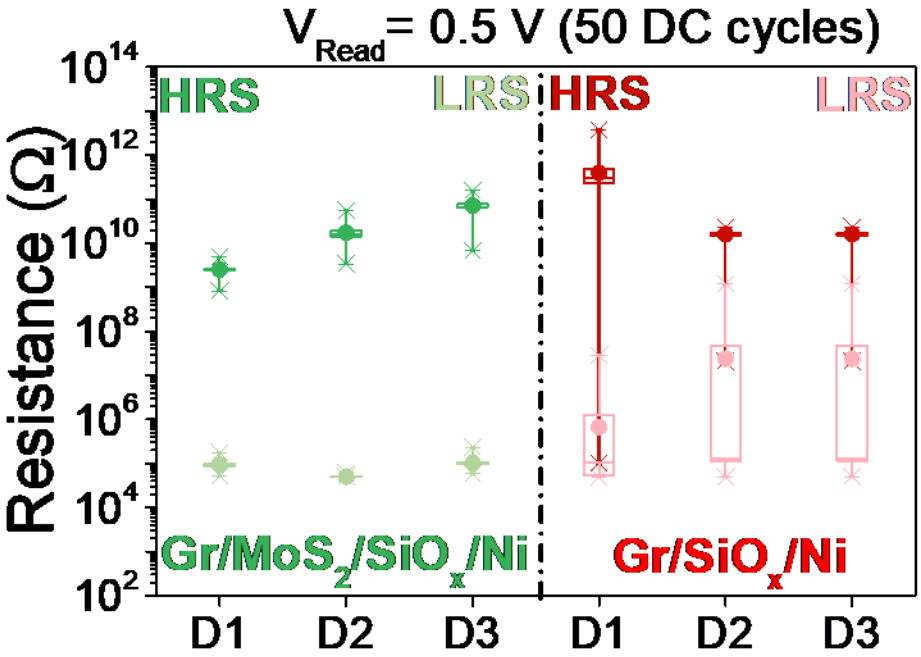

Figure 53: OFF (HRS) and ON (LRS) state resistance comparison of graphene/MoS_2/SiO_x/Ni devices with graphene/SiO_x/Ni devices. The devices with MoS_2/SiO_x active medium exhibit low C-C variability in ON and OFF state resistances.

8.4.3 Electrode engineering

To understand the contribution of the electrodes to the device characteristics, we vary the electrode materials with MoS_2/SiO_x being the active layer. The incorporation of graphene as the bottom electrode in graphene/MoS_2/SiO_x/Ni device decreases the programming current. **Figure 54(a)** shows that when Au is used as the bottom electrode on which MoS_2 is grown directly, the OFF current of the device increases by $>10^3$, thereby increasing the operating current, hence

operating power of the device. This observation is in agreement with previous reports of the use of graphene in RRAM devices in the reduction of operating current.[33, 88, 89] Keeping Ni as the top electrode and MoS_2/SiO_x as the active material, we use graphene as barrier layer with with Au (Ti adhesion layer) as the bottom electrode (**Figure 54(b)**). These devices exhibited potentiation and depression with lowest programming current of 100 nA as shown in **Figure 54(b)**. These results indicate the role played by the graphene in the reduction of programming current through the devices.

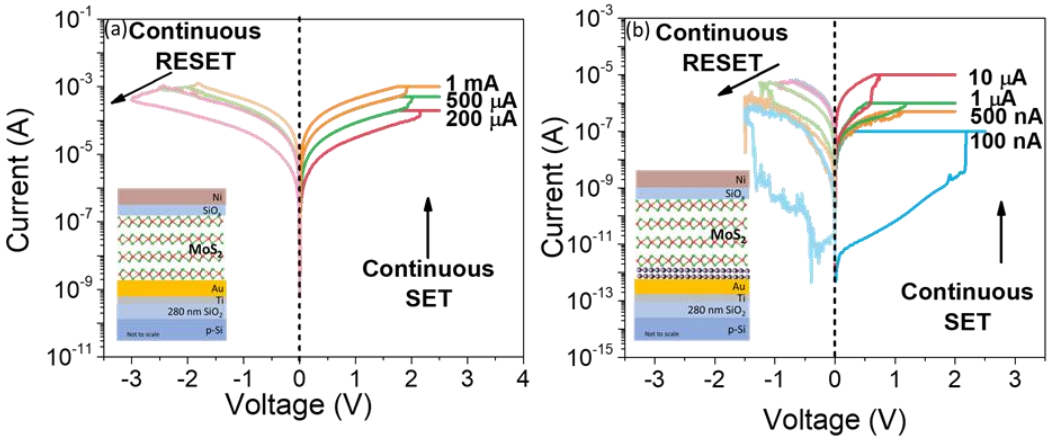

Figure 54: (a) Potentiation and depression characteristics observed in $Ti/Au/MoS_2/SiO_x/Ni$ devices. The low OFF state resistance with high programming current demonstrates the role played by graphene in the reduction of programming current. Inset: Device schematic. (b) Potentiation and depression observed in $Au/graphene/MoS_2/SiO_x/Ni$ where graphene is used as the barrier layer. The inclusion of graphene as the barrier layer shows the necessity of graphene in the reduction of operating current of the device with increased OFF state resistance. Inset: Device schematic.

While keeping graphene as the bottom electrode we change the top electrode to Ti capped with Au as shown in **Figure 55(a)** to understand the role played by the top electrode. The devices require forming and operate in vacuum as opposed to devices with Ni top electrode where they operate in ambient conditions as shown in **Figure 55(b)**. These devices undergo DC potentiation and depression, as shown in **Figure 55(c)**. However, due to the requirement of vacuum to operate

these devices while the devices with Ni as top electrode operate favorably in ambient air, we do not explore the devices with Ti/Au top electrode further in this work.

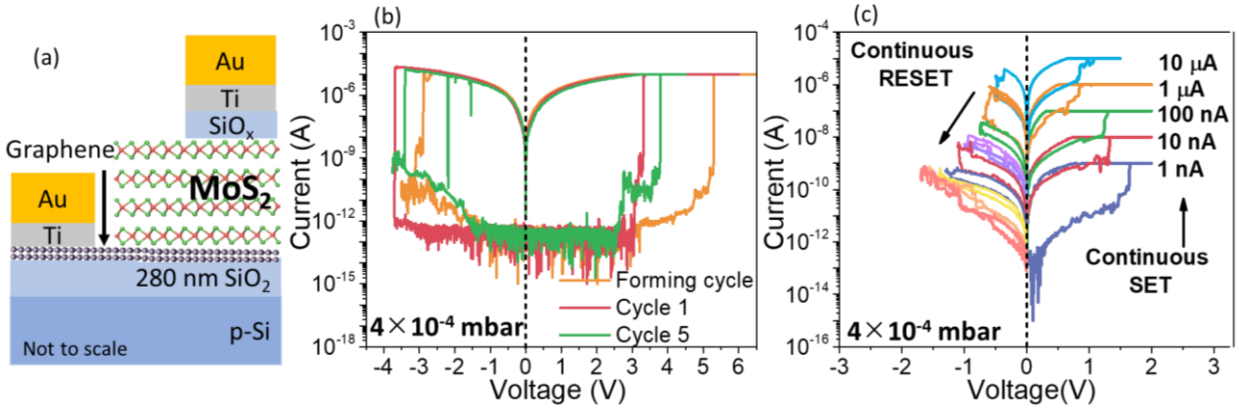

Figure 55: (a) Device schematic of graphene/MoS_2/SiO_x/Ti/Au device. (b) Electro-forming step observed in graphene/MoS_2/SiO_x/Ti/Au where the stable switching is observed in a pressure of $4x10^{-4}$ mbar. (c) Potentiation and depression observed in graphene/MoS_2/SiO_x/Ti/Au device.

Figure 57 shows the DC I-V of graphene/MoS_2/SiO_x/Ti/Ag device indicating the significance of using inert electrode as the MoS_2 contact to obtain non-volatile switching. Here, we observe that the use of active Ti/Ag electrode induces volatile switching behavior which is a clear signature of formation of weak Ag^+ filaments.[90, 91]

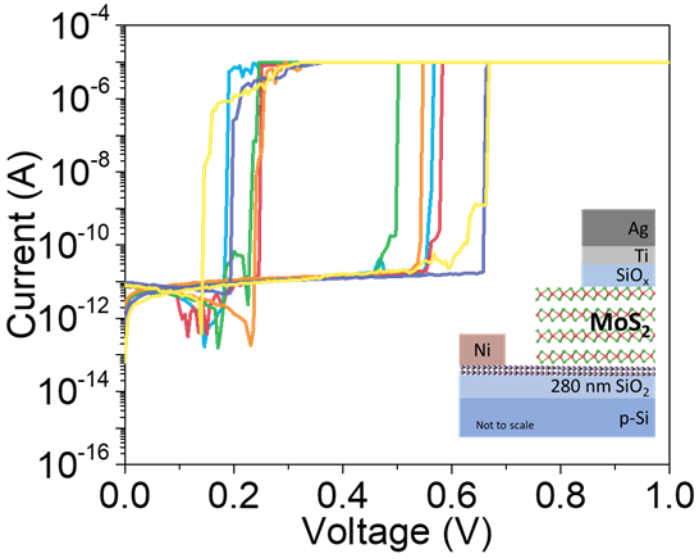

Figure 56: Volatile resistive switching observed in graphene/MoS_2/SiO_x devices with active Ti/Ag electrode. Inset: Device schematic.

8.5 Synaptic Characteristics

8.5.1 DC potentiation and depression

Consequently, we have focused on graphene/MoS_2/SiO_x/Ni devices for various synaptic characteristics. We initiate the characterization to examine the existence of multiple conductance states. Here, the device is subjected to a continuous SET process by varying the current compliance from 100 nA to 10 µA, as shown in **Figure 57**. The graphene/MoS_2/SiO_x/Ni device exhibits 5 states by a continuous SET process indicating the ability of the device to undergo DC potentiation. The device is subjected to depression by applying negative bias to the bottom electrode. The negative bias on the graphene electrode is increased in successive steps until the device is completely reset to its HRS. We observe 7 distinct conductance states during the process of depression (**Figure 57**).

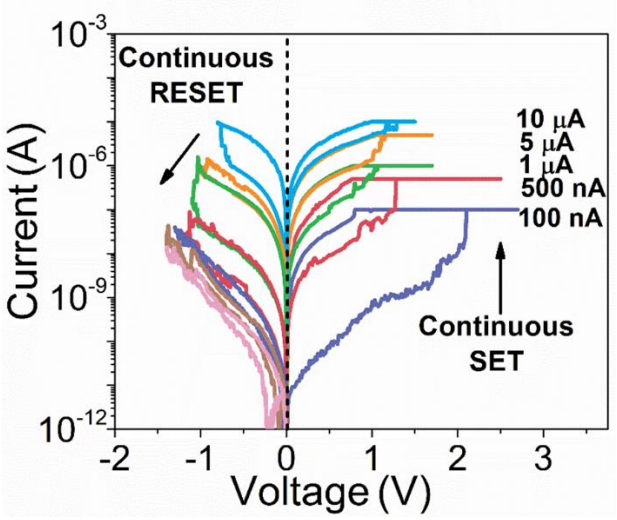

Figure 57: DC potentiation and depression. The graphene/MoS_2/SiO_x device exhibits 5 potentiation and depression states.

8.5.2 Retention and linear weight update

A synapse should exhibit long-term retention in multiple conductance states for efficient inference. The graphene/MoS_2/SiO_x/Ni devices exhibit stable retention for 10^3 s at room temperature for 15 distinct conductance states ranging between 100 pA (~330 pS) to 10 µA (36 µS), as shown in **Figure 58(a)**. The conductance states of the synapse correspond to the synaptic weight in a neural network (NN). The trajectory of the weight update plays a critical role for online training in NN. Ideally the synapse device should exhibit linear and symmetric weight update for high learning accuracy in terms of online training because this would allow direct mapping of conductance states to weights in the algorithms.[92] We applied 64 pulses of 50 µs pulse width and amplitude of 4.5 V (-3 V) for potentiation (depression). The conductance of the device is normalized to the highest conductance obtained and is plotted against the pulse number. **Figure 53(b)** shows the weight update characteristics observed in graphene/MoS_2/SiO_x/Ni devices. The NLF is calculated using a behavioral model described by Chen et al.[93] For high online learning accuracy the NLF <1 is required. It is observed that graphene/MoS_2/SiO_x/Ni devices exhibit ideal linearity with NLF=0 in both potentiation and depression regimes. This ideal linearity corresponds to ideal symmetry, which is given by the asymmetry factor, $|NLF_{potentiation} - NLF_{depression}|$.[92] Thus, we find that MoS_2/SiO_x active stack with graphene as the bottom electrode and Ni as the top electrode yields a synaptic device with lower operating current than conventional oxide-based and 2D h-BN based RRAM devices.[42, 92, 94] Additionally, the devices also exhibit linearity in weight update characteristics essential for efficient synaptic operation.

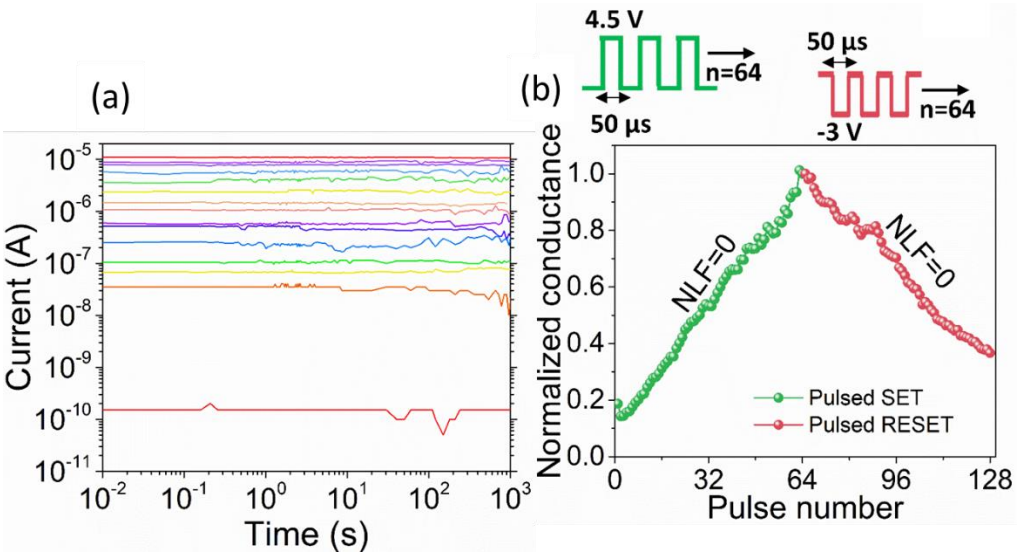

Figure 58: (a) Stable room temperature retention of 10^3 s for 15 distinct conductance states. (b) Linear and symmetric weight update observed in graphene/MoS_2/SiO_x device giving ideal asymmetry of '0'

We varied the thickness of the MoS_2 layers to examine the role of the MoS_2 film in the switching process as shown in **Figure 59**. Mo of 5 nm is deposited by e-beam evaporation and then sulfurized to MoS_2 by CVD. The thickness of the MoS_2 film is estimated by the AFM technique. **Figures 59(a) (i)-(ii)** show the AFM image and Raman spectrum for an MoS_2 film ~15 nm thick. The devices with 15 nm MoS_2 exhibit forming-free characteristics as shown in the **Figure 59(a) (iii)**. **Figure 59(a) (iv)** shows the DC potentiation and depression as shown in the aforementioned device. Further, we also performed weight update measurements as shown in the **Figure 59(a) (v)**. When a train of identical pulses as shown in is applied to the device, the device exhibits linearity in potentiation and depression with n = 25. While the potentiation regime is linear for n = 50 and 100, the nonlinearity in depression increases with increasing number of applied pulses. Additionally, we performed the aforementioned characterizations on the devices with MoS_2 thicker than 15 nm. Here, the thickness of Mo deposited was 10 nm which yielded MoS_2 of ~20

nm thick. **Figures 59(b) (i)-(ii)** show the AFM image and Raman spectrum for an MoS_2 film ~20 nm thick. The DC I-V characterization in the **Figure 59(b) (iii)** shows the requirement of electroforming process due to the increased thickness of MoS_2. The device requires a high forming voltage of ~ 8 V. Further, the device undergoes DC potentiation and depression as shown in the **Figure 59(b) (iv)**. When a train of identical pulses as shown in **Figure 59(a) (v)** is applied to the device, the device exhibits a nonlinear weight update with near-linear weight update in potentiation for n = 8 as shown in the **Figure 59(b) (v)**. Thus, we observe steady increase in the non-linearity in the weight update with increase in the MoS_2 thickness.

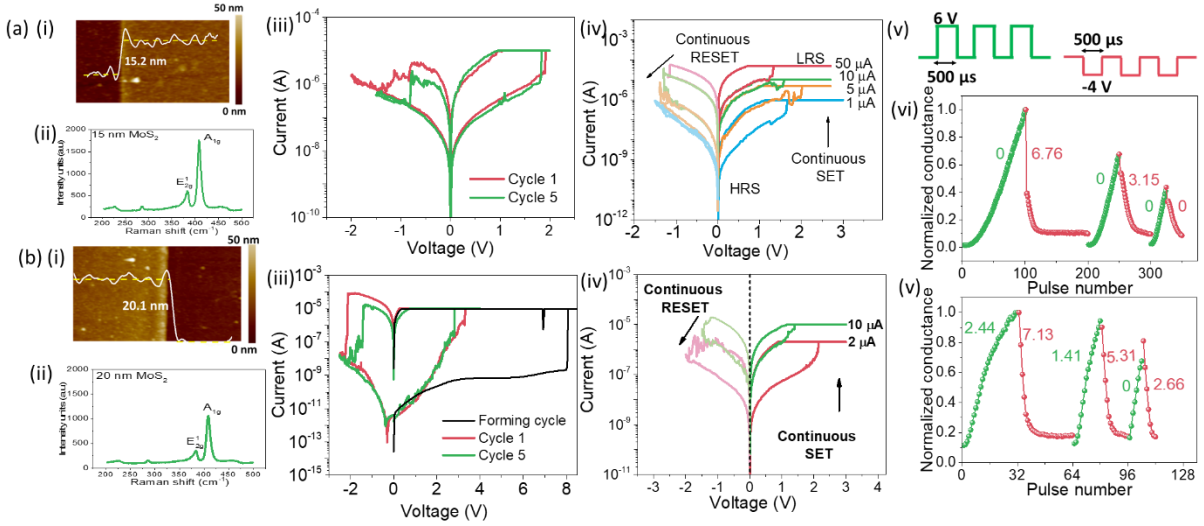

Figure 59: (a) (i) AFM image of graphene/MoS_2/SiO_x device with 15 nm MoS_2. (ii) Raman spectra of 15 nm MoS_2. (iii) Forming free DC I-V characteristics of device with 15 nm MoS_2. (iv) DC potentiation and depression of graphene/MoS_2/SiO_x device with 15 nm MoS_2. (v) Pulsing Scheme (vi) Weight update characteristics observed in graphene/MoS_2/SiO_x device with 15 nm MoS_2. The device exhibits ideal linearity along both potentiation and depression with *n=25*. These devices exhibit linearity along potentiation for higher pulse numbers while the depression is observed to be non-linear. (b) (i) AFM image of graphene/MoS_2/SiO_x device with 15 nm MoS_2. **(ii)** Raman spectra of 20 nm MoS_2. (ii) Raman spectra of 20 nm MoS_2. (iii) Forming free DC I-V characteristics of device with 20 nm MoS_2. (iv) DC potentiation and depression of graphene/MoS_2/SiO_x device with 15 nm MoS_2. (v) Non-linear weight update observed in graphene/MoS_2/SiO_x device with 20 nm MoS_2. Here, the device exhibits ideal linearity with *n=8* along potentiation. However, the depression is observed to be non-linear with *n=8*.

The observation of linear and symmetric weight update in graphene/MoS_2/SiO_x/Ni device demonstrates the potential of these devices in implementing unsupervised learning. However, it is imperative to investigate if the linearity is maintained with varying input pulse parameters, such as the number of applied pulses, pulse width and pulse amplitude. **Figure 60(a)** shows the effect of varying the number of input pulses, *n*, on the NLF in the potentiation regime. Here, we apply identical pulses with a pulse width of 100 µs and amplitude of 4.5 V and vary the number of pulses. Notably, the device shows linearity in weight update when the pulse number is increased from 32 to 64. Next, we study the effect of increasing the pulse width on the NLF in the potentiation regime, keeping the number of applied pulses as 128 and pulse amplitude as 4.5 V. The linearity in weight update is maintained for pulse widths of 50 µs and 100 µs, as shown in **Figure 60(b)**. **Figure 60(c)** shows that the NLF remains 0 during potentiation as we apply identical pulse trains of amplitude 4.5 V and 4.75 V, with n = 128 and pulse width of 50 µs. The slope of the weight update curve is higher for the higher pulse amplitude since a higher voltage causes a larger change in the conductance path. In **Figure 60(d)**, trains of identical pulses with a pulse width of 250 µs and amplitude of -3 V are applied for n=8, 16 and 32. The weight update is linear for n=8, but the NLF increases with increasing values of n. It should be noted that the device was in different conductance states prior to the application of the depression-inducing pulses. In **Figure 60(e)**, we apply 128 identical pulses of amplitude of -2 V and vary the pulse widths. The NLF decreases from 3.8 to 1.17 with the pulse width decreasing from 250 µs to 100 µs. In **Figure 60(f)**, we apply 128 pulses of a pulse width of 100 µs for pulse amplitudes of -2 V and -3 V. The NLF reduces from 4.57 to 1.17 with decreasing pulse amplitude. These results indicate that the graphene/MoS_2/SiO_x/Ni system is capable of exhibiting linear weight update for relatively low

pulse width and pulse amplitudes while keeping the number of applied pulses as high as 128, enabling the realization of a high accuracy neural network with a resolution of 7 bits.

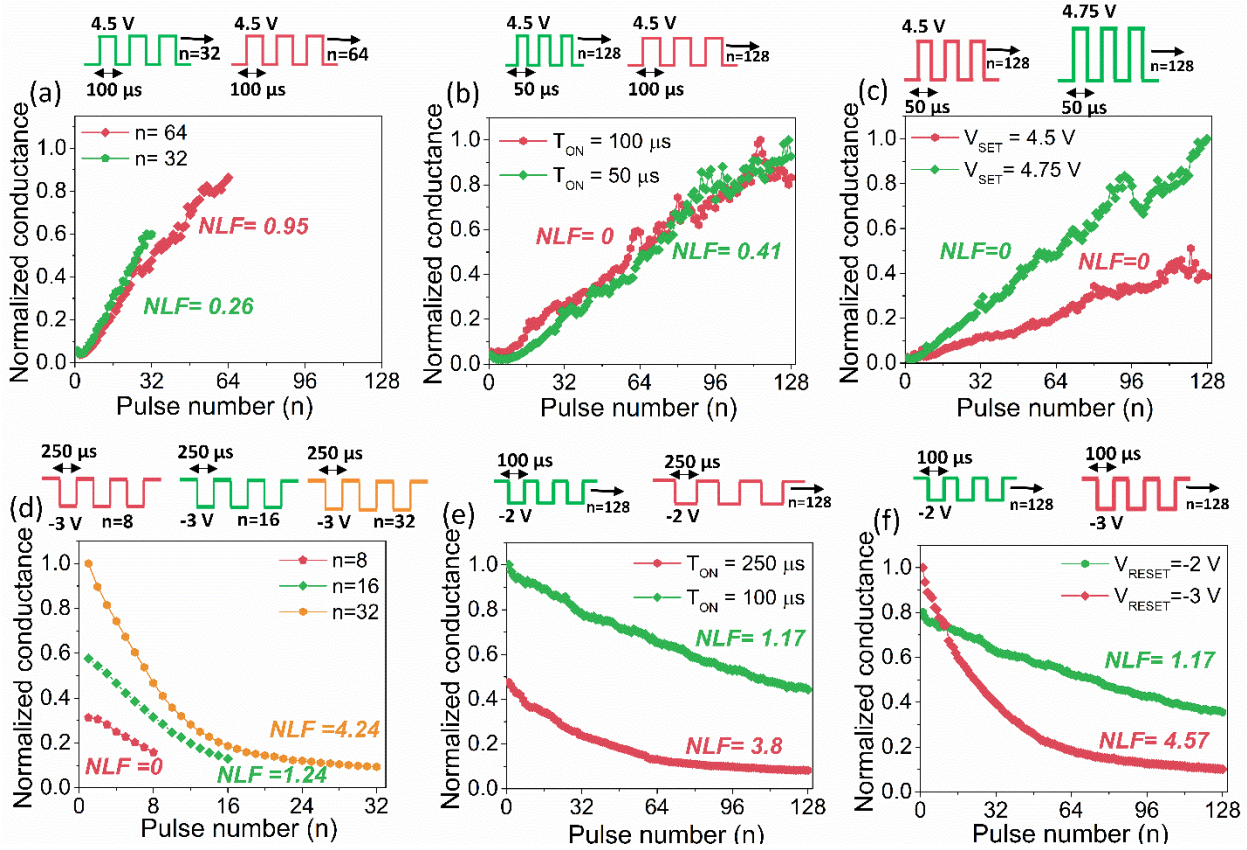

Figure 60: (a) Pulse number scaling in the potentiation regime of graphene/MoS_2/SiO_x synapse where the high linearity is maintained for n=32, 64. (b) Pulse width scaling of the graphene/MoS_2/SiO_x synapse. Here, we observe that the linearity is maintained for higher pulse width of 100 µs. (c) Pulse amplitude scaling of the graphene/MoS_2/SiO_x device where the linearity is maintained for different pulse amplitudes *viz.*, 4.5 V and 4.75 V. (d) Pulse number scaling observed in graphene/MoS_2/SiO_x device in depression regime where NLF=0 is obtained for n=8. (e) Pulse width scaling observed in graphene/MoS_2/SiO_x device for depression regime where linearity is observed with relatively lower pulse width of 100 µs. (f) Pulse amplitude scaling observed in graphene/MoS_2/SiO_x device for depression regime where linearity is observed with relatively lower pulse amplitude of -2 V.

8.6 Mechanism

8.6.1 Area-dependent resistance scaling

Linearity in conductance weight update in resistive switching devices has been attributed to interface-mediated switching.[95, 96] We compare the ON and OFF currents of the graphene/MoS_2/SiO_x/Ni devices as a function of device area. The OFF state resistance scales with device area while the ON state resistance remains constant, as shown in **Figure 61**, indicating that the switching in these devices is filamentary. [92] [68]

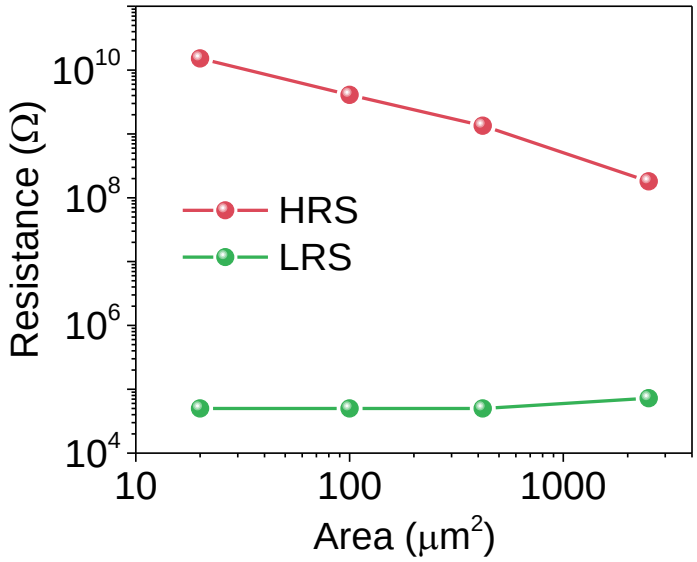

Figure 61: Area dependent OFF/ON state resistance variation observed in graphene/MoS_2/SiO_x devices.

8.6.2 Temperature dependent I-V measurements

We conducted temperature-dependent I-V measurements on the graphene/MoS_2/SiO_x/Ni devices to shed light on the nature of the conductive filaments at both HRS and LRS. We SET the device at a current compliance of 10 μA and subsequently reset the device at temperatures varying

from 310 K to 370 K in vacuum (8×10^{-5} mBar). **Figure 62(a)** shows that the current in the HRS increases as the temperature increases for both bottom electrode injection (positive bias on bottom graphene electrode) and top electrode injection (negative bias on bottom graphene electrode) conditions. The I-V characteristics of the graphene/MoS_2/SiO_x/Ni device are symmetric in spite of the dissimilar work-functions of the top Ni and bottom graphene electrodes. This indicates that the conduction in the HRS is not limited by the Schottky barrier at the electrodes.[68] The observed symmetric I-V characteristics further indicates that the conduction in the HRS state is bulk-controlled. One of the prominent bulk-controlled conduction mechanisms is PF emission. The current density *J* due to PF emission is governed by

$$J = J_0 \exp\left(\frac{\beta_{PF} E^{1/2} - \emptyset_t}{kT}\right) \quad (1)$$

where J_0 is the low-field current density, $\beta_{PF} = \left(\frac{q^3}{\pi \varepsilon_0 \varepsilon}\right)^{1/2}$, q is the electronic charge, ε_0 is the dielectric constant of the free space, ε is the high frequency dielectric constant, T is the temperature, k is the Boltzmann constant, and $\emptyset_t$ is the trap energy level with respect to the conduction band. To verify the temperature dependence as predicted from the equation defining the PF model, we plot $\ln\left(J/E\right)$ as a function of 1000/*T* as shown in the **Figures 62(b-c)** for both bottom and top injections. We observe that ln (*J*/*E*) varies linearly with 1000/*T*, with the slope of the line being dependent on the electric field. The slope of the line in the Arrhenius plots gives the activation energies E_a. **Figure 62(b)** shows that the activation energy decreases with the increase in the voltage for bottom electrode injection. The same trend is observed with respect to the top electrode injection as shown in the **Figure 62(c)**. By plotting the extracted activation energies as a function of electric field we obtain the trap energy state $\emptyset_t$, which corresponds to the y-intercept at zero electric field. The trap energy state $\emptyset_t$ is 0.66 eV for both positive and negative bias

conditions, as shown in **Figure 62(d)**. The qualitative study pertaining to the identity of traps that play role in resistive switching deserves a study of its own which is out of scope from this work. Thus, we can conclude that resistive switching is due to the conductive filaments formed by the defects that contribute to the extracted trap level in both SiO_x and MoS_2. After the device switches from HRS to LRS, it is necessary to extract the conduction mechanism in the LRS. **Figure 62(e)** shows the increase in current at LRS with increasing temperature. To understand the conduction mechanism, a double logarithmic plot of current *vs.* voltage is plotted for temperatures ranging from 320 K to 370 K for both bottom and top electrode injection conditions. For every temperature, we extract the slope (α) of the I-V curve as shown in **Figures 62(f-g)**. We obtain a unit slope with varying temperatures which is a clear indication of ohmic conduction. **Figure 62(h)** presents the conduction mechanism in a graphene/MoS_2/SiO_x/Ni device.

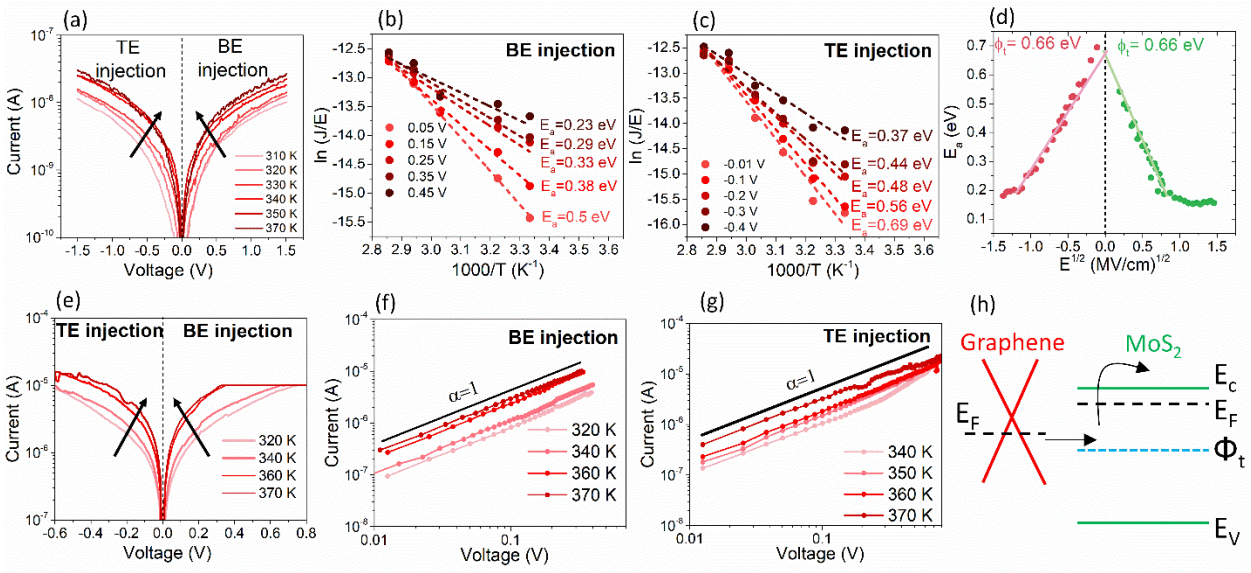

Figure 62: (a) I-V characteristics of graphene/MoS_2/SiO_x device in HRS state where a clear temperature dependence is observed. (b) Arrhenius plot of the graphene/MoS_2/SiO_x device in HRS for bottom electrode injection following the PF model. (c) Arrhenius plot of the graphene/MoS_2/SiO_x device in HRS for top electrode injection following the PF model. (d) The extracted activation energy is plotted as the function of electric field where the intercept at E=0 gives the electron trap energy state. (e) I-V characteristics of graphene/MoS_2/SiO_x device at LRS

states where a clear signature of temperature dependence is observed. (f) The double logarithmic plot *of* I-V at LRS state for bottom electrode injection indicating ohmic conduction. (g) The double logarithmic plot of I-V at LRS state for top electrode injection indicating ohmic conduction. (h) The band diagram of the graphene/MoS_2/SiO_x device showing the mechanism of switching in these devices.

8.7 Integration of grapheneMoS_2/SiO_x/Ni synapses with MoS_2 LIF neurons

Next, we show the modulation of spiking frequency of an MoS_2-based LIF neuron monolithically integrated with the MoS_2-based synapses. This experiment is designed to understand if the graphene/MoS_2/SiO_x/Ni synapses can replace a resistor in the RC circuit to bring about spiking of a LIF neuron. This can be regarded as the one of the preliminary results for the array level integration of MoS_2 based neurons and synapses. The DC I-V characteristics of a graphene/MoS_2/SiO_x/Ni synapse integrated with an MoS_2 neuron in series is shown in **Figure 63(a)**. The voltage bias is applied to one end of the neuron device. Here we observe two distinct steps in the I-V characteristics corresponding to the volatile switching of the neuron device at a lower voltage followed by the switching of the synapse device at a higher voltage. Further, in the reverse sweep, we observe the transition of the neuron from LRS to HRS. We enforce a current compliance to control the growth of the filament in the graphene/MoS_2/SiO_x/Ni synapse. In the subsequent runs, we increase the current compliances of the measurements to observe the potentiation in the synapse. A similar two-step switching is observed for the higher current compliances as well. The integrated neuron and synapse circuit is now subjected to a stream of input voltage pulses. The circuit implementation of MoS_2 neurons and synapses is shown in **Figure 63(b)**. The conductance state of the MoS_2 synapse is tuned to 11.6 µS. We applied a stream of pulses of a duration of 60 µs and an amplitude of 5 V. The conductance state of the synapse determines the RC time constant of the capacitor charging loop of the RC circuit. As a response to

applied stream of pulses, we observe current spikes from the MoS_2 neuron, as shown in **Figure 63(c)**. Further, we test the frequency of spiking of the neuron-synapse integration circuit by varying the pulse amplitude, as shown in **Figure 63(d)**. Here, we observe that the frequency of spiking increases with the increase in the pulse amplitude. Additionally, we observe an increase in the neuron spiking frequency as we increase the pulse width of the input train of pulses, as shown in **Figure 63(e)**. The spiking frequency is also dependent on the synapse conductance state. As shown in **Figure 63(f)**, the increase in conductance of the synapse results in a higher spiking frequency of the integrated neuron. With increasing synapse conductance, the RC time constant of the charging loop reduces and charges the capacitor C_o faster (integration process of integrate-and-fire neuron), hence increases the spiking frequency. Next, we connected 3 different graphene/MoS_2/SiO_x/Ni synapses of the same device area to a single neuron. The current through the three synaptic resistances connected in parallel add up and flow through the neuron, following Kirchoff's current law. The schematic of the integration is shown in **Figure 63(g)**. **Figure 63(h)** shows the chip image of the arrays of graphene/MoS_2/SiO_x/Ni synapses connecting to a neuron. The conductance states of the synapses are varied. We start with defining two distinct conductance states of the synaptic devices. The synapse is said to be in low conductance state (LCS) when the conductance is < 10 µS. Similarly, the synapse is in a high conductance state (HCS) when the conductance is ≥ 10 µS. State A corresponds to the condition where all three synapses are in LCS. State B corresponds to the state where only one synapse is in HCS and the other two are in LCS. State C corresponds to two synapses in HCS and one synapse in LCS. State D corresponds to all three synapses in HCS. In **Figure 63(i),** we observe that the frequency of the neuron spiking increases as more synapses are tuned to LCS across State A to State D. These results demonstrate that the graphene/MoS_2/SiO_x/Ni synapses are compatible with the MoS_2-based neuron without the

need of any external circuitry for current matching, and their conductance states can aptly modulate the spiking behavior of the LIF neuron.

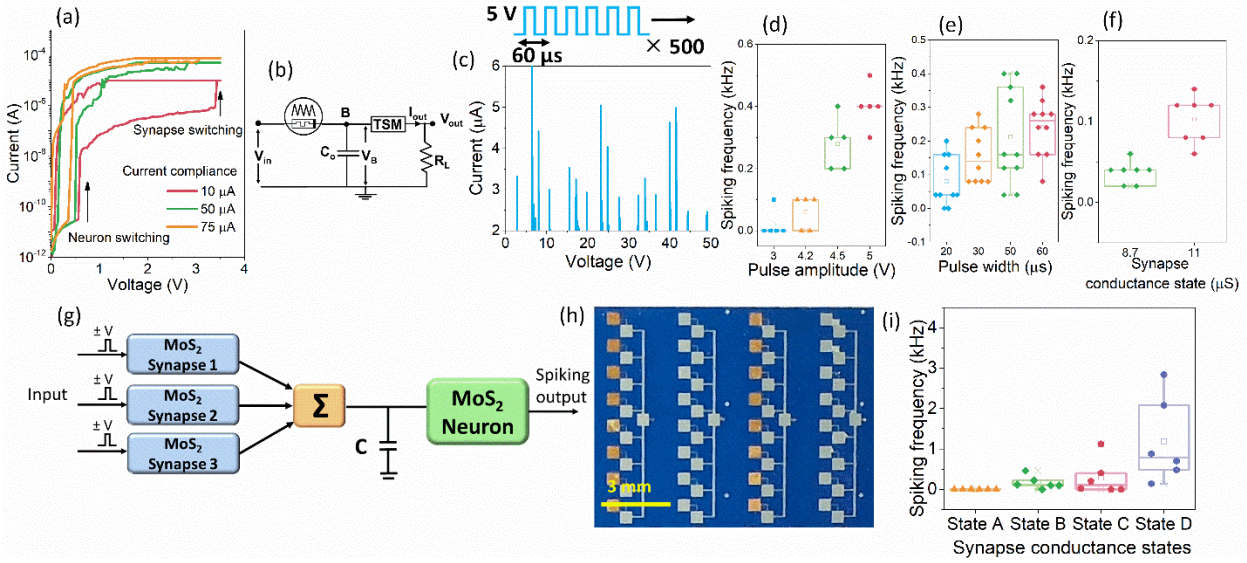

Figure 63: (a) I-V characteristics of series connected individual neuron and synapse. The first switching at lower voltages is due to LIF neuron, because the resistance state does not change as the device is switched with increasing compliance current. The second switching observed at higher voltages is due to artificial synapse (non-volatile) – the resistance state decreases with increasing compliance current. The individual neuron and synapse preserve their characteristics even after integration. (b) The circuit implementation of monolithic integration of single MoS_2 based LIF neuron and single graphene/MoS_2/SiO_x synapse device on the same chip. (c) Output spikes from integration circuit. Spiking increases with increase in input (d) pulse amplitude and (e) pulse width. (f) Spiking frequency increases as synapse conductance increases. (g) Integration of 3 graphene/MoS_2/SiO_x synapses with one LIF neuron. (h) Optical image of chip showing multiple arrays of synapses connected to an LIF neuron (i) Spiking frequency varies as input states of synapses changes.

8.8 SNN simulation

For validating the performance of the monolithically integrated MoS_2 neuron and synapse devices from the system perspective, we apply the extracted experimental parameters for a Spiking Neural Network (SNN) simulation[97], on image classification task with classic MNIST dataset. The SNN is trained with triplet STDP learning rule, while the on-chip training with the proposed

synaptic device can be realized through utilizing the pre-/post-spike interval modulation circuit in[98] and the linear programming region. Note that, the neuron characteristics can be adjusted through configuring the peripheral RC component as well. The simulation shows 89.0% classification accuracy on 10K test images, where the results are shown in **Figure 64.**

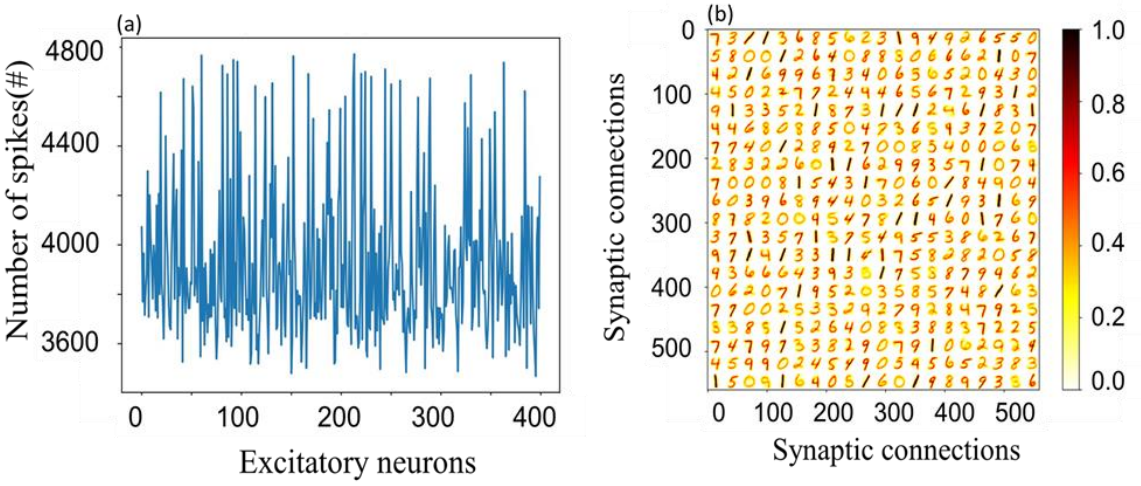

Figure 64: (a) Input spike count of 400 excitatory neurons during inference, on 10K MNIST test images. (b) Normalized synaptic weight of graphene/MoS_2/SiO_x synapse trained by triplet STDP learning rule on MNIST dataset. The simulation shows a classification accuracy of 89 % on 10K test images

8.9 Conclusion

In conclusion, we demonstrate MoS_2/SiO_x synapses with graphene electrode, which exhibit linear and symmetric weight update in response to identical input pulses. The linearity in potentiation is retained for varying pulse width, amplitude and number of applied pulses. The nonlinearity in depression increases with increasing pulse width, amplitude and number of pulses. The process of switching in these devices is through conductive filaments governed by PF emission. We integrate the synapses with MoS_2-based neurons to show the complete control of the neuron through the synaptic conductance states. The integration paves the path for a monolithically

integrated MoS_2-based neural network for pattern recognition. This demonstration exhibits the viability of these devices for future neuromorphic applications and edge computing.

CHAPTER 9 SUMMARY AND FUTURE PERSPECTIVES

9.1 Summary

In summary, this dissertation explored the solutions for high variability and non linear weight updates observed in conventional memristive systems using 2D materials as the switching medium. In this work, we have realized robust memristive synapses using 2D molybdenum disulfide (MoS_2) to address the concerns like high variability and non-linear weight update and asymmetry. We have utilized device engineering techniques like electrode and stack engineering to realize ultra-low variability and linear and symmetric weight update in MoS_2 synapses. The ultra-low C-C and D-D variability is demonstrated in Au/MoS_2/Ti/Au synapses. The interface mediated switching observed in these devices is due to SCLC transport mechanism corroborated by the temperature dependent I-V measurements. We demonstrate ultra-low variability in SET voltage, RESET power and weight update characteristics. Material characterization like TEM reveals the robustness of the stack after biasing. XPS and EELS profile exposes the role played by Ti electrode in obtained ultra-low variability. Further, these synapses were integrated with MoS_2 based LIF neurons to realize AND, OR and NOT logic gates proving the viability of these synapses for in-memory computing. However, these MoS_2 synapses suffer from low G_{max}/G_{min} ratio. Therefore, stack engineering is employed to increase G_{max}/G_{min} ratio while preserving low variability. In that regard, the active medium has been modified from MoS_2 to a heterogenous stack of MoS_2/SiO_x with Ti/Au bottom and top electrodes. Here, an increase in the G_{max}/G_{min} ratio from 2 to ~10 is observed demonstrating the applicability of 2D materials for future neuromorphic applications. Finally, electrode engineering is employed on MoS_2/SiO_x based synapses to demonstrate linear and symmetric weight update. The device configuration from

Au/MoS_2/SiO_x/Ti/Au is changed to graphene/MoS_2/SiO_x/Ni to obtain linear and symmetric weight update with identical pulses essential for their role in online training of neural networks. The linearity in weight update holds for a range of pulse width, amplitude and number of applied pulses. These graphene/MoS_2/SiO_x synapses are integrated with MoS_2-based LIF neuron to demonstrate the efficacy of neuronal spiking. A system-level simulation of an SNN with the behavior model of graphene/MoS_2/SiO_x synapses and MoS_2 neurons exhibits an accuracy of 89% in classification of hand-written digits on MNIST dataset. This work substantiates the necessity of engineering techniques to implement essential synaptic characteristics like ultra-low variability and linear and symmetric weight update.

9.2 Future Perspectives

This dissertation successfully demonstrated the realization of robust synapses showing ultra-low C-C and D-D variability. Preliminary circuit implementations demonstrate the possibility of monolithic integration MoS_2 synapses and neurons. This also opens many avenues that can be pursued with these devices. The implementation of cross bars using MoS_2 synapses and neurons for pattern recognition will further the cause of 2D materials for future computing applications. The successful implementation of 2D materials cross bars depends on the robust synaptic and neuron devices. However, these implementations can suffer from sneak path currents and IR drop. Sneak path currents can be reduced by engineering the device to show non-linear resistive switching. The IR drop can be alleviated by increasing the thickness of the interconnect metal.

The XPS spectra comparison between the pristine and biased devices shall reveal the role played by dominant species that is responsible for obtaining ultra-low variability. This can further studied by changing the top electrode from Ti to other active metal like Ni. Additionally, it is also essential to understand the role played by SiO_x layer in Ti/Au/MoS_2/SiO_x/Ti/Au device in obtaining ultra-low variability. Therefore, it is necessaryl to optimize the thickness of SiO_x that can ensure ultra-low D-D variability.

The optimization of SiO_x layer is also helpful in obtaining robust linear weight update synapses. The devices exhibit excellent potential for unsupervised learning applications. The linear weight update should be explored for low C-C and D-D variability.

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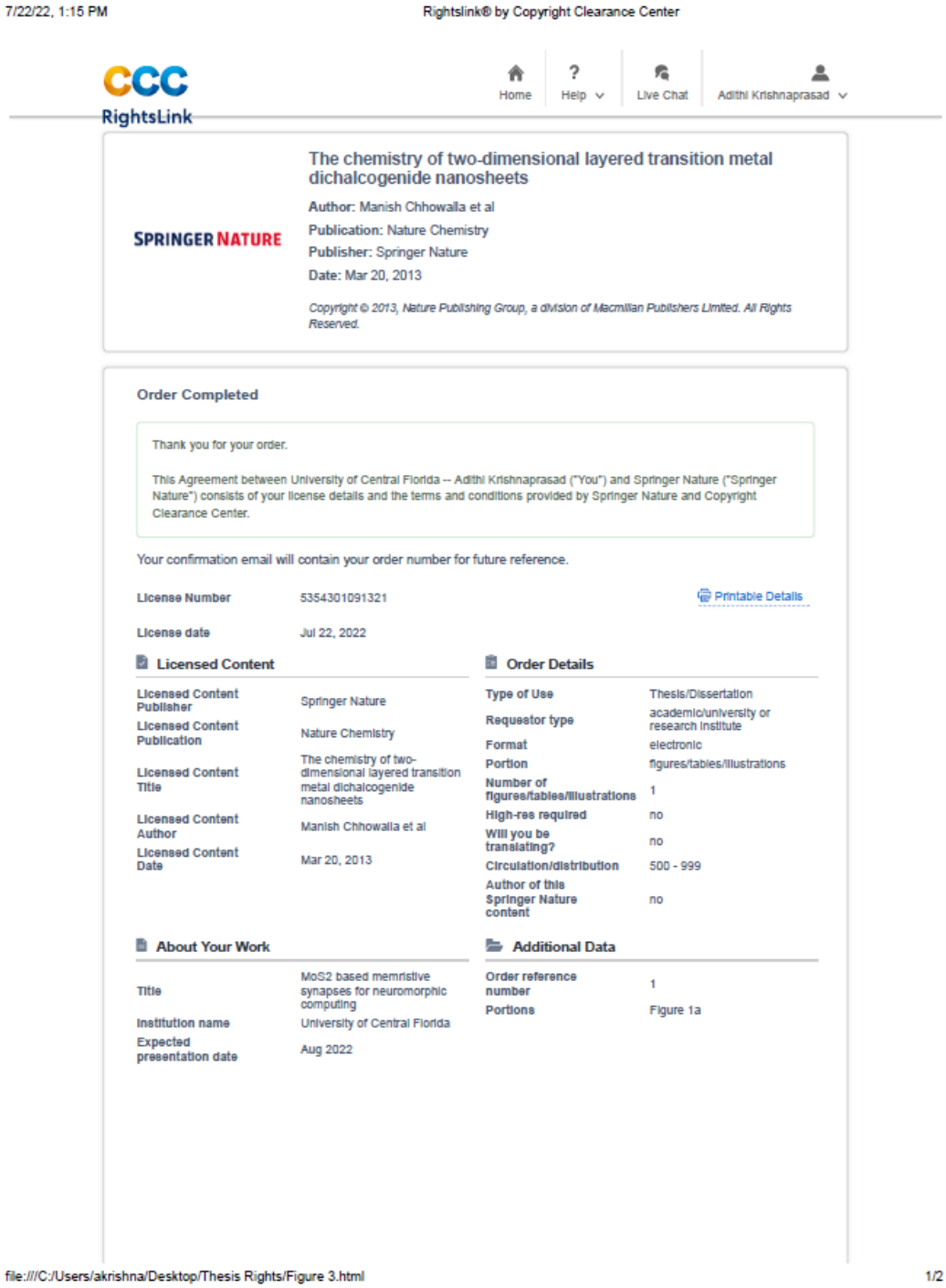

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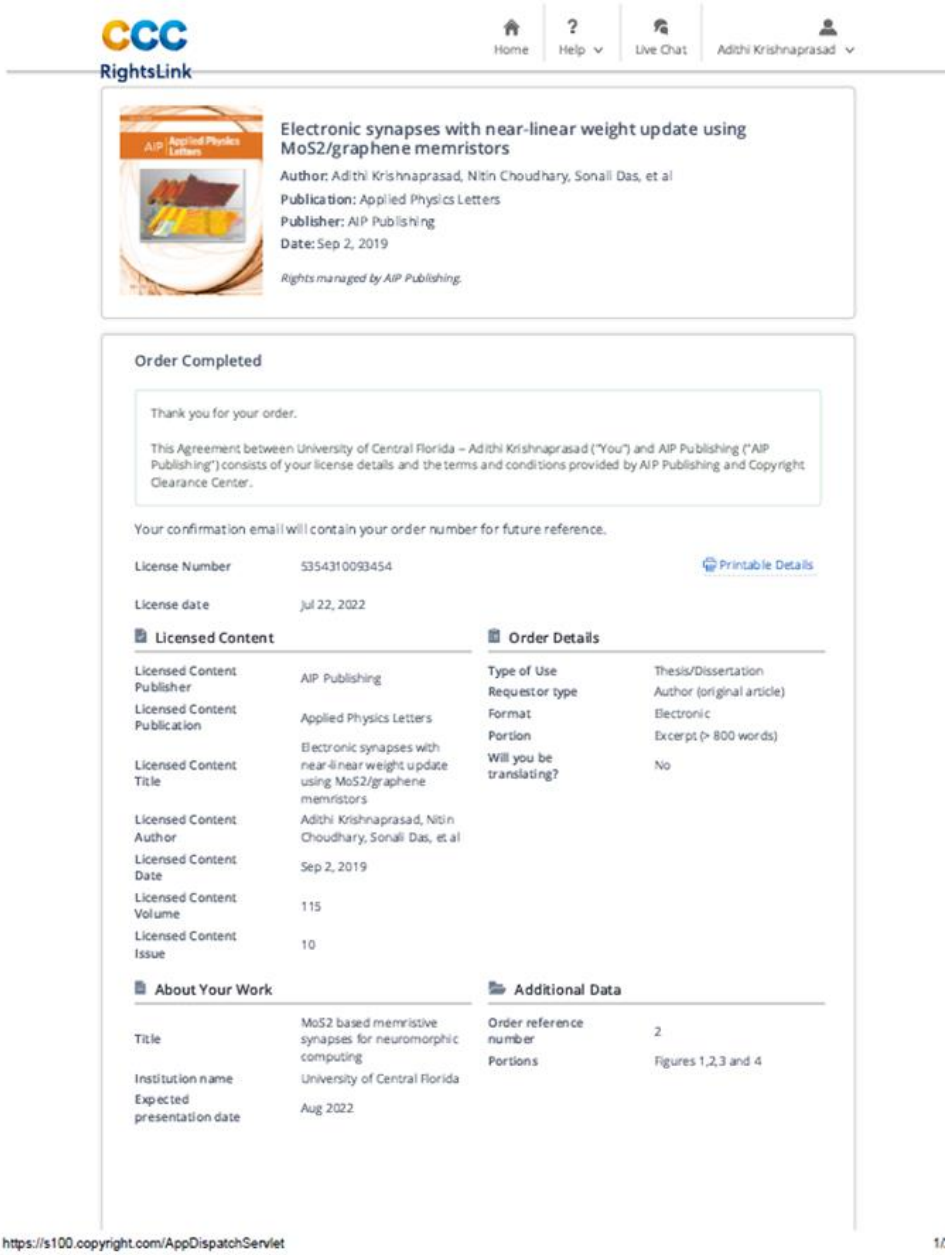

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MoS2 Synapses with Ultra-low Variability and Their Implementation in Boolean Logic

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