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Design of Low–power 4-bit Flash ADC Using Multiplexer Based Encoder in 90nm CMOS Process

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***Abstract*—This work describes a 4-bit Flash ADC with low power consumption. The performance metrics of a Flash ADC depend on the kind of comparator and encoder used. Hence open-loop comparator and mux-based encoder are used to obtain improved performance. Simulation results show that the simulated design consumes 0.265mW of power in 90nm CMOS technology using cadence-virtuoso software. The circuit operates with an operating frequency of 100MHz and a supply voltage of 1V.**

***Keywords*—FLASH ADC; Low Power; Dynamic Comparator; Encoder**

I. Introduction

AMONG the different types of ADC, the Flash ADC is proven to be the high-speed ADC[1-3]. The Flash ADC consists of a series of resistor strings and the input analog signal is compared with a reference voltage. The number of comparators required to convert the sample and held analog input signal to digital output is $2^n - 1$[4-5].

A set of comparators are used for conversion, hence called Flash type ADC. Also known as the parallel A/D converter its circuit is the simplest to understand. It consists of a series of comparators. The sample and held analog input signal and the reference signal is compared in the comparator and the digital output obtained is given to the encoder. The output is produced by the merging of the outputs of the comparator and inputs of the encoder.

Flash ADCs use lots of comparators. The input signal is given to the series of comparators at an instant therefore the output delay is very less. The $2^n - 1$ comparator outputs act analogously. Since the outputs from the comparator are not practical, an encoder is required to produce N-bit output[6]. The resistance of the resistor ladder should be less to supply enough current to the fast comparators.

II. Proposed Methodology

The main components in Flash ADC are comprised of 3 units. The Resistive Ladder network, Comparator, and the proposed multiplexer-based encoder circuit.

Resistive Ladder Network

The resistor string network is used to give the reference voltage (V_{ref}) to the comparator circuit. The resistive ladder network consists of a set of resistors. Depending on the resistor values the reference voltage gets divided when it is given to the beginning of the resistive ladder. Figure 1 shows the resistive ladder network.

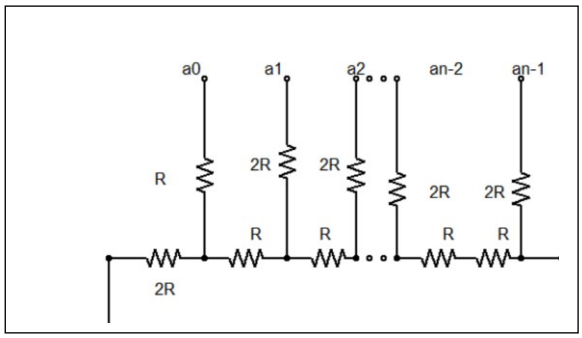

Fig.1. Resistive ladder Network

A. Comparator

The Comparator forms the main building block of FLASH ADC. The input analog signal is compared with a reference voltage in the comparator and produces a digital signal[7-9]. When the input voltage is greater than the reference voltage the comparator output is logic 1. When the input voltage is less than the reference voltage the comparator output is logic 0. Fig.2 shows the basic block of a comparator. The comparator used in the Flash ADC is an open-loop comparator.

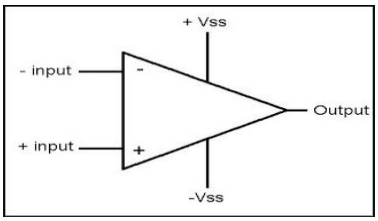

Fig. 2. The basic block of Comparator

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B. *Open Loop Comparator*

Mehdi Nasrollahpour [10] proposed the open-loop comparator circuit which comprises analog input and reference input. This comparator consists of the differential amplifier, input, and output phase. The main usage of this loop comparator is the reduced complexity. Hence the circuit occupies a small area. Fig.3 shows the circuit of an open-loop comparator. To achieve high gain two-stage comparators were used. To implement a high gain, open-loop comparator, the 2-stage op-amp will be appropriate.

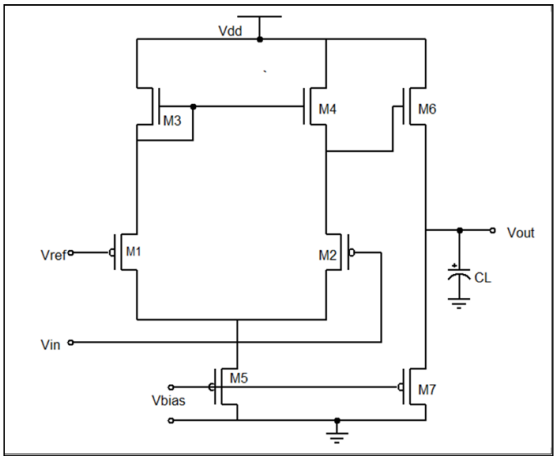

Fig. 3. Two stage open-loop comparator [17]

C. *Encoder*

An encoder performs the reverse function of the decoder. It encodes data from 2^n inputs into an n-bit output. The basic block of the encoder is shown in Fig.4.

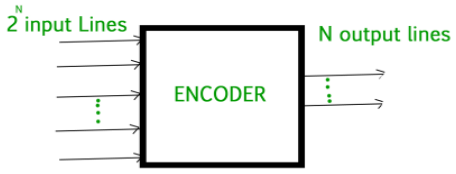

Fig.4. Block diagram of an encoder

A multiplexer-based Transmission Gate (TG) is used in the proposed encoder. The main advantage of using a TG-based multiplexer is to reduce the complexity. By using the mux-based encoder the performance of the 4-bit Flash ADC is improved. The multiplexer acts as a data selector which consists of input lines, select lines, and output lines. The performance of the mux-based encoder using TG has been improved when compared with the conventional type of encoders.

D. *Mux based encoder*

Fig. 5 shows the implementation of Mux based encoder for 15-bit thermometer code input. The speed of the Mux-based encoders is high when compared with the existing encoders. Among the various encoder architectures used by the FLASH ADC, the proposed Mux-based encoder is used for high-resolution applications. Fig.6 shows the symbolic representation of a multiplexer. The multiplexer acts as a data selector and provides a single output.

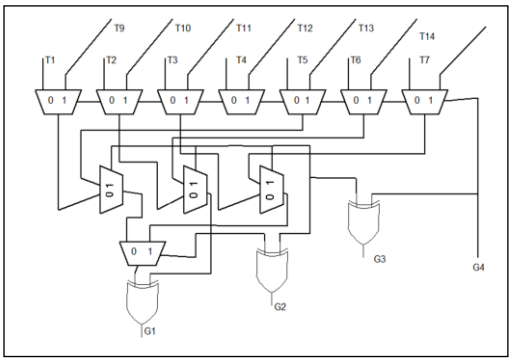

Fig.5. Circuit diagram of Mux based encoder

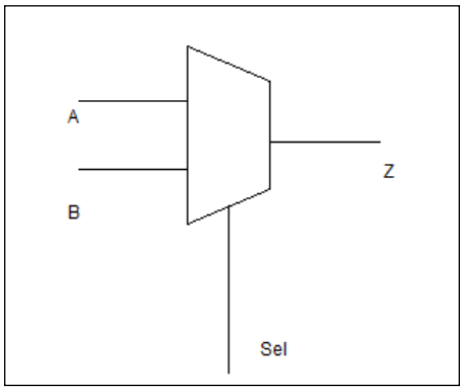

Fig.6. Symbol of MUX

TABLE I
TRUTH TABLE OF 2X1 MUX

Sel	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

In 2-to-1 multiplexer, A and B are the two inputs, Sel is the selector input, and Z is the output. Table-1 shows the truth table of MUX.

III. RESULTS AND DISCUSSION

The designed 4-bit FLASH ADC comprises of resistive ladder circuit, open-loop comparator, and multiplexer-based encoder circuit. All the blocks are designed based on the aspect ratio of transistors. The simulation is done in a cadence-virtuoso tool using 90nm CMOS technology. The simulation results show that the proposed FLASH ADC consumes less power when compared with the conventional FLASH ADC.

IV. RESISTIVE LADDER NETWORK

The resistor ladder divides the reference voltage Vref into 8 parts[11-12]. The value of the resistor used is 1kΩ from the analog library of cadence-virtuoso software

V. COMPARATOR BLOCK

The basic function of the comparator is to compare both the reference voltage and the input voltage supplied. The input given to the comparator is an analog input. Fig.7 shows the circuit diagram of two-stage open-loop comparator block.

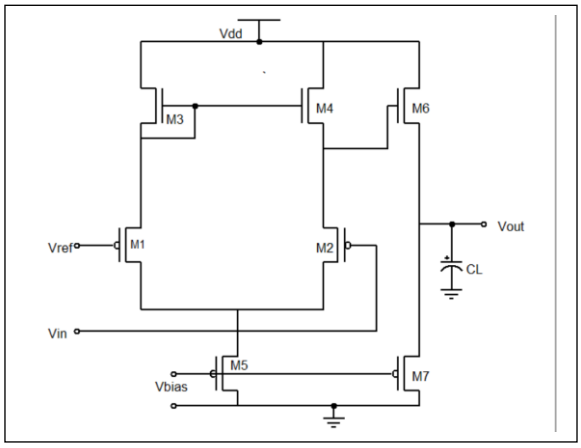

Fig.7. A 2- stage open-loop comparator

When the analog input signal is more than the V_{ref} the comparator turns high. When the analog input signal is less than the V_{ref} the comparator output turns low [13-14]. Fig.8 shows the waveform of the open-loop comparator.

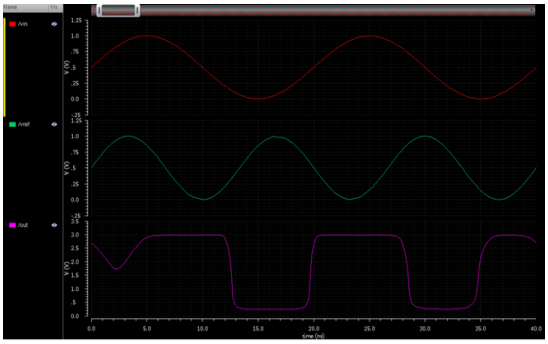

Fig.8. Waveform of 2- stage open-loop comparator

The output waveform is generated by comparing the analog input signal and the reference signal. Fig. 9 shows the power consumption of the open-loop comparator.

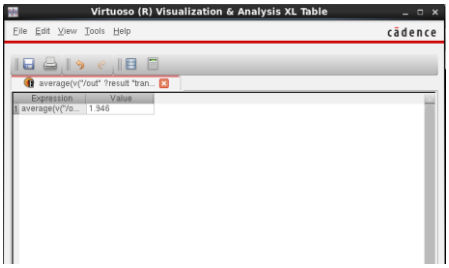

Fig.9. Power result of 2- stage open-loop comparator

The comparator circuit is further converted to a symbol.Fig.10 shows the symbol of the comparator.

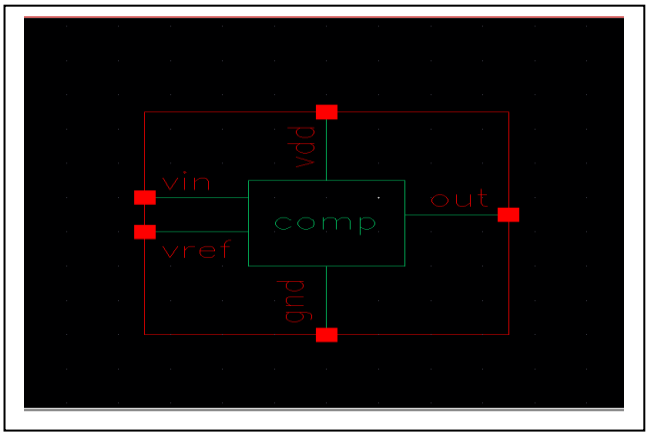

Fig.10. Symbol of 2- stage open-loop comparator

VI. ENCODER BLOCK

The encoder block consists of two circuits namely inverter, multiplexer. These circuits are designed as cell views and then converted to symbols.

VII. INVERTER

Input is given to the inverter, the output obtained is the inversion of the given input signal. Fig.11 shows the circuit of an inverter.

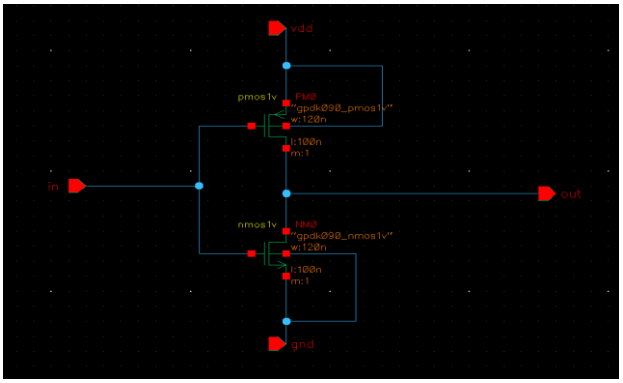

Fig.11. Schematic of Inverter

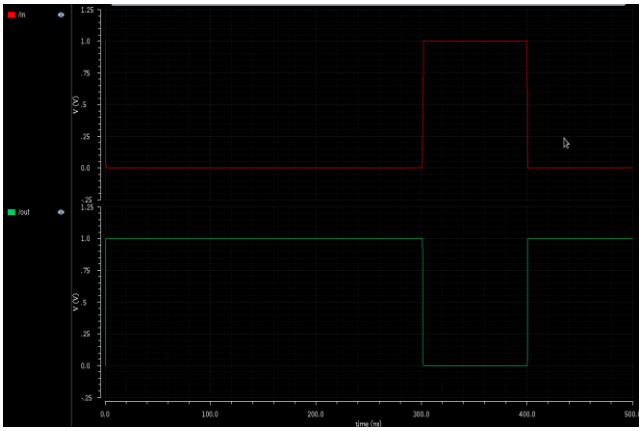

Fig.12. Waveform of an inverter

Fig.12 shows the waveform of the inverter. The inverter circuit is further converted to a symbol. Fig.13 shows the symbol of the inverter.

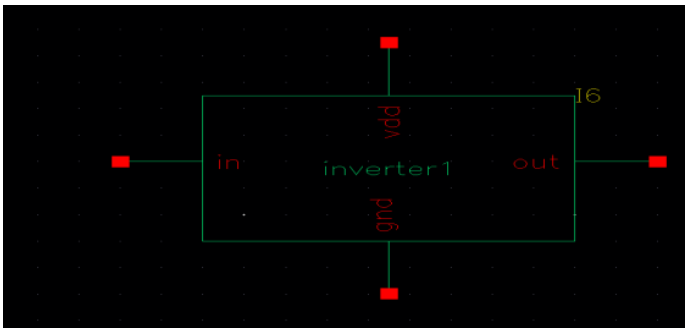

Fig.13. Symbol of Inverter

VIII. MULTIPLEXER

A multiplexer also called a data selector selects between several input signals and forwards it to a single output line. A multiplexer selects a particular input line to send to the output. Fig.14 shows the circuit of the multiplexer.

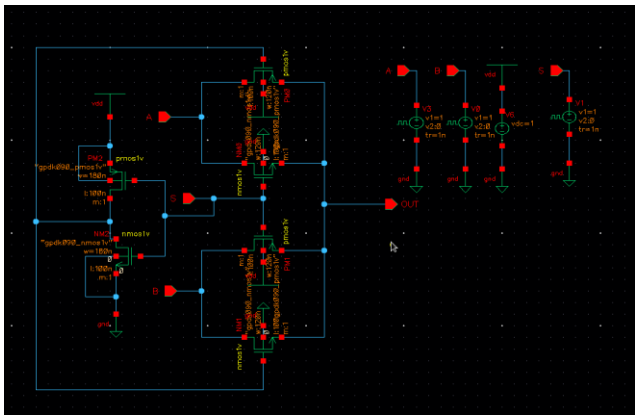

Fig.14. Schematic of multiplexer

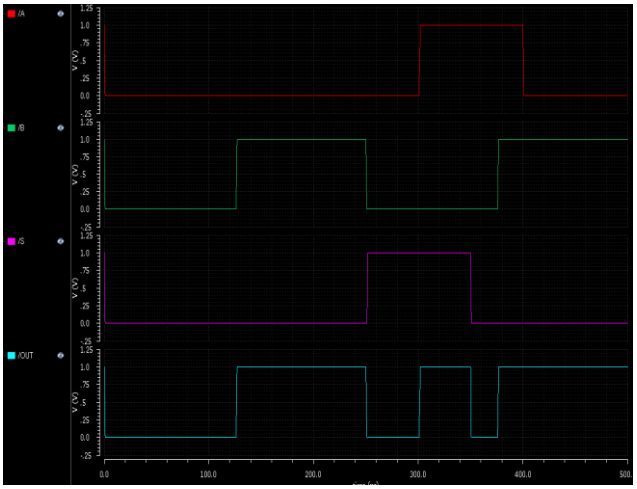

Fig.15. Waveform of the multiplexer

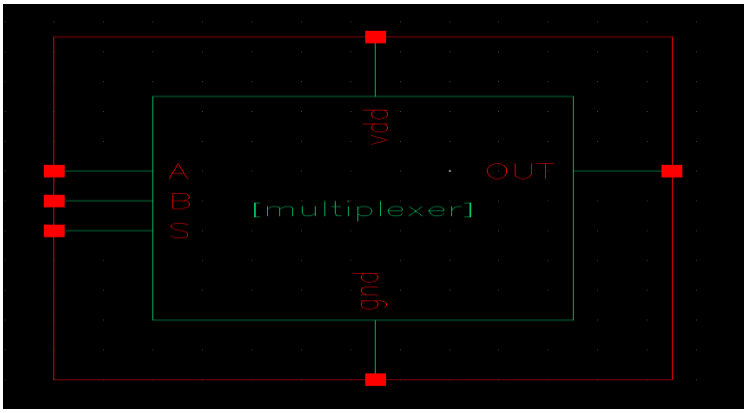

Fig.16. Symbol of multiplexer

The multiplexer circuit is then converted to a symbol. Fig. 16 shows the symbol of the multiplexer.

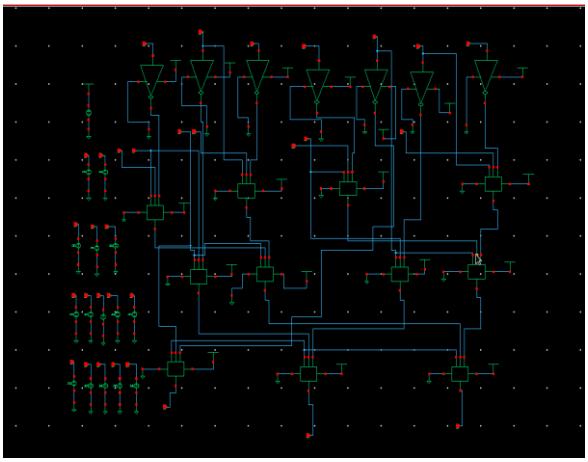

Fig.17. Schematic of MUX-based encoder

Fig.17 shows the circuit of MUX based encoder. The proposed mux-based encoder consists of multiplexers and NOT gate. Fig.18 shows the average power of the MUX-based encoder. The Flash ADC is designed by integrating various sub-blocks including resistive string network, comparator, and mux-based encoder. The Flash ADC is the fastest ADC among all the types of ADCs[16-21].

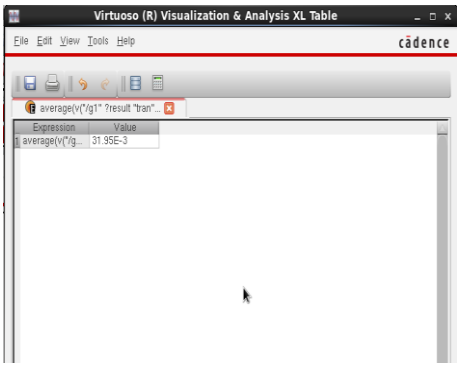

Fig.18. Average power of MUX based encoder

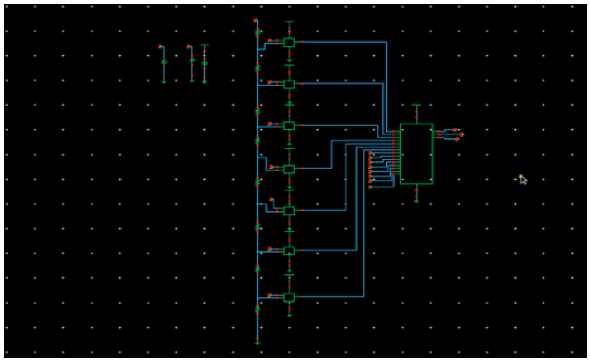

Fig.19. Schematic of Flash ADC

Figure 19 shows the circuit of the 4-bit Flash ADC. As the designed sub-blocks consume less power the proposed 4-bit Flash ADC consumes less power when compared with other types of ADCs.

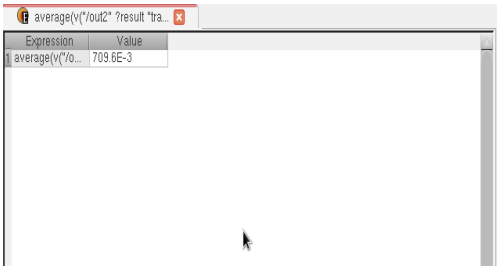

Fig.20. Power of Flash ADC

Figure 20 shows the average power of the Flash ADC. The obtained power for the 4-bit Flash ADC is 0.265mW. The analog input signal is converted into a digital signal in the designed 4-bit Flash ADC. Table 1 shows the parameter values obtained for the 4-bit Flash ADC circuit under 90nm technology with a supply voltage of 1V.

TABLE II
COMPARATIVE STUDY OF THE DESIGNED FLASH ADC WITH OTHER REPORTED WORKS

Parameters	[15]	[7]	**This work**
Technology	90nm	90nm	90nm
Resolution	4-bit	4-bit	4-bit
Supply Voltage	1V	1V	1V
Delay	5.85us	3.97us	2.425us
Power	8.49mW	4.43mW	0.265mW

CONCLUSION

Among the various ADC architectures, FLASH ADC is proved to be the high-performance ADC. The proposed ADC comprises of Multiplexer based encoder, open-loop comparator, and resistive ladder network. The proposed ADC is simulated in 90nm CMOS technology. The main advantage of the proposed ADC is low static power consumption. This was achieved by integrating the multiplexer-based encoder in Flash ADC. The power dissipation of the proposed ADC is 26.65µw for the input of 1V at 100MHz frequency. The designed Flash ADC can be used for high-speed applications.

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