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Abstract: In this study, a three-level hysteresis current-control (HCC) strategy is proposed for three-phase four-switch shunt active power filters. The four-switch topology which utilises four switching devices together with two series connected capacitors is able to reduce the cost, switching losses and improve the reliability of system. In this topology, when the current control of phases A and B is achieved successfully, the current control of phase C which is connected to the midpoint of the series connected capacitors is achieved automatically. The current control is achieved by using a three-level HCC strategy. An important consequence of using this control strategy is that it enables access to the zero level of the input voltage of active filter so that a switching device is only switched when the current error is negative, while it remains off when the current error is positive. Furthermore, the imbalance in the capacitor voltages is eliminated by adding a feedback term (the difference in the capacitor voltages multiplied by a suitable gain) to the current control. The proposed control strategy offers a reduced switching frequency, losses and cost. The steady-state and dynamic performance of the proposed control strategy is verified through simulations and experimental studies.

1 Introduction

Owing to the common use of power electronics in domestic, industrial and commercial devices, the harmonic current distortion on the utility is increasing. This current distortion causes low-power factor, I^2R losses and harmful disturbance to neighbour loads which are tied at the point of common coupling (PCC). Conventional switched capacitors with tuned LC filters are usually employed to reduce the current harmonics. However, the use of such filters has many disadvantages such as resonance problem, fixed compensation ability and large size. Also, the performance of the system may be adversely affected from the changes in the filter parameters due to temperature and ageing.

As a remedy to these drawbacks, the use of shunt active power filters (APFs) to solve current harmonic problems has drawn much attention since the 1970s, because they have good filtering characteristics [1–3]. Voltage-source inverter (VSI) with six switching devices is the most preferred topology for the three-phase shunt APF [4–13]. The control methods that have been studied for shunt APFs have three important parts: (i) determination of reference compensation current from the distorted load current; (ii) the current control of the VSI; and (iii) the voltage control on the DC-link capacitor. The compensating current reference generation process usually involves various methods. The quality of the current-control strategy greatly influences the overall performance of the APF system. Besides this, these methods play a very important role in the improvement of steady-state and dynamic performances and the stability of the filter. Since the load current harmonics may change rapidly, the APF should have a fast dynamic response for achieving a high accuracy. The current-control loop is known to be always faster than the voltage-control loop. Therefore, the reference current tracking is accomplished by using the current control. The DC voltage stabilisation is achieved by the voltage-control loop. Despite the satisfactory performance of existing control strategies developed for the three-phase six-switch topology, various control strategies are also developed for the three-phase four-switch topology which are successfully implemented in the control of rectifiers [14–16], inverters [17–20] and shunt APFs [21–27]. An important consequence of using four-switch topology is that the total cost and switching losses are reduced and the reliability of the system is improved [21]. Reducing the number of converter legs from three to two decreases the switching losses by one third which means that the efficiency of four-switch topology is improved by one third compared with the six-switch topology [21].

The existing control strategies proposed for shunt APFs employing four-switch topology yield various advantages and disadvantages. The control strategies presented in [21, 22] are based on proportional–integral (PI) control which requires four gains. The control strategy presented in [23] has two separate parts, one for three-phase sinusoidal waveform generation and the other for the current control which makes use of the conventional two-level hysteresis current-control (HCC) method. The one cycle control approach presented in [24] offers a good performance and does not require generation of the reference waveform. The space vector pulse-width modulation (PWM) algorithm and DC-side voltage-control strategy proposed in [25] is complicated by the fact that it involves transformations from *abc* frame to rotating *dq* frame and vice versa. Moreover, two PI controllers with a total number of four gains are needed for a successful operation. The variable parameter PWM-based current tracking approach presented in [26] improves the utilisation of DC voltage and widens the voltage range of the four-switch topology. In addition, the proposed strategy exhibits better performance in transient response and tracking accuracy compared with the triangle-based PWM. Though the advanced current-control strategy proposed in [27] offers a good steady-state and dynamic response, it does not consider the imbalance problem of the capacitor voltages.

In this paper, a three-level HCC strategy involving an imbalance compensation loop for three-phase four-switch shunt APFs is proposed. An important consequence of using this control strategy is that it enables access to the zero level of the active filter's input voltage so that a switching device is only switched when the current error is negative, while it remains off when the current

error is positive. The three-level HCC strategy not only maintains the advantages of conventional two-level HCC (higher accuracy, fast dynamic response, robustness and easy implementation), but also offers additional advantages such as reduced switching frequency and switching losses. Furthermore, the imbalance problem existing in the capacitor voltages is eliminated. The performance of the three-level HCC strategy under non-linear load currents is investigated by computer simulations and experimental study under real time-laboratory (RT-LAB) developed by OPAL-RT.

2 Three-phase four-switch shunt APF modelling

A three-phase four-switch shunt APF configuration is shown in Fig. 1. It can be seen from Fig. 1 that the APF is connected to PCC which makes it shunt with the non-linear load and mains supply. A VSI which contains four switching devices is utilised in the APF. The phase C is connected to the mid-point of the split DC-link capacitors. This implies that the phase C current is forced to flow through the DC-link capacitors which cause a fluctuation in the capacitor voltages. The main goal of the APF is to consume three-phase currents (i_{Fa}, i_{Fb} and i_{Fc}) from the mains supply so as to obtain undistorted source currents (i_{sa}, i_{sb} and i_{sc}) at unity power factor which are deteriorated by the non-linear load currents (i_{La}, i_{Lb} and i_{Lc}). It is required that the source currents are sinusoidal and in phase with the source voltages. Operation of the three-phase four-switch shunt APF can be described by the following equations

$$L\frac{\mathrm{d}i_{Fa}}{\mathrm{d}t}+ri_{Fa}=e_{sa}-v_{an} \tag{1}$$

$$L\frac{\mathrm{d}i_{Fb}}{\mathrm{d}t}+ri_{Fb}=e_{sb}-v_{bn} \tag{2}$$

$$L\frac{\mathrm{d}i_{Fc}}{\mathrm{d}t}+ri_{Fc}=e_{sc}-v_{cn} \tag{3}$$

$$C_1\frac{\mathrm{d}v_{c1}}{\mathrm{d}t}=\frac{1}{2}(p_a i_{Fa}+p_b i_{Fb}-i_{Fc}) \tag{4}$$

$$C_2\frac{\mathrm{d}v_{c2}}{\mathrm{d}t}=\frac{1}{2}(p_a i_{Fa}+p_b i_{Fb}+i_{Fc}) \tag{5}$$

where r is the inductor resistance. The phase-to-neutral voltages of phase A, phase B and Phase C (v_{an}, v_{bn} and v_{cn}) in terms of the capacitor voltages and switching functions are given by [14, 16]

$$v_{an}=\frac{1}{6}(2p_a-p_b+1)v_{c1}+\frac{1}{6}(2p_a-p_b-1)v_{c2} \tag{6}$$

$$v_{bn}=\frac{1}{6}(2p_b-p_a+1)v_{c1}+\frac{1}{6}(2p_b-p_a-1)v_{c2} \tag{7}$$

$$v_{cn}=\frac{1}{6}(-p_a-p_b-2)v_{c1}+\frac{1}{6}(p_a-p_b+2)v_{c2} \tag{8}$$

The three-phase source voltages are assumed to be balanced as

$$e_{sa}=E_m\cos(\omega t) \tag{9}$$

$$e_{sb}=E_m\cos\left(\omega t-\frac{2\pi}{3}\right) \tag{10}$$

$$e_{sc}=E_m\cos\left(\omega t-\frac{4\pi}{3}\right) \tag{11}$$

The four switching devices are controlled with the bipolar switching functions defined by

$$p_k=\begin{cases}1 & S_k \text{ closed}\\ -1 & \bar{S}_k \text{ closed}\end{cases},\quad k=a,\ b \tag{12}$$

Also, it is assumed that the series connected capacitors are identical ($C_1=C_2$). However, in practice, the values of these capacitors may not be equal which cause imbalance between v_{c1} and v_{c2}.

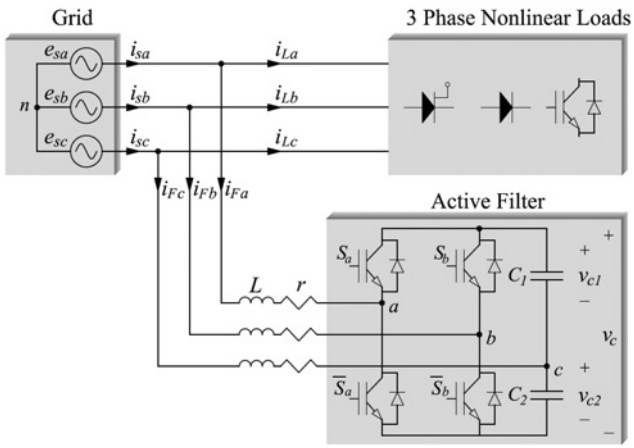

Fig. 1 *Three-phase four-switch shunt APF*

3 Control strategy

It should be noted that regardless of the topology, the control strategy of a three-phase shunt APF has two objectives. The first objective is to have sinusoidal source currents in phase with the source voltages. The second objective is the stabilisation of the DC output voltage (v_c) at a required value. These objectives can be achieved by utilising an inner loop for shaping the source currents and an outer loop for regulating the DC output voltage.

3.1 Two-level HCC

The sinusoidal source currents in phase with the source voltages (the first objective mentioned above) can be accomplished by forcing phases A and B source currents to follow their references defined as

$$i_{sa}^{*}=I_m(t)\cos(\omega t) \tag{13}$$

$$i_{sb}^{*}=I_m(t)\cos\left(\omega t-\frac{2\pi}{3}\right) \tag{14}$$

where $I_m(t)$ represents the amplitude of three-phase source currents. Having generated i_{sa}^{*} and i_{sb}^{*}, the active filter current references for phases A and B can be generated by subtracting the measured load current from the reference source current as follows

$$i_{Fa}^{*}=i_{sa}^{*}-i_{La} \tag{15}$$

$$i_{Fb}^{*}=i_{sb}^{*}-i_{Lb} \tag{16}$$

Here, it is important to note that the control of phase C current is achieved automatically by controlling the currents of phases A and B. In the conventional two-level HCC strategy, the current (in the case of APF, it is filter current) which is supposed to be controlled is maintained inside the hysteresis band in the vicinity of its reference by turning corresponding switching device on and off.

The gate signals of the switching devices (g_1, g_2, g_3 and g_4) are generated from the current error obtained for each phase as follows

$$i_{ek} = i^*_{Fk} - i_{Fk} \tag{17}$$

Fig. 2*a* shows the switching in the two-level HCC strategy for phase A. It is obvious that this control strategy has two levels only. The on and off periods of the switching devices S_a and $\bar{S}_a$ during the evolution of the active filter current i_{Fa} are also depicted in Fig. 2*a*. It is worth noting that the DC output voltage should be large enough for effective current tracking. The switching of S_a and $\bar{S}_a$ during one complete cycle occurs according to the following switching logic

$$S_a = \begin{cases} \text{off} & \text{when } i_{Fa} > i^*_{Fa} + h \\ \text{on} & \text{when } i_{Fa} < i^*_{Fa} - h \end{cases} \tag{18}$$

$$\bar{S}_a = \begin{cases} \text{on} & \text{when } i_{Fa} > i^*_{Fa} + h \\ \text{off} & \text{when } i_{Fa} < i^*_{Fa} - h \end{cases} \tag{19}$$

The switching for phase B is done similarly, using the corresponding reference and measured current.

3.2 Three-level HCC

It can be seen from Fig. 2*a* that the current error in the two-level HCC strategy has two levels which means that the switching devices connected to one leg (phase A or B) of the VSI are turned on and off continuously in one cycle. Such operation leads to high switching frequency, and therefore increases the overall switching losses. The three-level HCC strategy proposed here aims at reducing the switching losses. Fig. 2*b* shows the three-level HCC for phase A when the current error is positive. It can be seen that S_a is turned on and off ($p_a = 1$ and $p_a = 0$) when the current error is positive. In this case, $\bar{S}_a$ is continuously off. When the current error becomes negative, $\bar{S}_a$ is turned on and off ($p_a = -1$ and $p_a = 0$). During this time S_a is continuously off. From Fig. 2*b*, the following equations can be written for T_{on} and T_{off} (for sake of simplicity r is neglected)

$$\frac{\mathrm{d}i^+_{Fa}}{\mathrm{d}t} T_{\text{on}} - \frac{\mathrm{d}i^*_{Fa}}{\mathrm{d}t} T_{\text{on}} = h \tag{20}$$

$$\frac{\mathrm{d}i^-_{Fa}}{\mathrm{d}t} T_{\text{off}} - \frac{\mathrm{d}i^*_{Fa}}{\mathrm{d}t} T_{\text{off}} = -h \tag{21}$$

Adding (20) and (21) yields

$$\frac{\mathrm{d}i^+_{Fa}}{\mathrm{d}t} T_{\text{on}} + \frac{\mathrm{d}i^-_{Fa}}{\mathrm{d}t} T_{\text{off}} - \frac{1}{f_{\text{sw}}} \frac{\mathrm{d}i^*_{Fa}}{\mathrm{d}t} = 0 \tag{22}$$

where $f_{\text{sw}} = 1/(T_{\text{on}} + T_{\text{off}})$ is the switching frequency. Subtracting (21) from (20) gives

$$\frac{\mathrm{d}i^+_{Fa}}{\mathrm{d}t} T_{\text{on}} - \frac{\mathrm{d}i^-_{Fa}}{\mathrm{d}t} T_{\text{off}} - \left(T_{\text{on}} - T_{\text{off}}\right) \frac{\mathrm{d}i^*_{Fa}}{\mathrm{d}t} = 2h \tag{23}$$

Since $\left(\mathrm{d}i^+_{Fa}/\mathrm{d}t\right) = -\left(\mathrm{d}i^-_{Fa}/\mathrm{d}t\right)$, then (22) and (23) can be simplified as

$$T_{\text{on}} - T_{\text{off}} = \frac{\mathrm{d}i^*_{Fa}/\mathrm{d}t}{f_{\text{sw}}\left(\mathrm{d}i^+_{Fa}/\mathrm{d}t\right)} \tag{24}$$

$$\frac{1}{f_{\text{sw}}} \frac{\mathrm{d}i^+_{Fa}}{\mathrm{d}t} - \left(T_{\text{on}} - T_{\text{off}}\right) \frac{\mathrm{d}i^*_{Fa}}{\mathrm{d}t} = 2h \tag{25}$$

Substituting (24) into (25) and $\left(\mathrm{d}i^+_{Fa}/\mathrm{d}t\right) = \left(1/L\right)(e_{sa} - v'_{an})$ into the resulting equation yields

$$f_{\text{sw}} = \frac{\left(e_{sa} - v'_{an}\right)}{2Lh} \left[1 - \frac{m^2 L^2}{\left(e_{sa} - v'_{an}\right)^2}\right] \tag{26}$$

where $m = \left(\mathrm{d}i^*_{Fa}/\mathrm{d}t\right)$ and $v'_{an} = \left(1/6\right)\left[\left(3 - p_b\right)v_{c1} + \left(1 - p_b\right)v_{c2}\right]$ is the phase-to-neutral voltage of the active filter when S_a is turned on ($p_a = 1$). It is clear from (26) that the switching frequency (f_{sw}) is time-varying and is a function of the hysteresis band (h) and inductor L. It is well known that the value of L determines the amount of ripple in the current. Hence, the filter inductor L is to be chosen to make a compromise between targeted switching frequency and current ripple. On the other hand, since the value of h determines f_{sw}, it should be selected so as to achieve a reasonable total harmonic distortion (THD) of source currents under targeted f_{sw}.

3.3 Output voltage control

The second objective was the stabilisation of the DC output voltage at a required value. To accomplish this, it is needed to regulate the amplitude of three-phase source currents to a desired reference.

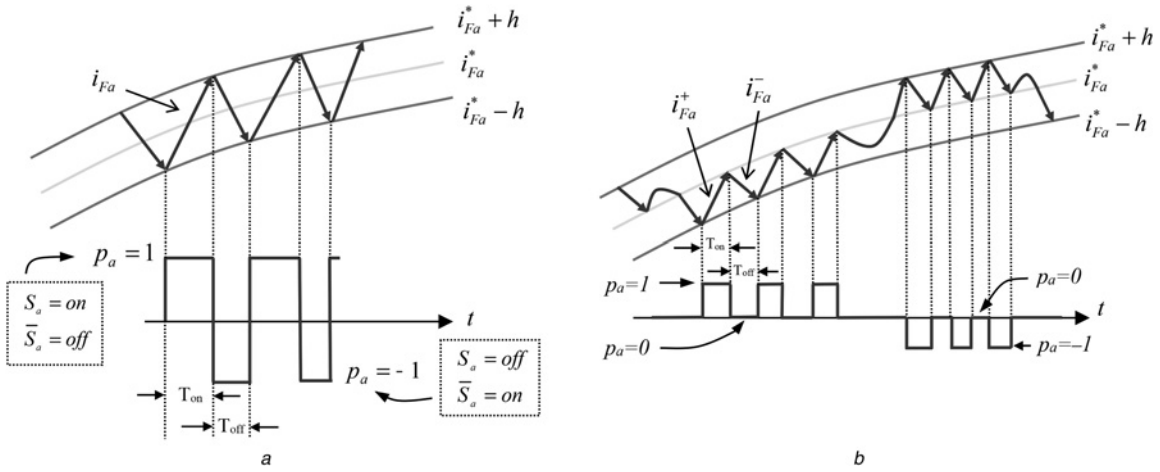

Fig. 2 *HCC for phase A*

a Two-level
b Three-level

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Table 1 Parameters of the system

Symbol	Value
E_m – line to neutral voltage amplitude	50 V
f – supply frequency	50 Hz
C_1, C_2 – DC capacitors	750 μF
L – inductor	4 mH
r – inductor resistance	1 Ω
V_c – reference voltage	250 V
h – hysteresis band	0.1 A
k_p – proportional gain	0.12
k_i – integral gain	1.0
k_e – imbalance compensation gain	−0.05
T_s – sampling time	25 μs
load$_1$ – non-linear load res. and ind.	20 Ω, 80 mH
load$_2$ – non-linear load res. and ind.	40 Ω, 40 mH

When the source current regulation is achieved successfully, the output voltage reaches to its reference (V_c) indirectly. The value of source current amplitude reference is determined by a PI controller which operates as an outer voltage loop [10, 11]

$$I_m(t) = k_p(V_c - v_c) + k_i \int (V_c - v_c)\mathrm{d}t \tag{27}$$

where k_p and k_i denote the PI gains, respectively.

3.4 Compensation of imbalance in capacitor voltages

It is mentioned in [14, 16] that there exists an imbalance in the capacitor voltages (v_{c1} and v_{c2}). One of the reasons of this imbalance comes from a DC offset caused by the system's initial condition. The other reason is the non-equal capacitance values ($C_1 \neq C_2$) in practice. Inspired from the method presented in [28], this imbalance in capacitor voltages can be eliminated by feeding back the imbalance variable ($v_{ce} = v_{c1} - v_{c2}$), multiplying it by a gain (k_e) and adding the multiplication result to i^*_{Fa} and i^*_{Fb} as follows

$$i^*_{Fa,e} = i^*_{Fa} + k_e v_{ce} \tag{28}$$

$$i^*_{Fb,e} = i^*_{Fb} + k_e v_{ce} \tag{29}$$

where $k_e < 0$. In this case, the active filter currents (i_{Fa} and i_{Fb}) track the modified references ($i^*_{Fa,e}$ and $i^*_{Fb,e}$) instead of i^*_{Fa} and i^*_{Fb}. The capacitor voltage difference ($v_{ce} = v_{c1} - v_{c2}$) utilised in (28) and (29) converges to zero through imbalance compensation loop action. Let us validate this mathematically. The capacitor currents and their sum are given by

$$\begin{aligned} i_{dc1} &= -p_a i_{Fa} - p_b i_{Fb} \\ i_{dc2} &= -(1-p_a) i_{Fa} - (1-p_b) i_{Fb} \\ i_{dc1} + i_{dc2} &= -(i_{Fa} + i_{Fb}) = i_{Fc} \end{aligned} \tag{30}$$

In the derivation of $i_{dc1} + i_{dc2}$, it is assumed that $C_1 = C_2$. The capacitor currents in terms of switching functions and filter

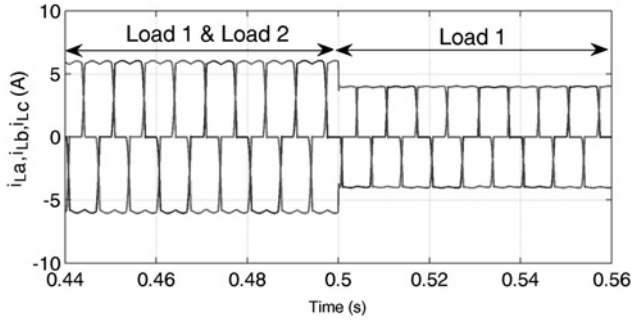

Fig. 3 *Non-linear load current waveforms*

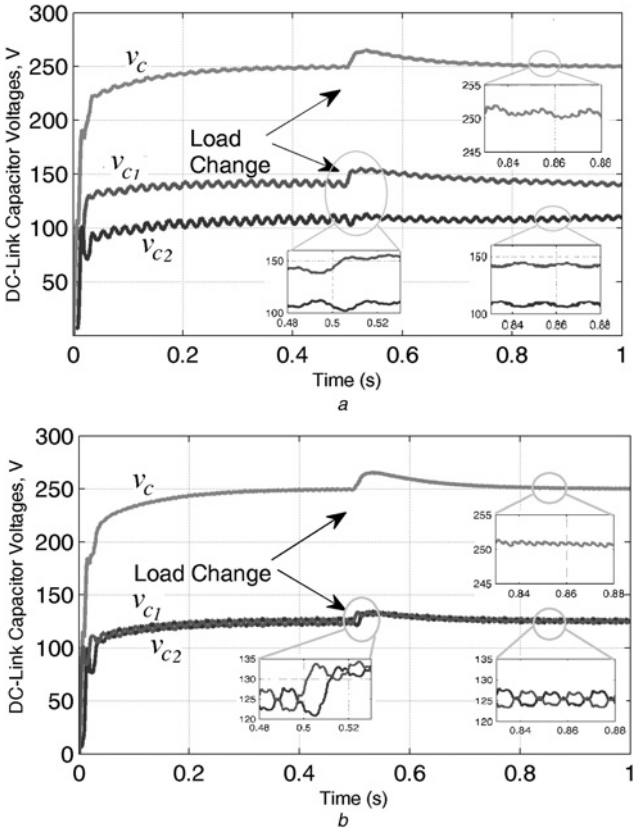

Fig. 4 *DC-link capacitor voltage waveforms*

a Without imbalance compensation loop
b With imbalance compensation loop

currents are

$$\begin{aligned} i_{dc1} &= -p_a i_{Fa} - p_b i_{Fb},\ i_{dc2} \\ &= -(1-p_a) i_{Fa} - (1-p_b) i_{Fb},\ i_{dc1} + i_{dc2} = -(i_{Fa} + i_{Fb}) \\ &= i_{Fc} \end{aligned} \tag{31}$$

Equating (30) and (31) gives

$$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t} = -\frac{1}{C_1} i_{Fc} \tag{32}$$

Now, adding (28) and (29) gives

$$i^*_{Fa,e} + i^*_{Fb,e} = i^*_{Fa} + i^*_{Fa} + 2k_e v_{ce} \tag{33}$$

Assuming that the filter currents track their references and substituting (33) into (32) with the fact that $i^*_{Fa,e} + i^*_{Fb,e} = -i^*_{Fc,e}$, we obtain

$$\frac{\mathrm{d}v_{ce}}{\mathrm{d}t} = -\frac{1}{C_1}\left(i_{Fc} - 2k_{ce} v_{ce}\right) \tag{34}$$

Taking Laplace transform of (34) yields

$$V_{ce}(s) = \frac{1}{C_1(s - 2k_{ce})} I_{Fc}(s) + \frac{1}{(s - 2k_{ce})} v_{ce}(0) \tag{35}$$

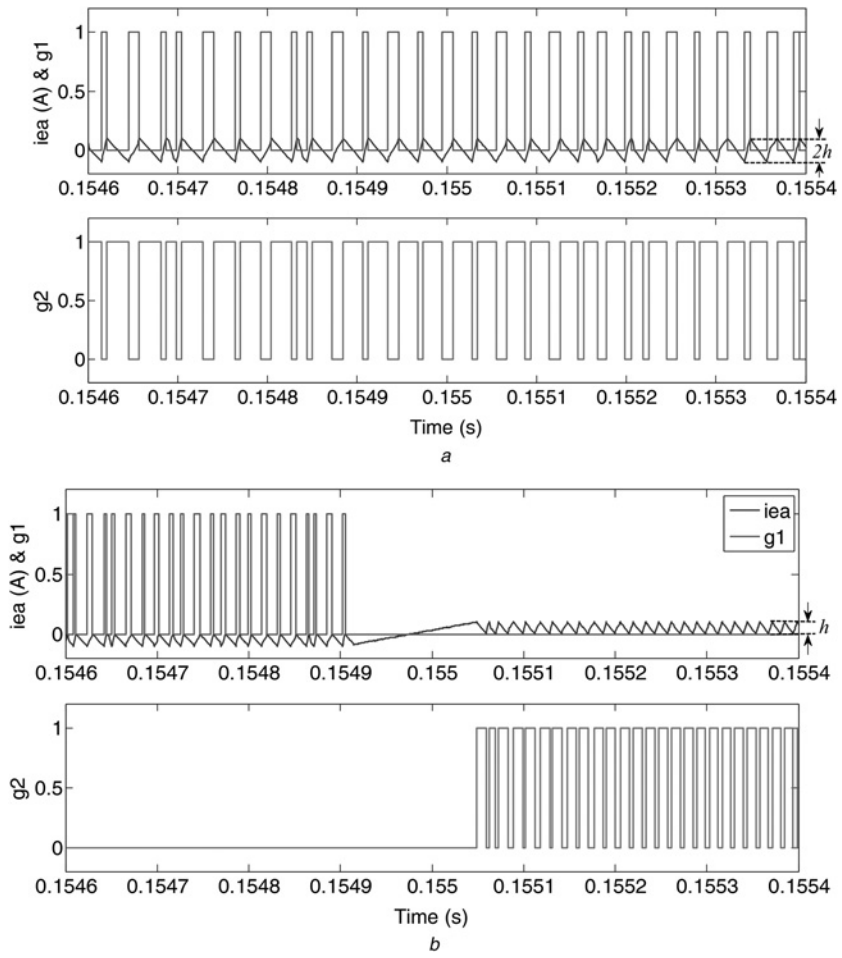

Fig. 5 *Current error of phase A and gate signals of S_a and $\bar{S}_a$ for*
a Two-level HCC
b Three-level HCC

The solution of (35) in time domain can easily be obtained as

$$v_{ce}(t) = \frac{1}{C_1} i_{Fc}(t) e^{2k_{ce}t} + v_{ce}(0) e^{2k_{ce}t} \tag{36}$$

Clearly, $v_{ce}(t)$ decays to zero for all t since $k_{ce} < 0$.

4 Computer simulation results

In this section, the effect of imbalance compensation loop on the capacitor voltages is first presented. Then, the simulation results of the three-level HCC and the two-level HCC are discussed. Moreover, the THDs of the three-phase source currents obtained by the proposed control strategy are compared with the results obtained from state-of-the-art using MATLAB/Simulink. The simulation studies have been carried out by using the parameters as shown in Table 1.

The non-linear load group is modelled such that it draws non-sinusoidal currents from the three-phase supply as shown in Fig. 3.

Fig. 4 shows the start-up and dynamic responses of capacitor voltages (v_{c1} and v_{c2}) and DC-link voltage (v_c) when load$_2$ is disconnected from PCC at $t = 0.5$ s. Initially, the system starts with both load$_1$ and load$_2$ which are connected in parallel. It is clear from Fig. 4*a* that the capacitor voltages are not equal to each other ($v_{c1} \neq v_{c2}$) when the imbalance compensation loop is not utilised. When the imbalance compensation loop is activated, the imbalance in the capacitor voltages is eliminated as shown in Fig. 4*b*. This result clearly shows that the imbalance compensation loop acts correctly to eliminate the imbalance in the capacitor voltages. Also, the oscillations seen on the total capacitor voltage (v_c) obtained without imbalance compensation loop are not visible on v_c when obtained with imbalance compensation loop.

Fig. 5 shows the current error of phase A (i_{ea}) and gate signals (g_1 and g_2) of S_a and $\bar{S}_a$ obtained by two- and three-level HCCs, respectively. It is clear from Fig. 5*a* that the current error remains between the defined upper and lower hysteresis bands by making a zigzag movement between $h = +0.1$ A and -0.1 A without having a zero level. Having a zigzag motion of i_{ea} between two levels forces the switching devices (S_a and $\bar{S}_a$) to be turned on and off continuously. Eventually, this would increase the switching frequency and losses.

In the case of three-level HCC as shown in Fig. 5*b*, the current error makes a zigzag motion between three levels. When the current error is negative, it changes between $h = -0.1$ A and 0. On the other hand, when the current error is positive, it changes between $h = +0.1$ A and 0. With such switching scheme, S_a is turned on and off when the current error is negative, while $\bar{S}_a$ is always off and vice versa. Comparing Figs. 5*a* and *b*, the number of pulses for three-level HCC is seen to be smaller than that of two-level HCC for the same time interval from $t = 0.1546$ to 0.1554 s. This means that the three-level HCC leads to smaller switching frequency than two-level HCC.

Fig. 6 shows the steady-state waveforms of three-phase source currents obtained by three- and two-level HCCs using four- and six-switch APF topologies. Figs. 6*a* and *b* show the source current waveforms obtained by the three- and two-level HCCs using four-switch topology, respectively. The THDs of phase A current are computed as 1.81 and 1.54%. Though the three-level HCC leads to a higher THD than that of three two-level HCC, it is still

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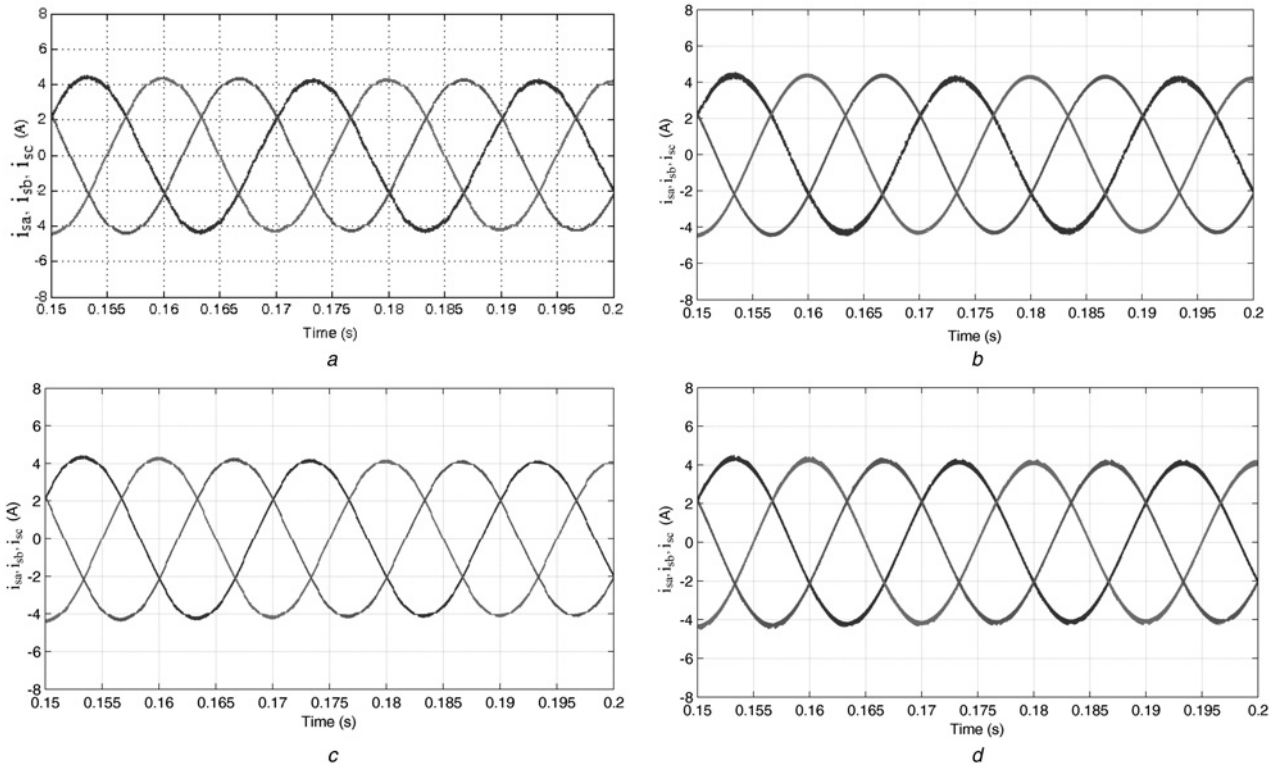

Fig. 6 *Three-phase source current waveforms obtained by*

a Three-level HCC-based three-phase four-switch APF
b Two-level HCC-based three-phase four-switch APF
c Three-level HCC-based three-phase six-switch APF
d Two-level HCC-based three-phase six-switch APF

below the IEEE-519 standard. The main contribution of three-level HCC is that it offers smaller switching frequency compared with the two-level HCC. Figs. 6*c* and *d* show the source current waveforms obtained by the three- and two-level HCCs using six-switch topology, respectively.

The THDs of three-phase source currents obtained by the proposed control strategy are compared with the THDs of source currents obtained by the four-switch two-level HCC and traditional six-switch APF topology under two- and three-level HCCs. The THDs of phase A current are computed as 1.81 and 1.54% which are equal to the THD values computed for the four-switch case. The THD values regarding the other phases obtained by three- and two-level HCCs under four- and six-switch APF topologies are reported in Table 2. As a consequence of using three-level HCC, the source current distortions are only affected by 0.27% in phase A, 0.06% in phase B and 0.07% in phase C which are still below the IEEE-519 standard.

5 Real-time control in software-in-the-loop results

The performance of the proposed control strategy under four-switch topology was investigated in a real-time environment. RT-LAB allows for the distributed simulation of complex power systems. Specifically, the proposed system is realised on a field programmable gate array architecture using the Xilinx system generator toolbox.

Fig. 7 shows the steady-state waveforms of load current, active filter current, source current and spectrums of load and source currents for phase A obtained by the proposed control strategy. Despite the highly distorted load current, the proposed control strategy works correctly by injecting the required active filter current to PCC so as to produce a sinusoidal source current as shown in Fig. 7*a*.

The spectrums of the load and source currents are depicted in Figs. 7*b* and *c*, respectively. It is clear from Fig. 7*b* that the load current contains odd harmonics (3rd, 5th, 7th and 9th) which are successfully eliminated by the proposed control strategy so that they do not appear in the source current as shown in Fig. 7*c*.

Fig. 8 depicts the steady-state waveforms of three-phase source currents and source voltage together with source current for phase A. It is obvious from Fig. 8*a* that the proposed control strategy with four-switch topology is able to control i_{sa} and i_{sb}. When the control of phases A and B currents are achieved, the control of phase C current is done automatically. Also, it can be easily noted from Fig. 8*b* that the unity power factor requirement is achieved successfully.

Table 2 Comparisons of four- and six-switch APFs under three- and two-level HCCs

Topology	Three-phase four-switch APF						Three-phase six-switch APF					
Current control methods	Three-level HCC, proposed method			Two-level HCC			Three-level HCC			Two-level HCC		
	THD of phase currents, %			THD of phase currents, %			THD of phase currents, %			THD of phase currents, %		
	A	B	C	A	B	C	A	B	C	A	B	C
load currents	26.33	25.88	25.92	26.33	25.88	25.92	26.33	25.88	25.92	26.33	25.88	25.92
source currents	1.81	1.51	2.03	1.54	1.45	1.96	1.83	1.67	1.75	1.73	1.51	1.60

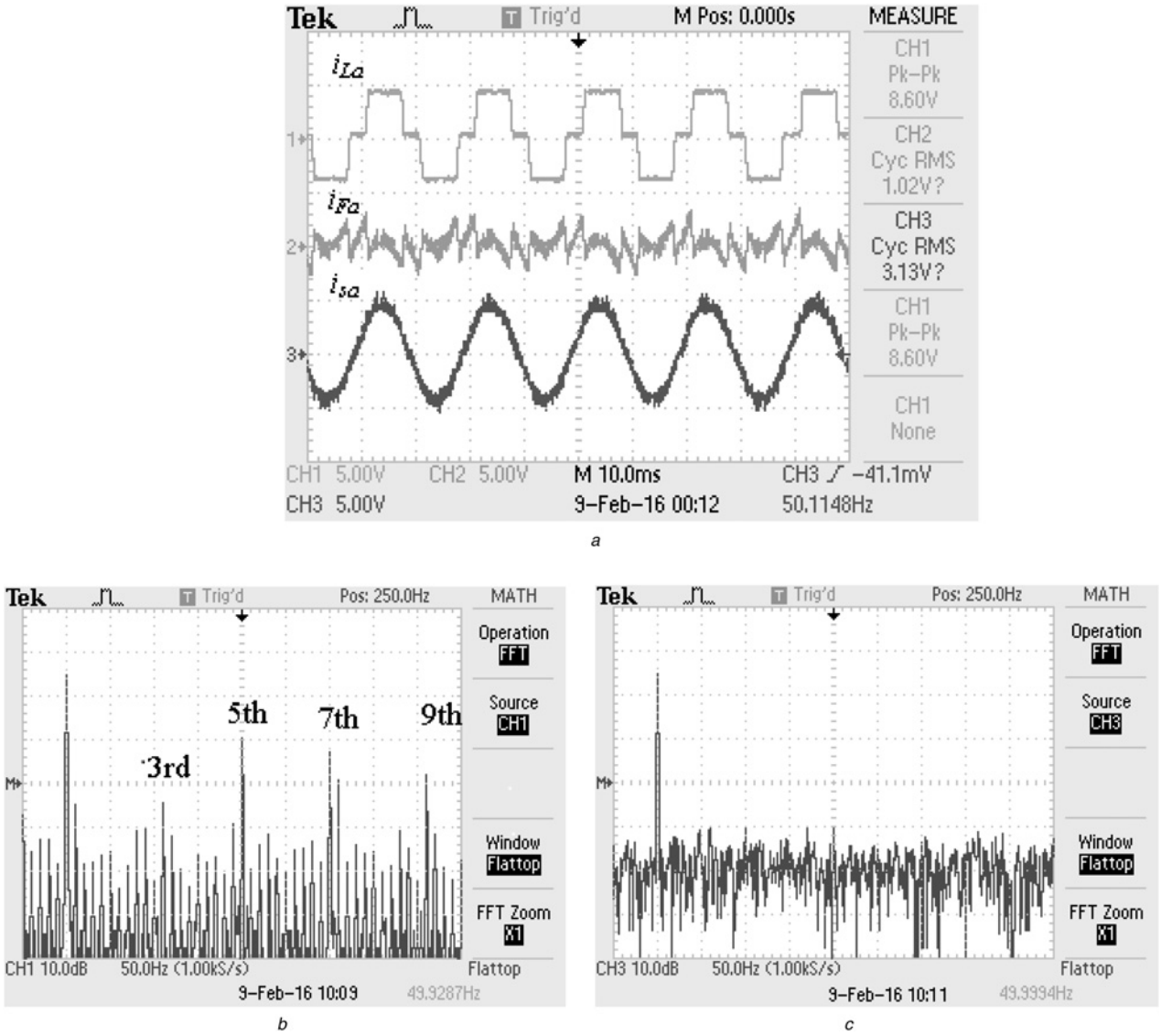

Fig. 7 *Steady-state waveforms of load current, active filter current, source current and spectrums of load and source currents for phase A*

a Steady-state waveforms (scale: 5 A/div)
b Load current spectrum
c Source current spectrum

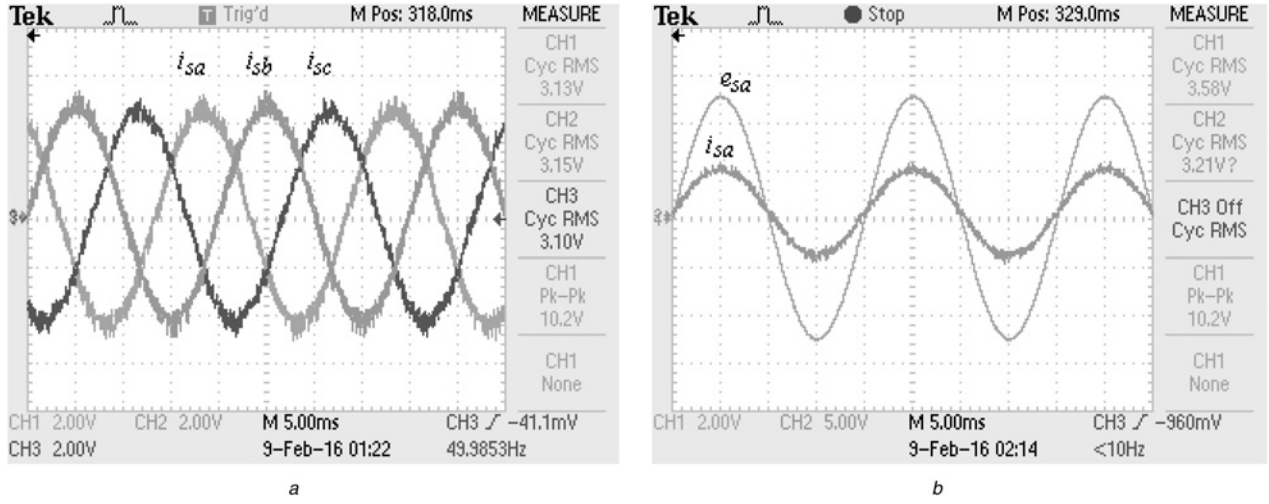

Fig. 8 *Steady-state waveforms of three-phase source currents and source voltage for phase A*

a Three-phase source currents
b Source voltage and current for phase A (scale: 2 A/div, 20 V/div)

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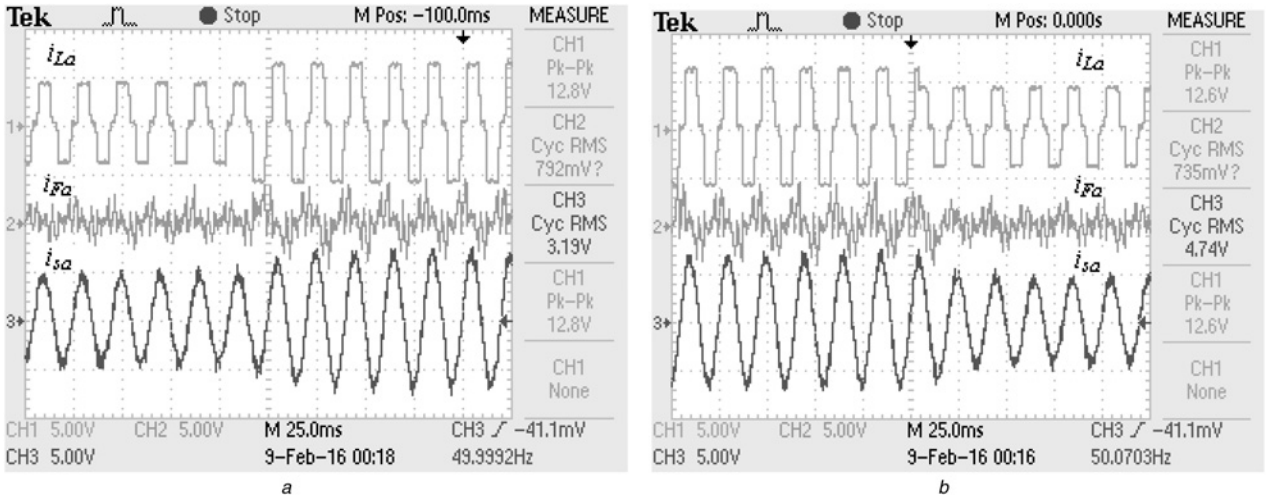

Fig. 9 *Dynamic response of currents for a step change in load*

a From $load_1$ to $load_1$ and $load_2$
b From $load_1$ and $load_2$ to $load_1$ (scale: 5 A/div)

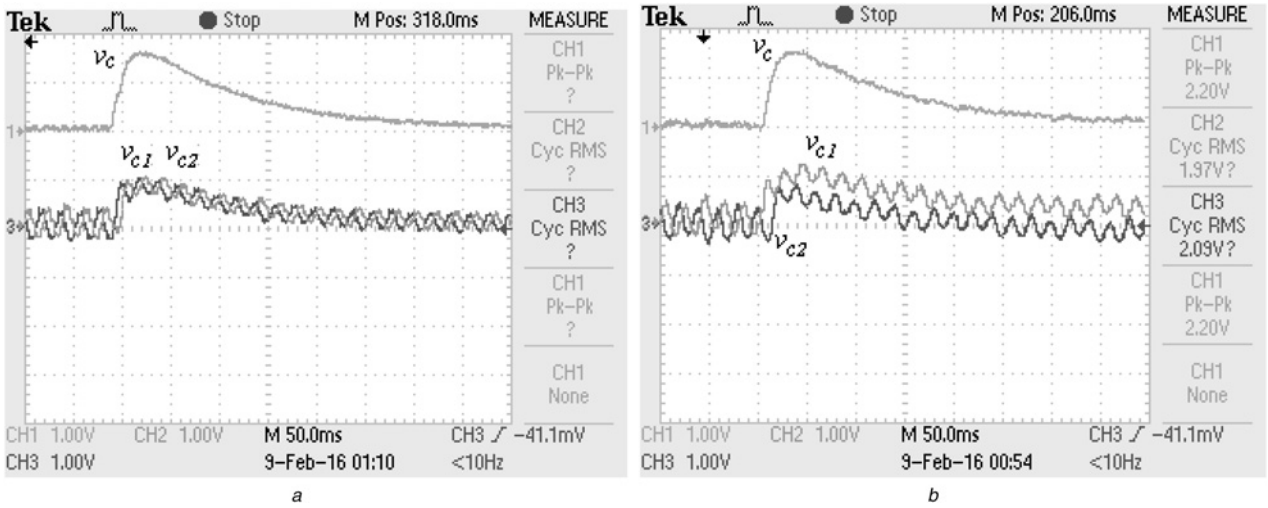

Fig. 10 *Dynamic responses of v_c, v_{c1} and v_{c2} when the $load_2$ is disconnected from PCC*

a With imbalance compensation loop
b Without imbalance compensation loop

Figs. 9*a* and *b* show the dynamic performance of the proposed control strategy under step changes in the load. Fig. 9*a* shows the response of i_{La}, i_{Fa} and i_{sa} when $load_2$ (40 Ω, 40 mH) is connected in parallel with $load_1$ (20 Ω, 80 mH) at PCC and Fig. 9*b* shows the response of i_{La}, i_{Fa} and i_{sa} when $load_2$ is disconnected from $load_1$. It can be seen that the dynamic response is reasonably fast in both cases.

Fig. 10 shows the dynamic responses of capacitor voltages obtained with and without the imbalance compensation loop when

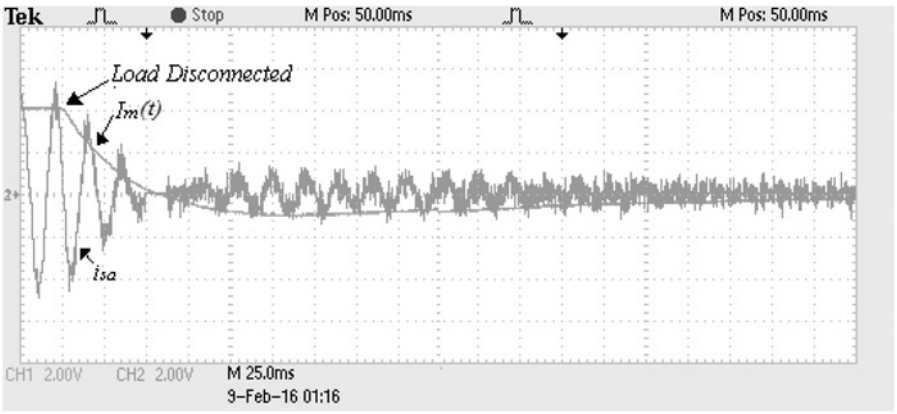

Fig. 11 *Dynamic responses of i_{sa} and $I_m(t)$ when the $load_1$ is disconnected from PCC*

$load_2$ (40 Ω, 40 mH) is disconnected from PCC. Initially, both $load_1$ and $load_2$ are connected in parallel at PCC. It is clear from Fig. 10*a* that both capacitor voltages are equal to each other which clearly show that the imbalance compensation loop acts correctly to eliminate the imbalance in the capacitor voltages. However, when the imbalance compensation loop is removed, there exists an imbalance in the capacitor voltages as shown in Fig. 10*b*. In both cases, the DC output voltage is stabilised successfully by the PI regulator existing in the voltage-control loop.

Fig. 11 shows the dynamic responses of source current of phase A and the time-varying reference amplitude [$I_m(t)$] produced by the PI regulator for a step change in load from (20 Ω, 80 mH) to no load ($load_1$ is disconnected from PCC). It is obvious from Fig. 11 that the actual amplitude of the source current tracks its reference amplitude before and after the $load_1$ is disconnected from PCC. It should be noted that, before the load is disconnected, $I_m(t)$ is non-zero which means that the load should draw a non-zero current from AC supply. After the load is disconnected from PCC, $I_m(t)$ converges to zero meaning that the load does not draw a current from the AC supply.

6 Conclusions

In this paper, a three-level HCC strategy employing an imbalance compensation loop is proposed for three-phase four-switch APFs. It is pointed out that regardless of the control strategy the four-switch topology offers a reduced cost than what would be achieved in the widely used six-switch topology. The four-switch APF is controlled by using three-level HCC strategy. An important consequence of using HCC strategy is that it enables access to the zero level of the input voltage of the active filter so that a switching device is only switched when the current error is negative, while it remains off when the current error is positive. The three-level HCC strategy not only maintains the advantages of conventional two-level HCC such as higher accuracy, fast dynamic response, robustness and simplicity in the implementation, but also offers additional advantages such as reduced switching frequency and switching losses. Furthermore, the additional feedback term, which involves the difference in the capacitor voltages multiplied by a suitable gain, is added into current control to eliminate the imbalance in the capacitor voltages. Simulation and experimental results are presented to demonstrate the steady-state and dynamic performance of the proposed control strategy.

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