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Optimizing the fabrication process for next generation nano-textured solar cells with high conversion efficiency using industrially viable solar cell processes

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Optimizing the fabrication process for next generation nano-textured solar cells with high conversion efficiency using industrially viable solar cell processes

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For Research Carried Out Under the Guidance of

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Candidate

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Abstract

The need for photovoltaic (PV) cells with high conversion efficiency and low surface reflectance has been on the rise. With this in mind, the fabrication process of PV cells has been investigated with interest in the surface etching phase in order to reduce surface reflectance using nanotexturing. The purpose of this thesis is to investigate how to improve the etching phase by optimising the key parameters for an atmospheric dry etch (ADE) with different processes to determine which can aid in reducing surface reflectance.

To obtain a process which provides a low surface reflectance, parameters in the etching phase are changed, including multicrystalline versus monocrystalline , the etch time and the use of different cleaning techniques. Once the Si wafers have been put through the etching process, they are tested using a spectrometer to determine surface reflectance. A scanning electron microscope (SEM) and an atomic force microscope (AFM) were then used in order to observe how the etching process has affected the surface morphology.

Different parameters have been shown to have a varying effect on the surface reflectance of the etched Si surface, in particular cleaning processes before etching and etch time. Etch time has shown to have the greatest effect on surface reflectance. It can be seen that reflectance will vary with etch time as a result of the chemical reaction between the Si found on the surface of the Si wafer and the etching gas.

Certain conditions influence the Si etch rate and surface reflectance better than others. Further investigation into the use of multicrystalline silicon (mc-Si) using monocrystalline Si samples as a reference to assist in determining optimum etching

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phase. Etched mc-si samples can be processed using the same parameters and cleaning processes as the monocrystalline Si, resulting in identifiable crystal orientations. Application of the same test conditions in order to determine the surface reflectance and morphology will provide a further insight to what degree the etching phase needs to be improved upon in order to obtain low surface reflectance.

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1 Introduction

1.1 Overview of thesis

In this thesis, the etching phase of the solar cell fabrication process will be investigated with particular interest to the following research question:

How can surface reflectance be reduced during the surface texturing phase while applying an etching process that can be used in industry?

In order to answer this question adequately, the question is broken down into research objectives. These objectives are:

1. How does the etching parameters affect the surface characteristics?

2. How do the resulting structures impact the light trapping abilities of the solar cell?

3. How can the etching process be optimized in order to achieve low surface reflectance?

Chapter 1 provides an overview of the issue being faced, background and operation of solar cells. Chapter 2 reviews the state of the art in the surface texturing of silicon based solar cells. Chapter 3 investigates the light trapping abilities of textured solar cells, with particular interest to nanotextures. Chapter 4 discusses how the ADE process works and the experiential techniques which will be used to investigate samples which are processed. Chapter 5 discusses the results obtained for processed samples, including monocrystalline silicon (mono-Si) and multicrystalline silicon (mc-Si), surface morphology and surface reflectance. Chapter 6 draws conclusions from the work carried out and possible further development.

1.2 Project motivation

The use of depleting fossil fuel resources and their environmental impact on the planet has given rise to the need for widespread implementation of renewable energy resources that are not harmful to the environment. Fossil fuel reserves are finite and based on the current rate of consumption, these resources will be depleted in a short timeframe. Projections based on proven reserves suggest that there are 150 years worth of coal reserves [23] and 50 years of oil reserves [24] remaining.The reserves of natural gas in America are projected to last approximately 92 years [25]. Moreover, it is now widely recognised that the burning of fossil fuels is responsible for increasing average global temperatures. This has lead to weather instabilities and rising sea levels, which threaten populations across the globe. This has prompted 197 governments to sign up to the Paris Climate Agreement, which commits to increase energy efficiency, reduce CO_2 emissions and increase the renewables contribution to the global energy market in order to lessen the global temperature rise to 2 °C by the end of this century. Figure 1.1 outlines the projected gigatonnes of CO_2 emissions based on reserves of fossil fuels against the carbon budgets which were outlined by the Paris Climate Agreement.
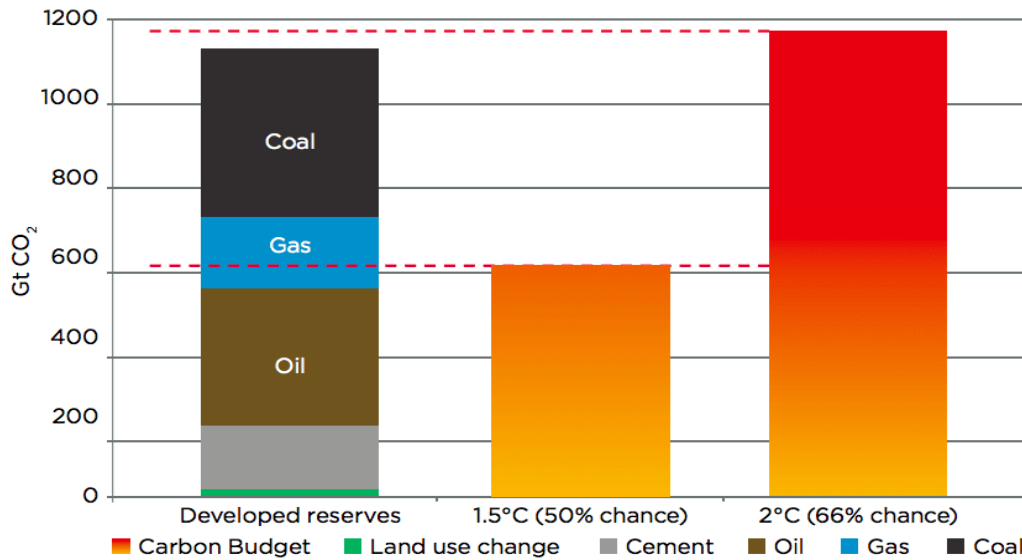
Figure 1.1: Greenhouse gas emissions of fossil fuels expressed in gigatons of CO_2 [1]

The first bar represents developed reserves. The second bar depicts the emissions

needed in order to achieve a 1.5°C rise in global temperature whereas the third bar illustrates a 2°C increase based on increased emissions.

In light of these factors, there has been a significant uptake in several renewable energy resources over the past three decades, including wind, nuclear, hydro, and solar, with each of these having a number of advantages and disadvantages. In the case of wind, the advantages include lower cost in comparison to other resources, the lifetime of wind turbines is 20-25 years and wind energy does not produce global warming potential (GWP) emissions during operation [26]. Disadvantages include that wind energy can be intermittent, due to its dependence on weather conditions, and that wind turbines can be a source of noise due to the blades and can be hazardous to wildlife [26]. Nuclear has a number of advantages including producing ample and reliable energy that is low cost, it can be used as a base load for energy, has low pollution and high energy density [27]. Disadvantages of nuclear include the difficulties related with dealing with nuclear waste and decommissioning obsolete power stations, that it relies on the use of a finite uranium resource, initial construction costs are extremely large and there is always the risk of an accident happening such as Chernobyl and Fukushima [27]. The advantages of hydro power include it being able to be generated at any time and the ability to supply power to the grid quickly which is useful for power outages or disruptions [28]. Disadvantages include that hydro is limited to where it can be implemented, can be expensive and can be affected by drought [29]. Lastly, the advantages of solar includes that solar PV installations are low maintenance, solar is abundant, there is no noise pollution, the technology for producing solar is constantly improving, solar panels typically have a lifetime of 20 years and can be installed on different scales ranging from individual residential units up to utility scale solar farms [30]. The disadvantages of solar PV include the fact that energy generation only occurs during the day when energy consumption is typically lower, so that an energy storage system is often needed and CO_2 emissions can be high as a result of the manufacturing process [30]. The cost of solar PV has traditionally been high, which has limited its uptake. However that cost has decreased substantially during the past

two decades to the point where currently the price of solar PV per kWh for utility, residential and commercial scale is USD $ 0.06, $ 0.16 and $ 0.11, respectively [31]. The lifetime cumulative CO_2 emissions from production to decommission of renewable energy resources is also a key aspect to consider. Fig. 1.2 shows the CO_2 emissions of several energy resources, including fossil fuels and renewables, showing that the emissions produced by solar PV are considerably lower than traditional fossil fuel energy sources and compare quite favourably to other renewable sources.
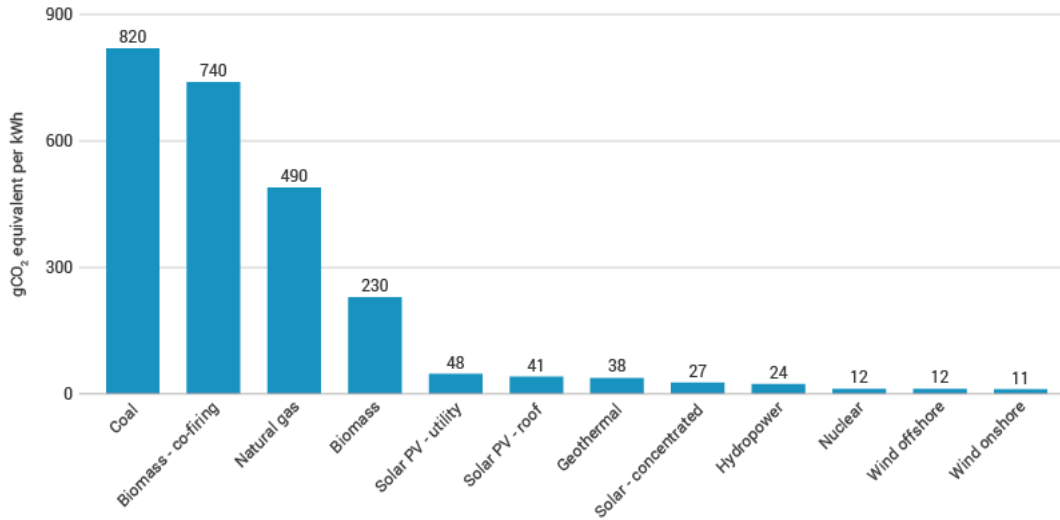
Figure 1.2: Comparison of CO_2 emissions per kWh for different energy resources [2]

Given the low associated emissions, the abundance of solar energy and its low environmental impact, it is clear that solar PV can provide a significant contribution to the total energy production. For example, the production of energy using renewable methods has been risen significantly in the European Union (EU) between 1990 and 2016, as shown in figure 1.3, which is in line with its commitment to increase the renewables production of its energy market to 20% by 2020. Renewable energy production has risen in the EU in this period, from 309.2 TWh being produced in 1990 to 951.4 TWh (81,771 ToE) produced in 2016 [3]. The breakdown of the production of renewable energy resources as of 2017 are as follows: biofuels made up the highest portion with 42% of production, wind power provided 13.8%, hydro power with 11.4%, biogas yielded 7.4%, liquid biofuels contributed 6.7%, solar generated 6.4%, ambient

heat, which is obtained by heat pumps, supplied 5.0% and geothermal energy produced 3.0% [32]. Wave, tide and ocean did contribute to the renewable energy produced, however there are low levels of these as they are mainly based in France and the UK [32]. It is worth noting that solar is the fastest growing renewable energy resource, with a 44% increase year on year outside of China [33]. The advantages and disadvantages of wind, hydro and solar have been previously discussed. In relation to biofuels, they do not rely on fossil fuels and they limit the amount of greenhouse gases. However, they can aid in deforestation, reduce biodiversity and lead to increases in price of agricultural products [34].
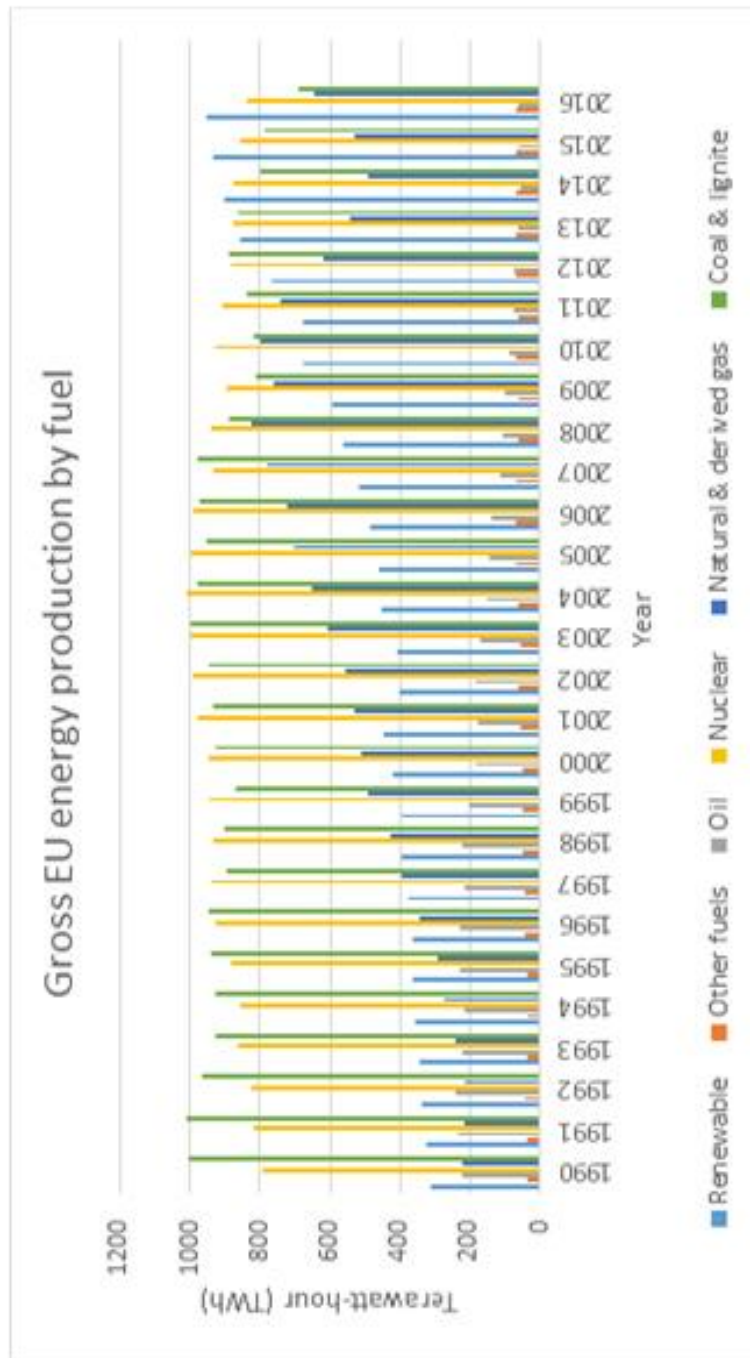
Figure 1.3: Energy production of the EU broken down by sector from 1990 to 2016 [3]

As mentioned earlier, solar energy has several advantages over other renewable energy techniques; it is not limited to where it can be applied like hydro as solar PV panels can be installed at different scales such as residential or in large numbers as part of a solar farm, can be readily installed where the population is located unlike wind and provides

no emissions during the energy production process unlike biomass. Most significantly, solar energy is hugely abundant, with energy from the sun, around 1.73×10^{17}Wh, striking Earth's surface per hour [9].
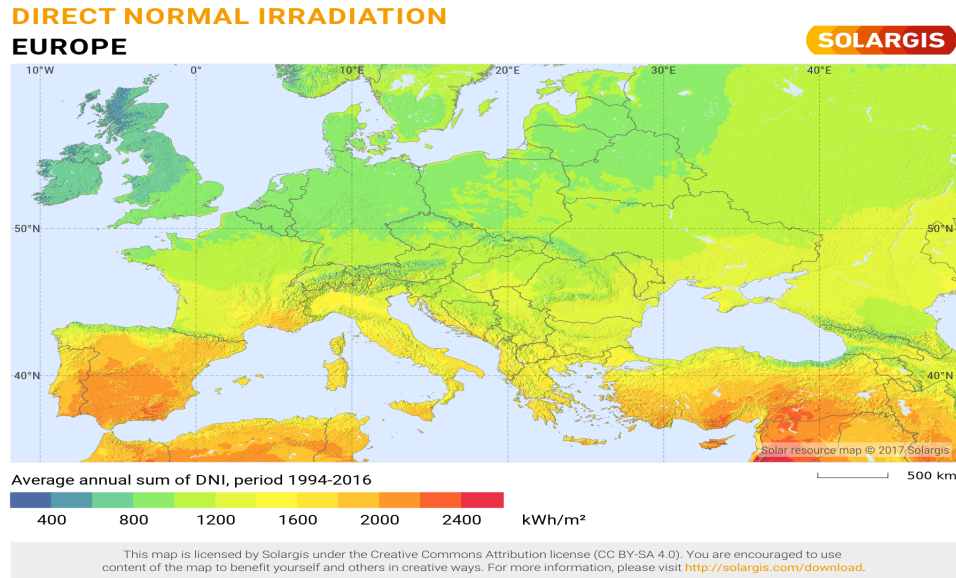
Figure 1.4: Annual average direct normal irradiation for Europe from 1994 to 2016 [4]

Putting this amount of energy into perspective, it is roughly the same amount of energy which is consumed by the global population annually. As Europe has been investigated in regards to solar irradiation and energy production, the energy usage will also be looked at. In Fig. 1.5, the energy usage of several EU states over a ten-year period are shown.
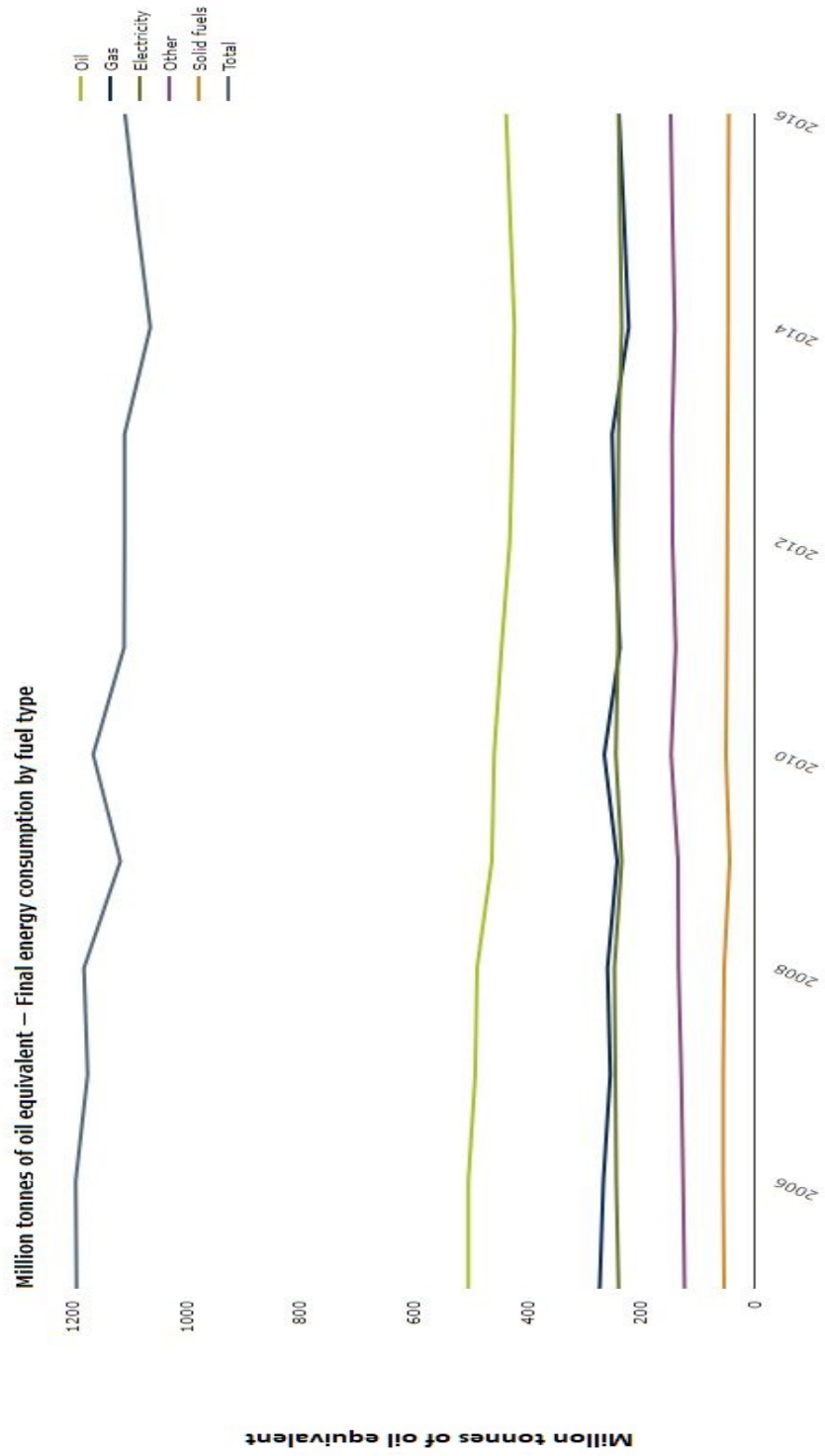
Figure 1.5: Energy consumption of several EU states from 2005 to 2016 [5]

1 Introduction

As of 2015, over 21,400 GWh was used by the EU states alone [35]. In 2018, 161,400 TWh was consumed by the world's population which was an increase on previous years [35], with Asia making up 42% of the energy usage whereas Europe used 13%.

The energy which the earth receives continuously is 1.73×10^{14}kWh, which corresponds to an available power of 22000kW per person. This compares to an average power consumption of 2.3 kW per person, demonstrating that the amount of available solar energy far outstrips human energy needs. To put this another way, in a 24 hour period, the sun hits the earth with around 4.2×10^{15}kWh worth of energy. Global consumption by humans annually is approximately 600 quadrillion BTU or 1.7×10^{14}kWh [36].This equates to an energy usage of approximately 4.8×10^{11}kWh in a day. Therefore the sun produces around 9000 times our daily energy requirements on a daily basis. In regards to land area covered by solar cells required in order to fulfil the daily energy needs, the assumption of a daily solar irradiance of 5kWh/m^2 at the equator and a cell efficiency of 20% can be used to determine that the area needed is 480,000km^2 which is approximately 0.3% of the earth's landmass. The amount of diffuse sunlight has an effect on how much land is needed, as it is the portion of sunlight which has been scattered or refracted in the atmosphere before reaching the surface of the earth. The amount of diffuse light is dependent on geographical location and weather. In regards to weather, cloudless conditions result in diffuse light making up 10% of light whereas cloudy conditions produce 50% to 100% of light as diffuse light. In regards to geographical location, diffuse light can make up almost 60% of light in northern Europe [37]. As a consequence, light management at the front surface of the solar cell in order to harvest diffuse light becomes crucial for solar installations in northerly latitudes.

Despite the advantages, solar PV is one of the smallest contributors to the global energy market. This is a result of efficiency, panel costs, diurnal intermittency and dependence on local weather and latitude. Over the past two decades, however, solar PV technology has witnessed a dramatic growth with global cumulative installed PV capacity having risen from 5 GW in 2005 to almost 627 GW in 2019 [38, 33]. In 2019 nearly 115 GW of solar PV was installed [33], making solar PV one of the fastest growing renewable

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energy sources.

Investment in solar power market on a global scale has increased tenfold from €9.7 billion in 2004 to €98 billion in 2016 [39], while global employment in the solar PV sector reached 3.1 million jobs [40]. Global installation of rooftop solar PV alone was valued at €25.7 billion in 2016 and is forecast to reach €55.8 billion by 2023 [41]. The global PV market is currently dominated by Si-wafer based PV technology, which accounts for over 90% of the global production [42]. Manufacturers are continually trying to reduce manufacturing costs and increase cell efficiencies in order to reduce €/kWh costs. This has lead to thinner wafers requiring new approaches to increase light trapping to minimise transmission and reflection losses.

1.3 History of solar cells

The operation of solar cells are based on the photovoltaic (PV) effect, which was discovered by Edmond Becquerel in 1839 [43]. Becquerel noted that by placing two gold or platinum plates into a solution and illuminating them, a voltage could be created as a result. However, it was not until the 20th century when a better understanding of solid state theory and quantum mechanics occurred, that the PV effect could be understood and applied [37].

In the 1930's, the first noted fabrication of a solar cell was reported with the use of selenium (Se) [37]. However, Se was not a very effective material as only approximately 1% of the incident light was converted into electricity. In the 1950's, Bell laboratories began to produce solar cells as a power source for remote communications systems. Se was initially used, however, it was soon dropped due to it's low efficiency. In place of Se, silicon (Si) was used and achieved 4% conversion efficiency solar cells. By 1954, Bell laboratories had reached 6% conversion efficiency for their fabricated Si solar cells [37]. As a result of the reliability and lightweight nature of solar cells, they were applied to NASA spacecraft and satellites as a power source. As a result, solar cells have become the main power source for space applications [37]. Companies including Texas

Instruments, Heliotek and Hoffman (now Applied Solar Energy Corporation) produced solar cells for space which were dependable and efficient though expensive. Sales were 80kW annually in 1970 with an average cost of \$150 per watt.

The next influence on solar cells was the energy crisis in the 1970's, with the price of gasoline increasing dramatically in the United States [37]. It was perceived that energy was in short supply and would run out. Alternative energy resources were investigated as a result, including solar power.

Efficiency of solar cells has also improved over the years as a result of further research, with the earliest solar cells having an efficiency of 1% compared to Si solar cells with an efficiency 22.3% for mc-Si and 26.7% for c-Si in recent years [44] compared to a theoretical efficiency limit of 29.6% for a single-junction crystalline silicon (c-Si) cell. This is a result of the implementation of various strategies to reduce losses including techniques which reduce surface reflectance [45], such as antireflective coatings (ARC) and surface texturing. The cell configuration also plays an important role in determining the energy conversion efficiency achieved.

Back surface field (BSF) is one technique used to achieve low effective recombination velocities at the rear of the cell. Using this technique boosts the sensitivity to long wavelengths and increases the collection probability for generated carriers at the back contact [43]. The use of the aluminium back surface field (Al-BSF) technique has been used for decades and has made up 90% of the production in this time [46]. This design offers moderate efficiency and makes use of experience regarding materials, procedures and manufacturing tools.

Passivated emitter and rear contact (PERC) processes for solar cells require few changes from the standard AL-BSF process. Despite being similar processes, the motivation for using PERC is improved efficiency, as well as reduced rear-surface recombination [46].

Passivated emitter rear totally diffused (PERT), in particular n-type PERT, provide stabilised and high conversion efficiencies [6]. Efficiencies for PERT solar cells have reached as high as 22.5% [47]. Figure 1.6 displays a schematic design of a n-type

PERT solar cell.
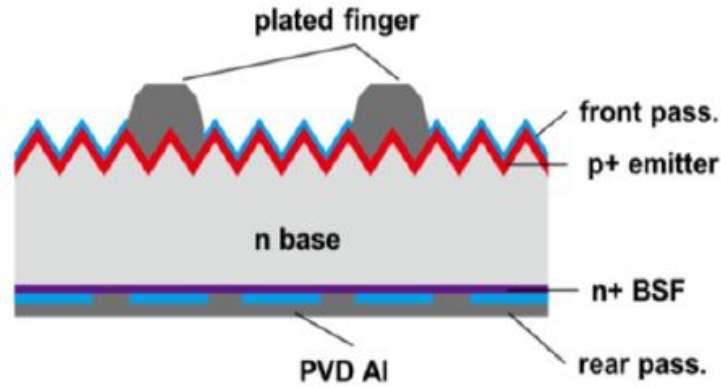
Figure 1.6: N-type PERT solar cell schematic designed by Wenhao Cai et al in [6]

Back surface reflectors (BSR), which includes a back contact that is designed to be reflective, provides a boost to the performance of thin cells and assists in maintaining low operating temperatures [43]. A wide variety of different materials and device configurations have been employed in order to fabricate solar cells with varying efficiencies. A full discussion of these various materials and devices is beyond the scope of this thesis. However, the efficiencies achieved by these methods are summarised in figure 1.7. Fig. 1.7 shows that over the past three decades, the efficiencies of solar PV has dramatically risen without depending on approach or materials used. It is also worth noting that the theoretical efficiency is being approached for non-concentrator Si-based solar cells. The material which is most commonly used for solar cells is silicon (Si) as it is readily available and is widely used in semiconductor fabrication. The focus of this thesis is on the nanotexturing of silicon in crystalline-silicon (c-Si), including both monocrystalline silicon (mono-Si) or multicrystalline silicon (mc-Si). Both materials are widely used in the commercial manufacture of silicon solar cells. Mono-Si tends to produce higher efficiency solar cells, since mc-Si has higher surface recombination at grain boundaries, but it is more costly to manufacture, making mono-Si cells more expensive. As a result, mc-Si cells have a larger market share, representing over 60% of silicon cells manufactured globally.
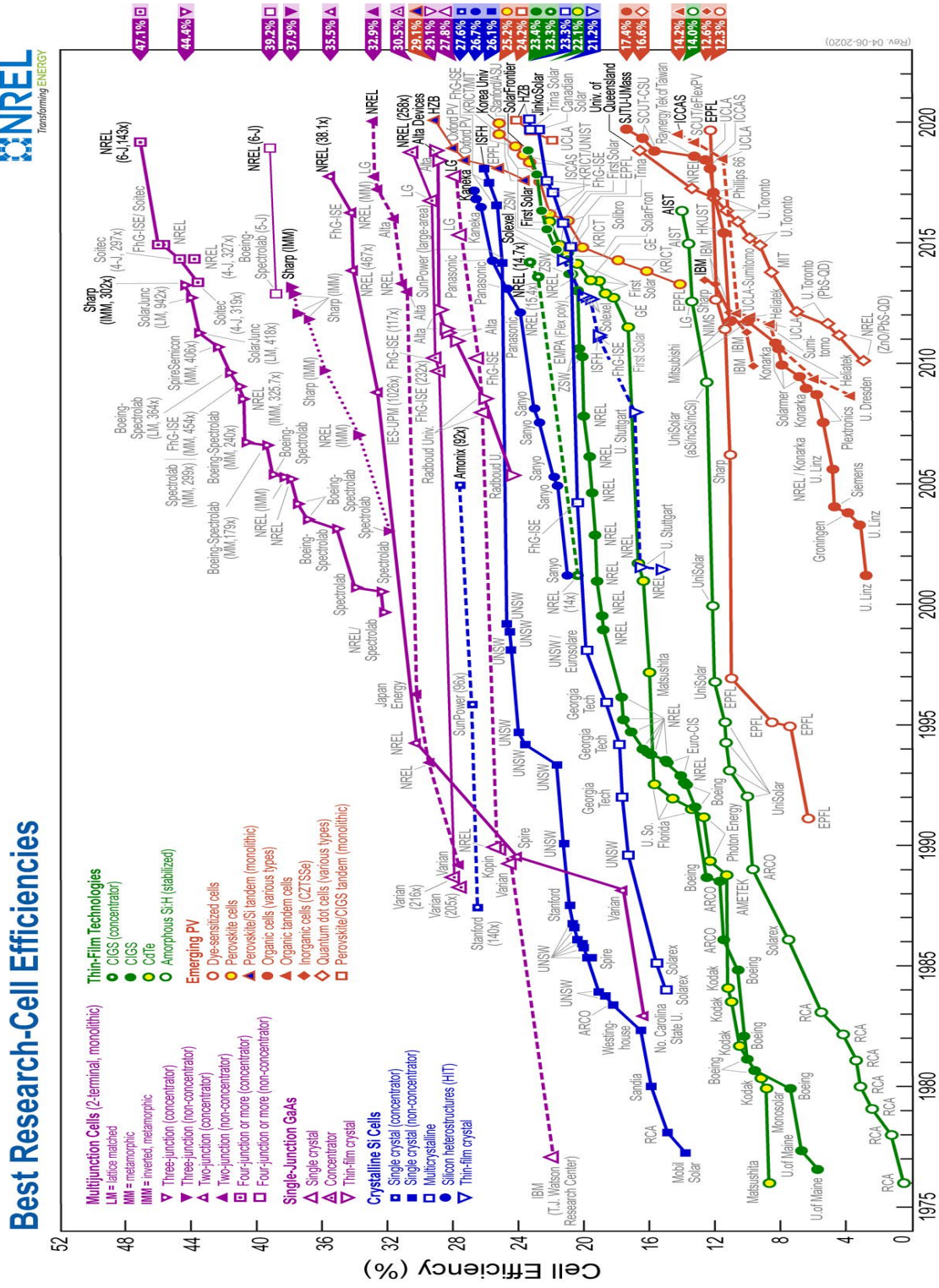
Figure 1.7: Best cell efficiencies found reported in the research literature [7]

1.4 Operation of solar cells

The purpose of solar cells is to produce electricity from light. This occurs when incident light interacts with the electrons in a semiconductor material, providing enough energy for the electron to move from the valence band to the conduction band. Each electron will remain in the conduction band once it has enough energy to do so until it recombines with a hole in the valence band through either Auger, radiative or Shockley-Read-Hall recombination. The photon energy required to promote an electron from the valence band to the conduction band of the semiconductor material is given by Planck's equation [48]:

$$E(eV) = \frac{1.24}{\lambda(\mu m)} \tag{1.1}$$

The photon energy must be equal or greater than the bandgap of the absorber material for an electron to be promoted. In order for an electron to move from the valence band to the conduction band in silicon, at least 1.12eV is needed. A maximum value for λ can be calculated in order for photogenerated charge carriers to be produced.

$$\lambda \leq 1.107 \mu m$$

The highest wavelength which will give the required energy is 1.107μm. Once enough energy is passed from the photon to the electron, the electron will move to the conduction band from the valence band. The electron will remain in the conduction band while its energy level is equal to or above 1.12eV, otherwise the electron will return the valence band. The excess energy of the electron in the conduction band is released in the form of heat via electron-photon interactions in a process known as thermalisation. Light interaction with the solar cell in order to form electron-hole pairs in the semiconductor material can be seen in figure 1.8.
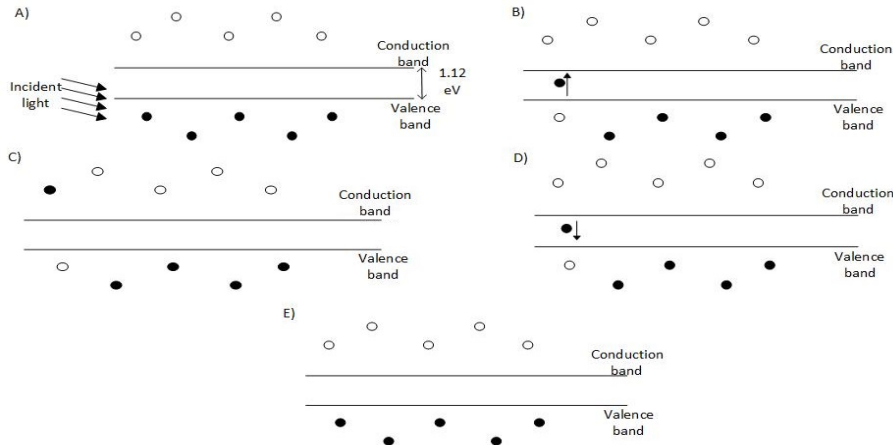
Figure 1.8: A)Photons interact with electrons B) An electron moves across the bandgap C) An electron remains in the conduction band D) An electron moves across the bandgap E) The electron remains in the valence band

Figure 1.9 shows a schematic of the basic structure of a p-type mono-Si solar cell. The cell consists of front contacts, an antireflective coating (ARC) layer, n-type emitter layer, p-type absorber layer and a rear contact.
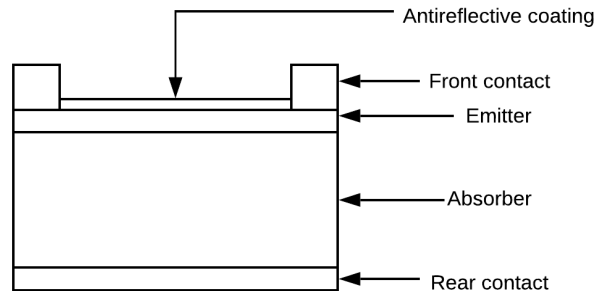
Figure 1.9: Basic structure of a p-type silicon solar cell [8]. The basic components of the cell are the front-side contacts, antireflective coating, n-type emitter layer, p-type absorber layer and rear contact. Under illumination photogenerated electron-hole pairs are separated at the p-n junction and travel to the front and rear contacts to create an open-circuit voltage, V_{oc}

When light interacts with the surface of the cell, it enters through the ARC, which prevents reflection from the front side of the solar cell. Light then enters the emitter and absorber layers, which results in the creation of electron-hole pairs. The photogenerated carriers are separated by the built-in field of the p-n junction at the emitter-absorber

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interface, with electrons travelling to the front contacts and holes travelling to the rear contacts. It is worth noting that band diagrams further describe the process as it deals with the p-n junction, which is shown in Fig. 1.10. Figures 1.10 and 1.11 demonstrate a series of diagrams that depict the principle of the operation of a single-junction solar cell. At the p-n junction, the carrier concentration gradient across the interface between the two layers results in the diffusion of majority carriers from one side of the interface to the other. Holes diffuse from the p-type region into the n-type region, leaving behind a region of negatively-ionised accepter atoms. Conversely, atoms diffuse from the n-type region into the p-type region, leaving behind a region of positively-ionised donor atoms. As a result, an internal electric field is established across the depletion region, causing electrons to drift from the p-type region to the n-type region and vice versa for holes. Under zero external bias, thermal equilibrium and in the absence of illumination, the diffusion and drift currents compensate one another. In the absence of illumination, the solar cells behaves as a diode.
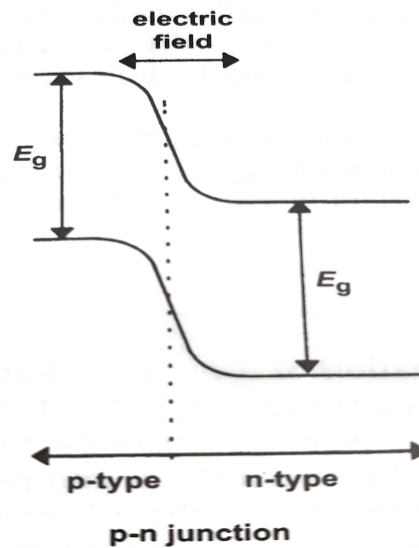
Figure 1.10: Band diagram of the p-n junction of a semiconductor material such as silicon [9]
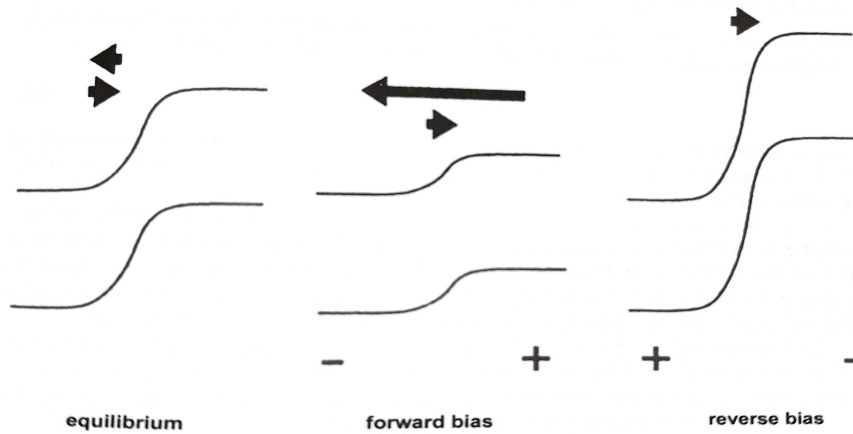
Figure 1.11: Equilibrium, forward bias, and reverse bias band diagrams of a semiconductor material. Arrows indicate the direction and magnitude of the diffusion and drift currents under different bias conditions. [9]

Under forward bias, a reduction in the electric field across the depletion region and the associated potential barrier results in an increase in the diffusion current which is not fully compensated by the drift current in the opposite direction. Reverse bias results in an increase in the electric field across the depletion region and the corresponding potential barrier, which suppresses the diffusion current while still allowing a small drift current to flow. In the case of solar cells, illumination results in the generation of electron-hole pairs on either side of the interface as well as inside the depletion region. electrons that are photogenerated in a region of the absorber that is sufficiently close to the depletion region can diffuse to it and are drifted across it by the built-in electric field. In this way, electrons are separated to the front contact of the cell, while holes are separated to the back contacts. The separation of charge results in the formation of an open circuit voltage across the device. When an external load is placed across the front and back contacts, electrons can flow through the external circuit and recombine with holes at the interface between the absorber and rear contacts of the cell.

1.5 Solar cell fabrication process
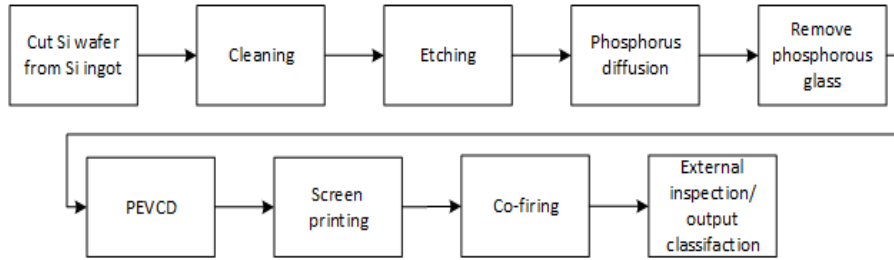
Figure 1.12: The solar cell process for p-type Si based solar cells. The main process steps are cutting the Si wafer from the ingot, cleaning the wafer, etching the surface of the wafer, a phosphorus diffusion, removing the phosphorus glass, followed by plasma-enhanced chemical vapour deposition (PECVD), screen printing, co-firing and lastly classification of the cell

Figure 1.12 shows the the steps carried out in the fabrication process of Si based solar cells, which are typically manufactured from c-Si or mc-Si. A number of steps are carried out in the process of fabricating solar cells. The process begins in a similar manner as any semiconductor device, with a silicon (Si) wafer being cut from a Si ingot and polished. Once retrieved, the Si wafer is cleaned using a standard RCA clean[1] in order to remove any impurities and native oxide layers from the surface. The etching phase can then be carried out in order to aid in light trapping abilities. Phosphorus diffusion is carried out in order to form a p-n junction in the case of a p-type Si wafer being used. After the diffusion process, a layer of phosphorus glass will be present on the surface of the wafer. This phosphorus glass layer is removed by using HF based solutions [49]. Other methods have been shown to work such as using SF_6, however these can result in a damage layer [49]. Plasma-enhanced chemical vapour deposition (PECVD) is carried out in order to apply an anti reflection coating [50] or PECVD hydrogenated silicon nitride (SiN_x:H) layers having good surface and bulk passivation properties [51]. Screen printing of back contacts is carried out by applying an aluminium paste layer to the back of the cell to create contacts to the Si. Co-firing is applied in order to form a bond between Si and the aluminium paste, along with

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[1]5 parts DI water, 1 part NH_4OH, 1 part H_2O_2

creating the back contacts. External inspection/output classification is carried out by determining the characteristics of the completed solar cell such as open circuit voltage (V_{oc}), short circuit current (I_{sc}), maximum power point (P_{max}), maximum power point voltage (V_{mpp}) and maximum power point current (I_{mpp}). These are tested under standard test conditions (STC), which consists of air mass 1.5 (AM1.5) spectrum, an irradiance of 1000W/m^2 and 25 degrees Celsius cell temperature [52]. Normal operating cell temperature (NOCT) conditions are also investigated, which considers real world conditions and is more realistic than STC. The conditions NOCT uses includes irradiance of 800W/m^2, with an ambient temperature of 20 degrees Celsius [9]. V_{oc} and I_{sc} are tested when there is no load connected [53]. Several of these characteristics impact the I-V curve of the solar cell under illumination, which is seen in Fig. 1.13 (b).
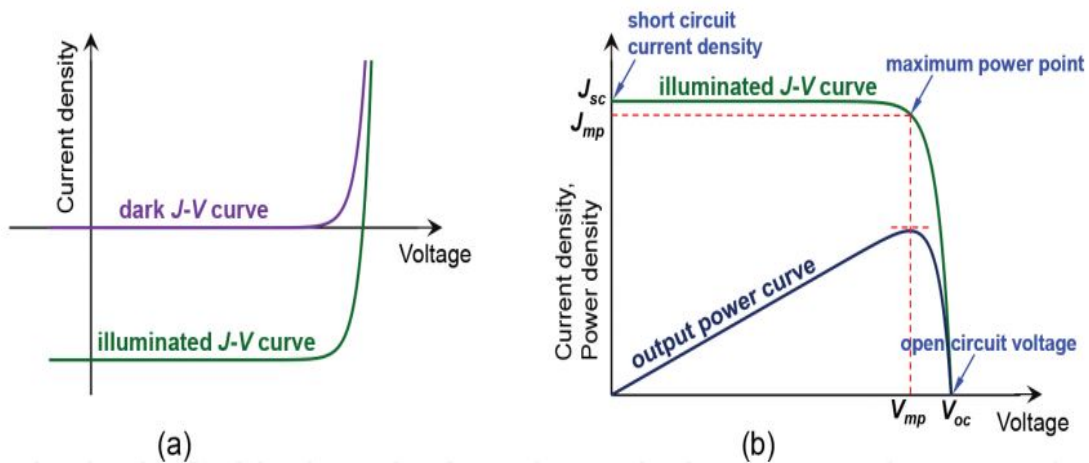
Figure 1.13: (a) Typical I-V curve of a solar cell displaying illumination and dark current characteristics (b) I-V curve under illumination, with characteristics including short circuit current, open circuit current and maximum power point [10]

In Fig. 1.13 (a), a typical I-V curve for a solar cell under illumination and dark current conditions is displayed. Dark current conditions are taken when no light is present for the solar cell, therefore creating little to no electron-hole pairs. The I-V curve for a solar

cell under illumination is obtained by light interacting with the cell and resulting in the process of electron-hole pair formation.

1.6 Strategies for improving Si based solar cells

Several strategies have been been investigated in order to improve the absorption and efficiency of Si wafer-based solar cells. Some of these would include light trapping techniques such as surface texturization. Losses in Si based solar cells are a result of various characteristics, including front surface shading, recombination, reflection, transmission and resistive and shunt losses.

Spectral mismatch - Thermalisation and non-absorption of photons

Spectral mismatch refers to the situation where the bandgap of the absorber material in the solar cell is such that it does not efficiently capture all photons of incoming light into electrical current. For example, long wavelength photons in the solar spectrum have insufficient energy to overcome the bandgap and photons with a short wavelength lose excess energy through thermalisation [54]. Losses as a result of spectral mismatch and thermalisation can be reduced though the implementation of multi-junction solar cells which use different absorber layers with different bandgaps to increase the usable fraction of the incident solar spectrum. Multi-junction configurations are more complex than single junction cells with larger associated manufacturing costs.

Parasitic absorption by non-active layers

Parasitic absorption occurs when a material absorbs the light which it interacts with and does not generate photocurrent [55]. For example, front and back surface contacts can also absorb photons without contributing to the photogenerated current.

Shading by front surface fingers

Shading losses in solar cells are a result of the metal fingers on the surface of the cell, which blocks light from entering. Shading losses can also be affected by the area covered by the metal, which is determined by the width and the spacing of the metal fingers. One limitation which has to be considered with the attempts to resolve this issue is the

minimum line width with metalization technology. One method which could be used is a narrow width and close finger spacing which reduces the emitter resistance losses [56].

Surface reflection and transmission

Solar cell surface reflection occurs when the light which interacts with the surface of the wafer is reflected. The amount of light which is reflected will depend on the material which is used. In the case of Si, the theoretical polished surface reflectance is 33% [43]. In the case of transmission, light will transmit through the cell and not be absorbed. In both these cases, no energy will be generated in the solar cell. The management of light in order to reduce optical losses will be discussed in detail in the following chapters.

Surface/Bulk recombination - Radiative/Auger/Schockley-Read-Hall (SRH)

Recombination in solar cells can be high, particularly in areas where the lattice structure is disrupted such as at the surface of the cell [57]. Limiting surface recombination can aid in increasing cell lifetimes, as it allows for a reduced rate at which the minority carriers are depleted. Radiative recombination occurs when an electron which is in the conduction band recombines with a hole in the valence band. This results in a photon emission at the bandgap energy [58]. Radiative recombination occurs in direct bandgap materials such as GaAs. As silicon is an indirect bandgap material, radiative recombination is not an issue. The process of Auger recombination occurs when an electron and a hole recombine in a band to band transition and the excess energy is given to another electron or hole [59]. It is worth noting that Auger recombination is prevalent at high dopant concentrations. Schockley-Read-Hall (SRH) recombination, also known as trap-assisted recombination, arises when an electron falls into an energy level which is in the bandgap which is a result of the existence of a foreign atom or structural defect [59]. This can be considered as a "trap". Once this is filled, the trap can not accept another electron. The electron within the trap can go into an empty state in the valence band and this would complete the recombination process. Surface passivation is used to reduce surface trap density.

Resistive losses/Shunt losses

It is worth noting that lower shunt resistances is a result of a processing defect and is not a consequence of the solar cell process [37]. Low shunt resistance can cause power losses in the cell.

A full investigation of these various loss mechanisms is beyond the scope of the present work. The focus of this thesis has been on the optimisation of the novel atmospheric dry etch (ADE) process, developed by Nines PV, for surface texturization in order to reduce light losses occurring in PV cells through surface reflection. As will be shown in the next two chapters, light trapping via surface texturing is a key design element used in Si PV cells to maximise energy conversion efficiency. Conventionally, Si PV cells are textured with micron-scale features using wet etching processes that yield reflectance values of 10-23% compared to a value of 36% for the untextured wafer surface. However, lower reflectance values and improved efficiency can be obtained using nanotextured surfaces, where texture dimensions are comparable to the wavelength of incident light. The ADE process investigated in this thesis produces nanotextured surfaces by thermally activated etching of silicon using fluorine gas. ADE is an industrially viable process, allowing for fast and continuous in-line processing, that displays competitive advantages over other available technologies such as reactive ion etching and metal-assisted etching, which will be discussed in the next chapter.

2 Review of surface texturing in c-Si solar cells

2.1 Introduction

Texturing of the silicon surface to reduce reflection losses is a crucial step in the fabrication process of a Si based PV solar cell. Without carrying out the texturization step, up to 33% of light will be reflected from the front surface of the solar cell and lost [43]. By giving the cell a textured surface on the micron scale, incident light strikes the surface on the inclined plane of a pyramidal or similar microstructure which results in the reflected light having a high probability of striking the surface of an adjacent microstructure leading to an increased likelihood of absorption. The surface textures also result in an increase of the optical path length in the absorber layer of the cell by scattering light through the absorber, and providing total internal reflection of long wavelength light which is reflected from the back surface of the cell. This considerably reduces light losses in the solar cell, leading to a considerable increase in efficiency.

The process of surface texturing used depends on whether a c-Si or mc-Si wafer is being used as the material for the cell. Currently, the predominant method used for producing textured surfaces on c-Si is an anisotropic alkaline wet etch, whereas an isotropic acid etch is applied to mc-Si in order to obtain a textured surface. These processes produce micron-sized textures on the silicon surface that reduce the surface reflectance before the application of an antireflective coating (ARC). It is possible to obtain lower reflectance values by reducing the texture dimensions to the point where

they are comparable with the wavelength of the incident light. In this regime, the surface texture behaves effectively as an antireflection layer with a graded refractive index [60]. A number of methods have been developed to produce such structures, which includes metal-catalysed chemical etching (MCCE) and reactive ion etching (RIE). These methods have seen some uptake by industrial manufacturer's in recent years. For example, the tenth edition of the International Technology Roadmap for Photovoltaic (ITRPV) gives the breakdown for the texturing processes used in industry for mc-Si. This is still dominated by acidic texturing, which accounts for over 70% of industrially-manufactured cells, with the remainder comprising of approximately 20% for MCCE and less than 5% for RIE [61]. Some of the different texturing processes available for texturing Si wafer-based cells will be introduced below, followed by a discussion of their relative benefits and disadvantages in the following sections before focusing on the atmospheric dry etch (ADE) process which is the topic of this thesis.

2.2 Alkaline etch

Alkaline etching solutions commonly consist of NaOH or KOH combined with iso-propyl alcohol (IPA) at a temperature of 80°C. The IPA is used to smoothen the surface as it is a wetting agent [62]. This usually produces well defined pyramidal structures on a Si(001) surface, with sharply defined facets with a $\sim 57°$ angle which is shown in Fig. 2.1. Figure 2.2 provides an example of a textured surface using an alkaline etch. This method results in the surface being etched in an anisotropic fashion, with higher etch rates observed for (100) and (110) in comparison to (111). This rate of etching can be related to the lower number of dangling bonds presented by the (111) surface. The addition of IPA slows the etch rate, which results in a higher density of smaller features, giving a more uniform texture. This is important as high etch rates would otherwise result in the removal of the pyramid texture, producing a surface with high reflectance. It is worth noting that the alkaline etch is not suitable for etching mc-Si as it would etch the random grain orientations at different rates.
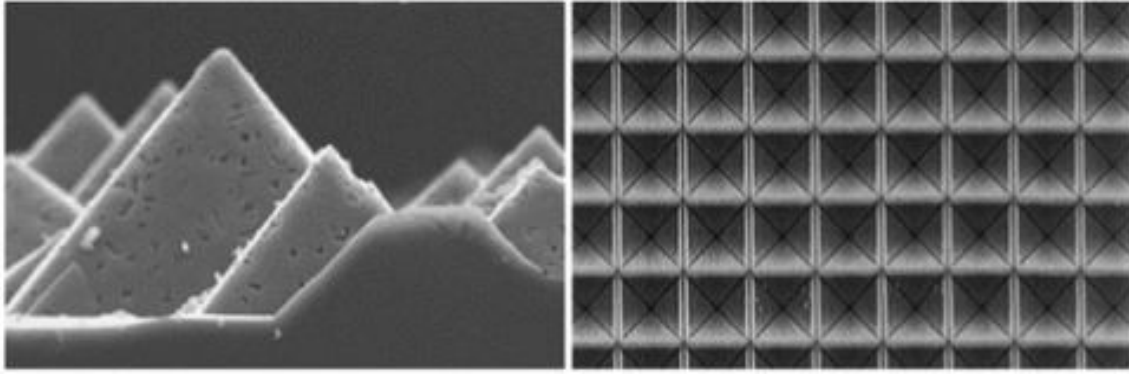
Figure 2.1: SEM image of a random pyramidal and photolithographically-defined inverted pyramid textured surfaces achieved by alkaline etching. Reproduced from [11]
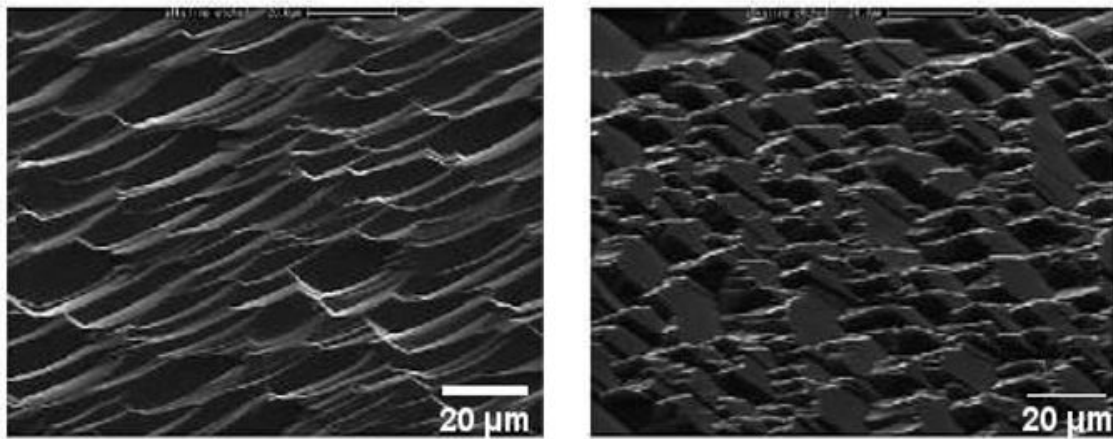
Figure 2.2: SEM images of an alkaline etch of two different grains of a mc-Si wafer with 500x magnification for both grains. The different textures obtained on each grain are the result of differing etch rates for the different grain orientations. Reproduced from [12]

2.3 Acidic etch

Acidic etching commonly applies a $HF/HNO_3/CH_3COOH$ solution, which results in the silicon surface being etched isotropically. With the use of HF/HNO_3, features on the surface tend to consist of concave pits with sharp peaks, which can be seen in Fig. 2.3. This provides adequate antireflection properties [12], with achieved reflectances of 8-

25

9.2% based on ARC and encapsulation. However, it is worth noting that it is possible to obtain a planar surface using an acidic etch if there are no defects, arising from surface damage or holes through protective layers. Manufacturers use an acidic etch to texture mc-Si as it is isotropic and therefore etches the different crystalline facets presented at the surface of the wafer at a similar rate.
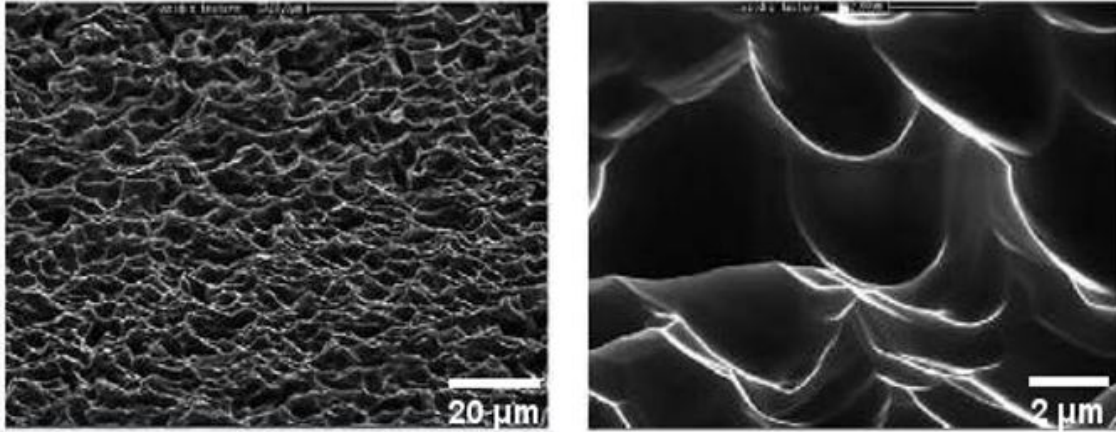
Figure 2.3: SEM images of an acidic-etched mc-Si surface with 500x magnification on the left and 5000x magnification on the right reproduced from [12]

2.4 Metal-catalysed chemical etch

As the name suggests, metal-catalysed chemical etch (MCCE) involves the use of metal particles to catalyse the chemical etching of the silicon surface. One method of MCCE involves a two-step process, the first step comprises an acidic etch of HF/HNO$_3$ to form structures on a micron scale, followed by a second step involving etching with a solution of H$_2$O$_2$/AgNO$_3$/HF to form a nanotexture on top of these microstructures [63]. The reduction of the silver nitrate during the etching process results in the precipitation of Ag particles on the silver surface, which catalyse the etching process. A MCCE-textured surface can be seen in Fig. 2.4. In order to remove any remaining Ag particles, the wafer is washed in a HNO$_3$ solution and rinsed by deionized water. As a result of the process, metal contamination, which can negatively impact photocarrier lifetimes, can occur if

traces of the metal particles are not completely removed by the subsequent cleaning steps.
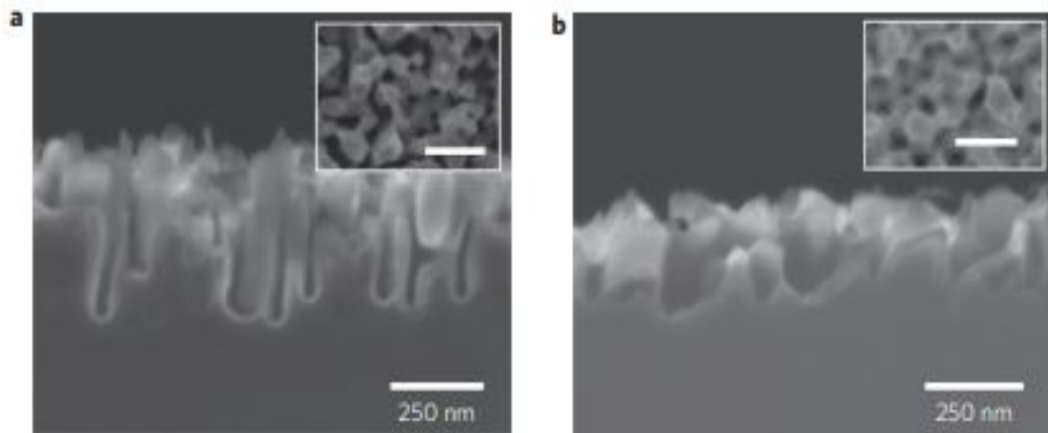
Figure 2.4: SEM image of a MCCE textured surface. **a)** Cross-sectional of unmodified structures **b)** Cross-sectional of modified structures, which has been treated with tetramethylammonium hydroxide (TMAH) for 30 seconds after etching. Reproduced from [13]
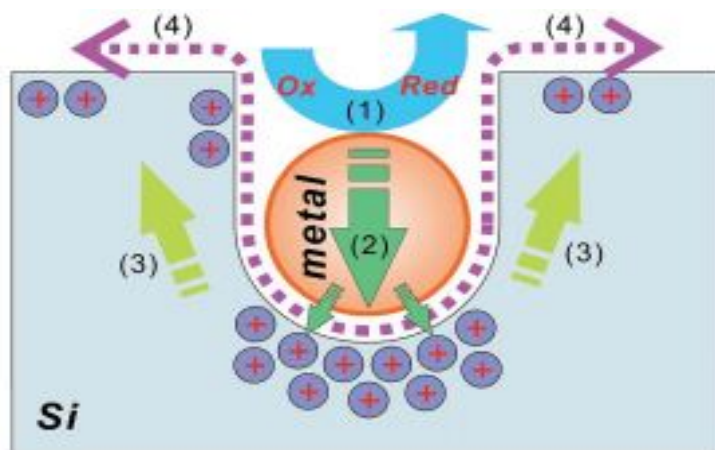
Figure 2.5: Overview of the MCCE process, (1) reducing the oxidative which has been catalyzed by the metal particle (2) movement of generated holes into the Si which has a high hole concentration under the metal particle (3) Holes moving to surface and sides of structures (4) Oxidized Si removal using HF. Reproduced from [14]

2.5 Reactive ion etch

Reactive ion etching (RIE) uses highly reactive ions in a plasma to etch the surface. The plasma is generated inside a vacuum chamber using either capacitively-coupled or inductively-coupled generation. A SF_6/O_2 gas mixture is commonly used in RIE. As with other etching techniques, photolithographically defined SiO_2 etching masks may be used to produce well-defined textures whereas maskless etching results in random structures. When a mask is used, a HF dip is used in order to remove the mask after the etching step is completed [15]. Examples of maskless and masked RIE after the etching are shown in Fig. 2.6 and 2.7. As the structures produced as a result of RIE have a high aspect ratio, very low wafer reflectance values ($< 5\%$) are obtained [15]. Despite the advantages, this etching process requires more expensive vacuum equipment in comparison to other etching methods making it cost-prohibitive for industrial scale implementation. In addition, the RIE process can result in damage to the silicon lattice that can increase surface recombination and thereby reduce cell efficiency.
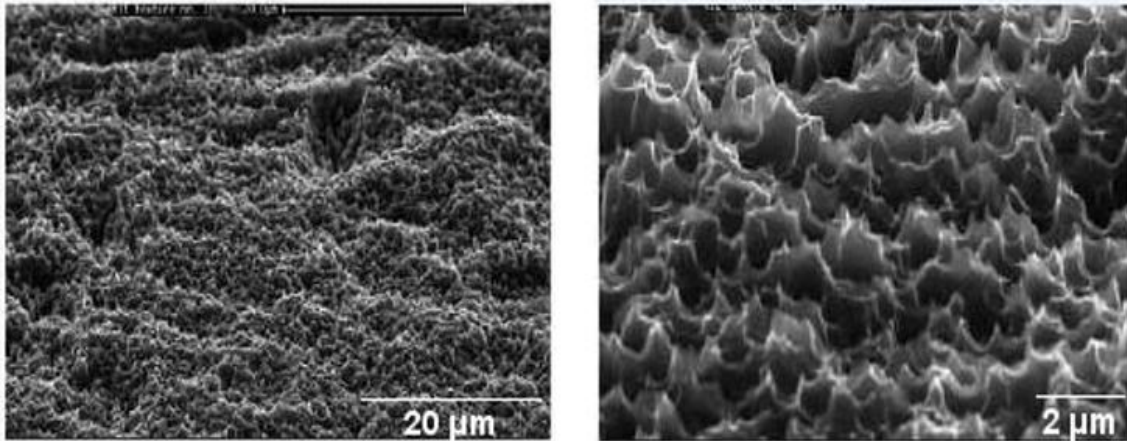
Figure 2.6: SEM images of a maskless RIE with 1000x magnification on the left and 5000x magnification on the right reproduced from [12]
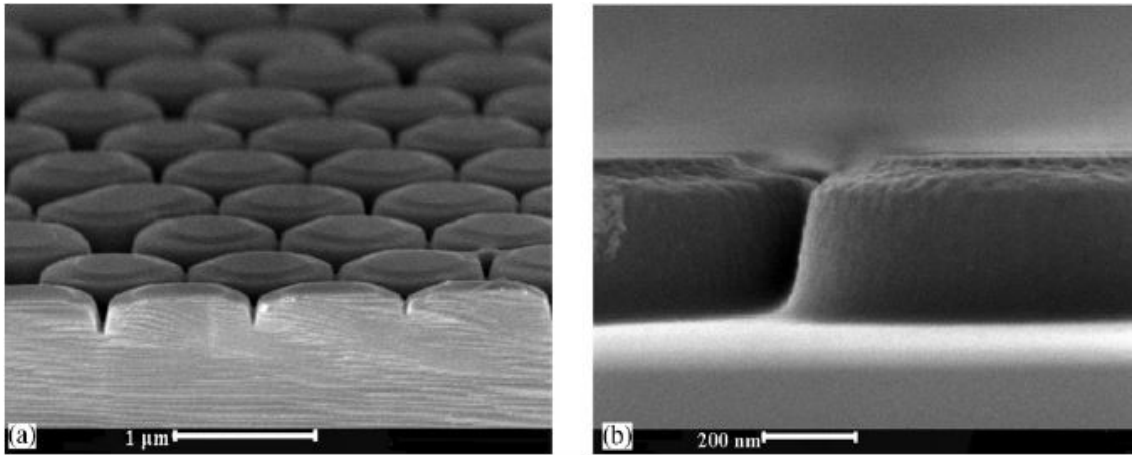
Figure 2.7: SEM images of Si after RIE with a photolithographically-defined etching mask, after the mask has been removed with a HF dip. Reproduced from [15]

2.6 Laser ablation

Textured surfaces may be obtained through exposure to a powerful pulsed-laser. The surface texture may be controlled through the maximum output power, the frequency at which the laser beam has been rastered across the surface, and the duration of the laser pulses. The pulse duration, during which the irradiated portion of the wafer surface is sublimated, ranges from femtoseconds (fs) [16] to nanoseconds (ns) [64]. The wavelengths used for laser ablation vary between different studies, however, values include 532nm, 800nm and 1064nm [16, 64]. Laser fluences of the order of tens of hundreds of kJ/m^2 are employed. The laser ablation process can be carried out in a reactive atmosphere (e.g. SF$_6$) to simultaneously texture the surface and dope the emitter layer. Use of laser ablation can also lead the formation of silicon slag that decorates the structures, which must be removed by a chemical etch following the ablation process. A textured silicon surface obtained using laser ablation using a fs laser can be seen below in Fig. 2.8.
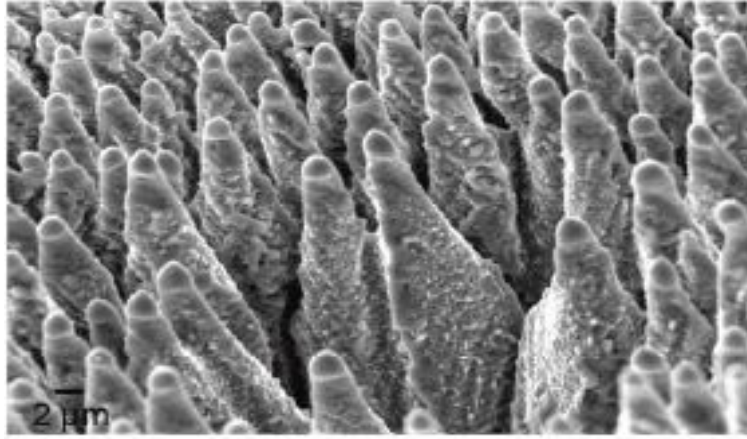
Figure 2.8: Etched surface as a result of laser ablation of 500 pulses with a duration of 80fs, wavelength of 800nm and 10kHz repetition rate reproduced from [16]

2.7 Dry etch

Dry etching techniques make use of vacuum equipment, plasma and lower water usage. Gases include but are not limited to chlorine trifluoride (ClF_3), sulphur hexafluoride (SF_6) and nitrogen trifluoride (NF3) are used as etchants, etching is carried out at sub-atmospheric pressures, with various by-products formed as a result of the processes which need to be disposed of accordingly. One example of a dry etching process which was discussed in a previous section is RIE. However, plasmaless dry-etching processes also exist which seek to avoid lattice damage encountered using RIE [65].

2.8 Comparison of texturing processes

The manufacturing of solar cells has changed over the years with the aim of reducing manufacturing costs and improving energy conversion efficiency. Some key practical issues that need to be addressed in this respect include the high water usage in certain processes, the high cost of manufacturing, equipment costs and the environmental impact. The wet etching processes which are currently used by industrial cell manufacturers are very well developed and efficient. However, as mentioned earlier, these processes are limited to the production of micron-sized surface textures as well as

consuming large quantities of water and chemicals, which affects the manufacturing costs and environmental impact.

Agnostelli et al. [66] provide projections of the dry etching process using gases such as SF_6 and perfluorocarbons (PFCs) while comparing the process to wet etching in terms of environmental impact and cost. Dry etching was determined to be a suitable alternative to wet etching. However, in order for dry etching to be a more widely-considered process for the fabrication of solar cells, the cost, environmental impact and management of the by-products, e.g. SiF_4, HF, SOF_2, SO, CO and SOF, need to be improved upon.

A study of nanotexture production on Si using laser ablation carried out by Kontermann et al. [16] noted that previous wet etching methods are limited as the resulting microstructures typically cannot reach low reflectance values. With a view to reducing how much light is reflected from crystalline silicon surfaces, the study investigated the light trapping abilities that occur as a result of a silicon wafer being textured using a femtosecond laser. Laser pulses with a duration of 80fs, wavelength of 800nm, laser fluence of approximately $20kJ/m^2$ and repetition rate of 10kHz were used. Several cells were fabricated, each having been textured with a different amount of laser pulses applied per irradiated spot including 1, 5 and 500 pulses. An increase in the amount of laser pulses applied resulted in a lower surface reflectance, with 4.5% surface reflectance achieved with 500 pulses per spot in comparison to the 1 pulse per spot reflectance having a similar result to polished Si.

Oh et al. [13] investigated the fabrication of solar cells using metal-catalysed chemical etching. Silver nanoparticles were deposited onto the Si surface using a mixture of $AgNO_3$ and HF, followed by etching in an aqueous solution of HF and hydrogen peroxide to produce a layer of nanoporous Si at the front side of the wafer. Samples were then etched using 1 vol% tetramethylammonium hydroxide (TMAH) at room temperature, with various etching times investigated. This step was carried out in order to reduce the surface area of the nanostructures. However, there are issues in relation to phenomena such as photocarrier recombination when nanostructured

surfaces are used. This paper highlighted that improvements obtained through the application of a surface nanotexture can be offset by negative issues, including Auger recombination, as a result of a higher surface area, limiting the cell efficiency and photogenerated charge collection.

In recent years, Dresler et al. [67] proposed a new process of texturing the front surface of AL-BSF solar cells based on atmospheric pressure dry etch with fluorine gas, which improved upon the issues faced by past techniques such as environmental impacts and expense of the fabrication process. Solar cell devices were processed until the contact firing phase. This allowed for testing of reflectance after etching and quasi-steady state photo conductance (QSSPC) measurements to occur before and after contact firing. After texturing, weighted reflectance values of 7.5% were achieved, a considerable difference from the iso-textured wafers which reached values above 30%.

Kafle et al. [68] provided a further investigation into the fabrication of solar cells using atmospheric pressure dry etch with fluorine as an etchant gas. Improvements over standard commercially-produced cells were noted, as the developed solar cell had some improvements in key areas, such as efficiency and fill factor, in comparison to the reference solar cell, which was produced with alkaline-etched iso-texture. This study achieved weighted reflectance values between 2% and 5% approximately for processed samples. The efficiency achieved was 15.2%, with a process which had not been fully optimized.

In a study by Abbott et al. [69], a laser was used to create a textured surface on Si to improve the light trapping abilities and reduce surface reflectance. Several parameters were varied in order to determine the optimum laser process, which was found to be a 200 ns pulse width with 1064 nm wavelength, 10J/cm2 fluence and 3 laser pulses applied. A NaOH etch and an isotropic etch were applied after laser ablation. The NaOH etch consists of 1 part NaOH to 3 parts DI water for 3 minutes at 40°C. The isotropic etch consists of 30 parts 70% nitric acid, 10 parts 99% acetic acid and 4 parts 49% HF for 3 minutes with constant manual agitation. Samples were created in order to have different pit depths to determine the optimum outcome.

2.8.1 Reflectance

With solar cells, a broad spectrum of light needs to be absorbed rather than reflected in order to have a greater possibility of creating energy. In order to benefit the most from the light being shone on the solar cell, the amount of light being reflected has to be near zero. As mentioned earlier, Kontermann et al. [16] examined the use of femtosecond laser pulses to generate nanotextures on monocrystalline Si by laser ablation. The surface texture was found to be highly dependent on the laser fluence and the number of laser pulses per spot. A single laser pulse resulted in the formation of surface rippling on the Si, while increasing the number of pulses to 500 per spot while maintaining the same laser fluence resulted in a black Si surface comprising of a surface texture of cone like microstructures. The changing surface texture was reflected in the reflectance values measured as the surface irradiated with 5 laser pulses per spot exhibited a surface reflectance no greater than 25% whereas the surface irradiated with 500 laser pulses per spot yielded a reflectance value that was less than 5%. The laser pulses had a 80 fs duration and a laser fluence of approximately 20 kJ/m^2 [16]. However, the potential issue in regards to laser ablation is that it can result in a laser-damaged surface layer due to the process of melting and recrystallisation, and chemical etching may need to occur after if there is formation of ablation slag [69]

Black silicon is attractive for solar cells as it reflects very little of the light that hits the surface of the silicon wafer. However, the much increased surface area has major implications for surface and Auger recombination. In the case of the research on metal catalysed chemical etching, carried out by Oh et al. [13], the resulting solar cell had a reflectance value of 4.6%, which is slightly above the average for black silicon solar cells. However, in comparison to the other research carried out in this area, similar reflectance values are seen [13]. Using reactive ion etching can also produce black silicon surfaces with reflectance values below 1%[70]

Using the atmospheric dry etch, Dresler et al. [67] fabricated solar cells from mc-Si with an average surface reflectance of 7.5%. This compared to a reference sample with a reflectance value of 30.3% which was produced using an isotropic etch with

HF/HNO$_3$/H$_2$O. Further study into the fabrication of solar cells using this texturing process yielded textured surfaces with reflectance values of 2% [68].

Jiang et al. [71] used an acid-based etching process, involving H$_2$O$_2$, with varying time between 30 and 600 seconds to produce an inverted pyramidal surface texture on mc-Si. The lowest reflectance achieved with this texture was 4.9% with a pyramid scale of 50 nm. However, a surface comprised of inverted pyramids with an average size of 500 nm was chosen for solar cell fabrication as a result of being distributed more evenly across the surface, having less structural overlap and for reflectance considerations. Before applying a SiN$_x$ layer, to the 500 nm inverted pyramid texture had a reflectance of 16.95%. After a SiN$_x$ layer was applied, the reflectance decreased to 3.29%. The improvement in reducing surface reflectance with this method can be seen when compared with values obtained for a pyramidal microtexture produced on monocrytalline silicon with an alkaline etch, which achieves a surface reflectance of around 10-12%, while acid etching of mc-Si achieves reflectance values of around 25%.

In the study carried out by Ying et al. [63], varying molar ratios (ρ) were used for the metal catalyst chemical etching (MCCE). Values of ρ include 7%, 15%, 20% and 25% with reflectance results of 31.93%, 16.80%, 10.37%, and 4.85% respectively. The MCCE process contribution to the these reflectance values could be a result of the gradient refractive index effect due to the nanostructures formed, which are 30 to 200 nm in size laterally. In comparison, the acidic etch applied beforehand achieved a feature size of 2 to 6μm which would have created a scattering effect. Abbott et al. processed several samples using laser ablation resulting in different ablation pits depths of 10 µm, 20 µm, 30 µm, 40 µm and 50 µm. The 50 µm ablation pit was the only depth to experience residual slag. Despite this slag, the 50 µm produced the lowest front surface refection, with a value of less than 10% across most wavelengths. It is also worth noting that the smaller the ablation pit depths, the more they follow the reflection characteristics of a planar silicon surface. Optical properties were then tested, in both reflection and transmission, for a single and double sided laser texture in comparison to single and double sided random pyramids. The absorption was then

calculated for each of these based on the measured results. The random pyramids produced highest and lowest results for the transmission and reflection, respectively, for wavelengths greater than 1000 nm, whereas shorter wavelengths resulted in little to no difference in the amount of light which was reflected [69].

Rahman et al. used block-copolymer self-assembly combined with plasma etching to produce nanostructures with varying values for feature height (t) and spacing (l), with 32 nm, 65 nm, 140 nm and 230 nm being used for t and 40nm, 52nm, 60nm and 67nm being used for l. At l = 52 nm, reflectance was determined with varying values of t. The lowest reflectance achieved was <1% with t = 52 nm, which is considerabley lower than 35% of a flat surface. Values lower than 230 nm for t with l = 52 nm resulted in more light being reflected from the surface. In order to achieve reflectance of <1% while varying l, t also needs to be changed. This occurs with l = 40 nm and t = 165 nm, l = 52 nm and t = 225 nm, l = 60 nm and t = 330 nm and lastly l = 67 nm and t = 440 nm. No antireflective coating (ARC) was applied before obtaining these reflectance values, which is beneficial as an ARC can be applied in order to further improve the light trapping abilities if needed. However, as the surface reflectance is already very low, it was noted that an application of an ARC would not yield any further benefit [72].

Koynov et al. [73] noted that surface reflectance could be reduced by application of ARCs, such as SiO_X, ZnO, ITO and Si_3N_4, that reduce surface reflection by 8-15%, or by is deep surface texturing to produce features that are smaller than the photon wavelength with optical constants which vary gradually. In order to reduce the visible light spectrum significantly, a texture depth of 200-300 nm should be used. Koynov et al. applied deep surface texturing using MCCE on three different types of wafers, n-type single crystal Si, p-type mc-Si and amorphous hydrogenated Si (a-Si:H, intrinsic). These wafers were rinsed in acetone and IPA following by a HF dip. Wafers were subject to either no treatment, front side treatment or treatment on both sides. A reflectance value of <5% was achieved by using a treatment on both sides.

2.8.2 Efficiency

The Schockley-Queiser limit describes the theoretical efficiency limit of an ideal solar cell under the conditions of illumination by a black body with a 6000 K surface temperature [74]. Currently the standard used is the AM 1.5G spectrum, as it takes into account the scattering of light in the atmosphere and light absorption. Several factors are assumed in order to calculate this limit, including that the only recombination path which cannot be zero is radiative recombination, photons whose energy is less than the bandgap do not interact with the solar cell, photons with energy above the bandgap interact with the solar cell and form electron-hole pairs.

Improving the energy conversion efficiency of a solar cell can be achieved in a number of ways, including increasing how much light is taken in by the cell resulting in an increase in the number of photo-generated carriers and increasing the number of carriers reaching the p-n junction [75]. As of 2018, the maximum efficiency achieved by the Fraunhofer Institute for Solar Energy Systems was 26.7% for single crystal Si and 22.3% for multi-crystalline Si [76]. It is worth noting the efficiency of the single crystal Si cell is approaching the theoretical efficiency of a single-junction c-Si cell of 29.6% . The improvement in efficiency is a key aspect in developing solar cells as a renewable energy resource.

The potential efficiency of solar cells fabricated by dry etching has been examined in comparison to the efficiency of solar cells manufactured by wet etching with the conclusion that texturing by dry etching would result in improved cell efficiencies compared to cells manufactured by wet etching processes [66]. Solar cells that use black silicon have been shown to have a higher absorption rate of sunlight that hits the surface. While more light is absorbed by the cell, there is a corresponding increase in carrier surface recombination due to the increased surface area. In the study by Kontermann et al. on surface textures produced by laser ablation [16], several solar cells were fabricated under different conditions of the number of laser pulses applied to the surface of the silicon wafer. Formation of the emitter layer was carried out simultaneously with the surface texturisation by performing the laser ablation in an

SF_6 atmosphere, resulting in sulphur-doping of the silicon surface to produce an n-type emitter layer. The resulting prototype cells had an efficiency of 4.5% maximum whereas previous laser processed black silicon solar cells had an efficiency of 2.2% [16]. With new methods of manufacturing solar cells, the efficiency can be improved further. Oh et al. demonstrated that nanoporous Si, produced by metal-catalysed chemical etching, can be used to significantly reduce the amount of light that is being reflected from the front surface of a c-Si solar cell, resulting in a corresponding increase in cell efficiency [13]. In that study, the efficiency of the solar cell, which was produced without an additional anti-reflection coating (ARC), was found to be 18.2% as compared to values of 13.1% for a polished Si surface with no ARC and 18.6% for a standard cell with a pyramid texture and ARC [13]. The authors of this study found the higher carrier recombination rate observed in nanotextured solar cells is a result of Auger recombination rather due to excessive dopant concentrations during emitter diffusion as a result of the nanotextured surface producing a high surface area. It is therefore crucial to consider the impact of the nanotexturisation process on the other process steps in the fabrication scheme of a solar cell, including emitter diffusion, passivation and metal contact formation [67].

With variations in the processing methods of solar cells, the efficiency varies between each. For the ADE process proposed by Kafle et al., the maximum efficiency of Al-BSF cells produced using ADE-textured mc-Si reached was 15.2%. While this is lower than the 16.4% efficiency of reference cells prepared using acid etched iso-texture, it was observed that these were first-generation cells using the ADE process and therefore further improvements with respect to contact adhesion, passivation and emitter doping levels would likely yield higher cell efficiencies [68].

Jiang et al. [71] produced a solar cell with inverted pyramids surface texture, using a modified acid-etch process involving hydrogen peroxide with an efficiency of 18.62%. This efficiency is approximately 0.5% higher than the comparable acidic textured mc-Si solar cell, which had an efficiency of 18.17%. The cells fabricated during this research used p-type mc-Si which had an ARC applied, with silver front electrodes and

aluminium back-surface contacts were formed through screen printing followed by co-firing in a belt furnace system which is lamp heated. A cell efficiency of 18.23% was achieved by Ying et al. [63] by using a two-step technique of acidic etch followed by MCCE. This is higher than the reference acidic etch and black Si cells that were produced for comparison in this study, which had efficiencies of 17.70% and 16.15%, respectively. Efficiencies for laser texture, random pyramid and a planar surface were compared by Abbott et al., with values of 18.4%, 18.5% and 14.6% reported, respectively. Both methods of surface texturing provided an increase in efficiency, with the random pyramid texture providing a slightly better result. However, the authors acknowledge that laser ablation process is potentially disadvantaged by the fact that it can result in the formation of a residual slag around etch pits as a by-product of the ablation process. In regards to the results achieved, the main concern can be considered to be the residual slag which the 50 µm ablation pit experienced exhibited. This slag can lead to recombination issues [69].

2.8.3 Expense

With any manufactured product, the cost of production and maintaining equipment will be looked at before it is rolled out on a large scale. This is carried out to determine if the process will be able to be maintained, in particular in the long term in the case of solar cells. With a process in place for manufacturing solar cells, the initial costs for dry etching could be compared to the costs at the time for wet etching. The comparison shows that there is little difference between the costs for the two, as wet etching has a total internal cost of 4 to 7 €c/Wp when considering cost of ownership, water and chemical costs whereas dry etching has a total internal cost of 3.5 to 5 €c/Wp with ownership costs and process gases in 2004 [66]. As of 2019, costs have decreased as low as 11 cents ($) per kWH in Hawaii [77]. There is another aspect to be considered; the increased water costs that are faced by the wet etching process. This is a result of the water resource being under strain.

In regards to texturisation by laser ablation, there is no indication how costly the

process can be to maintain, in particular in regards to the femtosecond laser and the test equipment. In the case of certain fabrication processes, the use of equipment, maintenance and materials needed for the process can be costly [16]. The fabrication of solar cells can be expensive; nevertheless, new methods of manufacturing can aid in the lowering of costs. Despite its advantages, reactive-ion etching is also considered to be too costly to implement on an industrial scale as buying and running the plasma and vacuum equipment can be high. With the fluorine (F) based atmospheric dry etch process, the cost can be reduced as there is no need for a vacuum. There are further cost reductions as the amount of chemical waste that needs to be disposed of and treated is reduced[67]. In this respect, the ADE process has several advantages [68], including no need for a vacuum or a plasma pump. The reductions in chemicals and reduced wafer damage also aids in low production costs. The ADE process is also rapid, with etching taking less than one minute.

The expense of fabricating solar cells will continue to reduce in coming years as new methods of manufacturing come on stream. This reduction in cost will benefit both the manufacturer and the consumer. Through research and innovation, solar cells have shown improvement in recent years, in particular in areas such as efficiency, environmental impact and manufacturing methods. However, further research and development is needed to further optimise the operation of solar cells. Enhancements in the efficiency and the fabrication process, including making the method of manufacturing the cells more eco-friendly are required. This can be achieved by improving current processes or through implementation of new processes. New processes need to be investigated in order to determine their viability to be sustained, along with confirming that they will be able to compete against other existing processes.

2.8.4 Environmental impact

The fabrication process of different devices including solar cells has had an impact on the environment in the form of global warming potential gases, harmful by-products and

high water usage. The importance of being able to produce solar cells on a large scale while being environmentally friendly during the process of the production is becoming more evident. If as a result of manufacturing the solar cells global warming potential gases are emitted and/or an extensive use of water is used, then the benefits may be outweighed by the costs. Therefore, creating an environmentally friendly process is vital. When comparing the viability of new processes to old ones it is important to weigh the possible impacts that they can have on the environment. While wet etching makes use of mature technologies, the current acid and alkaline etch processes used as texturing methods for wafer based silicon solar cells require use of harmful chemicals such as HF, KOH, NaOH and HNO_3 as well as requiring large amounts of water. When dry etching was being considered as an alternative texturing process for solar cell production, it had to be compared to existing processes. The main advantage of dry etching was the reduced consumption of water, which would aid in preserving this resource. Despite this advantage, the use of sulphur hexafluoride (SF_6) and other gases results in a higher global warming potential (GWP). The environmental impact of gases used in dry etch processes is not widely discussed in the research being done in [16, 13].

Prather et al. [78] provided annual emissions of greenhouse gases, which include SF_6, NF_3 and PFCs. NF_3 has a greater impact then SF_6 and PFCs, equivalent to 67, 25 and 42 equivalent million metric tons of CO_2 ($MMTCO_2$), respectively. As these gases are commonly used in the dry etching process, the impact which they have on the environment has to be considered. In regards to NF_3, it will take centuries to remove it from the atmosphere. The gases used in typical dry etching processes are SF_6 and NF_3, both of which have more than 10,000 times greater greenhouse warming potential than carbon dioxide (CO_2) [78, 79]. With the new atmospheric dry etch manufacturing process proposed by Dresler et al. [67], the use of GWP gases is eradicated as fluorine (F_2) replaces the use of SF_6 and NF_3. This new process also makes use of little or no water during manufacturing, reducing the strain on the resource. With these improvements, dry etching has become a more feasible option for creating solar cells [67]. It is worth noting that F_2 gas can be regenerated from the etching by-product and therefore reused,

reducing the environmental impact and operation costs.

2.9 Atmospheric dry etch (ADE)

The ADE process that is the focus of this thesis, is a novel dry etch process developed by Nines PV [67]. They have developed two commercial ADE tools, the single lane ADE-100 tool for pilot lines and the multi-lane ADE-6000 tool for industrial production. It is an industrially viable process that displays competitive advantages over other available technologies such as RIE and MCCE in that it is a rapid process, suitable for continuous in-line processing, it is a dry process, it can preform single sided etching, is effective on both monocrystalline and multicrystalline wafers, operates without the requirement for vacuum generation as no plasma generation is involved and the ADE tool has a small physical footprint compared to current wet etch systems. The silicon etching is carried out at atmospheric pressure using fluorine gas. Inside the ADE reactor, F_2 is supplied and diluted with nitrogen (N_2), with the gas mixture heated at the gas diffusion plate [68] and at the surface of the Si wafer due to the exothermic reaction of the reaction process. By heating the F_2 gas, F radicals are formed as a result of thermally-activated bond scisson. The Si wafer being etched is secured in a wafer holder, which is heated to assist the reaction rate between Si and F. The wafer moves through the etching zone at a rate defined before the process begins. An overview of the ADE tool in operation can be seen in figure 2.9.
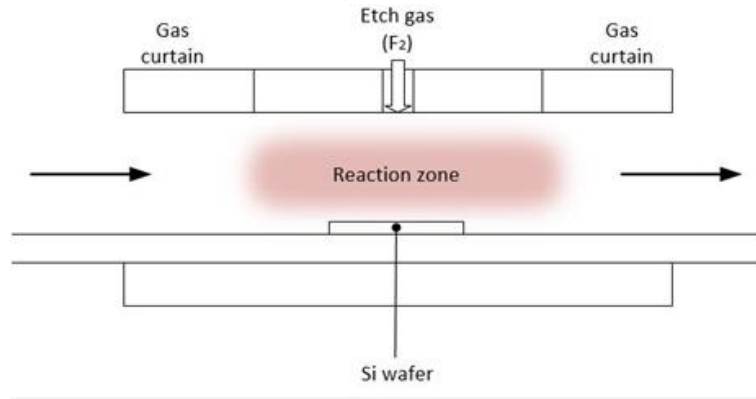
Figure 2.9: Overview of ADE tool, operating parameters include F_2 concentration, wafer velocity, temperature [17]

It has been found that higher a substrate temperature can have a major effect [68] on the etching process in two ways; it may aid in enhancing the absorption of F or it will increase the rate in which SiF_x is formed and removed from the surface in the form of SiF_4 gas [80]. This is due to the reaction rate between F and the Si surface being limited at lower temperatures. The main parameters include F_2 concentration which can be adjusted during the etching process, gas diffusion plate temperature, substrate temperature and wafer speed through the etching zone [68]. Variations in these parameters will result in different etch rates and surface textures which will determine the light trapping abilities of the solar cell. Variations in the etch rate can be determined by weighing the wafers before and after the etching phase and by using microscopy techniques such as atomic force microscopy (AFM) and scanning electron microscopy (SEM).
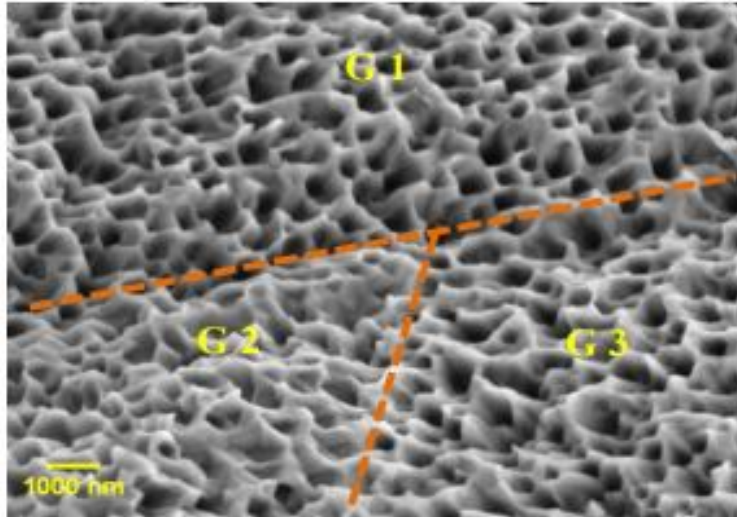
Figure 2.10: SEM image of mc-Si after processing through the ADE tool, reproduced from [18]

2.9.1 Process overview

F_2 plays a central role in the reaction mechanism leading to the etching of the Si. In order to etch the Si, F_2 will need to be split to form F radicals. This is achieved by heating the F_2 gas, resulting in the release of F radicals due to thermal dissociation [68]. Once this occurs, F becomes an excellent means for forming bonds with Si due to Si having a lone pair of electrons in its outer shell [81] or a dangling bond occurring [80]. When a bond occurs between Si and F, SiF_x (x=1,2,3,4) is formed [80], with x varying across the Si surface. The forms in which SiF_x can occur are shown in figure 2.11, along with Si with no bonds formed with F.
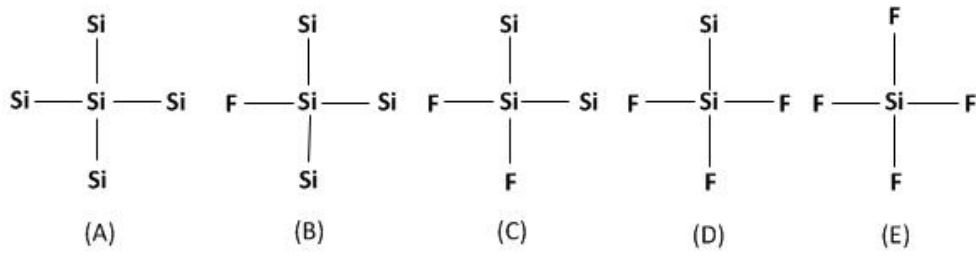
Figure 2.11: Si and SiF$_x$ bonds, where (A) is Si with no F bonds, (B) is SiF$_1$, (C) is SiF$_2$, (D) is SiF$_3$ and (E) is SiF$_4$

With SiF$_x$ occurring as a result of the chemical reaction between Si and F, a layer of SiF$_x$ is formed on the surface of the Si wafer [81]. When F atoms develop a bond with the Si underneath the SiF$_x$ layer, Si can be removed in the form of two gaseous products, SiF$_2$ and SiF$_4$, which is achieved through desorption [82, 81]. In the case of SiF$_2$, it can be emitted from the surface or can remain to form higher SiF$_x$ products by forming bonds with more F [81]. Figure 2.12 displays the reaction in which SiF$_2$ can be formed due to the chemical reaction of F atoms and the Si surface.
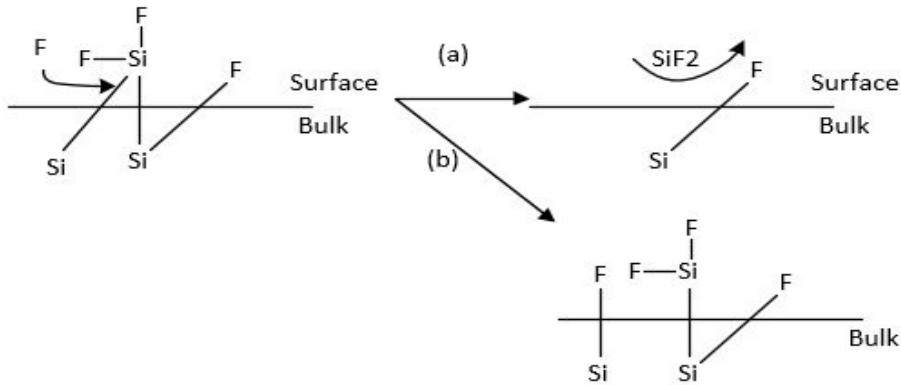
Figure 2.12: Formation of SiF$_2$ on the surface, where (a) is the release of the gas and (b) is SiF$_2$ remaining on the surface

As SiF$_4$ is a stable product [81] of the reaction between F and the SiF$_3$ species, it is noted that it can be created with no deformation to the lattice of Si. This is important as it does not lead to reduced carrier lifetimes due to lattice damage, It is formed as a

result of the outer shell of F not being complete and accepting an electron from a Si bond on the surface and weakening the Si-Si bond, resulting in the SiF_3 species forming a bond with F [80]. With the high temperature which arises as a result of the exothermic reaction, SiF_4 will want to escape if there are no restrictions in regards to geometry [80]. However, the release of heat during the reaction can lead to SiF_4 being desorbed from the surface [80] in the form of a gas. This allows for Si to be removed from the surface of the wafer [81], resulting in the surface being textured. The process of SiF_4 desorption can be seen in figure 2.13.
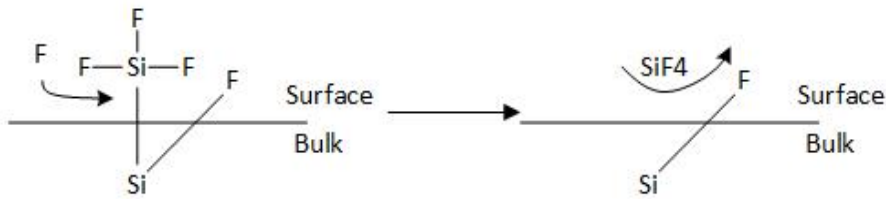
Figure 2.13: Release of SiF_4 from the surface mechanism

The process of F interacting with the surface of the Si wafer resulting in the release of Si in the form of SiF_2 and SiF_4 with a SiF_x layer can be seen in figure 2.14.
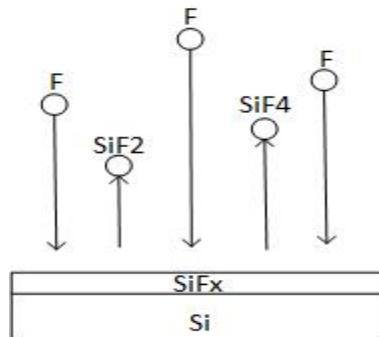
Figure 2.14: Si wafer with a SiF_x layer, with SiF_2 and SiF_4 being released from the surface

Various factors can effect the formation of the nanostructures and the rate at which Si is etched during the process, these include doping of the Si and if a native oxide layer is present. The doping of the Si being used can be affect the removal of Si from the surface as n-type Si will be etched by F with more ease in comparison to p-type Si [80]. This is due to the electron density of the n-type Si being higher than the electron density of

the p-type Si, allowing for bonds to be produced as there are more free electrons. In the case of the native oxide layer which occurs, it is normally very thin (1-2 nm) and does not impact the etching process. The native oxide layer can arise on the surface within 24 hours after being it cleaned and etched. However, if this layer is too thick it can slow down the beginning of the etching process. In order to avoid a thick native oxide layer, etching within a day of removing the surface oxide or storing the wafers under an inert gas is required.

With the use of multicrystalline silicon (mc-Si) wafers, the rate at which a specific SiF_x species is formed will vary between crystals. The emission of SiF_2 and SiF_4 from the surface will therefore vary between the crystal grains, resulting in the texture differing between the grains of the wafer [18].

2.9.2 Process by-products and disposal

Recycling of gases is recommended where possible particularly with gases that are either high value or are expensive or difficult to dispose of. However, it is only possible with gases that are not a by-product. In the case of the process being carried out, SiF_4 is formed as a consequence and can be hazardous if not dealt with accordingly. As a result of how unsafe SiF_4 can be, it must not be discharged directly into the atmosphere and in a location which it could be dangerous [83]. In order to meet the requirements which have been set out, a scrubber is used in order to correctly handle the SiF_4 gas [84]. Scrubbers within the ADE tool collect the SiF_4 until they are full. The full scrubbers, and therefore the SiF_4, are removed and disposed of according to local and national regulations for disposal of gases. It is also worth noting that passing Si_4 through a water scrubber can cause it to break down into SiO_2 and HF, which can be separated, collected and disposed of [85].

2.10 Dry etching process vs Wet etching process

Wet etching is common practice throughout not just the solar cell fabrication process, but also for the fabrication process of semiconductor devices. Dry etching, on the other hand, is not as common. However, industry is increasing its use of dry etching techniques. The ADE process and a wet etch process are compared in 2.1, where the key areas of interest of both processes are looked at.

	Wet etch	**Atmospheric dry etch**
Water usage	High water usage	Low water usage
Equipment cost	Inexpensive	Low, no vacuum equipment
Chemical cost	High	Low [86]
Submicron features	Difficult	Easy
Environmental impact	Can be high	Lower than wet etch [86]
Current industry use	Common	Not as common
Process knowledge	Well established	Not as established

Table 2.1: Comparison between dry and wet etching

In contrast to the wet etch, the ADE process demonstrates a number of advantages. This includes submicron features for light trapping and little to no water usage.

In comparison to other dry etching techniques, this method uses F_2 instead of global warming potential (GWP) gases such as sulphur hexafluoride (SF_6) and nitrogen trifluoride (NF_3) [67]. It also benefits from lower equipment costs due to no requirement for plasma and vacuum or vacuum pumps as the process is carried out at atmospheric pressure.

3 Light management in solar cells

3.1 Introduction

Light management can be considered vital to the operation of solar cells as it influences the surface reflectance and absorption factor of the cell. The use of light trapping and surface reflectance reduction in solar cell applications allows for a reduction in the amount of material used, a reduction in production cost and an improvement in efficiency [87]. Light trapping is used in order to confine light in the absorber layer and is related to transmission losses whereas reducing surface reflection is related to reflection losses. The nanostructures which are formed as a result of the etching process, which were described in chapter 2, are used in order to aid in the reduced surface reflectance and light trapping abilities of the solar cell. This chapter will investigate the theory of light trapping and the absorption abilities of nanostructures formed on the surface of a silicon (Si) wafer.

In the operation of solar cells, the use of light trapping techniques have become more vital as it reduces optical losses and allows a thinner absorber layer to be used, reducing material losses. Textured surfaces allow for more light to be absorbed at the front surface of the solar cell in comparison to a cell where no light trapping techniques are implemented [88, 43]. This is a result of an increase in the amount of light being trapped at the surface and therefore creating a higher probability of the light being absorbed into the cell [43]. The thickness of the cell can be reduced as a result of improved light trapping, allowing for a reduction in costs [87]. Different methods of light management have been used including stacked cells with different bandgaps [89], inclusion of back

surface reflectors, texturing of front and back surfaces of the cell, anti-reflective coatings (ARC) [90] and textured surfaces on a micron and nano scale [91, 92]. Based on the theory of light trapping, the maximum absorption enhancement for a solar cell is $4n^2$ (n = refractive index), also known as the Yablonovitch limit [93]. The Yablonovitch limit is also referred as the Lambertian limit.

3.2 Reducing surface reflectance

Light management can be considered vital to the operation of solar cells as it influences the surface reflectance and absorption factor of the cell. Different light management strategies are used, including stacked cells with different bandgaps that address spectral mismatch [89], optimising front contact geometries to balance shading losses and series resistance, inclusion of back surface reflectors to reduce transmission losses, texturisation of the front and back surfaces of the cell, and anti reflection coatings [90]. A full discussion of these various strategies is beyond the scope of this thesis. This chapter will instead focus on methods that reduce surface reflection and increase light trapping within the absorber layer of the solar cell. These methods allow for an improvement in efficiency through reduced optical losses, and a reduction in the amount of material required, since a thinner absorber layer can be used, leading to reduced production costs [87]. Anti reflection coatings and surface texturing allow for more incident light to be transmitted through the front surface of the solar cell [88, 43], while light trapping via diffuse scattering, back surface reflection and total internal reflection increase the amount of light that is absorbed inside the cell [88]. The nanostructures which are formed as a result of the ADE process, as described in chapter 2, impact both front surface reflection and light trapping within the solar cell. As such, this chapter will investigate the fundamental principles of reducing front surface reflection and light trapping in Si wafer-based solar cells.

One of the major issues regarding solar cells is the amount of the incident light which is reflected from the front surface of the cell. About 33% of the light incident on a

polished, flat single crystal Si surface will be reflected on the first pass. The reflection and transmission at the air-silicon interface is dependent in the refractive indices of the different media and the angle of incidence. The Fresnel equations can be used to describe this. Under normal incidence, the surface reflectance reduces to [94]:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \tag{3.1}$$

Where n_1 is the refractive index of the first material (air) and n_2 is the refractive index of the second material (silicon). The strategies used to reduce reflection from the front surface include application of an anti reflection coating, surface texturing with micron-scale structure and nanoscale texturing. Surface texturing is based on two typical textures, which include [95]:

1. A microscale texture which leads to multiple reflections, which leads to light interacting with the surface several times.

2. A nanoscale texture which has a graded refractive index.

3.2.1 Anti-reflective coatings (ARC)

Anti-reflective coatings are used to reduce the reflection of light from the front surface of the solar cell. They are typically quarter-wavelength coatings, in that the thickness (d) and refractive index (n_1) of the ARC is chosen for an optimum wavelength (around 600 nm) such that the optical path length (OPL = n_d) in the ARC is one quarter of a wavelength. Light of this wavelength reflected at the ARC-silicon interface is 180 degrees out of phase with the incident light, thus destructively interfering and reducing surface reflection. The reflectance is minimised where the refractive index of the ARC, $n_1 = \sqrt{n_0 * n_2}$, where n_0 is the refractive index of the incident medium (air or glass encapsulant) and n_2 is the refractive index of Si ($n_2 = 3.5$). Assuming that the solar cell is protected by a glass encapsulant ($n_0 = 1.5$), then the refractive index of the ARC is typically around $n_1 = 2.3$, which can be obtained by depositing a thin layer of

TiOx or SiNx:H. The disadvantage of an ARC is that the interface effect works best for a single wavelength and at normal incidence. It's effectiveness decreases for broadband radiation under oblique illumination.

3.2.2 Surface microtexturing

Textured surfaces, where the texture structures have dimensions on length scales larger than the wavelength of the incident light, have been shown to be useful in light trapping [87, 95]. One possible surface texture is the micron-scale pyramid structures produced on Si(100) using an anisotropic alkaline etch. The geometry of these structures is such that it can result in the incident light being reflected from one pyramid to another and allowing another chance for the incident light to be absorbed into the cell [43]. This arises because light that is obliquely incident on the pyramid facets can be reflected forward onto one of the facets of an adjacent pyramid, as shown in fig. 3.1. The degree of the forward reflection is dependent on the angle, α, between the facet and the macroscopic surface plane. The angles which determine how the incident light is reflected are as follows [96]:

- $\lambda > 60°$: The incident light can have triple reflections into the surface.

- $\lambda > 45°$: The incident light can have double reflections into the surface.

- $30° < \lambda < 45°$: The incident light is less likely to have double reflections into the surface, but double reflections could occur.

- $\lambda < 30°$: Light will not have multiple reflections into the surface. The surface reflectance will be comparable with that of a flat, planar surface.

The angles of the pyramids which are formed are defined as a result of the orientation of the silicon crystal. Alkaline etching of the Si(100) surface exposes (111) oriented facets that form an angle of 54.7° with the (100) surface. These angles determine how many chances the incident light have to be absorbed into the cell [43]. In the case of the pyramid structure on the alkaline etched Si(100), the 54.7° angle means that the light will

be reflected forwards twice. For bare silicon, 33% of light is reflected with each interaction with the surface [43]. Therefore, two interactions would result in approximately 11% of the incident light being reflected from the surface, due to 33% of the light being reflected with each interaction with the surface, as seen in figure 3.1. As discussed in previous research [97], the use of randomly microtextured surfaces aids in light scattering as the incident light is distributed in different directions if it is not absorbed increasing the number of surface interactions, leading to greater transmission through the front surface of the solar cell. The use of random textures also has a considerable advantage over their periodic counterparts, this is due to periodically textured solar cells having lower electrical properties when attempting to optimize the optical properties of the periodically textured cells [97].
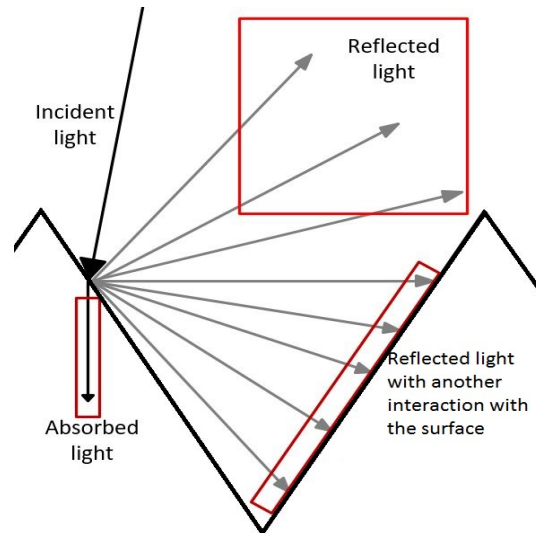
Figure 3.1: Incident light interacting with the front surface of structures, with some light which was reflected interacting with the surface again while the remaining is reflected from the surface

3.2.3 Surface nanotexturing

In the above section, the effect of microtexture on surface reflectance was discussed. It is now possible to produce surface nanostructures of high aspect-ratio structures that have dimensions on a length scale that is less than the wavelength of incident light

using methods such as atmospheric dry etching, laser ablation, metal-catalysed chemical etching and reactive ion etching. In this scenario, the angle α is so large that the light is reflected forward at each interaction, deeper into the nanotexture. The interface between air and Si can effectively be viewed as undergoing a gradual shift in refractive index, proportional to the volume fraction of each medium at a given depth in the nanotexture layer. As a result, there is no abrupt interface at which incident light is reflected back out of the surface. Instead, the light is guided deeper into the nanotextured layer so that it is almost completely transmitted into the Si.

The nanostructures are most effective if they improve the photocurrent across the active light spectrum range for the particular semiconductor as well as multiple angles of incidence [98]. Several techniques used for nanoscale structures, including gratings, plasmonic nanostructures and nanowires. These nanostructures are considered most effective in solar cells when they have multiple incidence angles and the photocurrent must be improved across the active spectral range for the semiconductor being used. Use of graded-refractive indices allows for reflection to be considerably reduced or eliminated for a range of wavelengths and incidence angles. This occurs as the light is not met with a sharp interface and instead encounters a gradual change in refractive index [91]. In relation to the Lambertian limit for Si based solar cells, as the structures are nanometres in height then it is more achievable to have a c-Si wafer thickness of 1-3 μm rather than the usual 300-400 μm in order to reach this limit [99]. This will also aid in reducing production costs. Several methods have been considered to achieve this, including gratings. Gratings which are achieved as a result have three conditions for them to be considered highly functioning, which include:

1. 2D gratings are better than 1D gratings, as 2D gratings provide more diffusion channels [99]

2. Tapered gratings are well coupled to incident light as optical density varies gradually. Application of these tapered gratings on the front surface can result in a reduction in reflection [99]

3. The period size of the grating should be slightly smaller than the wavelength. With a period that is too small, structural detail cannot be detected and diffraction is weak. [99]

It is worth noting that when nanostructures are applied, wave optics concepts are required in order to determine new limits for performance [93]. With a considerable understanding of these limits, solar cells with high performance could be designed. The aspect which needs to be considered is the wave-optics domain, as it provides important insights into the process of light trapping. One method which this theory brings forward is over-coupling, achieved by coupling in and out of the absorber by the greatest extent possible. Application of structures on the front surface of a solar cell can reduce reflection due to coupling light in the cell. This can be seen with transparent conductive oxides which have been used as contacts which have been roughened to achieve some level of light trapping [93]. For a bulk solar cell, the wave-optics also uses the limit of 4n². The theory also shows that bulk limit is similar to the limit of a wavelength scale thin film.

3.3 Light trapping

In addition to reducing reflection from the front surface of the cell, the incident light can be more efficiently harvested by increasing the light absorption within the absorber layer of the cell. Selective absorption occurs when either only a section of the light spectrum is absorbed by a material. The selective absorption characteristics of Si are as follows:

1. Short wavelength photons ($\lambda < 1.0\mu m$) have a larger energy than the bandgap of Si resulting in absorption and creation of electron-hole pairs [100]. Carriers generated by photons with energies in excess of the Si bandgap are thermalised through photon interactions with the Si lattice.

2. Long wavelength photons ($\lambda > 1.2\mu m$) are hardly absorbed and cannot create electron-hole pairs [100]

3. Photons in transition region($1.0\mu m < \lambda < 1.2\mu m$) are weakly absorbed as they have to travel long distances before they can be absorbed [100]

It would, in principle, be possible to increase the absorption of the weakly absorbed longer wavelengths by increasing the thickness of the absorber layer. However, this would increase material costs and necessitate longer carrier diffusion lengths in order for the resulting photo-generated carriers to reach the p-n junction for charge separation. Instead, increasing light absorption in a thin absorber layer can be achieved by increasing the optical path length and the number of passes the light makes through the absorber layer. This can be achieved by introducing a back surface reflector, using texturing of the front and back surfaces to scatter the light through the absorber layer at oblique angles and increasing the total internal reflection of light reflected from the back surface at the air-silicon interface.

3.3.1 Back surface reflectors

The optical path length can be increased through the absorber layer simply by creating a reflector at the back of the solar cell so that weakly absorbed light is reflected from the back surface. A thin film of Al or Ag can be used for the metallistaion of the back surface, which can result in a significant increase in back surface reflectance. The reflectance can be further improved to >90% by the addition of a thin dielectric layer between the Si and the metal to reduce absorption losses in the metal layer. The dielectric layer also provides passivation of the rear surface of the cell against surface recombination. Further improvements to the back surface reflectance can be achieved by texturisation to increase total internal reflection, which will be discussed in more detail below [101, 102].

3.3.2 Increasing optical path length in absorber

Optical path length is affected by the application of light trapping techniques as it represents the length in which unabsorbed solar radiation travels in a solar cell before it can escape from it [103]. It is possible to increase the path length as a result of using

surface texturing to scatter light incident on the front surface of the cell through oblique angles in the absorber layer. With an increase in optical path length, absorption is increased according to the Beer-Lambert relation, $I = 10e^{-acl}$, and transmission losses are reduced. Equation 3.2 is used to calculate the optical path length in a material [104].

$$S = Ln \tag{3.2}$$

Where S is the optical path length , L is the distance through the absorbing medium and n is the refractive index. By texturing the front surface of the solar cell with structures which have dimensions on a comparable scale to the wavelength of the incoming light, the textured front surface effectively acts as a diffraction grating for the incoming light. The diffraction of normally incident light of wavelength λ on this grating is defined by the relation

$$m\lambda = dsin\theta \tag{3.3}$$

where m is the order of diffraction and d is the pitch of the texture pattern on the front surface of the cell and θ is the scattering angle at which destructive interface occurs, resulting in diffraction minima. As a result, normally incident light is diffracted through a series of diffraction angles θ, which increases the path length through the absorber layer.
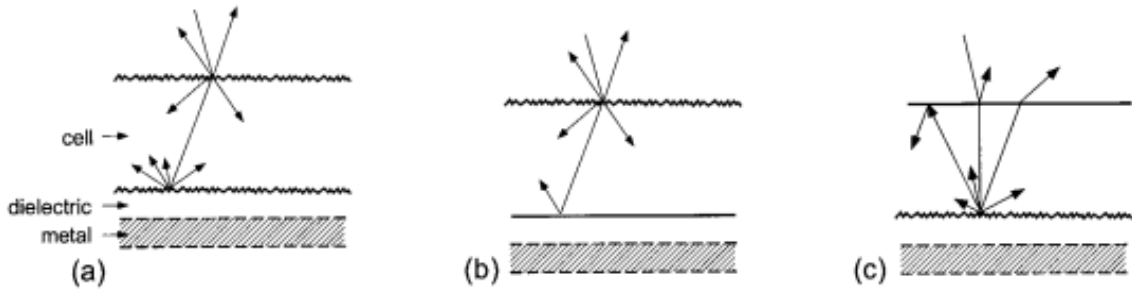
Figure 3.2: Use of different texture combinations in order to trap light and increase optical path length (a) Cell with a textured front surface, textured dielectric layer with a back surface reflector (b) Cell with a textured front surface, dielectric layer with no texture with a back surface reflector (c) Cell with no textured front surface, textured dielectric layer with a back surface reflector. Reproduced from [19].

3.3.3 Increasing total internal reflection

By texturing the front and rear surface of a solar cell, it will increase the number of passes that the light makes through the absorber layer by increasing the total internal reflection at each textured interface. As defined by Snell's law, the critical angle for the total internal reflection at the Si-air interface is 13.4°, while for glass-Si interface is 20.4°. This means that light incident at an angle greater than the critical angle will be reflected from the interface. This can be readily achieved by texturing the interface such that light will be obliquely incident on the surface facets of the texture structures at angles exceeding the critical angle of the interface. As a result, light transmitted through the solar cell is largely reflected from both the front and rear surfaces of the cell, trapping it within the absorber layer until it is fully absorbed. Only a small cone of light, defined by the critical angle, will be transmitted and lost with each pass. In relation to BSR, effectively using the dielectric interlayers between the BSR and the semiconductor interface can increase the total internal reflection [105]. The light which was weakly absorbed initially can be increasingly absorbed once the reflection at the back contact is high.

3.4 Conclusion

Based on light trapping theory, applying a surface texturing technique aids in reducing surface reflectance and transmission losses within the solar cell. As outlined above, pitch and angles of the surface structures produced during the texturing process are important parameters which affect the effectiveness of reducing surface reflectance and increasing light trapping. Therefore, it is vital to have a comprehensive picture of these parameters for the structure produced by the ADE process. To this end, the surface textures produced under different etch conditions and for different wafer orientations have been characterised using a combination of reflectance measurements, scanning electron microscopy and atomic force microscopy. A brief summary of the techniques and methodology is presented in the next chapter.

4 Experimental techniques

4.1 Methodology

In this thesis, the aim was to achieve a low surface reflectance from textured Si-wafer based solar cells using a novel atmospheric dry etch process. Two etching methods are available with the ADE tool, static and dynamic etching. Static etching has the Si wafer stationary under the gas nozzle whereas dynamic etching moves the Si wafer through the reaction chamber. Surface characteristics such as surface roughness and exposed surface area will be important data. The use of techniques to quantitatively characterise surface reflectance and surface morphology are key in obtaining the optimum process to achieve low surface reflectance. These characteristics will be compared for ADE textured surfaces with control wafers of different orientations, namely (100), (110) and (111), that have not been etched and therefore exhibit negligible surface roughness and high reflectance. Therefore, a spectrometer with an integrating sphere will be used in order to determine surface reflectance and a combination of atomic force microscopy (AFM) and scanning electron microscopy (SEM) has been used in order to determine surface morphology. The AFM data has been analysed using the open source software package Gwyddion [22] to understand the surface characteristics of each sample. ImageJ [106] was also be used in order to determine feature shapes which are unique for particular orientations.

4.2 Solar cell surface reflectance

In order to determine the surface reflectance of the etched Si wafers, a spectrometer with a reflectance sphere, light source and calibration standard is used.

4.2.1 Spectrometer

A Flame-S-UV-VIS-ES spectrometer, HL-2000-HP light source, RSA-FO-150 Reflectance Sphere and Labsphere SRS-99-010 Reflectance Calibration Standard from Ocean Optics were used in to order to obtain reflectance values for the etched surfaces. OceanView software was used to record the spectral reflectance output, with a wavelength range of 200 nm to 850 nm based on the spectrometer wavelength range. The spectrometer operates by using a reflectance standard in order to measure the detected light intensity when the light source is on or off within the sphere to calibrate. After this calibration, the sample can then be placed under the integrated/reflectance sphere and the light source will be directed towards the sample underneath the sphere in order to establish the surface reflectance. This data can then be viewed using OceanView software both in graph and table form. An overview of the spectrometer setup can be seen in figure 4.1.
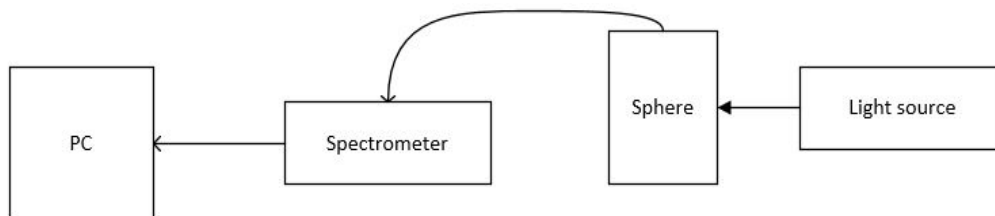
Figure 4.1: Spectrometer setup consisting of a HL-2000-HP light source with wavelength range of 360 nm - 2400 nm, RSA-FO-150 Reflectance Sphere, Flame-S-UV-VIS-ES spectrometer and a PC with OceanView installed.

The role of the integration sphere is to take in the light which has been reflected from the surface of the sample and is guided into the sphere, which is coated by a highly reflective material and its geometry allows any light entering to undergo multiple reflections until it enters the collection port connected to the spectrometer by an optical

fibre. This light will be used to determine the reflectance, based on the initial setup using the reflectance standard with a light source and no light source. The reflectance is calculated from the data obtained from the spectrometer, using the following equation

$$R(\lambda) = \frac{(S(\lambda) - B_0(\lambda))}{(B_{100}(\lambda) - B_0(\lambda))} C(\lambda) \tag{4.1}$$

Where $R(\lambda)$ is the calculated reflectance, $S(\lambda)$ is the sample scan, $B_0(\lambda)$ is the dark scan, $B_{100}(\lambda)$ is the blank scan and $C(\lambda)$ is the data in relation to the reflectance calibration standard [20, 107]. The reflectance factor of the calibration standard is a wavelength-dependent instrumental factor that accounts for the transmissivity of light through the optical components of the spectrometer and the detector efficiency. It is calculated for the equipment as seen in Fig. 4.2, with the wavelength range of interest highlighted in the red box.
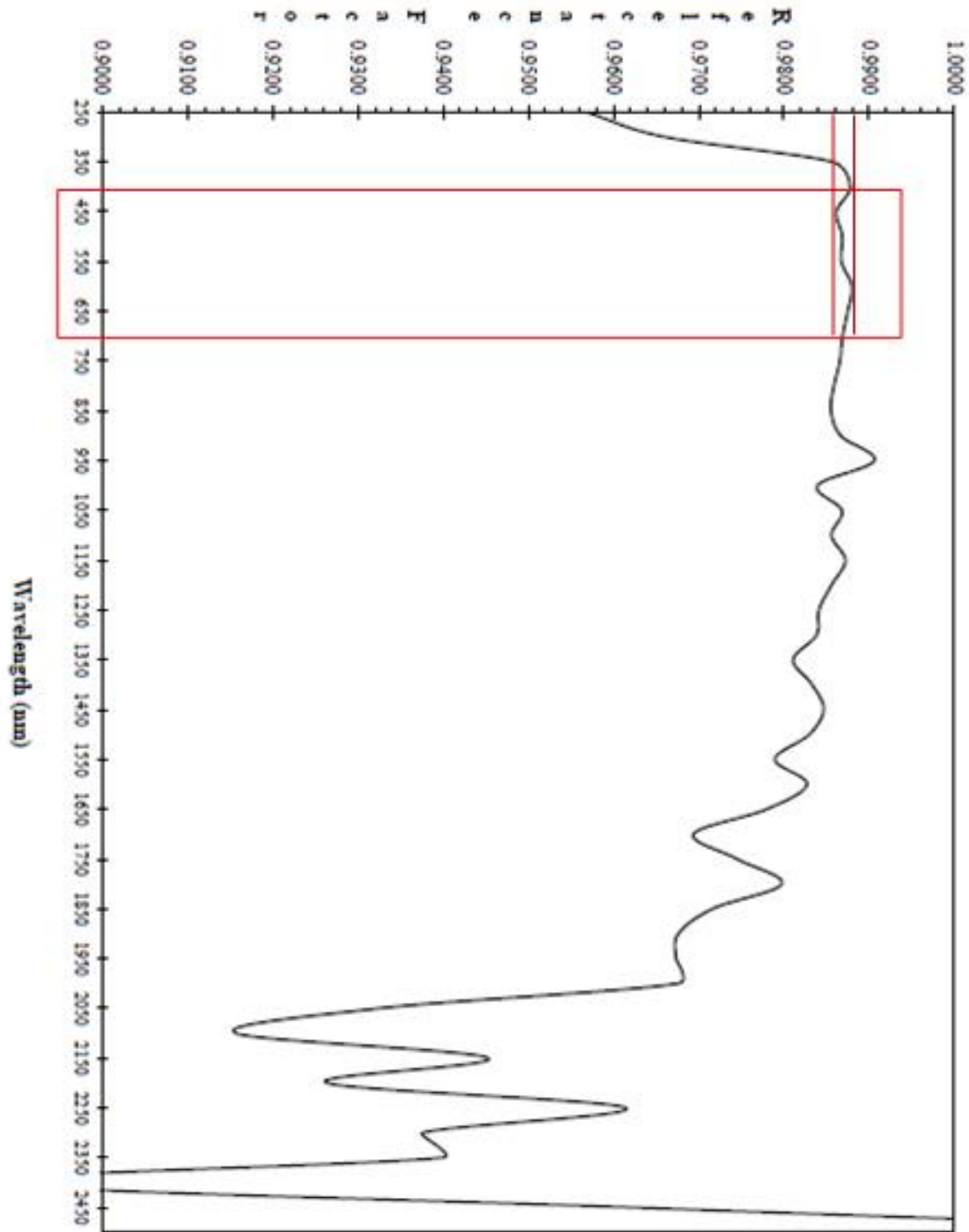
Figure 4.2: Reflectance factor of the calibration standard, which determines up to how much of the incident light is reflected from it. The wavelength range of interest has a reflectance factor between 0.986 and 0.988 [20]

4.3 Surface morphology

4.3.1 Scanning Electron Microscope

A Jeol JSM 6390 LV scanning electron microscope (SEM) and a Hitachi S2400 SEM were used in order to obtain images of the top down view of the surface morphology, with the Jeol JSM 6390 LV SEM being with primarily used. In SEM, a beam of energetic electrons, also known as primary electrons, is scanned across the sample surface in an evacuated chamber. The interaction between the primary electrons and the atoms of the sample generates different species with different energies, that have different probe depths, which will be picked up by the electron detector. It is worth noting that the secondary electron detector detects secondary electrons (SE) which are ionisation products that occur when a primary beam electron from the SEM column collides with an electron orbiting an atom inside the sample, causing it to be ejected from the sample. They have low energies (<50 eV) and, as a result, come from a region near the specimen surface (5-50 nm). SE images provide topographic information about the specimen. Primary beam electrons which have been scattered through Coulombic interaction with the nuclei of the atoms inside the specimen are backscattered electrons. These can be scattered multiple times, which means that they can be spread out before they are scattered back out of the sample surface. They can be elastically or inelastically scattered so that their energy ranges up to the primary beam range. As a result, they can come from much deeper in the sample, up to 1 μm, compared to SE and have a lower surface sensitivity and resolution. The BS electron yield is strongly dependent on the atomic number of the atoms inn the sample so that BS images offer compositional contrast as well as topographic contrast, which depends on the detector configuration. The electron detector processes the electrons that come back and then the software produces a two dimensional grey-scale image of the surface. The schematic of a SEM can be seen in figure 4.3.
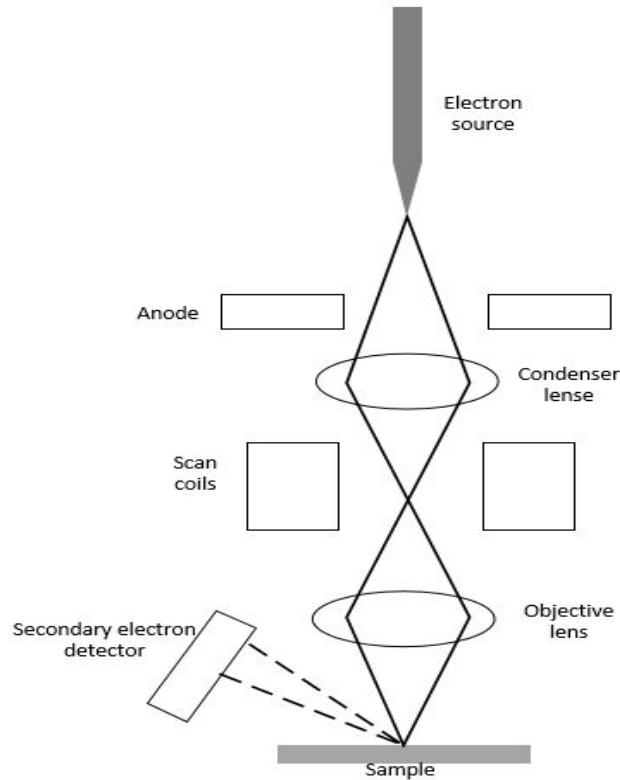
Figure 4.3: Basic SEM operation where electrons are emitted from the electron source and passed through the anode to accelerating the electron beam. Several lenses to form a focused beam of electrons onto the surface of the sample. Coils allow for the electron bean to scan across the surface.

The SEM column comprises of a hairpin filament for thermionic emission of electrons, a Wehnelt cylinder which shapes the electron beam, an anode to accelerate the electrons to higher energies, a spray aperture removes off-axis electrons, condenser lenses to demagnify the electron beam, an adjustable objective aperture to control probe current and spot size on the sample, scan coils to raster the electron beam across the surface of the sample, stigmators to correct for astigmatism and an objective lens to focus the electron beam in the sample. In order to detect secondary electrons, an off-axis Everhardt-Thornly detector is used which located on one side of the column. This uses a positively-biased collector grid to deflect the SE into the detector. Backscattered electrons are collected by the annular detector located directly beneath the end of the SEM column. The detector is divided into quadrants, where summing the detected signal from all quadrants provides BS images showing compositional

contrast, while taking the difference in signal from a pair of opposing quadrants is used to produce a topographic image. Before the sample can be placed into the SEM and imaged, it needs to be prepared accordingly. The sample is cleaved and is no bigger in size than the sample stub on which it will be mounted. The stub are made from aluminium in order to provide an electrical path to ground. The sample is kept in place with a double sided conductive adhesive pad on the bottom, between itself and the sample stub. The front surface of the sample can be coated with a thin layer of either sputter-deposited gold, which gives a good secondary electron yield or thermally-evaporated carbon, which has a low atomic number and is useful for backscattered electron imaging with compositional contrast. Metal deposition is needed to making non-conducting samples electrically conducting by depositing a thin conducting film on the sample. This is carried out as a non-conducting sample would charge up and prevent imaging. A strip of Al conductive tape is then used in order to provide the sample an electrical path ground. Once this is complete, the sample stub can be placed into the sample holder once the sample chamber has been vented. Once the sample is mounted and placed in the sample holder and the camera has been aligned, the opening to insert the sample into the SEM is closed and the chamber is evacuated to a pressure of 10^{-6} mbar. It is possible to obtain top down and side profiles of the sample based on how the sample is mounted onto the sample stub and the tilt angle of the sample stage.

4.3.2 Atomic force microscopy

An Agilent Technologies 5500 Atomic force microscope (AFM) is used in to order to obtain topographical information for the surface morphology of the etched silicon (Si). In atomic force microscopy, a sharp tip is connected to a microfabricated Si cantilever which is rastered across the sample surface. Minute forces of less than 10^{-9} N occur between the tip and the sample. Repulsive and attractive interatomic forces between the sample and the tip cause deflection of the cantilever, which is registered by laser which is aimed at the tip of the cantilever. The laser beam will then be reflected and is

detected by a photodiode. The photodiode is divider into quadrants in order to measure the up and down movement of the cantilever as the tip travels over bumps and hollows of the surface. This also provides information on the lateral bending of the cantilever due to frictional forces as the tip is rastered across the surface. Intensity changes of the voltage signal collected from each quadrant can be used to measure cantilever displacement in a given direction. Distance between the sample and the tip is controlled by a feedback loop which is adjusts the separation between the two in order to maintain a constant value for the setpoint deflection. Topographical information using PicoView. Further information about the surface characteristics will be investigated using Gwyddion. Two modes can be used to image with the AFM, which have been used in this thesis; contact mode and AC tapping mode. Contact mode uses lateral force as the tip is continuously in contact with the surface of the sample. A laser is pointed towards the cantilever tip and is reflected back into the photodetector, which consists of four quadrants, that will control the force of which the cantilever will press against the surface. Before the scan begins, the scan size, x location, y location and points/lines are selected and can not be changed during whereas scan speed, I gain and P gain can be changed. The topographic image is produced by the feedback control of the cantilever deflection of the photodetector. The operation of contact mode can be seen in figure 4.4.
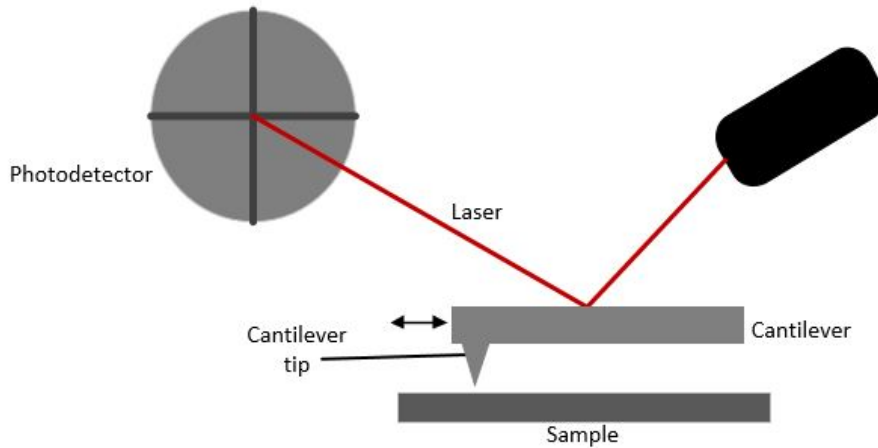
Figure 4.4: AFM contact mode operation. The laser hits the cantilever, which is moving laterally across the surface of the sample. The laser is deflected from the cantilever into the photodetector.

AC tapping mode, which was most commonly used in this thesis, moves the tip across just above the sample while moving the cantilever up and down in a tapping motion, making intermittent contact with the surface. When the cantilever is placed into the AFM, the resonant frequency is determined using the scanning software. The frequency range used to determine the resonant frequency is supplied with the cantilever. As with contact mode, a laser hits the cantilever tip and gets directed into the photodetector. As with contact mode, the scan size, x location, y location and points/lines are selected and can not be changed during the scan whereas scan speed, I gain and P gain can be changed. The topology image in tapping mode is based on the oscillation amplitude setpoint. The feedback loop controls the distance between the tip and the sample and the separation between the two is maintained in order to maintain a constant setpoint value of the amplitude oscillation. The topographic image is produced by the applied voltage to the scanner z-piezo. A phase image is also produced which is based on the phase difference between the drive piezo and the detected signal. A phase shift is produced due to sample indentation by the tip, providing information on local variations in sample elasticity or due to tip adhesion to the sample.

The operation of the AFM in AC tapping mode can be seen in figure 4.5.
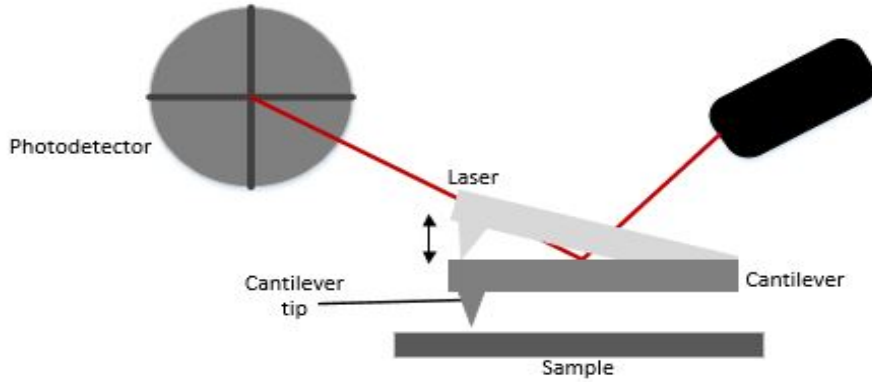
Figure 4.5: AFM tapping mode operation. The laser hits the cantilever and is reflected into the photodetector. The cantilever tip moves up and down, making intermittent contact with the surface of the sample.

Different cantilevers are used for the two modes, both manufactured by Nanosensors. The contact mode (PPP-CONTR) cantilevers are typically soft, with a nominal spring constant of k = 0.2 N/m. This allows for subtle changes in the repulsive force between the sample and the cantilever tip to be determined. Whereas, the tapping mode cantilevers (PPP-NCHR) are more stiffer than its contact counterpart, with a nominal spring constant of k = 42 N/m and resonant frequency range of 204 kHz - 497 kHz. The contact and tapping mode cantilevers can be seen in figure 4.6 and 4.7.
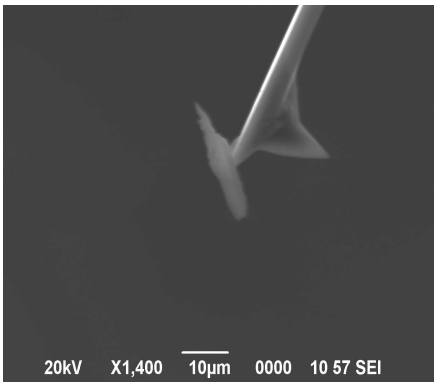
Figure 4.6: SEM image of the cantilever used for AFM contact mode
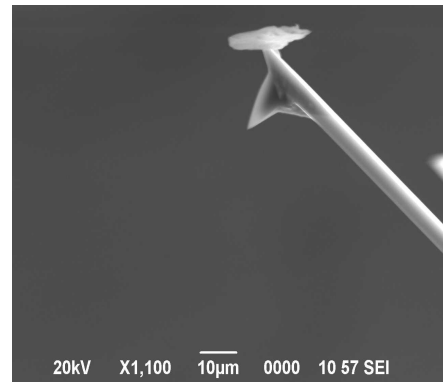
Figure 4.7: SEM image of the cantilever used for AFM tapping mode

Information such as surface area, mean surface roughness, skewness and kurtosis can be obtained in order to analyse the characteristics of the surface texture produced by

the ADE process.

4.3.2.1 Tip convolution

One issue which needs to be considered while using AFM is tip convolution. Tip convolution occurs when the structure being scanned is comparable in size to the tip itself [21]. In effect, the surface images the shape of the tip at the same time as the tip is imaging the shape of the surface. As a result, the shape of the structure is not adequately measured and results in structures being perceived as larger. Figure 4.8 shows this effect using different tips. This can affect the surface area and mean surface roughness data obtained from the AFM measurements. In principle, it is possible to deconvolve the shape of the AFM tip from the recorded image in order to get a true representation of the surface topography. This requires a good knowledge of the exact tip geometry for every recorded image, which may be determined by SEM analysis or by deconvolution of test images on well-defined geometrical structures. However, this is a time consuming process and was not carried out in the present work.
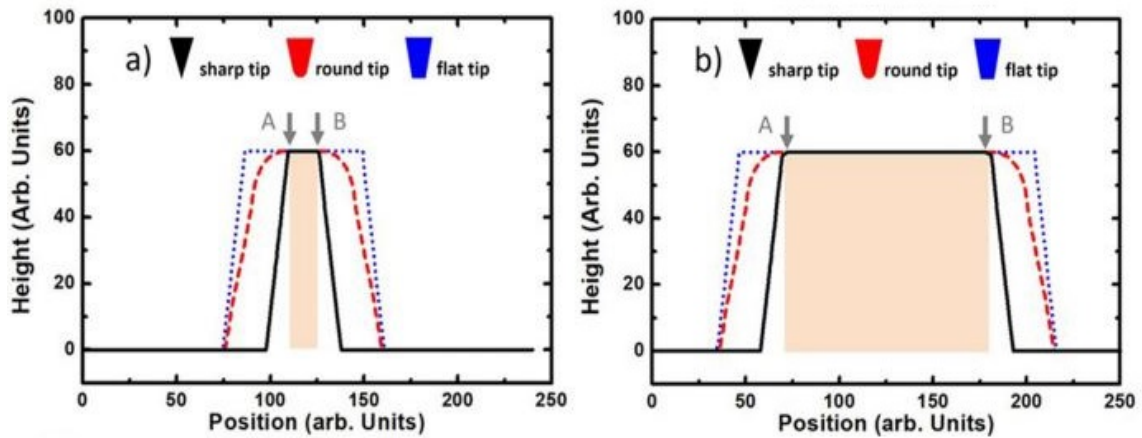
Figure 4.8: Examples of tip convolution using different tips. (a) shows a narrow rectangular object being scanned whereas (b) shows a broad rectangular object being scanned. The sharp tip (black continuous line) provides the closest in shape however tip convolution occurs. The sharp tip is followed by the round tip (red dashed line) then the flat tip (blue dotted line) Reproduced from [21].

4.4 Processing samples

Some samples were put through a cleaning process before entering the ADE tool. Application of cleaning processes are implemented in order to remove any impurities which may be on the surface of the wafers. Cleaning is carried out before the etching phase occurs. The cleanings methods which were implemented include a hydrofluoric (HF) dip, partial RCA clean and full RCA clean. This was carried out with some of the Si wafers in order to determine the effect cleaning has on the subsequent dry etching process.

4.4.1 Partial RCA

The partial RCA consists of a RCA1 clean, whose mixture consists of 5 parts by volume of deionized (DI) water, 1 part hydrogen peroxide (H_2O_2) and 1 part ammonium hydroxide (NH_4OH). The wafers are immersed in this solution at 80°C. RCA1 is used in order to remove organic residue from the surface of the wafer. The Si wafer is placed into the RCA1 solution for 20 to 30 minutes, rinsed with DI water then dried using compressed nitrogen (N_2).

4.4.2 Full RCA

This consists of a RCA1 washed followed by a RCA2 wash. The RCA2 mixture consists of 6 parts DI water, 1 part hydrogen peroxide (H_2O_2) and 1 part hydrochloric acid (HCL). RCA2 is used in order to remove metal ions from the Si surface. As with the partial RCA, the solution is also held at 80°C when the wafers are placed into it. The Si wafer is placed into the RCA2 solution for 20 to 30 minutes, rinsed with DI water and dried using N_2.

4.4.3 HF dip

Samples which were cleaned using the partial RCA and full RCA also were subjected to a HF dip. The HF dip solution consists of 480ml DI water and 20ml HF acid and

is used in order to remove native oxides from the surface of the wafer. This is carried out at room temperature. The Si wafer is placed into the solution for 1 to 2 minutes, followed by a rinse using DI water and dried using N_2.

4.4.4 Subsequent steps

Samples were initially tested using the spectrometer as the wafer had not been cleaved, with several measurements taken for each sample over different regions of each wafer. With several measurements, the average etching across the wafer could be determined. Once each sample has been tested for surface reflectance, each sample was cleaved and blown with dry nitrogen (N_2) to remove any debris from cleaving. The samples were examined at using AFM, looking at different areas of the surface. As different areas were looked at, it can be theorised further the amount of etching which has occurred on the surface. A scan sizes of 80 μm was used in order to determine surface characteristics. Smaller scan sizes were used to examine the topology of individual etch pit structures and etch pits, allowing for analysis for different orientations. SEM analysis was used to provide insight to the surface etching as well, including etch density and etch pit structures for specific orientations.

5 Results and discussion

5.1 Introduction

Si wafers with different orientations, (100), (110) and (111), were etched using the ADE technique with different etch parameters, using either dynamic or static etching (i.e. where the Si wafer was placed on the conveyor belt and remained in one position or moved through the chamber with a constant velocity) and employing different wafer pre-cleaning processes. Polished wafers for each orientation, which had not been put through the dry etching process, were also tested for surface reflectance in order to obtain reference reflectance values. This allows for any improvements in surface reflectance due to the dry etching process to be seen.

5.2 Etch parameters

In order to determine the optimum etching process parameters, several Si wafers were dry etched to produce a low surface reflectance. The samples were etched using the ADE tool while varying process parameters such as belt velocity [68] or etch time, and whether a preliminary cleaning process was carried out. The etch process is also dependent on F_2 concentration (typical gas flow rates used were 5 slm F_2 with 2 slm N_2), wafer temperature (200 °C) and gas diffusion plate (GDP) temperature (200 °C). However, these parameters were not varied during this study as they have been investigated in detail elsewhere [68]. The variations in process parameters resulted in different surface morphologies, which affected the surface reflectance. As mentioned earlier, both static

and dynamic etching were preformed. Belt velocity is used as a measure of etching duration for dynamic etching as the samples moves through the ADE tool whereas etch time is used for static etching as the samples stay in one position.

Crystal orientation

With mono-Si, the wafer surface can be terminated by one of several crystal orientations. The crystal orientation is determined by the crystallographic direction along which the Si ingot is sliced during the Czochralski process. This is most easily achieved for wafers terminated by the (100) surface, which are most commonly used in microelectronics. However, (110) and (111) wafers can also be produced, but at a greater cost. The static etching experiments were performed with (100)-oriented Si wafers, while dynamic etching experiments were implemented with different wafer orientations, (100), (110) and (111), in order to determine the influence of the crystallographic termination on the dry etching process. Fig. 5.1 shows the surface reflectance results of the three orientations plotted against etch time with the values for the unetched reference samples shown at 0 seconds. Error bars and mean values are used throughout the results, to express the variation in reflectance values measured over different regions of each wafer. This variation in surface reflectance arises due to the inhomogeneity of the etching process which was not uniform across each wafer. This non-uniform etching may be due to these experiments being carried out using 3" wafers, rather than the 6" wafers that the tool is designed to work with. As suction holes are used to keep the wafers in place, the 3" wafers cover less of these holes which might result in turbulent flow of the etchant gas across the surface of the Si wafer. It is also worth noting that the 3" wafers are also at least 100 μm thicker than is normally used for the tool, it is possible that the Si wafers are not achieving a high enough temperature as they were moved through the reaction chamber due to thermal lag.
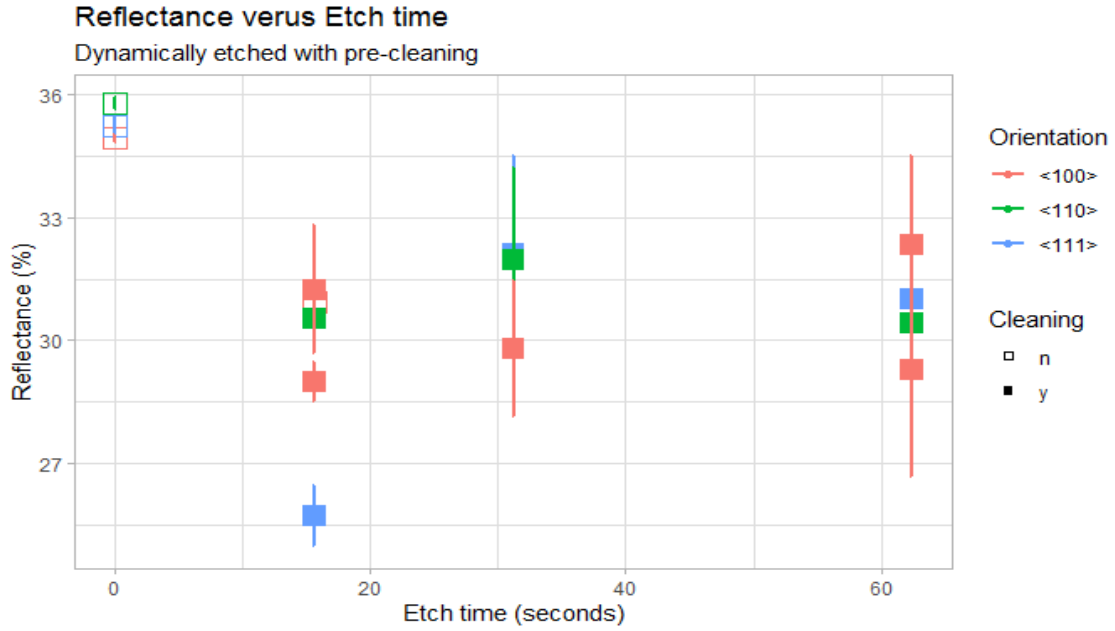
Figure 5.1: Surface reflectance plotted against dynamically etched Si samples with different orientations and etch times. Error bars represent the variance in surface reflectance measured across each wafer. Values shown at 0 secs are for polished wafers that have not been cleaned or etched.

It is worth noting that the dynamic etching conditions did not result in a significant reduction in surface reflectance. This is likely the result of thicker wafers being used and the wafers achieving a lower than expected temperature in the reaction chamber. The surface reflectance values for the samples which were etched at 31.2 and 62.4 seconds do not differ greatly, as the largest difference achieved for the (100)-oriented wafers is ~3%. It is also worth observing that in the case of the 15.6 second etched samples, that the (111) sample achieved the lowest surface reflectance. All orientations show roughening which leads to a reduced surface reflectance. Based on the data, it is difficult to determine if the etch rate varies for different orientations. As the surface reflectance does not vary much for etch times greater than 15.6 seconds, the etching process can be considered to occur most rapidly with a large amount of material being removed in the initial 15 seconds. Further etching appears not to cause a significant change in the overall surface roughness. However, the data in Fig. 5.7 shows that there is some increase. In order to determine if the etch rate for different orientations does vary as a result of the ADE

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process, it would be vital to either reduce the etch time, reduce the F_2 concentration or lower the etch temperature.

ADE process time

As discussed previously, the ADE process makes use of F radicals in order to etch the surface of the Si wafer. Several etch parameters can be changed in order to optimise the process such as fluorine gas concentration and wafer temperature. However, for the purposes of these experiments, a focus was placed on investigating the effects of etch time on surface reflectance and texture. In Fig. 5.2, shown below, all parameters except the etch time and use of a pre-cleaning step are unchanged.
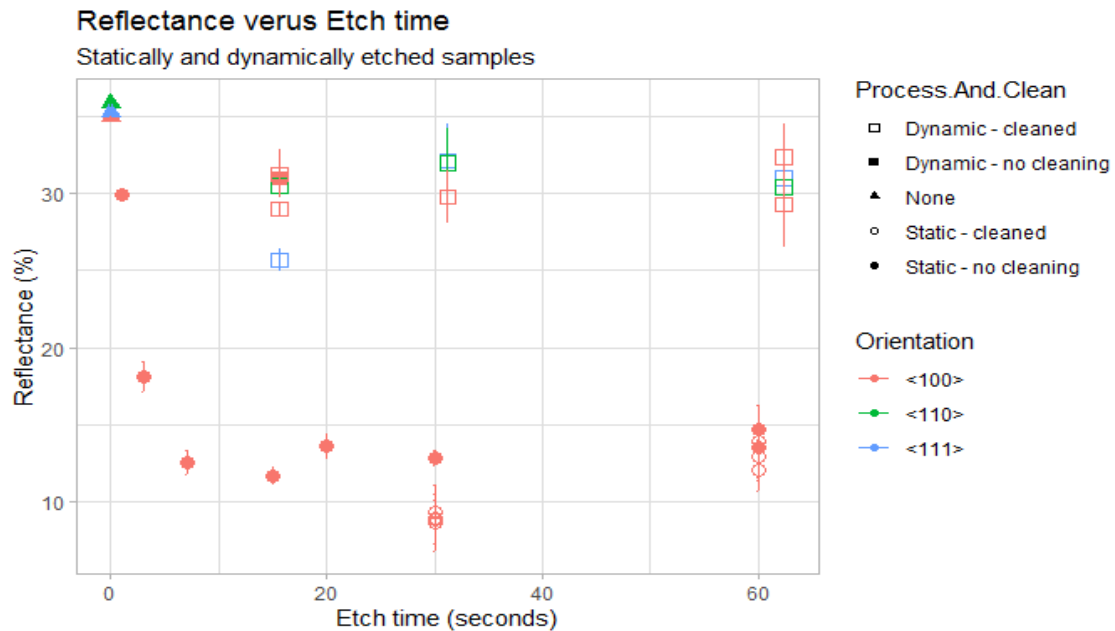
Figure 5.2: Surface reflectance plotted against etch time for all samples with orientation, process and cleaning represented by colour, shape and lines respectively. Samples with an etch time of 0 seconds refer to unetched, polished wafers.

Samples which were put through the static process achieved substantially lower surface reflectance values compared to the samples which were underwent the dynamic process. This could be the result of the wafers remaining under the nozzle in the case of static samples, the use of smaller wafers for the dynamic process and/or the temperature of

the wafer. During either process the wafer may have reached thermal equilibrium for static etching whereas the transient temperature of the dynamically etched wafer was lower due to thermal lag. It is worth noting that 3" wafers were used instead of 6" rectangular mc-Si wafers for which the tool is designed. It was found that 6" c-Si wafers with different orientations were too expensive to purchase. Given the wafer is held onto the conveyor by suction holes, it is possible that by using smaller diameter wafers than would normally be used, the etchant gas could be removed before it could interact with the Si wafer surface. The wafer thickness could also have an effect as the wafers used are at least 100 μm thicker than the wafers the tool is designed for. This would increase the thermal mass of the wafer, reducing the heating rate and therefore slowing the reaction rate between the etchant gas and the Si surface.

Pre-cleaning

Pre-cleaning of Si wafers is used to remove any potential defects or residues on the surface, which includes organic residues, metal ions and native oxides. Several wafers investigated underwent pre-cleaning before the ADE process, while others did not. A HF dip, partial RCA (involving removal of organics) or full RCA (involving removal of organics and metal ions) was used for each of the etched samples with pre-cleaning for the 30 and 60 second samples. Fig. 5.3 plots the data shown in Fig. 5.2 for the statically etched samples alone to show the effects of samples being pre-cleaned in comparison to samples with no pre-cleaning.
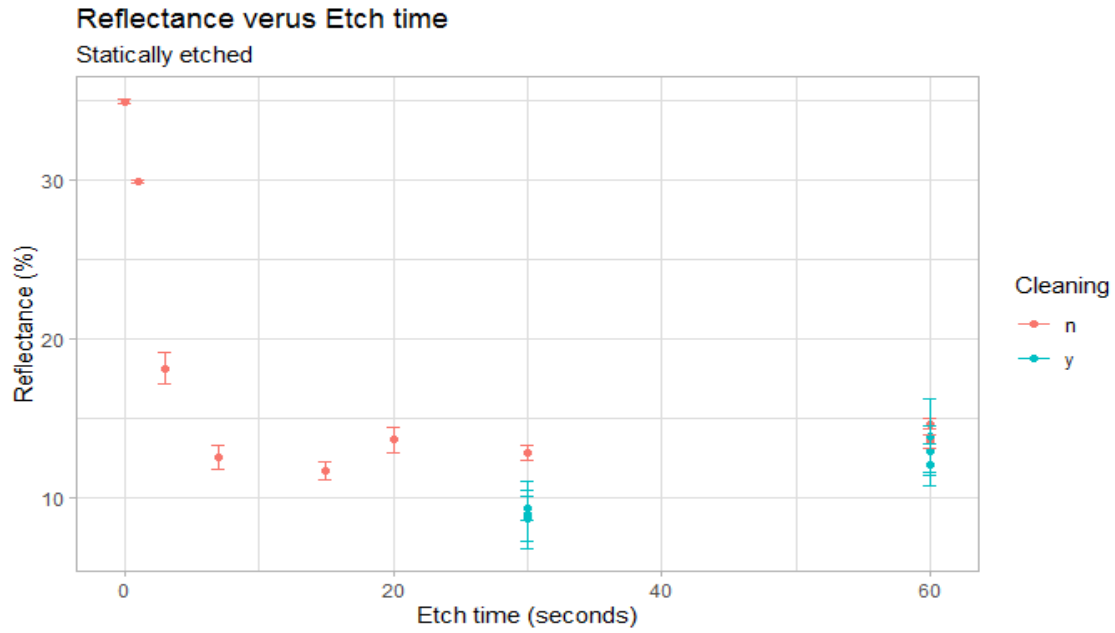
Figure 5.3: Surface reflectance plotted against etch time for statically etched (100) wafers with and without a pre-cleaning step. Reflectance values for unetched, polished samples are shown at 0 seconds for reference

With the use of pre-cleaning, there is a notable surface reflectance difference between the two sets of samples which have been etched for 30 seconds. However, for the samples which have been etched for 60 seconds, there is no noticeable difference between the wafers which have been pre-cleaned and those which have not been pre-cleaned. From this, it can be considered that use of pre-cleaning may benefit certain etch times. For dynamically etched samples, as pre-cleaning was used for the majority of the samples, the impact of pre-cleaning can not be determined.

5.3 Dynamic etch

A dynamic etch was carried out by placing a Si wafer onto the conveyor belt and passing it through the reaction chamber at a certain belt velocity. The etch times quoted here for dynamic etching were calculated by dividing the belt length by the belt velocity. The belt velocities used were 2.5, 5 and 10 mm/s. The results were examined by commencing with surface reflectance plotted against etch time, as shown previously in Fig. 5.1. As

the variation in surface reflectance of the samples with different pre-cleaning processes was minimal in Fig. 5.3, a HF dip was used as the pre-cleaning process. Using the unetched polished samples as a reference, it can be seen that the surface reflectance is improved regardless of how long the samples were etched. For the samples which were etched for 15.6 seconds, the (111) sample achieved the lowest surface reflectance without any error bar overlap. For wafers etched for 31.2 seconds, the (100) sample achieved the lowest mean surface reflectance for that set. The last etch time of 62.4 seconds, shows a wide variation in reflectance values with the error bars overlapping with each other. Two different (100) wafers were etched for this period, with a reflectance difference of approximately 3%. This variation in results may be due to the wafer not being the optimal size for the tool and the etchant gas not interacting uniformly with the surface. The surface reflectance dips at 15.6 seconds before increasing slightly for the longer etch times. This may be the result of the structure being somewhat more comparable in size to the wavelength of light when compared to the surface structures of the wafers etched for longer.

5.3.1 AFM images

AFM files were processed using Gwyddion [22] to obtain line profiles, surface roughness parameters and surface topography. Fig. 5.4 shows the surface topography with line profiles for three wafers with different crystallographic orientations which were dynamically etched for 15.6 seconds.
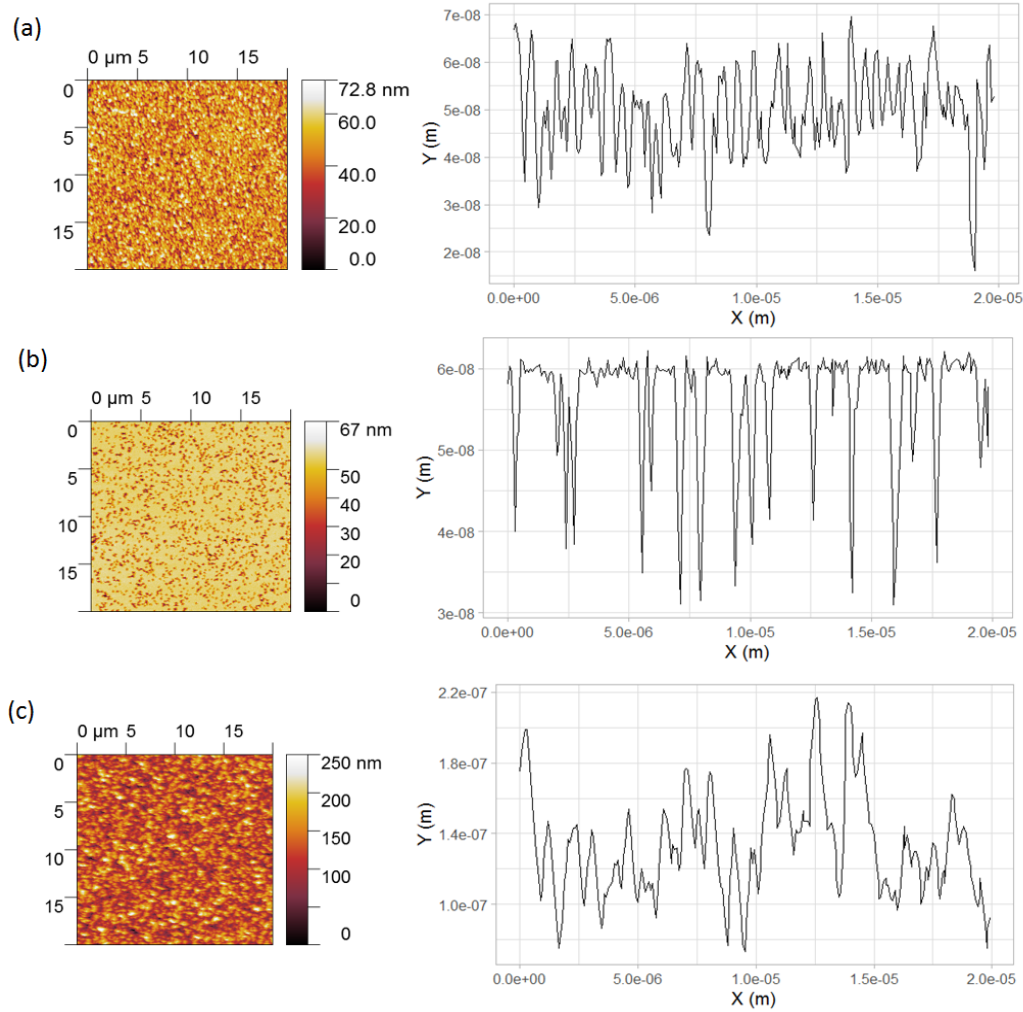
Figure 5.4: AFM topography images and line profiles for dynamically etched samples with an etch time of 15.6 seconds, obtained using Gwyddion [22] (a) (100) sample, reflectance of 30.92% (b) (110) sample, reflectance of 30.52% (c) (111) sample, reflectance of 25.7%

The (110) surface appears to have just started to be etched as the polished surface is present along with some etch pits. The (100) surface presents a more etched surface, which is slightly rough with peaks and pits. The (111) orientation has a rough surface with noticeable surface structures based on the topography image. The height variation between the highest peak and lowest valley for each of the wafers is 50 nm for (100), 30 nm for (110) and 110nm for (111). It is worth noting that the etching was not uniform across the surface of the wafers, possibly due to etchant gas distribution and or due to wafer temperature variations. This nonuniform etching can be seen in Fig. 5.5
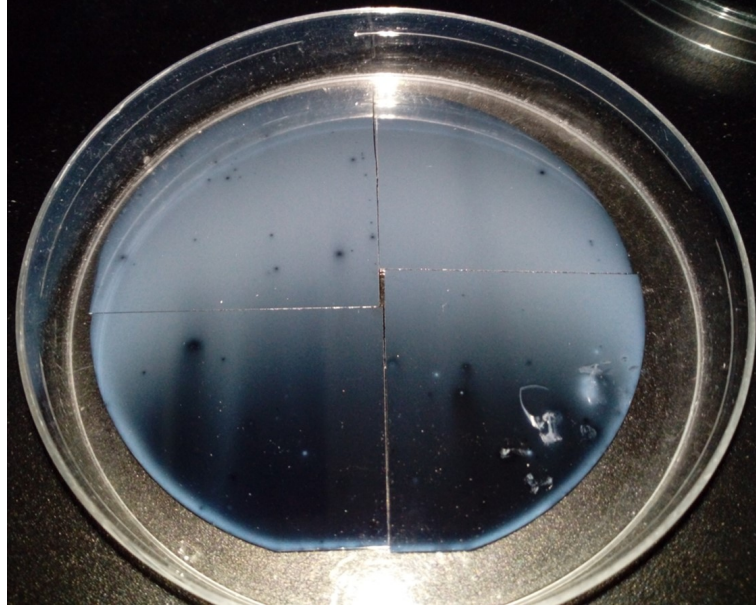
Figure 5.5: Dynamically etched wafer with nonuniform etching across the wafer surface which achieved a mean surface reflectance of 28.98%

5.3.2 Surface characteristics

The use of different surface characteristics were investigated in order to obtain a better understanding of the effect the etching has on the surface. The first characteristic to be examined is surface area increase, which is shown in Fig. 5.6, which was determined by the following equation:

$$\frac{measured \ surface \ area - calculated \ planar \ surface \ area}{calculated \ planar \ surface \ area} x100 \tag{5.1}$$

Where the calculated planar surface area is 6400 μm^2 based on a 80 μm x 80 μm scan of a flat polished Si surface. The measured surface area was determined by AFM data and measures the increased surface area resulting from surface roughing along the surface normal.
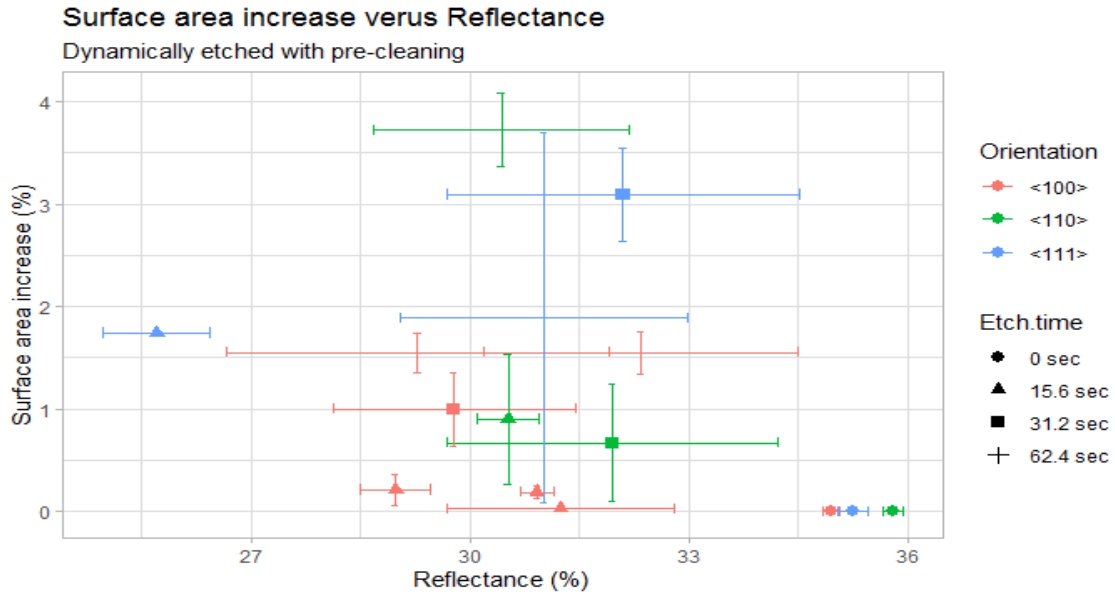
Figure 5.6: Surface reflectance plotted against surface area increase for the dynamic samples, with error bars for both reflectance and surface area increase

Considering the samples which have been etched for 15.6 seconds, the (111) sample achieved the best surface reflectance corresponding to a surface area increase of 1.75%, which is also the highest obtained increase in surface area for the 15.6 second etched samples. The (100) samples follow a trend of a reduction in surface reflectance with a corresponding rise in surface area increase. For the 31.2 second etched samples, the highest achieved reflectance did attain the highest increase in surface area, which could be considered as unusual as it would be expected that the wafer with the lowest surface reflectance would obtain the highest surface area increase. For the 62.4 second etch, one (100) sample achieves the lowest surface reflectance despite not achieving the highest increase in surface area. With the (100) sample, presented along side the 31.2 second etched example and two of the 15.6 second etched (100) samples, the (100) follows the trend of the an increase in surface area leading to a reduction in surface reflectance. The (110) samples also follow this trend, with the highest surface reflectance having the lowest surface area increase and the lowest surface reflectance achieving the highest increase in surface area. However there are some exceptions to this trend. This could be due to the nonuniform surface and certain areas being less etched in comparison to other

areas on the surface since reflectance values were determined by averaging measurements made over several areas of each wafer. The surface reflectance may depend on more than just the roughness of the surface, such as the lateral separation between the peaks on the surface or the variation between peak height and valley depth. Fig. 5.7 shows the RMS roughness for the dynamically etched samples.
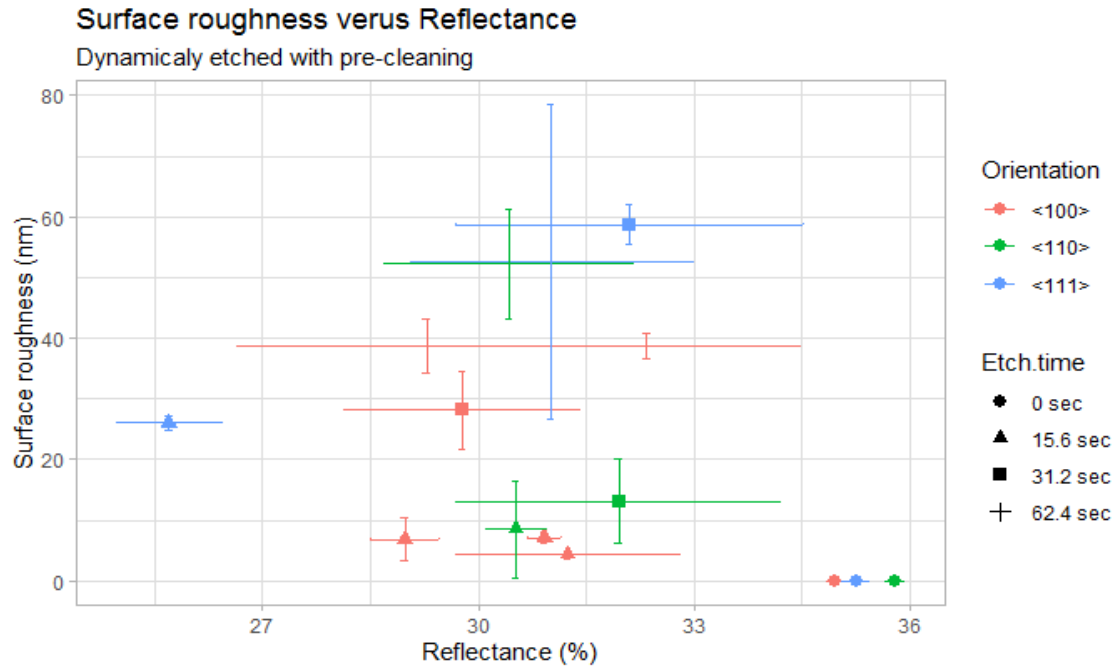
Figure 5.7: Surface reflectance plotted against RMS surface roughness for the dynamic samples

The roughness of the sample increases with an increased etch time. For the samples etched for 15.6 seconds, the highest measured roughness was achieved by the (111) sample with the lowest surface reflectance and largest increase in surface area. The (100) samples also follow a similar trend, as an increase in surface roughness corresponds to a reduction in surface reflectance. For the samples which have been etched for 31.2 seconds, the samples achieved a similar roughness result when compared to their increase in surface area. The highest surface roughness was achieved by the (111) sample, despite it having the highest mean surface reflectance. It can be seen however that similar reflectance values were achieved by samples which presented the roughest and least rough surfaces. It is worth noting that the measured roughness

parameters may not be completely reliable as they strongly depend on tip shape. For example, a blunter tip would smear out surface features and therefore reduce the measured surface roughness compared to the actual surface roughness value.

The last characteristic to be investigated is skewness, which represents where the structures are in relation to the mean surface plane. For example, a negative skewness value represents a pitted surface, a positive skewness value represents a peaked surface and a skewness value of 0 represents a symmetrical or distribution of peaks and valleys.
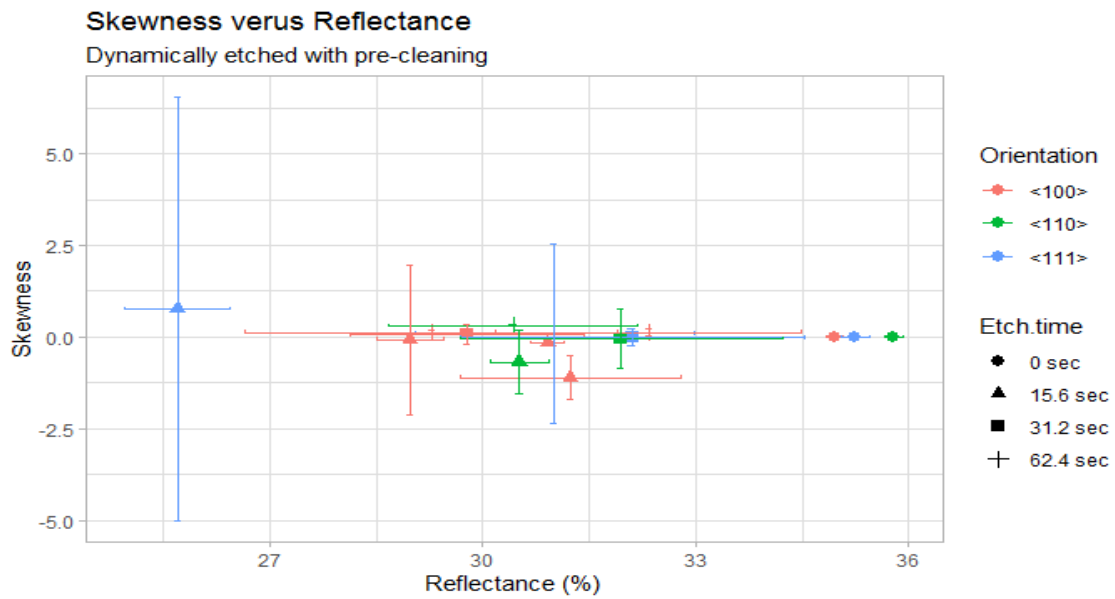
Figure 5.8: Surface reflectance plotted against skewness for the dynamic samples. Positive values indicate a predominantly peaked surface whereas negative values indicate a predominantly pitted surface

As etch pits are formed first during etching with some regions of polished surface between the pits, an etch time of 15.6 seconds provides a negative skew. With an increase in etch time, more pits are formed and will grow laterally removing any flat surface between each pit. The mean surface level is then shifted downwards, resulting in the remaining original surface to becoming peaks within the etched surface. Skewness indicates whether the surface is more pitted or peaked, with a negative value representing a pitted surface and a positive value representing a peaked surface. In most cases the measured samples have a combination of an equally peaked and pitted surface. However

there are three samples which vary from this, as follows:

- (111) with a surface reflectance of 25.7% has a majority peaked surface with some pits occurring. However this may be an outlier as it varies considerably in comparison to the other samples

- The (110) samples with a surface reflectance of 30.52% has a majority pitted surface with little to no peaks

- (100) with a surface reflectance of 31.24% with a completely pitted surface with no peaks

It could be said that the etching of the surface had just begun for samples with an etch time of 15.6 seconds, however this is more noticeable with the (110) sample. Based on these results, the etch time does not appear to have an impact on the surface reflectance of the (100) samples, with 15.6 seconds and 62.4 seconds producing the lowest surface reflectance for the (110) and a 15.6 second etch producing the lowest surface reflectance for (111). These reflectances, however, are not ideal as they are still considerably high. These values may be a result of wafers which were etched not reaching a sufficiently high temperature as they move through the etching chamber in order to obtain the desired etching rate. The difference in diameter and thickness of the wafers used in this study, compared to the optimal values specified for the etching tool, may have caused this temperature issue.

5.4 Static etch

Statically etched samples differ from the dynamically etched samples as the static samples remained immobile under the nozzle where the etchant gas is released. Wafers are loaded into the reaction chamber and the wafer temperature is increased to the desired value. The etching time corresponds to the interval during which F_2 gas is introduced into the etching chamber. Both pre-cleaned and non pre-cleaned wafers were etched in this fashion. As shown previously, Fig. 5.3 shows the surface reflectance

for statically etched samples with pre-cleaning occurring for a number of the samples. As etch time increases, there is a reduction in surface reflectance however it does not continuously reduce. Samples without pre-cleaning achieved varying reflectances, with a 15 second etch achieving 11.73%, a 30 second etch achieving 12.89% and a 60 second etch achieving 14.69%. This apparent increase in surface reflectance with time could be the result of the etching process as, for prolonged etch times, the etchant gas begins to remove the formed structures, resulting in the surface returning to a flatter state. For the samples with pre-cleaning, the lowest achieved reflectance was 8.67% which was achieved by a 30 second etch, with the surface reflectance of the two other samples being within 0.3% of this.

5.4.1 No pre-cleaning

With no pre-cleaning, Si wafers were placed into the reaction chamber of the ADE tool to be processed with varying etch times, comprising of 1, 3, 7, 15, 20, 30 and 60 seconds.

5.4.1.1 AFM images

Fig. 5.9 shows the AFM topography images and line profiles for samples with an etch time of 15, 30 and 60 seconds with no pre-cleaning. In order to view how the surface was etched, a 20 μm x 20 μm scan size was used in order to view several structures and obtain a line profile which shows this.
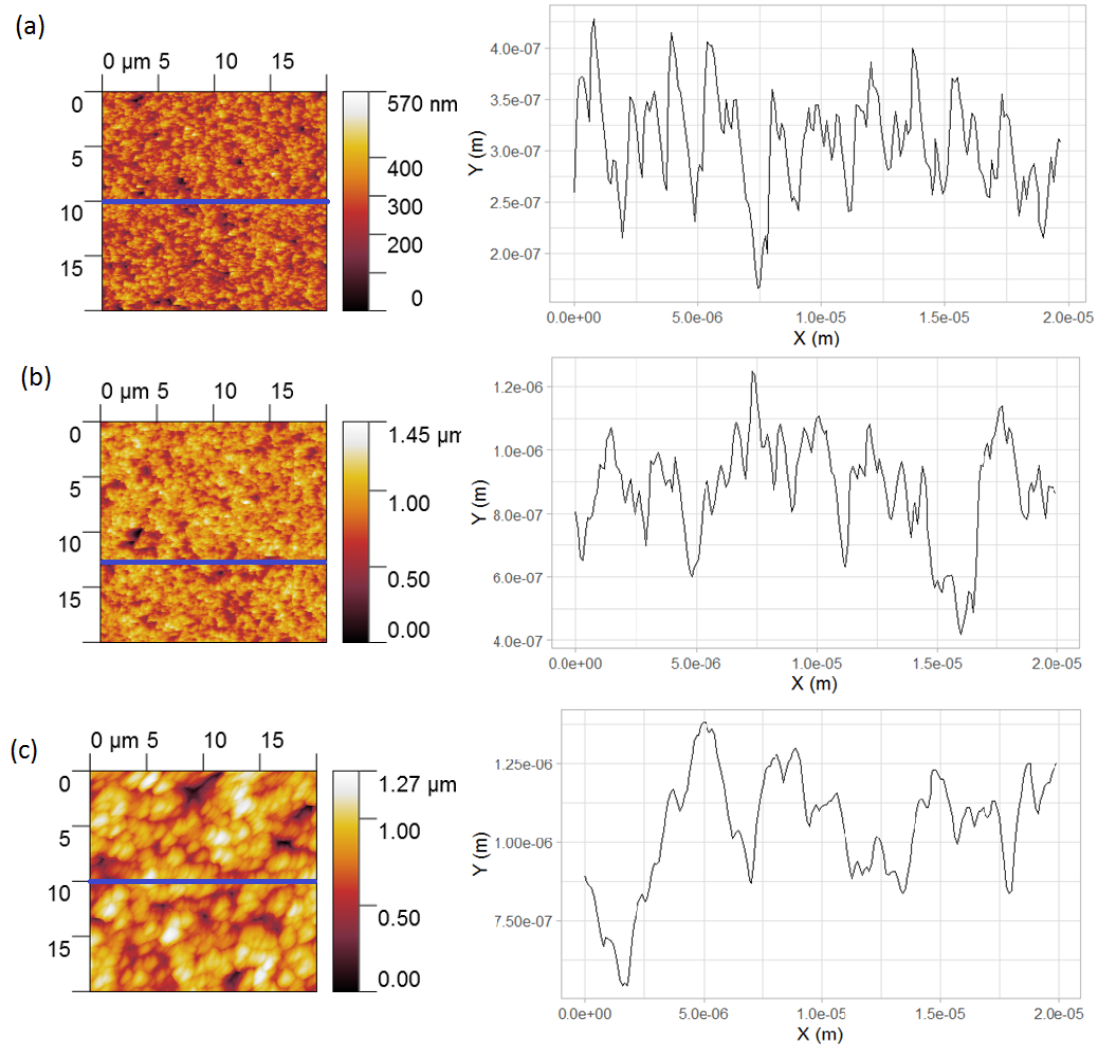
Figure 5.9: AFM topography images with a scan size of 40 μm and line profiles. The blue line on the topography image represents where the line profile was taken. (a) 15 second etch with a surface reflectance of 11.73% (b) 30 second etch with a surface reflectance of 12.89% (c) 60 second etch with a surface reflectance of 14.69%

From the line profiles, the structures achieved for (a) and (b) may be referred to as nanostructures whereas (c) could be referred to as a microstructure. The structures achieved in (a) and (b) are desired as nanostructures allow light to be scattered forward into the wafer due to the nanostructures effectively creating a graded surface index. It can be considered that the more closely-spaced the structures are on the surface, then the resulting surface reflectance will be lower as an increase in etch time results in the structures becoming larger in size with increased distance between peaks. Closed-spaced

structures allow for light to interact with the surface and are therefore more desirable in comparison to structures which are distanced from each other. It is also worth noting that the height variations seen in the measured line profiles for the statically etch samples (typically in the range of $\sim$ 250 nm - 1 μm) are considerably larger than those observed for their dynamically etched counterparts, shown in Fig. 5.4. The optimum surface texture can be considered to be where the height variation between pits and peaks on the surface is of the order of a few hundreds of nm and on the same scale as the wavelength of the incident light. For short etch times, there is a small height variation for the surface texture which results in most of the incident light being reflected from the surface. With an increase in etch time, the height variation of the surface texture will increase and the surface reflectance will decrease. However, if the etch time is too long, structures will combine to form larger bodies, similar to microtextures, resulting in the surface reflectance increasing again.

5.4.1.2 Surface characteristics

Surface characteristics were determined by using AFM data with a scan size of 80 μm x 80 μm, with several sections on the sample scanned. Fig. 5.10 shows the surface area increase plotted against surface reflectance for the static etched samples without pre-cleaning.
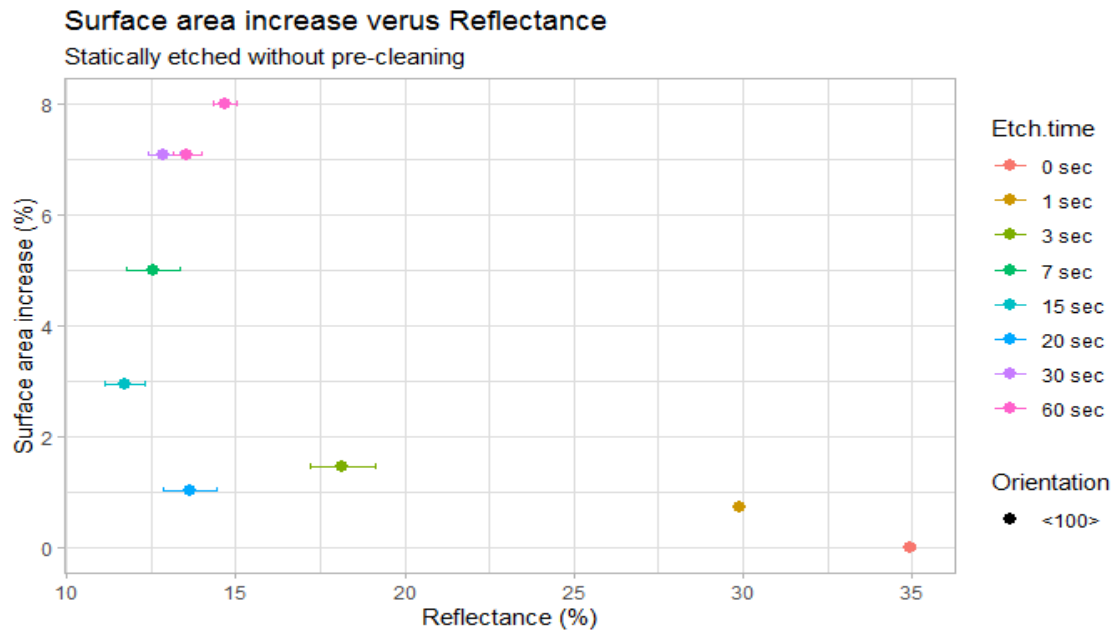
Figure 5.10: Surface area increase plotted against surface reflectance for statically etched samples with no pre-cleaning.

Normally a decrease in surface reflectance corresponds to an increase in surface area. There is a constant increase in surface area for samples with surface reflectance values between 18% and 35%. However, for surface reflectance values under 15%, this is not the case. For the 15 and 20 second etched samples, the increase in surface area with a reduction in surface reflectance is as expected. The remaining four samples have a surface reflectance higher than the 15 second etched sample, but show a greater surface area increase. Fig. 5.11 shows the surface roughness plotted against surface reflectance for the static samples without pre-cleaning.
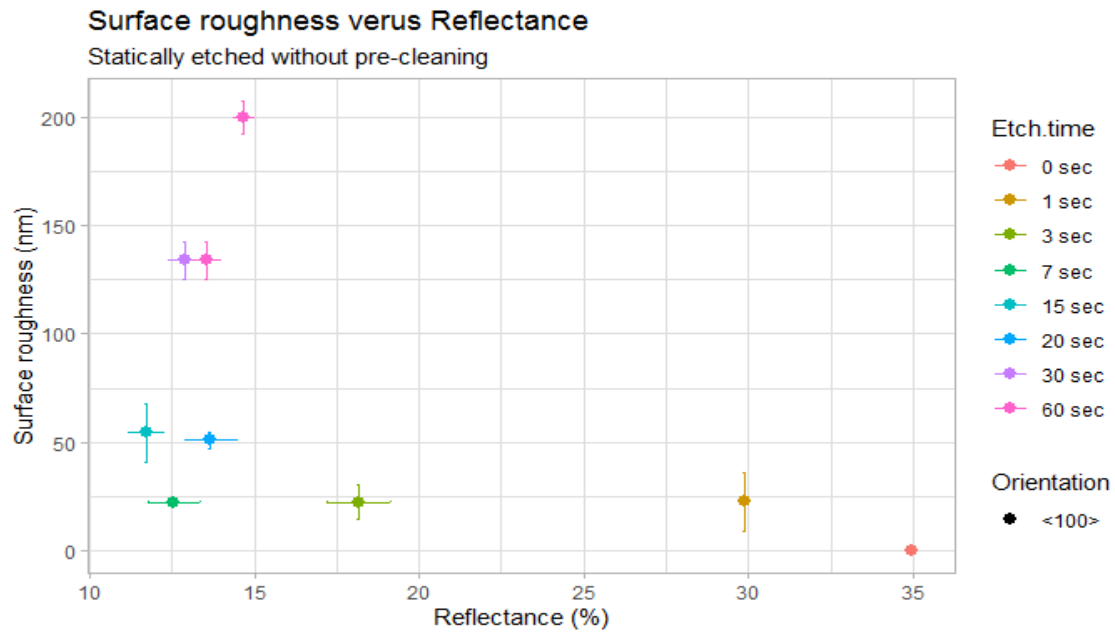
Figure 5.11: Surface roughness plotted against surface reflectance for statically etched samples with no pre-cleaning.

As with the results for the surface area increase, the roughness value of the 15 second etched sample which shows the lowest surface reflectance has not achieved the highest surface roughness. What would be expected is that with an increase in surface area and surface roughness, then a decrease in surface reflectance should occur. However, this could be a result of the 15 second etched sample having structures closer together (~0.5 μm between peaks) in comparison to the samples which achieved higher surface area increase and surface roughness values. In Fig. 5.9, the concept of this can be seen as the line profiles display a two dimensional cross-sectional slice of the surface. The 15 second structures are closer to each other in height, allowing more interactions between the incident light and the surface.
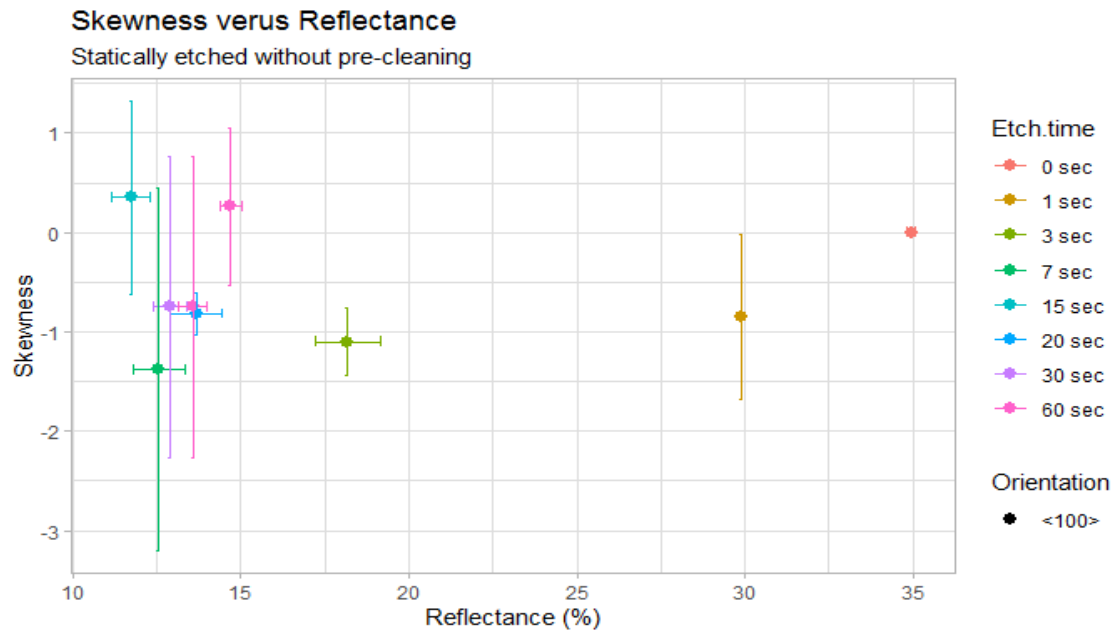
Figure 5.12: Skewness plotted against surface reflectance for statically etched samples with no pre-cleaning.

Fig. 5.12 shows the skewness plotted against surface reflectance for the static samples without pre-cleaning. For these samples, the initial etching shows a pitting of the surface which then modifies to a more peaked surface before returning back to a pitted surface and finishing with a peaks once again.

For the statically etched samples with no pre-cleaning, it can be seen that the 15 second etched sample achieved the best surface reflectance regardless of surface area and roughness. The surface roughness and surface area have some influence on the surface reflectance, however the surface structures need to be close to each other in order for the incoming light to achieve multiple bounces on the structure slopes.

5.4.2 Pre-cleaning

The use of pre-cleaning step was investigated to determine whether it had a beneficial effect on the etching process. As seen previously in Fig. 5.3, the use of pre-cleaning appears to aid in the reduction of surface reflectance. This could be a result of organic residue, native oxides or metal ions occurring on the surface of the Si wafer and the use

of pre-cleaning aids in removing these. One of three methods of cleaning were used on a Si wafer before it was etched; RCA1 cleaning followed by a HF dip, RCA1 and RCA2 followed by a HF dip or a HF dip alone. Once pre-cleaning was preformed, the wafer was rinsed with DI water and dried using N_2, before being placed into the reaction chamber.

5.4.2.1 AFM images

AFM topography images with a scan size of 40 μm x 40 μm and line profiles of the statically etched samples with pre-cleaning can be seen in Fig. 5.13 for the samples which achieved the lowest surface reflectance for the 30 and 60 second etched samples.
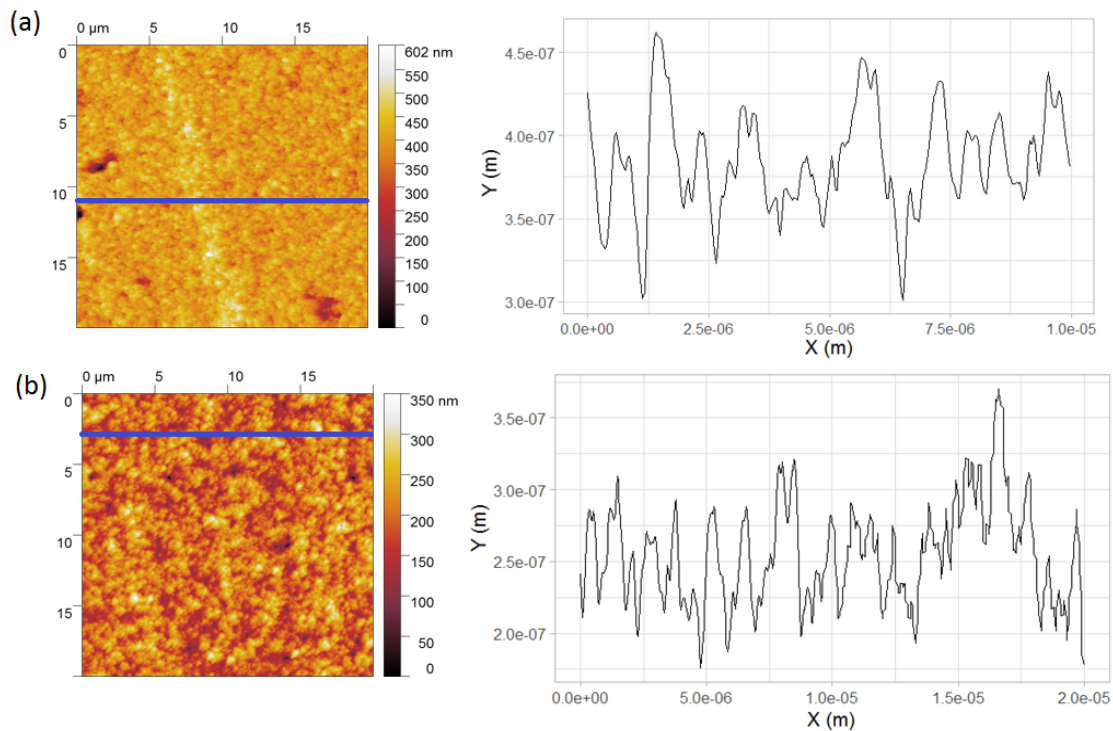
Figure 5.13: AFM images of the pre-cleaned samples which achieved the lowest surface reflectance. Blue line represents where the line profile was taken. Samples with a 30 second etch time had a surface reflectance within 0.3% of each other and the 60 etch time had a surface reflectance within 1.81% of each other. (a) 30 second etch with a surface reflectance of 8.67% with pre-cleaning consisting of RCA1 with a HF dip (b) 60 second etch with a surface reflectance of 12.1% with pre-cleaning consisting of RCA1 with a HF dip

Based on the line profile shown in Fig. 5.13 (a), structures for the 30 second etch

achieved a height variation of ∼150 nm. In comparison, the 60 second etch produced structures with a height variation of ∼200 nm, which is primarily a result of the peak at $x = 1.65x10^{-5}$. Based on the topography images, the 60 second etched wafer appears to have a coarser surface texture compared to the 30 second etched wafer. With more coarse surface features, an increase in surface reflectance is expected and is mirrored in the obtained surface reflectance results.

5.4.2.2 Surface characteristics

As with the static samples without pre-cleaning, surface area increase, surface roughness and skewness will be investigated for the static samples with pre-cleaning. AFM scan sizes of 80 μm x 80 μm were used in order to obtain values for each characteristic. Fig. 5.14 shows the surface area increase plotted against surface reflectance for the static samples with pre-cleaning.
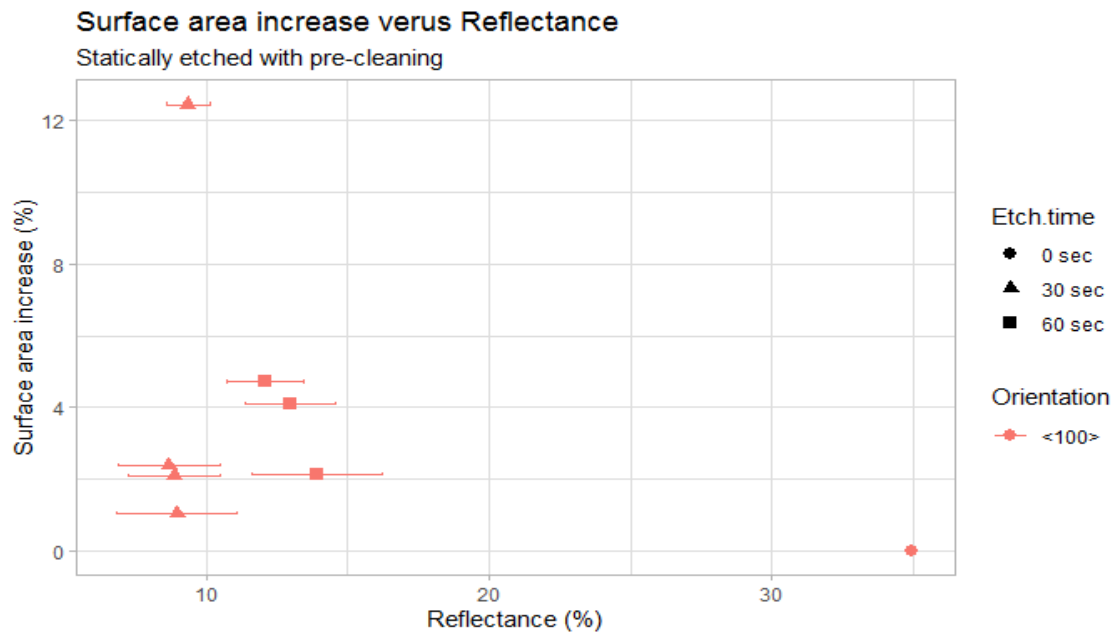
Figure 5.14: Surface area increase plotted against surface reflectance for statically etched samples with pre-cleaning.

Samples with an etch time of 60 seconds show an increase in surface area with a reduction in surface reflectance. This can be seen for the 30 second etched samples

with a mean surface reflectance $< 9\%$, as well as the 9.35% sample. Both of these cases display an increase in surface area. Fig. 5.15 shows the surface roughness plotted against surface reflectance for the static samples with pre-cleaning.
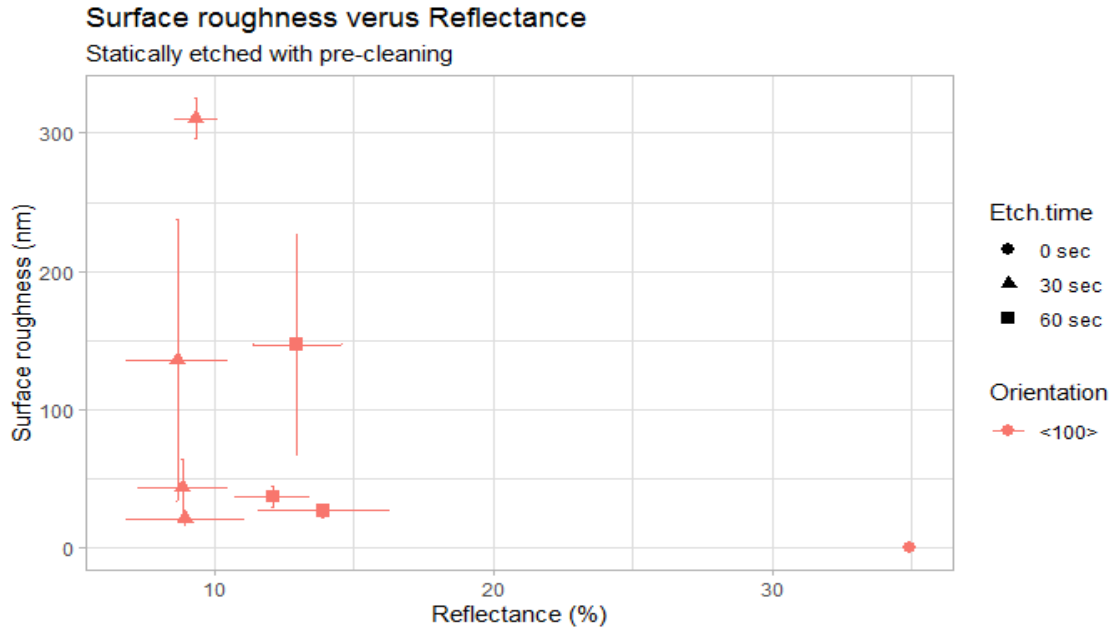
Figure 5.15: Surface roughness plotted against surface reflectance for statically etched samples with pre-cleaning.

As with the increase in surface area, the surface roughness increases as the surface reflectance decreases for the 30 second etched samples, with a mean surface reflectance $< 9\%$. The 30 second etched samples present the same increase in surface roughness as surface area increase, however the 60 second counterparts do not completely follow this trend. The 60 second sample with the highest surface reflectance (13.91%) has the lowest surface roughness and achieved the lowest surface area increase. However the 60 second sample which achieved the lowest surface reflectance (12.1%) achieved the middle surface roughness, whereas it achieved the highest surface area increase.
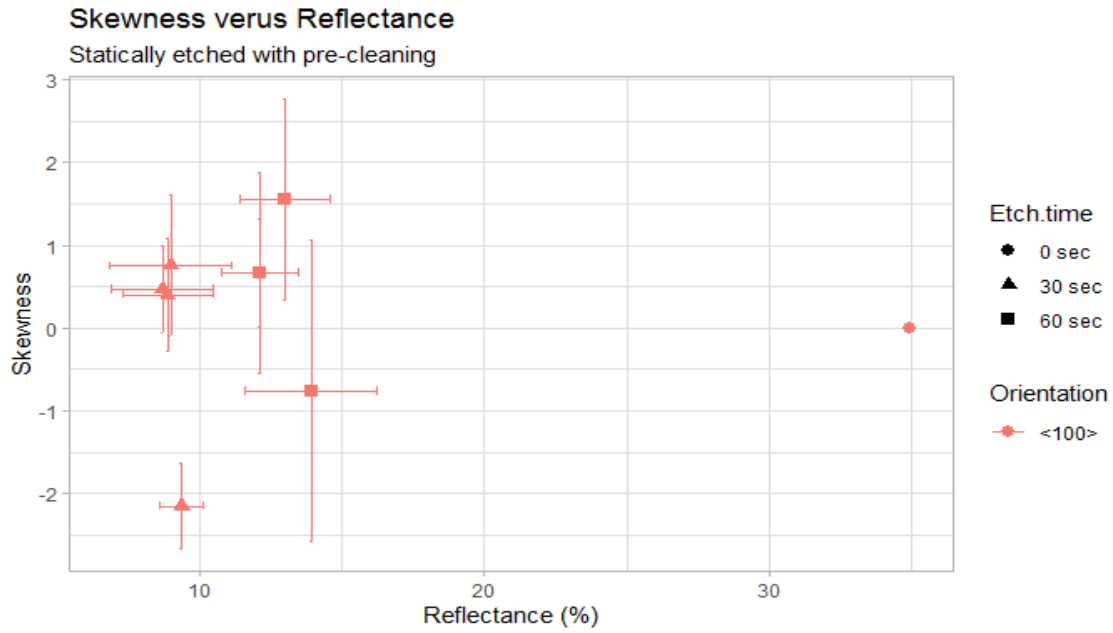
Figure 5.16: Skewness plotted against surface reflectance for statically etched samples with pre-cleaning.

Fig. 5.16 shows the skewness plotted against surface reflectance for the static samples with pre-cleaning. In most cases for these samples, the skewness values indicate surface textures that are predominantly peaked. Two samples do not follow this, with the sample with the mean surface reflectance of 9.35% having a pitted surface and 13.91% having a mainly pitted surface with some peaks. With the AFM images and line profiles shown in Fig. 5.13, the samples with a surface reflectance of 8.67% and 12.1% have a peaked surface which agrees with the skewness values.

For the cleaned statically etched case, the 30 second etched samples have a mean reflectance value within 0.3% of each other, regardless of the pre-cleaning method used, whereas the 60 second etched samples show a mean reflectance value within 1.81% of each other. With the static etching process, the samples which have not been pre-cleaned obtained the lowest surface reflectance with a 15 second etch, whereas for the samples with pre-cleaning the 30 second etched obtained the lowest surface reflectance. Pre-cleaning does not always improve surface reflectance, as seen in Fig. 5.3 with the 60 second etched samples. Even with no improvement, the pre-cleaning

does not appear to negatively effect the surface reflectance.

5.5 Static etching versus dynamic etching

Based on the results shown in the static etch and the dynamic etch sections, the samples which were etched statically achieved results which were considerably better in comparison to the dynamically etched samples. In respect of the dynamic samples, it can be considered that these results do not reflect what the process can achieve. This is due to a number of issues, including the wafers used being too small for the tool and also thicker, needing more time to reach the desired temperature. It can be considered most likely that the temperature is the factor which is the cause for this difference, as the transient temperature does not reach the equilibrium temperature achieved during static etching. This maybe a result of the velocity of the wafers passing through the reaction chamber and the thicker wafers create thermal lag. As a result, the dynamically etched samples have a lower etch rate when compared to the statically etched samples for comparable times. In relation to the reflectance results obtained, one optimum etch time cannot be determined as each orientation shows some variation. It can be seen that regardless of the process, there is an improvement in surface reflectance compared to unetched samples. For the static samples, the optimum etching time to achieve a low surface reflectance is 30 seconds with pre-cleaning. Based on these dynamic samples, the optimum etching time varies for each Si orientation and appears to be 15.6 seconds for (111), 15.6 and 62.4 seconds for (110) and no optimum time was found for (100). As the etch time increases, the surface reflectance decreases initially before it increasing. This increase could be a result of a change in surface structure dimensions as the structures which achieved lower surface reflectance are comparable in size to the incident light. This creates a graded surface index, allowing for the light to be scattered forward into the wafer. With an increase in etch time, the surface structures combine to form larger bodies, which reduces the amount of light that can be absorbed.

Sample no.	Orientation	Pre-cleaning	Etch time (secs)	Process	Ave. reflectance
1	100	None	0	None	34.95%
2	110	None	0	None	35.79%
3	111	None	0	None	35.25%
4	100	None	1	Static	29.9%
5	100	None	3	Static	18.17%
6	100	None	7	Static	12.56%
7	100	None	15	Static	11.73%
8	100	None	20	Static	13.66%
9	100	None	30	Static	12.89%
10	100	None	60	Static	13.57%
11	100	Pre-treatment used	30	Static	9.35%
12	100	None	60	Static	14.69%
13	100	RCA1, HF dip	30	Static	8.67%
14	100	RCA1, HF dip	60	Static	12.1%
15	100	RCA2, RCA1, HF dip	55	Static	12.9%
16	100	RCA2, RCA1, HF dip	30	Static	8.87%
17	100	HF dip	68	Static	13.91%
18	100	HF dip	30	Static	8.96%
19	100	HF dip	15.6	Dynamic	30.92%
20	110	HF dip	15.6	Dynamic	30.52%
21	111	HF dip	15.6	Dynamic	25.7%
22	100	HF dip	15.6	Dynamic	28.98%
23	100	HF dip	15.6	Dynamic	31.24%
24	111	HF dip	31.2	Dynamic	32.1%
25	110	HF dip	31.2	Dynamic	31.95%
26	111	HF dip	62.4	Dynamic	31.01%
27	110	HF dip	62.4	Dynamic	30.43%
28	100	HF dip	62.4	Dynamic	29.28%
29	100	HF dip	62.4	Dynamic	32.34%
30	100	HF dip	31.2	Dynamic	29.78%

Table 5.1: List of samples detailing the orientation, pre-cleaning, process, etch time and average surface reflectance for each sample

Table 5.1 provides a summary of the single crystal wafers studied during this project.

5.6 Raman spectroscopy

Raman spectroscopy was used in order to determine if any residues were left on the etched Si samples by the pre-cleaning or etching processes. Fig. 5.17 shows the Raman spectroscopy results for Si samples with different orientations, etch times and with or without pre-cleaning.
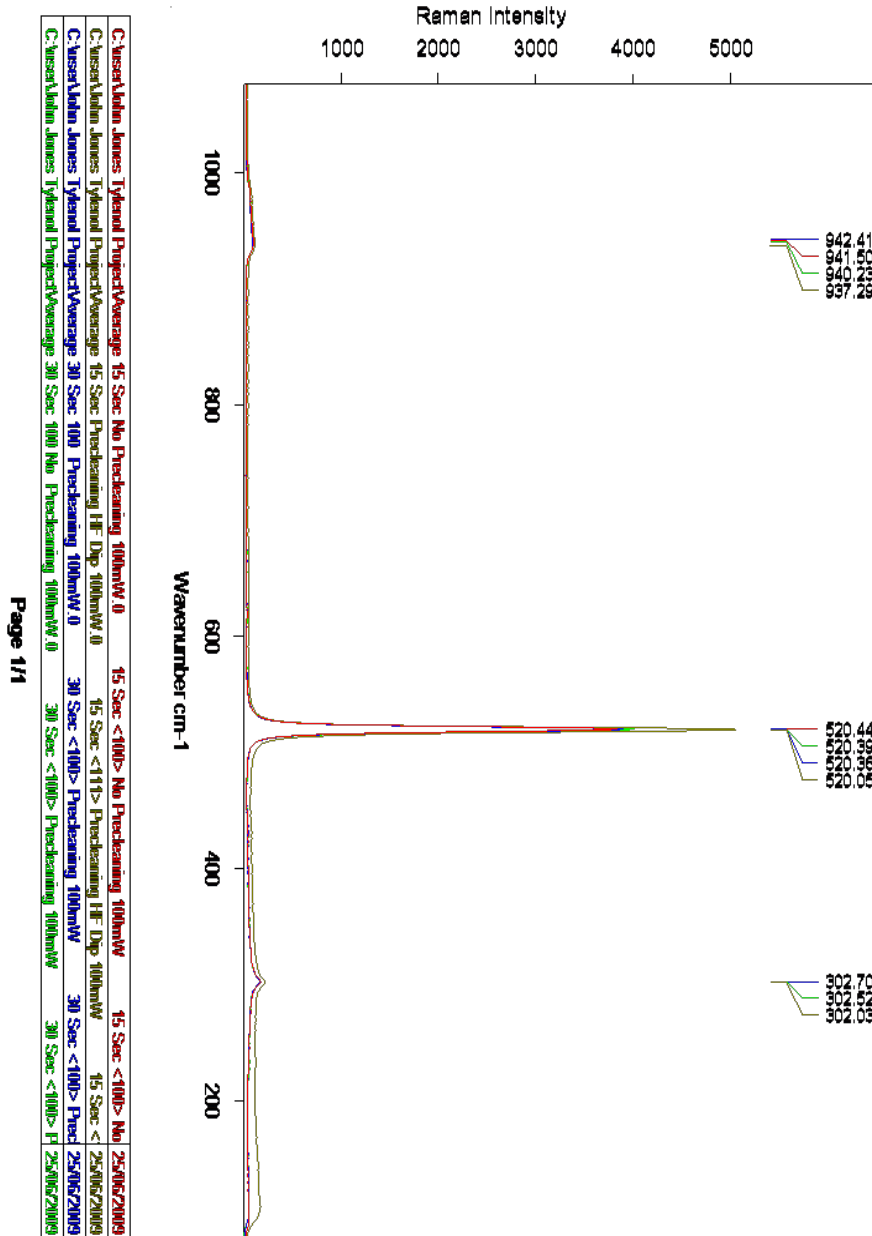
Figure 5.17: Raman spectroscopy of different samples with red representing 15 second etched (100) sample with no pre-cleaning, yellow represents 15 second etched (111) sample with HF dip, blue represents 30 second etched (100) sample with pre-cleaning and green represents 30 second etched (100) sample with no pre-cleaning

A peak is observed ~ 520 cm^{-1} and smaller peaks at ~ 940 cm^{-1} and ~ 302 cm^{-1}. As discussed in [108], the main Raman peak for c-Si occurs at 520 cm^{-1} with peaks

also occurring at 302 cm^{-1} and 935-990 cm^{-1} [109]. From these results, the Raman spectroscopic analysis indicates that the surface of the Si remains free from residues or contaminants from the pre-cleaning and etching steps. There may, however, be trace amounts of contaminants or residues present at concentrations that are below the level of detection.

5.7 Multicrystalline silicon

As the Si wafer-based PV market is dominated by cheaper multicrystalline silicon (mc-Si) cells, the effect of the ADE process on etching of mc-Si was briefly examined with the use of 6" square wafers. The mc-Si wafers were processed using a etchant gas mixture of 20 % F_2 and 80 % N_2 [68]. The surface reflectance achieved by the mc-Si wafer was 6.8 % with a standard deviation of 1.5 %, surface area increase of 6.48 % with a standard deviation of 3.43 % and an RMS surface roughness of 489.87 nm measured by AFM, with a standard deviation of 159.06 nm.

5.7.1 Surface texturing

SEM images for the resulting surface texture for a particular single grain of mc-Si can be seen in figure 5.18, with AFM topography images in figure 5.19, with AFM topography and line profiles in figure 5.20.
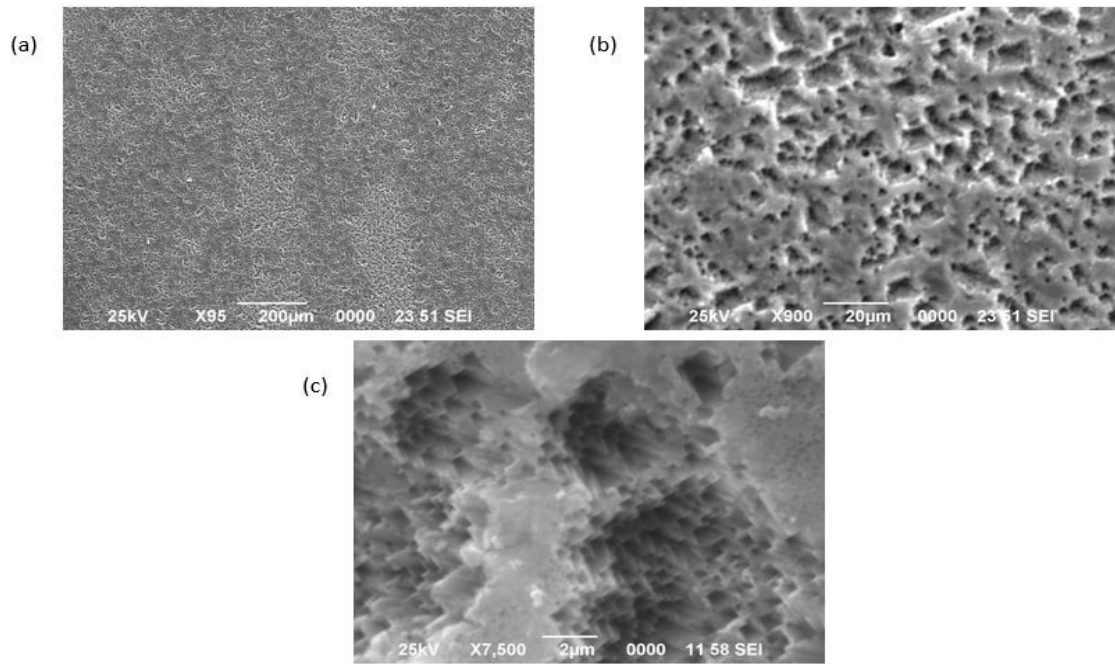
Figure 5.18: SEM images of the surface texture of a single grain on an ADE-etched mc-Si surface. Magnifications (a) x96 (b) x900 (c) x7500. The surface texture of the grain comprises multilayer rectangular etch pits consistent with a (100)-oriented surface
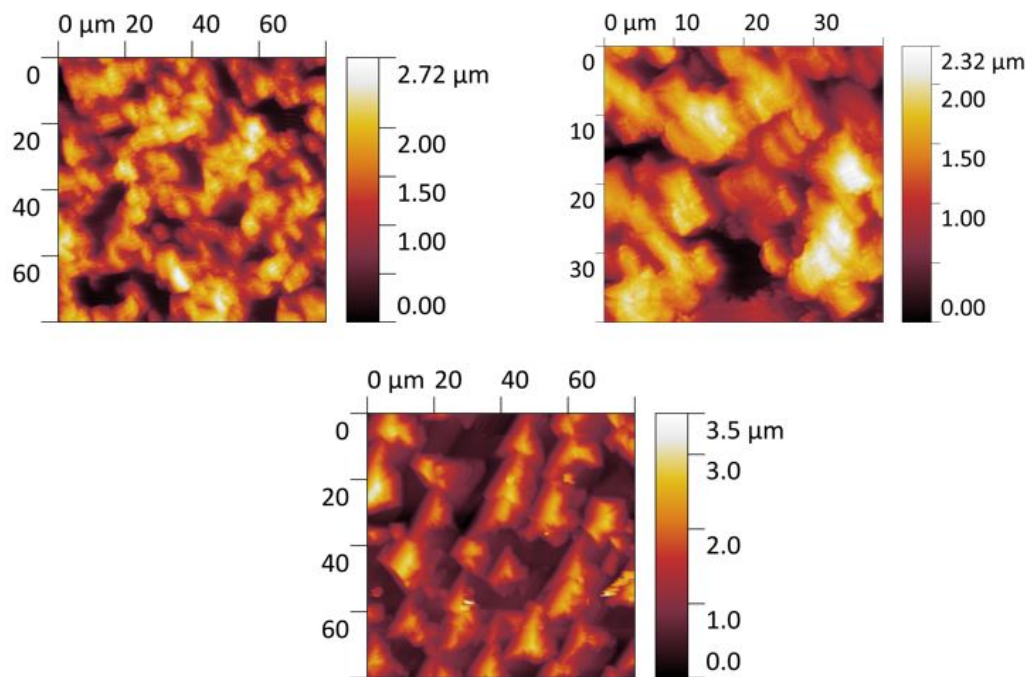
Figure 5.19: Topography images of AFM data obtained on different grain orientations in mc-Si using ADE
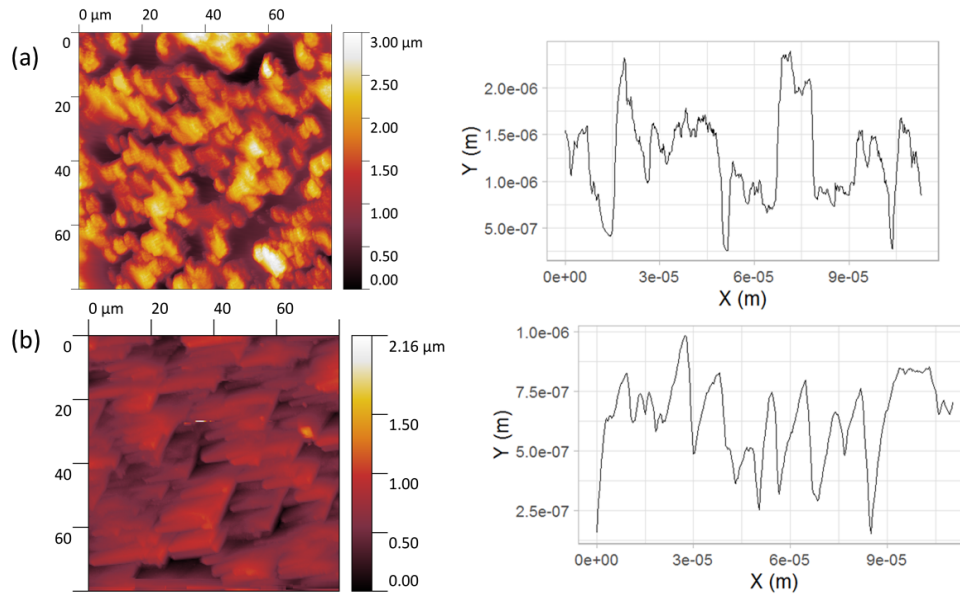
Figure 5.20: AFM topography images with line profiles of mc-Si wafer which has been put through the ADE process (a) has a height distribution of ˜1.6 μm (b) has a height distribution of ˜875 nm

It can be seen how the etching process can affect the the structures formed on the surface of the Si grain, with a height distribution differing from grain to grain. However with the use of mc-Si, each grain is affected by the etching process in a distinct manner. The variations in the etched grains can be seen at the grain boundaries, shown below in figures 5.21 and 5.22.
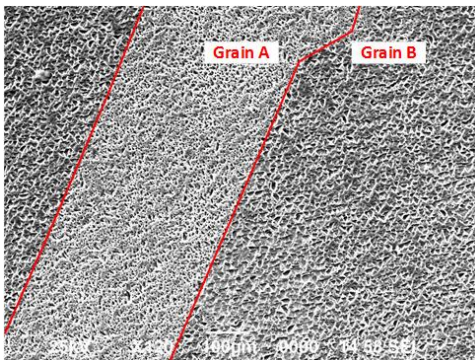
Figure 5.21: SEM image of grain boundary, with the grains indicated
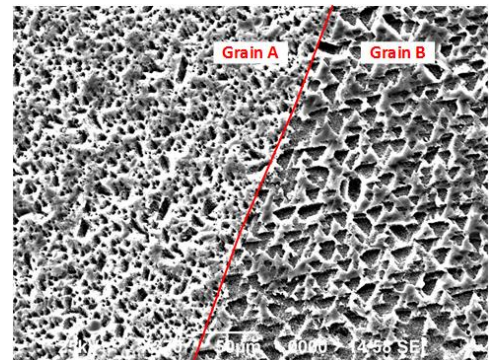
Figure 5.22: SEM image of grain boundary, with the grains indicated

A closer inspection of the etching which has occurred as a result of the process for

grain A and for grain B can be seen in figures 5.23 and 5.24 in figures 5.25 and 5.26 respectively.
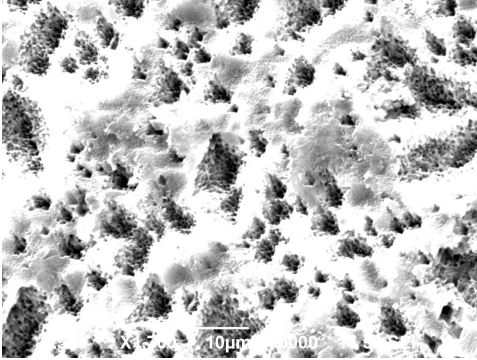
Figure 5.23: SEM image of grain A
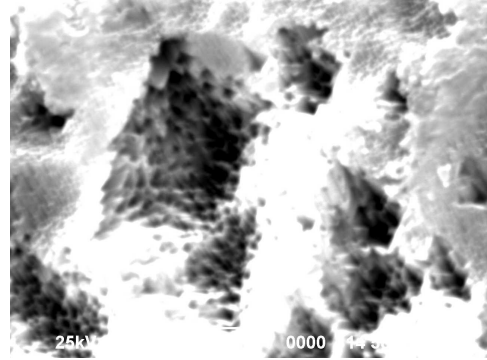
Figure 5.24: SEM image of grain A
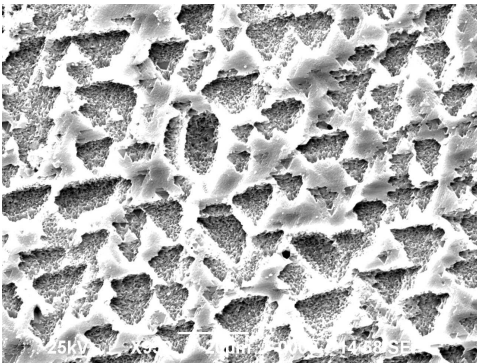
Figure 5.25: SEM image of grain B
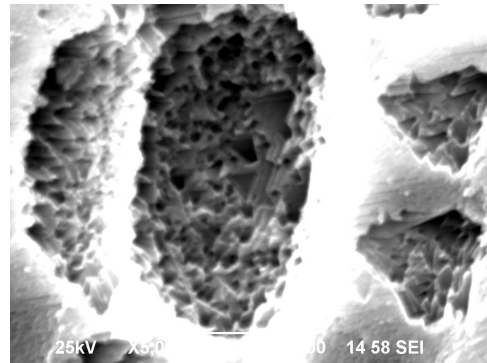
Figure 5.26: SEM image of grain B

Each crystal has shown to have a different reaction to the etching process, as seen in figure 5.21 and figure 5.22 with closer inspections in figures 5.23 to 5.26. This is due to each Si crystal having a different amount of free bonds at the surface as a result of the local grain orientation [110], as mc-Si is made up of several grains with different crystal orientations. To assess which grain orientations are present in the mc-Si sample, these images were compared with AFM data of etch pit geometries obtained on single-crystal wafers of different orientations, shown in figure 5.27.
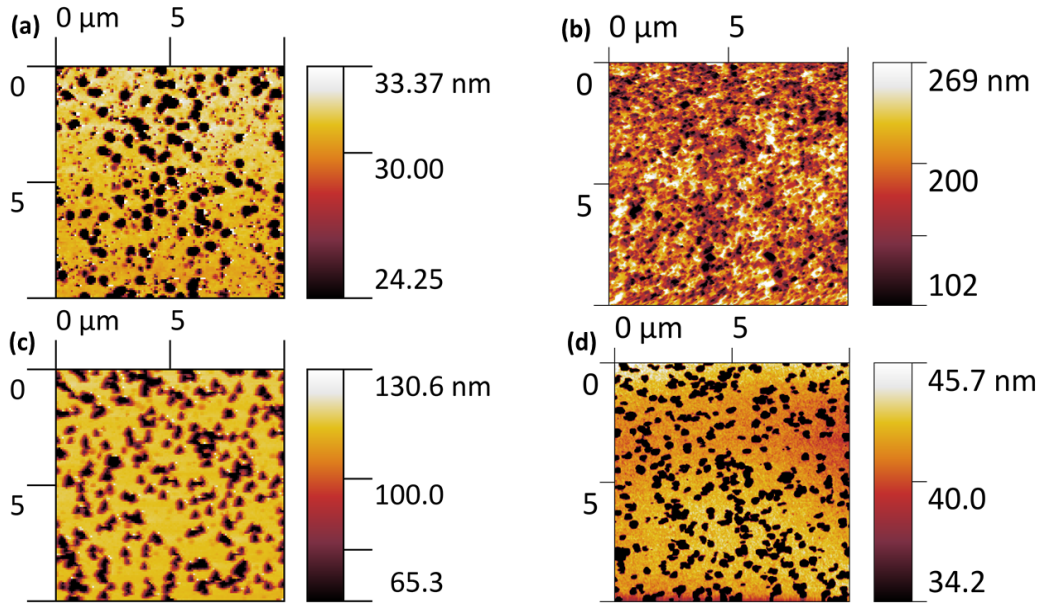
Figure 5.27: Etch pits for the three orientations used through this study (a) Circular etch pits for a dynamically etched Si(100) wafer (b) Square etch pits for a statically etched Si(100) wafer (c) Triangular etch pits for a dynamically etched Si(111) wafer (d) Oval etch pits for a dynamically etched Si(110) wafer

The etch pits which occur are circular/square, triangular and oval in shape for the (100), (111) and (110) wafers respectively. The appearance of triangular etch pits can be seen in grain B in Fig. 5.22, with a closer inspection in Fig. 5.25. This grain can be considered (111) as the monocrystalline (111) wafers have produced similar etch pits. Fig. 5.18 (b) consists of square and circular etch pits, it could be considered that this grain is (100). For (100), the combination of square and circular etch pits may be due to small circular etch pits becoming more etched and forming square pits as a result. The (100) surface produces shallow concave etch pits which are circular in shape when initially etched. With prolonged etching of the surface, the formation of deeper rectangular etch pits occur with well-defined facets. It appears that these rectangular etch pits tend to nucleate inside the shallow concave pits which are formed first on the surface. The shallow pits tend to range in depth from a few to 20 nm (Figure 5.28), whereas the rectangular etch pits have depths of several tens of nm deep with well defined facets and steps inside. It can be seen that the use of mono-Si and microscopy tools aids in identifying the orientations of each of the grains seen in mc-Si.
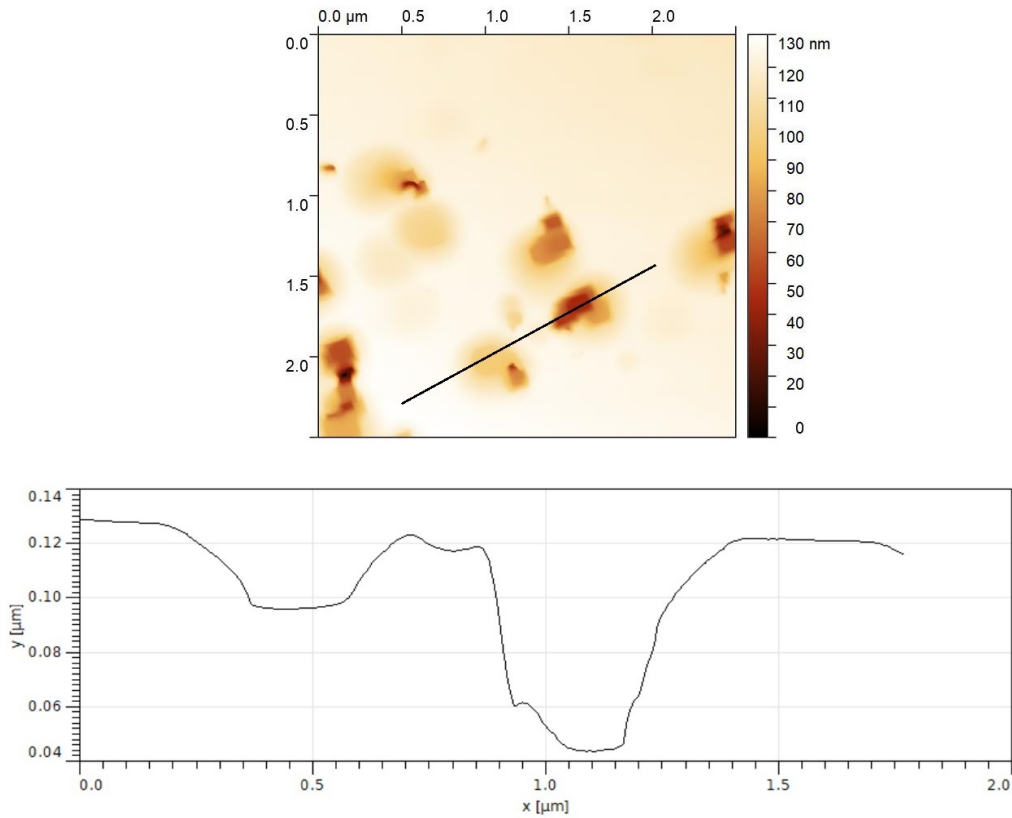
Figure 5.28: Topography and line profile of a Si(100) wafer which has been put through the ADE process. The shallow concave pit has a depth of ˜10 nm.

6 Conclusion

6.1 Introduction

The purpose of this thesis was to investigate the surface texturing step of the fabrication process for solar cells in order to reduce surface reflectance. The overall aim was to identify the optimum parameters that would minimise the surface reflectance of silicon wafers subjected to the atmospheric dry etch (ADE) texturisation process developed by Nines PV. This is a relatively new process that utilises fluorine gas to etch the silicon surface. This process can be readily implemented on an industrial scale for continuous in-line processing of c-Si and mc-Si wafers. It has the potential to be more environmentally-friendly than current wet-etching methods for texturing Si-wafer based PV cells, as it does not use large amounts of water, the by-products of the etching process are readily captured and eliminated, and it has a low global warming potential. This ADE process offers a path to producing surface nanotextures with low surface reflectance for next-generation Si wafer based solar cells. It is competitive with other methods for producing surface nanotextures on Si, as it does not have the high capital costs associated with reactive ion etching and is faster and more resource-efficient than metal-catalysed chemical etching. The effects of dynamic versus static etching, wafer orientation, etch time and the use of pre-cleaning have been investigated. The main research objectives in this study were to investigate how the ADE etch parameters affected the surface topography of the processed silicon wafers, assess how the resulting texture structures impact the light trapping properties of the surface, and identify the optimum process parameters to achieve low surface reflectance. To this end the impact

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on the resulting surface texture have been investigated using surface reflectance, AFM and SEM measurements. In this chapter, an overview of the findings of the processed samples will be provided followed by recommendations based on these findings.

6.2 Summary of findings

A number of important observations were made during the course of this research. It was found that (100) samples that have been cleaned before being placed in the ADE tool, have lower surface reflectances in comparison to samples which are not cleaned before processing. The use of both static and dynamic ADE methods provide an insight of how these techniques can affect the etching process. The statically etched samples showed considerably lower surface reflectance values compared to wafers that were dynamically etched (i.e. passed through the reaction chamber at constant velocity) using the same ADE etch parameters. This may have been down to the transient temperature of the wafers not reaching an optimum value during the dynamic process, it could also be liked to the size of the wafers used for these experiments, which were smaller and thicker than those that the ADE tool was designed for - this could for instance have affected the gas dynamics over the wafer surface. In any case, a deeper examination of how the dynamic process affects the etching of the surface is needed. The dynamic process provided surface reflectance values which did not vary greatly for different wafer orientations, with the lowest surface reflectance of 28.98% for (100) with a 62.4 second etch, 30.43% for (110) with a 62.4 second etch and 25.7% for (111) with a 15.6 second etch. Given time constraints, it would not be possible to repeat these experiments using static etching to determine whether different etch rates would be observed for ADE etching of different wafer orientations. However, an optimum time of 15-20 seconds was observed for the ADE texturisation of Si(100) wafers using static etching. Beyond this, the measured surface reflectance values did not decrease any further, and actually increased slightly. This is despite the surface roughness of these wafers, as measured by AFM, increasing with

etch time. It is speculated that this is either down to better anti-reflective properties of the nanoscale textures produced at shorter etch times compared to the microtextures formed during longer etches, or the fact that the distance between peaks and troughs increased at longer etch times, creating a more open surface. Either way, this demonstrates that the surface reflectance depends sensitively on the surface texture in a complex manner that requires further investigation, possibly through simulation of light reflection from various structures obtained.

To summarise:

1. Static etching process produces a much lower surface reflectance, and correspondingly rougher surface textures, than dynamic etching carried out under similar timeframe and with comparable etching conditions. This may be attributed to the fact that an equilibrium etch temperature is reached in the former case before the etchant gas is introduced, while the transient temperature achieved during the dynamic process is much lower, yielding a significantly reduced etch rate.

2. For statically etched samples, the surface reflectance was observed to drop significantly in the first 15-20 seconds of ADE etching, reaching $\sim$11-12 %. Further etching did not appear to produce lower surface reflectance values despite AFM roughness measurements increased. This may be attributed to two possible causes; (i) while the average height between peaks and troughs on the surface increased with etching time, AFM data suggested that the average separation between peaks also appeared to have increased. The more open surface (i.e) lower density of peaks and troughs) may result in higher surface reflectance being obtained. (ii) Shorter etch times produce surface textures with height variations on the order of optical wavelengths (i.e hundreds of nanometers) while longer etch times produce textures with dimensions slightly larger than optical wavelengths. The nanotextures produced at shorter etch times may be more effective at reducing surface reflection (e.g through a graded refractive index effect) compared to the microtextures produced at longer etch

times (where surface reflection is reduced through multiple reflections of incident light onto neighbouring microstructures). Further work, involving simulation of surface reflection from such structures using e.g the finite-difference time domain (FDTD) method, is required to elucidate which of these mechanisms might be the root cause of the observed increased in surface reflectance for long ADE etch times. Structures whose heights are in the hundreds of nm and do not have a vast lateral separation appear to have a lower surface reflectance in comparison to other structures.

3. A pre-cleaning step, such as RCA clean followed by a HF dip, to remove potential organics, residues, metal ions and native oxide layers is beneficial to the etching process, yielding lower surface reflectance values for most of the wafers that were cleaned prior to the ADE step to uncleaned wafers subjected to the same ADE etch parameters.

4. No significant difference in etching rate was observed for different wafer orientations, when Si(100), (110) and (111) wafers were dynamically etched with ADE. However, the etching conditions used were likely not optimal for this set of experiments as the achieved reflectance values were considerably lower for the observed statically etched samples. While further investigation is needed in future to confirm whether different etch rates are obtained for different wafer orientations using the ADE process, it was observed that the geometry of the etch pits observed for each orientation reflected the symmetry of the surface. For example, the etched Si(111) surface was characterised by triangular etch pits reflecting the underlying three-fold symmetry of the surface, while the Si(100) was characterised by rectangular etch pits reflecting its underlying four-fold symmetry. This could potentially be used to identify local grain orientations in etched mc-Si wafers. It would also be worthwhile to investigate whether the local variations in etch pit geometry observed for different grain orientations in mc-Si produces significant differences in local reflectance values and whether this could

also help identify local grain orientation. This would require the construction of a wafer mapping tool that would allow high-resolution (<100 μm) mapping of local variations in optical reflectance

Based on the findings in this thesis, wafers processed using a static etch achieved a more desirable surface reflectance in comparison to their dynamically etched counterpart. Statically etched wafers also highlighted that use of pre-cleaning processes does not appear to have any negative effects on wafers which were etched after cleaning, with some wafers achieving a lower surface reflectance then their non-cleaned counterparts. In regards to the dynamic etching, the process was not fully utilised as the typical conditions required for the tool were not possible to implement. This research work used smaller and thicker wafers than normally employed for the ADE tool. The use of monocrystalline Si allows for identification of how etch pits are formed for different orientations and how the etching occurs in each case. This understanding of etch pit formation on different wafer orientations could be used as a way to identify different grains on a mc-Si wafer after the etching process.

To conclude, it can be considered that the objectives of this project were in some way met as it was seen with AFM images that the surface structures vary with different etching. The formation of surface textures using the ADE process was demonstrated to decrease surface reflectance in comparison to a polished wafer with no etching. Finally, the use of certain etching parameters allows for structures to be comparable to the wavelength of light and reducing surface reflectance.

6.3 Future work

Based on the work carried out during this research, it can be considered that the following would be beneficial in future work:

- The use of larger diameter Si wafers with a reduced thickness for the dynamic etching process would be more preferable than the wafers used in this study as there was not a significant reduction in surface reflectance. This would provide a

greater insight particularly as dynamic etching is the process method for which the tool is designed. In addition, larger wafers would remove issues faced during this research, including etchant gas interaction with the surface and wafer temperature. This would allow for a better understanding of the dynamic process.

- Larger wafers could also be employed for the static etching process to determine any notable differences between the two etching processes.

- Further investigation into etching of different orientations is needed, as in this work it has not determined if the etch rate is substantially different for each orientation. This can be carried out for both static and dynamic etching process as the dynamic process results does not provide much information about the different orientations

- As monocrystalline silicon (mono-si) was primarily used in this research to show direct comparison between crystal orientations, the main focus in future should be more on the examination of the ADE process on multicrystalline silicon (mc-si) wafers as the majority of solar cells produced globally use mc-Si. Use of mono-Si in this project will allow for different orientations to be identified using the etch pits discussed in this research.

- New tools to map properties across different grain orientations, such as an automatic mapping tool to measure surface reflectance across the wafer, as well as an optical beam induced current tool to measure photocarrier generation, will be important particularly for future work involving multicrystalline silicon wafers.

- Work is still required in order to understand how the ADE process can be integrated into the full solar cell fabrication scheme. It will be important to investigate how the surface nanotextures affects subsequent solar cell fabrication steps including emitter diffusion, surface passivation and deposition of front surface contacts.

- Simulations of light reflection from structures similar to those seen here in AFM data could also be carried out, using e.g. FDTD method, to understand why the texture formed at 15-20 second etch times has a slightly lower surface reflectance than the coarser textures seen for longer etch times

- As much of the data here involved measurement of the surface textures using AFM, it would be worth trying to quantify the effect of top convolution on measured roughness parameters. This would involve SEM measurements of the AFM tip shape before and after scanning the etched Si wafers, as well as comparison of SEM and AFM data of the etched wafer surfaces.

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