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New grid-tied cascaded multilevel inverter topology with reduced number of switches

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***Abstract*- Performance of multilevel inverters (MLI) are distinguished because of their low harmonic waveform generation, low filtering requirements on AC side and high voltage application. Among different (MLI) topologies, cascaded multi-level inverters (CMLI) are easier to implement and are much more cost effective. The main drawback of multilevel inverters is requirement of more than one isolated DC source and a lot of switches which makes them bulky and expensive to implement. To address this issue, researchers have investigated new topologies with reduced number of switches compared to conventional multilevel converters. In this paper, a new grid-tied cascaded multi-level topology with reduced number of switches is proposed. Compared to a standard 11-level MLI, the number of switches are reduced. The objective of the design is to reduce the number of DC sources and switches in order to reach the same level of the output voltage. Finally, performance of the proposed topology with a range of modulation and load power factor, operation regarding connection to the grid with closed loop control and comparative study with the other topologies is presented.**

***Index Terms*—Cascaded Multilevel Inverters (CMLI), Cascaded H-bridge (CHB), Grid-tied cascaded multi-level, Load power factor, Low filtering requirements, Multilevel Inverters (MLI).**

I. INTRODUCTION

Multilevel inverter is a fresh emerging technology and has been introduced since 1975 as alternative in high power and medium voltage situations which is going to be the most preferable choice as a power conversion approach [1,2]. By application of multilevel topologies some problems of using two-level converters such as electromagnetic consistence, low power quality, high switching losses and high dv/dt can be mitigated to a great extent [3-5]. Due to these features, multilevel converters can be useful option in micro-grid systems [6], distributed generation [7] and adjustable-speed drives [8].

In recent years different topologies for multilevel inverters has been introduced. Neutral point clamped (NPC) [9], Flying capacitor (FC) [10] and Cascade H-bridge (CHB) [11,12] are three different basic multilevel converter topologies. Although these class of multilevel converters are widely used in high power applications, they have some drawbacks. The main drawbacks of (NPC) topology are unbalanced dc link and need for higher number of clamping diodes [13]. FC topology uses flying capacitor as clamping device but for higher voltage application needs an excessive number of storage capacitors [13,14].Among these topologies, Cascaded H-bridge (CHB) is proper option for high voltage application because of its modularity and simplicity of control. As this topology consist of series power conversion sub modules, the voltage and power level can be easily scaled. However, Cascaded H-bridge topology has the greatest disadvantage since it uses separate dc source for each H-bridge cell which make this structure bulky and expensive to implement. This topology is called classic cascaded H-bridge topology. To address this issue researchers proposed the other topologies with using of a single dc source for one H-bridge cell and storage devices for the rest of cells [15] so this structure reduces the cost of equipment and is called hybrid cascaded H-bridge topology. Furthermore, it needs less number of switches which can improve reliability and electromagnetic consistence. Another issue is that this version of topology has capability to generate higher number of levels with less number of switching components [16].

Novel multilevel topologies are designed to mitigate the drawbacks of conventional by reducing the output THD. The conventional way to improve THD is increasing the number of switches in order to reach higher level of voltage. However, reaching to higher level of voltage with decreasing the number of switches could be attractive which will cause low filtering requirements on AC side as well as well as reducing cost and volume because of using less switches. Low switching losses, low voltage stress and better power quality are the other advantages of reaching to higher voltage levels. In this paper, we will propose the new cascaded H-bridge topology which uses only one isolated DC source and has already the mentioned advantages. The main contribution of the paper is using the reduced number of switches to reach higher level of voltage.

The remainder of this paper is organized as follows. In section II, a brief description of the proposed topology with switching algorithm and control are given. Operation regarding to grid connection and operation with range of modulation index and load power factor are presented in section III. In Section IV, comparative study and simulation results are presented and Concluding remarks are made in section V.

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II. PROPOSED TOPOLOGY: SWITCHING ALGHORITM AND CONTROL

Fig. 1 shows the proposed topology with a single DC source. Two h-bridge cells are cascaded together where upper cell is connected to a DC supply and the lower cell is fed from a capacitor as an energy storage. Midpoint of the DC supply also is connected to upper cell through two back to back switches to take half of the DC voltage in some states. The capacitor is charged to a desired level of voltage according to our set up. In our case, the capacitor voltage is regulated at quarter of the DC source amplitude to have 11-level voltage waveform at the output of inverter. With assuming that DC source voltage is 4E, the capacitor voltage would be controlled at E. So, the voltage levels in the output are 0, ±E, ±2E, ±3E, ±4E and ±5E.The main principle for operation of this topology is using all possible combinations of DC source voltage and capacitor voltage. In some states, capacitor voltage will add or subtract from the main source DC voltage and also with using two back to back switches between the midpoint of dc source and first h-bridge, taking half of DC source voltage is possible. Table I shows different switching states, output voltage for each state, capacitor mode and different values of m=(V_{out_Peak}/V_{dc}).

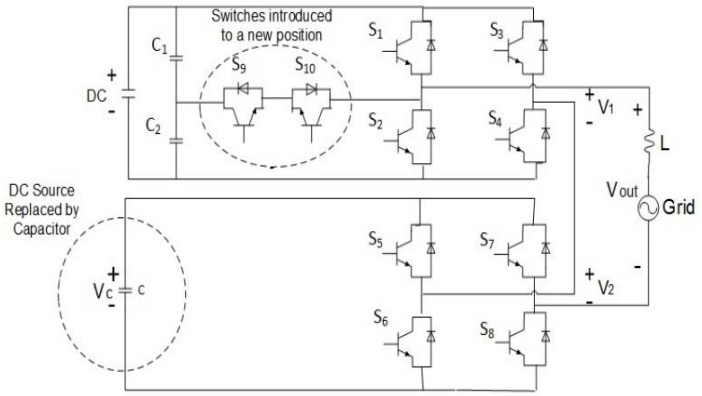

Fig. 1. Proposed Grid-tied Multi-level Topology

Regarding to Fig.1, the output voltage will be:

$$V_{out} = V_1 + V_2 \quad (1)$$

Where V_{out} is the output or load voltage and V_1 , V_2 are output voltage of each h-bridge.

Redundant switching states are presented in Table I. Switching states 3&4, 6&7, 9&10 and 12&13 are important to charging or discharging effects. A proper modulation technique is required to produce gate pulses for each state. There are different kinds of modulation techniques for multi-level inverters [17]. In this paper, we are using level-shifted PWM method where all the carriers are in phase. Fig. 2 shows the reference signal with multi-carrier level shifted PWM technique. In designing switching pattern, influence of switching states on capacitor voltage should be considered.

Table I. Switching States of 11-Level MMC

states	**S_1S_2 S_3S_4 S_5S_6 S_7S_8 S_9S_{10}**	**V_1**	**V_2**	**V_{out}**	**V_{out}/V_{dc}**	**Cap**	**m**
1	10 01 10 01 00	V_{dc}	V_c	$V_{dc}+V_c$	5/4	Dis	5/4>m>1
2	10 01 10 10 00	V_{dc}	0	V_{dc}	1	No Eff	3/4<m<1
3	10 01 01 10 00	V_{dc}	$-V_c$	$V_{dc}-V_c$	3/4	Ch	1/2<m<3/4
4	00 01 10 01 11	$V_{dc}/2$	V_c	$V_{dc}/2+V_c$	3/4	Dis	1/2<m<3/4
5	00 01 10 10 11	$V_{dc}/2$	0	$V_{dc}/2$	1/2	No Eff	1/4<m<1/2
6	00 01 01 10 11	$V_{dc}/2$	$-V_c$	$V_{dc}/2-V_c$	1/4	Ch	0<m<1/4
7	10 10 10 01 00	0	V_c	V_c	1/4	Dis	0<m<1/4
8	10 10 10 10 00	0	0	0	0	No Eff	m=0
9	00 10 10 01 11	$-V_{dc}/2$	V_c	$V_c-V_{dc}/2$	-1/4	Dis	-1/4<m<0
10	01 01 01 10 00	0	$-V_c$	$-V_c$	-1/4	Ch	-1/4<m<0
11	00 10 01 01 11	$-V_{dc}/2$	0	$-V_{dc}/2$	-1/2	No Eff	-1/4>m>-1/2
12	01 10 10 01 00	$-V_{dc}$	V_c	$-V_{dc}+V_c$	-3/4	Dis	-1/2>m>-3/4
13	00 10 01 10 11	$-V_{dc}/2$	$-V_c$	$-V_{dc}/2-V_c$	-3/4	Ch	-1/2>m>-3/4
14	01 10 01 01 00	$-V_{dc}$	0	$-V_{dc}$	-1	No Eff	-3/4>m>-1
15	01 10 01 10 00	$-V_{dc}$	$-V_c$	$-V_{dc}-V_c$	-5/4	Ch	-5/4<m<-1

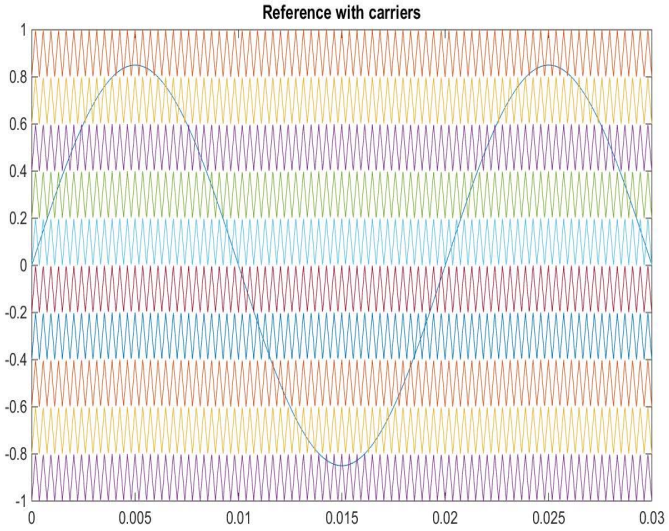

Fig. 2. Reference signal with multi-carrier level shifted PWM

Analyzing states shows that states 2, 5, 8, 11 and 14 don't affect the capacitor since it is disconnected from the other points. States 1 adds both DC link voltages so the capacitor current is reversed and causes discharging. For charging states, the logic subtract the capacitor voltage from DC link voltage so the current is in the direction that charges the capacitor. As shown in fig. 2, ten carrier waves modulate the reference signal (V_{ref}) to generate 11-level voltage waveform at the output of inverter. Table I and fig. 2 illustrate that each switching state could be produced by the comparison between reference signal and carriers. As example if the reference signal be greater than the highest level carrier (C_{r1}), the switching gate pulses that are related to state 1, should be produced by the logic. In order to balance capacitor voltage in desired value, its voltage is sensed and used in switching logic. Consider situation that reference voltage is between two carriers. In this case based on real time information received from voltage feedback, the proper switching state is selected to charge or discharge the capacitor voltage. The proposed switching algorithm and control ensures the capacitor voltage regulation at the quarter of DC source amplitude.

III. OPERATION: GRID CONNECTION, CHANGE OF MODULATION INDEX AND LOAD POWER FACTOR

A. OPERATION REGARDING TO GRID CONNECTION

Grid-tie inverters convert DC electrical power into AC power suitable for injecting into the electric grid. Multilevel cascaded topologies are suitable choice for applications where the input voltage is lower than the peak of the output voltage. The multi-level inverter converts dc power to grid-connected ac power by injecting sinusoidal current into grids and can provide power factor and VAR support during operation to help voltage stability so there is no need for installation of expensive voltage management devices. This grid-tied inverter control strategy is not only capable to control the active power, but also dynamically is able to change the magnitude of the reactive power injected into the grid. Fig. 3 shows the closed loop control procedure that we have applied to connect multi-level inverter to the grid. Simulation results for this section is presented in section IV.

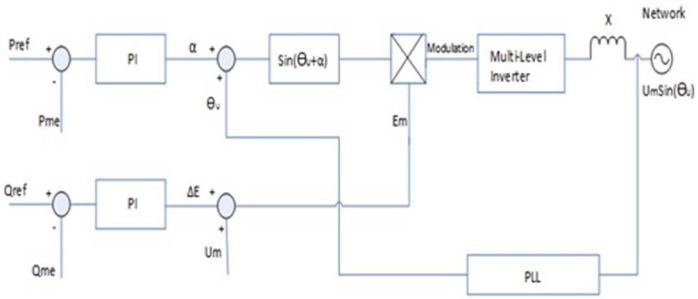

Fig. 3. Control structure for a single phase grid connected MMC

B. OPERATION WITH CHANGE OF MODULATION INDEX

As shown in Fig. 2, ten carrier waves modulate the reference wave (V_{ref}) to generate 11-level voltage at the output of inverter. In two level inverter the relation between the modulation index (m_a), the reference wave and carrier is:

$$m_a = \frac{V_{ref}}{V_{carrier}} \tag{2}$$

So according to the above relation, the modulation index can vary between 0 and 1 but in the case that over modulation happens, it can be greater than 1. In multi-carrier level shifted PWM method, because of limits, amplitude of (V_{ref}) could not be greater than 0.93. It should also be greater than {(number of carriers-2)/number of carriers} for keeping all voltage levels in the output. So the limits for variation of the reference voltage (V_{ref}) is:

$$\{(\text{Num of carriers-2})/(\text{Num of carriers})\} < V_{ref} < 0.93 \tag{3}$$

According to Table I, capacitor voltage is always adding to the output voltage so $m_a>1$. However, m_a can't reach to the value of 5/4 because the maximum value for V_{ref} is 0.93. The limits for m_a is:

$$1 < m_a < \frac{V_{dc} + V_c}{V_{dc}} \tag{4}$$

C. OPERATION REGARDING TO POWER FACTOR CHANGE

Changing the load has been made to show the good dynamic performance of the inverter. So for different cases of load power factor change, multi-level inverter is able to respond.

But the only limit is referring to maximum power that grid demands and is depended on the DC link voltage of inverter. As example if the DC link voltage be 400 v, and capacitor voltage be adjusted to 100 volt, the maximum active power that we can push to the grid is 2.9 kW (assume that the grid peak to peak voltage is 400 v).

IV. COMPARATIVE STUDY AND SIMULATION RESULTS

In This section, we will compare our topology with classic MMC topology and hybrid MMC topology regarding to their number of switches and DC sources. Simulation results confirm that suggested topology is able to work with lower switching frequency with acceptable amount of THD. Regarding to grid connection this topology has very good performance and is able to push different amounts of active and reactive power to the network. It has also ability to push higher amount of active power to the network which is useful for HVDC application.

A. COMPARATIVE STUDY

Table II, shows the comparative study, whereby the comparative approach is done with classic, hybrid and proposed topology.

Table II. Compare between classic, hybrid and proposed cascaded H-bridge topology

Topology	Number of switches	Number of DC sources	Output Voltage Level	Output Voltage THD
Classic Cascaded H-bridge[11]	20	5	11	11.5%
Hybrid Cascaded H-bridge[15]	16	1	11	12 %
Proposed Cascaded H-bridge	10	1	11	13 %

According to the above table, in order to reach 11 level voltage and THD around 12%, the proposed topology uses only 10 switches with single DC source so the volume and cost of the system goes down. The control and implementation of the proposed topology with reduce number of switches, is more easier and it has lower switching losses because of using less switches.

B. SIMULATION RESULTS: WORKING WITH LOWER SWITCHING FREQUENCY

Simulation results show that the proposed topology is able to work with lower switching frequency with acceptable THD amount in the output voltage. In our simulation if we decrease switching frequency from 2 kHz to 500Hz the THD of output voltage will be around 13%. It means that with this kind of topology, switching losses could be less with lower switching frequency.

C. SIMULATION RESULTS: OPERATION REGARDING TO GRID CONNECTION

Table III, shows the system parameters for our simulation.

Table III. Simulation Parameters

DC Source Voltage (V_{dc})	800 V
DC Capacitor	2500μF
Switching Frequency	2kHz
Resistor Between Inverter and Grid	3.5Ω
Inductance Between Inverter and Grid	35mH
Frequency	50Hz
Grid Voltage (RMS)	230V

The control strategy for grid connection of single phase cascaded H-bridge MMC has been explained in section III. With considering P_{ref} =10kW and Q_{ref} =500Var as initial reference values and changing P_{ref} =10kWto P_{ref}=7kW at t=3s, the dynamic of system for this change is shown in the following figures. Fig 4 and Fig 5 show the amount of active and reactive power that inverter pushes to the network regarding to the change of active power demand at t=3s.

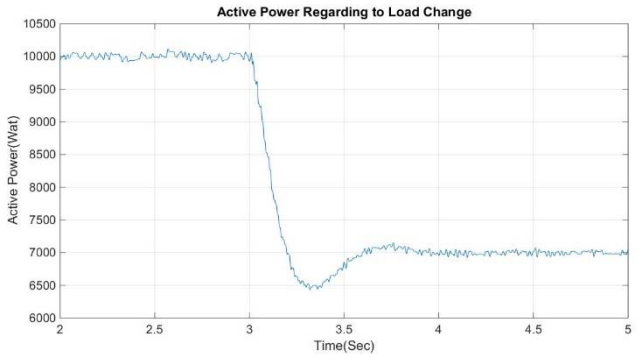

Fig. 4. Active Power to the Grid (Reference Changes from 10kW to 7kW)

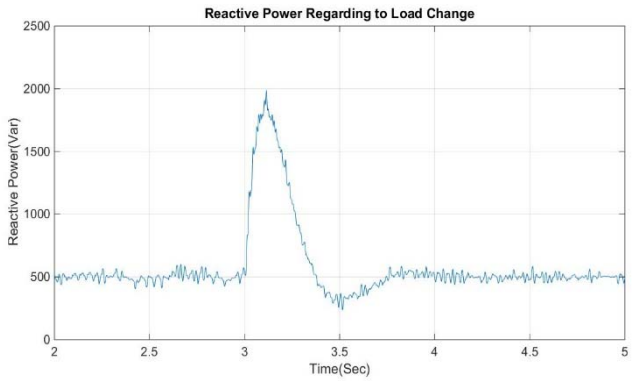

Fig. 5. Reactive Power to the Grid (Reference Changes from 10kW to 7kW)

Fig. 6 and Fig. 7 present the output voltage and current of multilevel inverter regarding to active power demand change at t=3s. It's obvious that inverter has a good dynamic response to significant load change. However the main issue here is that when the demand for active power changes from 10kW to 7kW, the amount of output voltage decreases so we lose two-level voltages in the output after t=3s and the THD of output voltage increases from 13% to 17%.

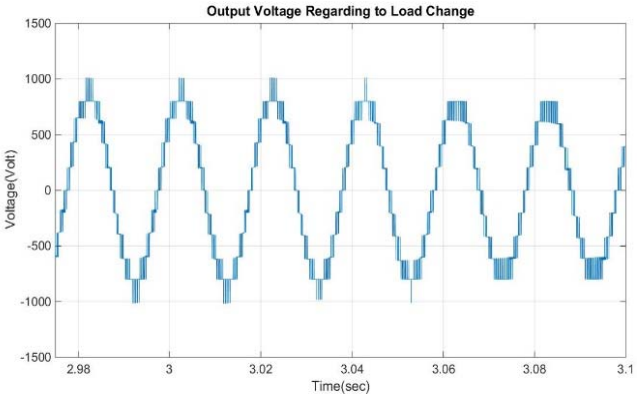

Fig. 6. Inverter Output Voltage with load change at t=3s

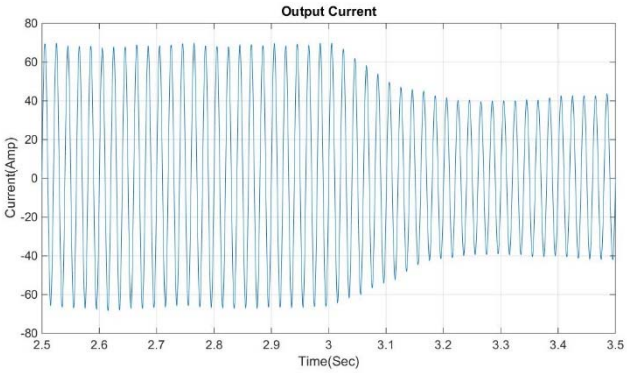

Fig. 7. Inverter Output Current (Reference Changes from 10kW to 7kW)

In Fig. 8 it can be seen that the capacitor voltage is fixed to 200V according to our set up and during the load change.

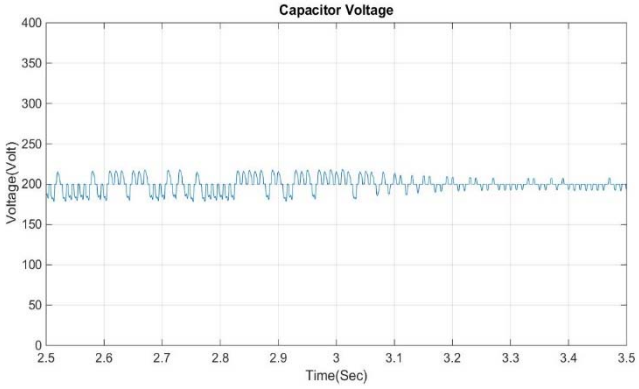

Fig. 8. Capacitor Voltage (Reference Changes from 10kW to 7kW)

The other test for verifying the grid tied multi-level inverter is changing P_{ref} from 7kW to 10 kW without changing the Q_{ref}. Fig 9 and Fig 10 show the active power and reactive power variation regarding to the change of active power at t=3s.

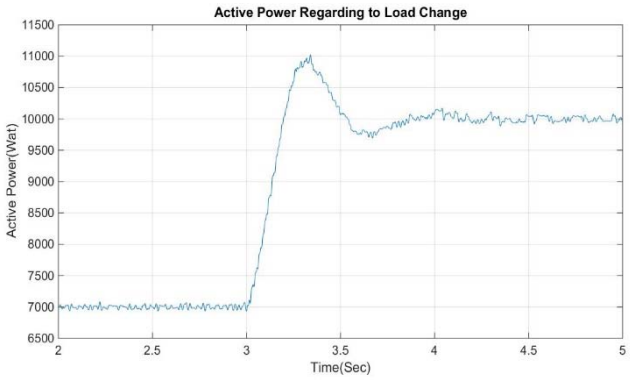

Fig. 9. Active Power to the Grid (Reference Changes from 7kW to 10kW)

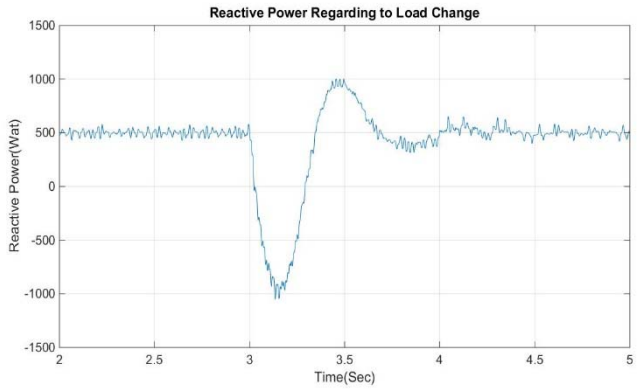

Fig. 10. Reactive Power to the Grid (Fixed Reactive Power Reference)

Fig.11 shows the output voltage of inverter when load changes from 7kW to 10kW. After t=3s, the level of voltage increases with THD improvement from 17% to 13%. Fig. 12 shows the output current which increase with load change and Fig. 13 presents the capacitor voltage which remains fixed during the load change.

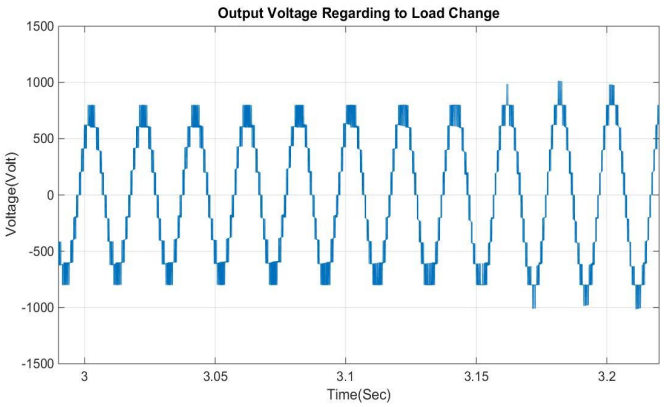

Fig. 11. Inverter Output Voltage with load change at t=3s

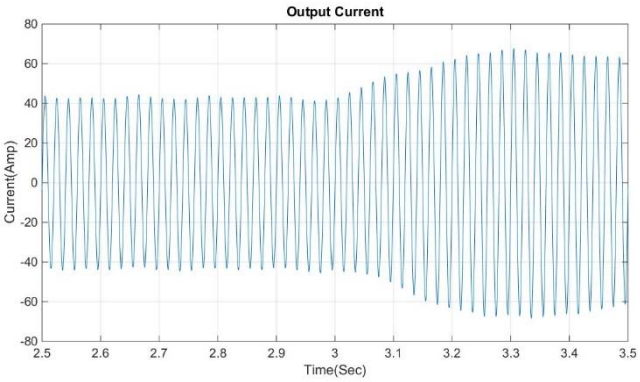

Fig. 12. Inverter Output Current (Reference Changes from 7kW to 10kW)

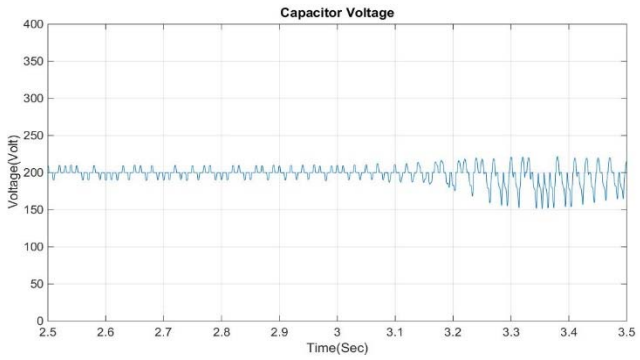

Fig. 13. Capacitor Voltage (Reference Changes from 7kW to 10kW)

V. CONCLUSION

In this paper a new 11-level cascaded multi-level inverter topology with multi-carrier level shifted PWM technique has been proposed. The main advantage of this new topology is that uses less number of switches to reach 11-level voltage in the output which causes simplicity in control and implementation, cost-effectiveness, low voltage stress. There is also no filter requirement in the output. The other good aspects for using this kind of topology are the ability to work with low switching frequency and capability to push higher amount of active power to the grid which could be useful for HVDC application. Simulation results also show that the system has a good dynamic performance to load change and the capacitor voltage tracks the reference value very well. The proposed scheme has limited modulation index range to retain all the voltage levels as shown, but the application may not be limited by this constraint.

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