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Grid Voltage Sensorless Single-Phase Half-Bridge Active Filter and DC Bus Voltage Regulation

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Abstract—In this paper, a method is presented for the control of grid voltage sensorless single-phase half-bridge shunt active power filter to reduce the grid current harmonics of low-power single-phase non-linear loads. The proposed system forces the grid current to be sinusoidal without sensing and processing the grid voltage on the line. For this reason, instead of grid voltage the load current is processed by using self-tuning filter to generate reference grid current to eliminate current harmonic distortions. In order to design a low-cost system, a half-bridge voltage source converter is used to reduce driver circuits. In addition, the switching losses are also reduced by employing half-bridge voltage source converter, where only two switches are used. The imbalance voltages are also successfully eliminated on the DC-side capacitors. The performance of the proposed system is verified by using a real-time platform, and experimental results are presented to verify the effectiveness of the proposed system in this study.

Keywords: active power filter, grid voltage sensorless, real-time experiment
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Color versions of one or more of the figures in the article can be found online at www.tandfonline.com/uemp.

1. INTRODUCTION

Harmonic distortion is a serious problem in the power systems. This is mostly due to the huge growth due to use of low-power electronic-based consumer products and the wide use of power semiconductor devices. Active power filters (APFs) have been developed and considered as a possible solution to eliminate the harmonic components of the non-linear loads. Therefore, shunt APF is one of the most investigated flexible alternating current transmission system (FACTs) devices and widely used in both single- and three-phase systems. The major components of an APF power system consist of a pulse width modulated (PWM) converter, DC energy storage element, current transformers (CTs), voltage transducers, AC-link inductance, and the associated control circuits. The power converter of an APF is controlled to create a converter current that is equal to the harmonic and reactive currents of the load(s). For this purpose, several strategies have been introduced in the literature, which applied to power filters play an important role in the improvement of the stability and performance of the system. The type of converters can be

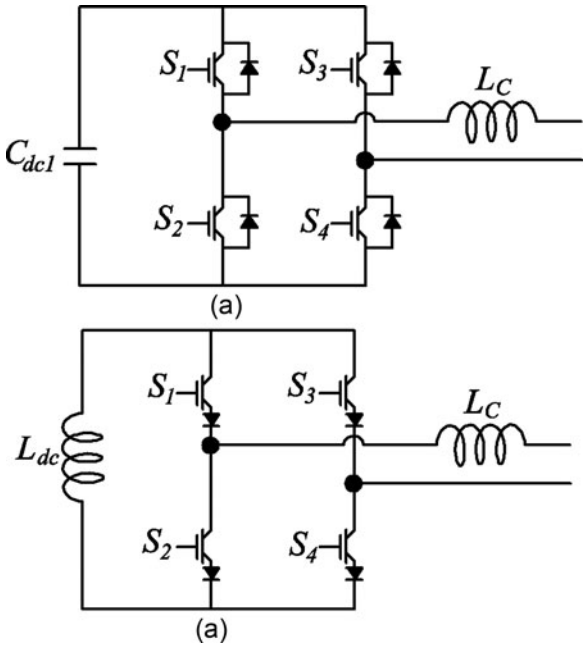


FIGURE 1. Single-phase half-bridge APF: (a) voltage source PWM converter and (b) current source PWM converter.

classified into single phase and three phases. Single-phase APFs are investigated in different topologies and control strategies [1]–[5]. There are also two main types of converters, *i.e.*, the voltage source converter (VSC) [4] and the current source converter (CSC). VSC is widely used to design the APF power stage. In this case, the VSC operates as a current-controlled voltage source. VSC and CSC shunt APFs were compared in Benchaita *et al.* [6] and Routimo *et al.* [7]. The filtering performances of both VSC- and CSC-based active filters are similar. However, the CSC-based APF is more complicated. The efficiency measurements in Routimo *et al.* [7] showed that VSC-based APFs have higher efficiency than the CSC. The main advantage of the VSC-based APF is in its capacitive energy storage element which is more efficient, smaller, and low-cost solution than CSC-based APF. Single-phase voltage source PWM converter equipment with a DC capacitor is seen in Figure 1(a) and single-phase CSC is seen in Figure 1(b).

Figure 2 shows a circuit configuration of a half-bridge VSC. This type of converter consists of two DC-link capacitors. Use of less driver circuit is one of the main advantages of the half-bridge topologies. Reduction on the switching power losses is another important advantage.

A lot of different work has been reported on the control of single-phase and three-phase APF. However, little attention has been paid toward the issues of voltage sensorless

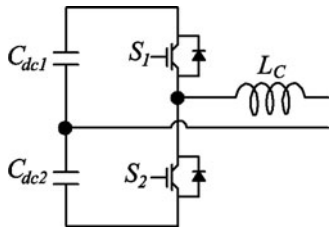


FIGURE 2. Single-phase half-bridge APF.

single-phase APFs. In order to reduce the manufacturing costs of the product, some research papers have been reported to reduce the number of sensors for both single-phase and three-phase APFs [1], [8], [9]. In Surendra and Sensarma [9], a parallel connected hybrid APF designed by using only one load current sensor and phase locking is achieved through a PLL by measuring grid voltages. In Wojciechowski [10], an estimation method is used on the three-phase APF to obtain three-phase voltages without measuring grid voltages. Some designers have attempted to use two current or two voltage sensors on the three-phase lines. By this method, the third-phase current or voltage information is obtained according to the other real measured two phases. In Ketzer and Jacobina [11], a strategy is proposed that involves measuring of the load currents only. In Barros and Perez [12], voltage sensorless control of full bridge single-phase APF based on SOGI algorithm is presented.

In this study, single-phase APF is investigated and only two switches with two capacitors are used on the DC terminal to reduce the number of switching devices and drive circuits. The voltage imbalances have been eliminated effectively. Moreover, switching losses are also reduced. By adapting self-tuning filter algorithm to the control system, the requirement to the grid voltage sensor is eliminated. As a result, only two sensors are used on the AC side of the system for only measuring the load and filter currents.

2. PROPOSED METHOD

In this work, the studied converter topology has two equal DC capacitors, (C_{DC1}, C_{DC2}). The AC side of the converter (midpoint of the switches) is connected to the phase of the grid with an inductor, L_c, and the midpoint of DC link is directly connected to the neutral point. The converter current, $i_C(t)$, is sensed by current transducer 2 (CT_2). Resistive and capacitive load groups are supplied from full-bridge diode rectifiers and current on the load terminal is measured by using current transducer 1 (CT_1). The studied single-phase half-bridge APF circuit is given in Figure 3.

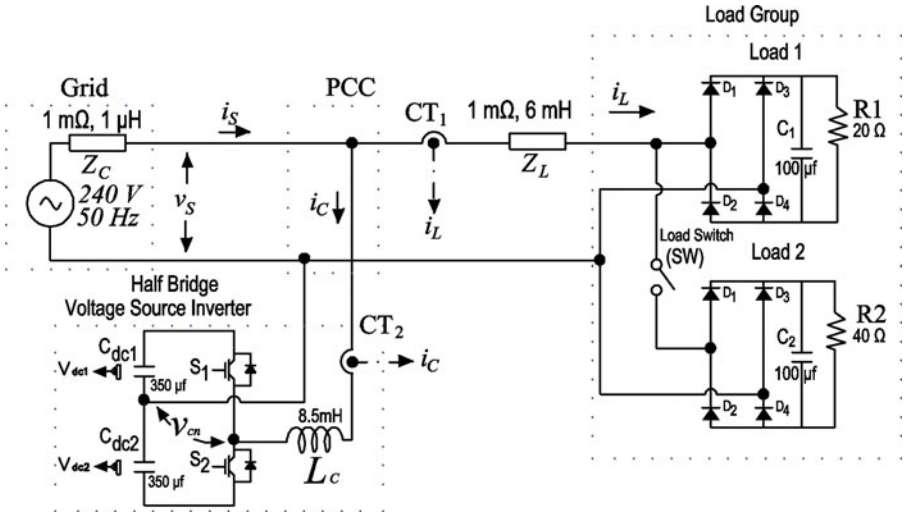


FIGURE 3. Studied single-phase half-bridge APF.

A non-linear load current in steady state is usually a periodic signal with only odd harmonics and can be given as

$$i_L(t) = \sum_{h=1}^{\infty} i_{L,h} \sin(h\omega t + \emptyset_h) = i_{L,1} \sin(\omega t + \emptyset_1) + \sum_{h=2}^{\infty} i_{L,h} \sin(h\omega t + \emptyset_h), \quad (1)$$

where ω is the angular frequency, and h and $\emptyset_h$ are the harmonic order and harmonic phase angle. As presented in Eq. (1), the consuming current of the non-linear load groups, $i_L(t)$, consists of current at the fundamental frequency, i_1, and harmonic currents $i_{L,h}$, *i.e.*,

$$i_L(t) = i_{L,1} + \sum_{h=2}^{\infty} i_{L,h}. \quad (2)$$

Therefore, Eq. (1) should be controlled to inject a current which is equal to the harmonics, $i_{L,h}(t)$, with opposite phase, *i.e.*,

$$i_C(t) = \sum_{h=2}^{\infty} i_{L,h} \sin(h\omega t + \emptyset_h). \quad (3)$$

It is well known that the control systems are designed to regulate voltage(s) on the DC link and to force grid current to become sinusoidal by controlling the current between the PCC and converter ($i_c(t)$) as

$$i_C(t) = \int \frac{v_s(t) - v_{cn}(t)}{L_c} dt. \quad (4)$$

In order to obtain reference compensation current amplitude of the fundamental current, I_s can be determined and multiplied with a unity sine function as

$$i_s^*(t) = I_s \sin(\omega t). \quad (5)$$

The amplitude of the current at the fundamental frequency can be determined by using a proportional integral (PI) regulator as

$$I_s = k_p \left(v_{DC}^* - [v_{DC1} + v_{DC2}]\right) + k_i \int \left(v_{DC}^* - [v_{DC1} + v_{DC2}]\right) dt, \quad (6)$$

where k_p and k_i are the proportional and integral gain of the DC-link PI regulator. The proper PI parameters, k_p and k_i, are obtained by trial and error method [13]. Voltage on the capacitors is equal to the half of the DC-link voltage, *i.e.*, $v_{DC}/2$. Therefore, voltages on the capacitors are added to determine total DC-link voltage, *i.e.*, ($v_{DC} = v_{DC1} + v_{DC2}$). PI regulator forces the DC-link voltage, v_{DC}, to follow pre-settled DC constant value, v_{DC}^*, during power exchange between the grid and the converter.

2.1. Determination of the Unity Sine Function by Sensing Grid Voltage Waveform

There is need to determine a unity sine function to use in Eq. (1). Generation of the unity sine function by using the measured grid voltage, (U_s.sin(ωt)), is a mostly preferred solution in the literature. The unity sine function of grid voltage, $\phi_v(t)$, can be obtained as

$$\varphi_v(t) = \frac{1}{U_s} [U_s . \sin(\omega t)], \quad (7)$$

where U_s is the amplitude of the grid voltage. However, the result in Eq. (1) can be difficult to obtain when grid voltages

are distorted, *i.e.*, contain harmonics. The distorted voltages usually occur because of the non-linear load current on the system or saturated transformers. Under such conditions, the pure sinusoid in Eq. (1) cannot be obtained correctly, causing degradation in the system performance. As a consequence, it may not be possible to reduce grid-current THD to less than 5%, as specified in IEEE 519-1992.

2.2. Determination of the Unity Sine Function Without Sensing Grid Voltage Waveform

As distinct from above-mentioned method, the unity sine function is generated by processing the load current waveform, i_L, with self-tuning algorithm (STF). Therefore, there is no need to sense grid voltage in the proposed control system. This algorithm needs two-phase input signal where the phase difference should be 90° between the phases [14]. In the three-phase system, this requirement is obtained by converting the three-phase currents to two-phase coordinate system using Clark transformation. In order to solve this issue, the sensed load current is considered as $i_\alpha(t)$ as

$$i_\alpha(t) = i_L(t) = I_L \sin(\omega t), \tag{8}$$

and a second phase is generated for the STF input by 90° phase shifting as in Biricik and Hasan [15], *i.e.*,

$$i_\beta(t) = I_L \sin\left(\omega t + \frac{\pi}{2}\right). \tag{9}$$

In this study, this shifting is obtained within the field programmable gate array (FPGA) but it is also can be obtained by using analog circuit as presented in Huang [16]. After applying the phase shifting as in Eq. (1), $i_\alpha(t)$ and $i_\beta(t)$ will still have harmonic components $\widetilde{i}_\alpha(t)$and $\widetilde{i}_\beta(t)$, respectively, *i.e.*,

$$i_\alpha(t) = \bar{i}_\alpha(t) + \widetilde{i}_\alpha(t), \tag{10}$$

$$i_\beta(t) = \bar{i}_\beta(t) + \widetilde{i}_\beta(t). \tag{11}$$

As mentioned above, fundamental harmonics $\bar{i}_\alpha(t)$ and $\bar{i}_\beta(t)$ are first obtained by STF algorithm as

$$\bar{i}_\alpha(s) = \frac{k_1}{s}\left[i_\alpha(s) - \bar{i}_\alpha(s)\right] - \frac{\omega}{s}\bar{i}_\beta(s), \tag{12}$$

$$\bar{i}_\beta(s) = \frac{k_1}{s}\left[i_\beta(s) - \bar{i}_\beta(s)\right] + \frac{\omega}{s}\bar{i}_\alpha(s). \tag{13}$$

Finally, the required unity sine function can be obtained by dividing the $\bar{i}_\alpha(t)$ with the amplitude of load current at fundamental frequency, $\bar{I}_\alpha$, as

$$\varphi_i(t) = \frac{\bar{i}_\alpha(t)}{\bar{I}_\alpha}. \tag{14}$$

It is important to mention that the determined unity sine function in Eq. (1) will vary between +1 and −1 Volt. However, due to the initial delay of the STF algorithm, the amplitude of the load current at the fundamental frequency, $\bar{I}_\alpha$, will be obtained after a cycle. This means that in the first or second cycle, the calculated $\bar{I}_\alpha$ will be less than amplitude of the load current at the fundamental frequency. As a result of this, output of Eq. (1) will be extremely high when the APF is turned ON. Solution of this, the obtained signal with Eq. (1) should be limited between +1.01 and −1.01 Volt by using a limiter as in Eq. (1).

$$\lambda(t) = \begin{cases} 1.01 & \text{when } \varphi_i(t) > 1 \\ \varphi_i(t) & \text{when } \varphi_i(t) < 1 \text{ and } < -1 \\ -1.01 & \text{when } \varphi_i(t) > -1 \end{cases}. \tag{15}$$

Now the reference waveform of grid current, i_s^*, can be determined by multiplying the amplitude of the grid current, I_s, with $\lambda(t)$ as in Eq. (1).

$$i_s^*(t) = I_s.\,\lambda(t). \tag{16}$$

It should be noted that there is no low- or high-pass filter in the proposed control algorithm. After obtaining the reference grid current, $i_s^*(t)$, the required reference compensation current, $i_c^*(t)$, can be determined by subtracting it from the sensed load current that is

$$i_C^*(t) = i_s^*(t) - i_L(t). \tag{17}$$

In this point, the current error, Δi_c, can be determined by subtracting reference compensation current from the sensed compensation current, i_c, thus,

$$\Delta i_c(t) = i_c^*(t) - i_c(t). \tag{18}$$

In the ideal conditions, subtraction of v_{DC1} from v_{DC2} should be zero. However, this is not possible in practice and these unbalanced voltages on the capacitors can be determined as

$$\Delta e_{DC}(t) = v_{DC1}(t) - v_{DC2}(t). \tag{19}$$

The existence of the imbalance in the capacitor voltages, $\Delta e_{DC}(t)$, may cause due to some DC offsets in the controller's analog components and non-equal capacitance sizes in practice. To ensure that the DC-link capacitors remain equally charged, a DC-link balance loop is included by feeding back the imbalance variable as

$$\gamma i_c(t) = \Delta i_c(t) + k_{DC}.\Delta e_{DC}(t), \tag{20}$$

where k_{DC} is a gain value on the imbalance loop. The final compensation current, $\gamma i_c(t)$, error in Eq. (1) is used to drive converter switches. In this study, a limit of the compensating current is controlled by a Hysteresis Current Controller, which

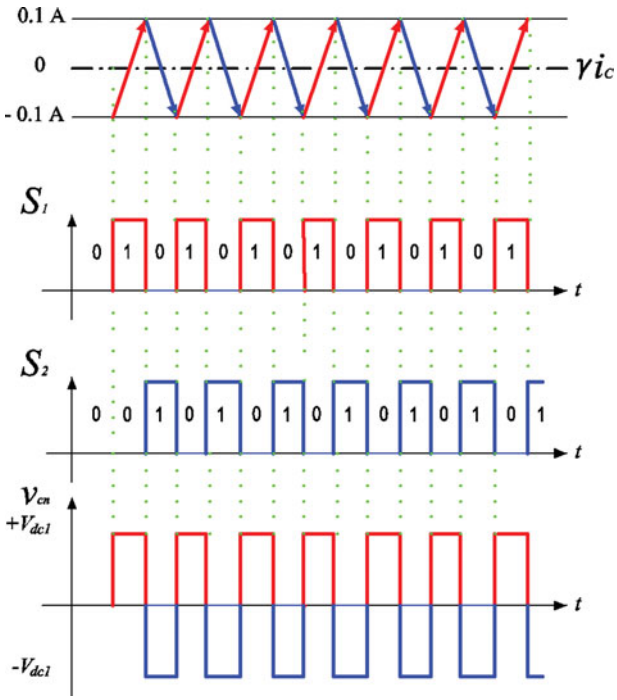


FIGURE 4. PWM gating signals generation with current error, $\gamma i_c(t)$, for the switching devices S_1 and S_2.

has been widely used for active filter applications because of its simple implementation [19], [20], [25].

The switching periods of S_1 and S_2 can be seen in Figure 4 (later experimentally in Figure 8). When $\gamma i_c(t)$ hits to the upper limit, S_1 is turned OFF and S_2 is turned ON. When γi_c hits to the lower limit, then S_1 is turned ON and S_2 is turned OFF. Although the hysteresis current controls simplicity in implementation, this method offers strong robustness and fast dynamic response. The disadvantage of this method is that the switching frequency is not constant, which may vary between 5 kHz and 12 kHz [17]–[20]. In order to solve this problem, many control strategies have been proposed in the literature to mitigate the switching frequency. However, the effect of high switching frequency variation is insignificant in the use of low-power applications. The proposed control method is presented in Figure 5.

Symbol	Quantity	Value
v_s	Grid voltage (RMS)	240 V
F	Grid frequency	50 Hz
R_L, L_L	AC load line resistance and inductance	1 mΩ, 6 Mh
L_c	Filter inductance	8.5 mH
C_{f1}, C_{f2}	DC capacitors	350 μF, 350 μF
v^*_{DC}	DC bus reference voltage	480 V
k_1	STF gain	50
k_{DC}	Basbar balance gain constant	0.004
k_i	Integral gain	3
k_p	Proportional gain	0.02
T	Sample time	15 μs
R_1, C_1	DC load resistance and capacitance	20 Ω, 100 μF
R_2, C_2	DC load resistance and capacitance	40 Ω, 100 μF

TABLE 1. The used system parameters.

3. LABORATORY RESULTS

The performance of the proposed system is tested by using RT-LAB real-time platform (Opal-RT Technologies, Montreal, Quebec, Canada) and results are presented in this section. The studied control system is realized on an FPGA architecture using the Xilinx system generator toolbox (Xilinx, Inc., San Jose, California, USA). The system is then tested after the real-time measurement of actual signals and implementation of the control signals [14], [15], [21].

The used parameters are given in Table 1. Laboratory results are observed in a digital storage oscilloscope and presented in Figures 6–13. Current harmonic pollution of

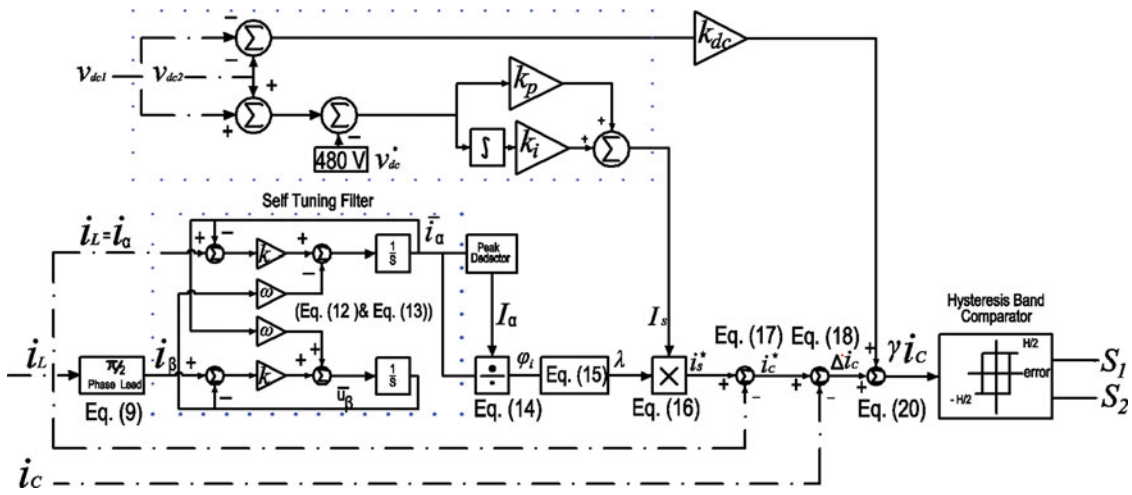
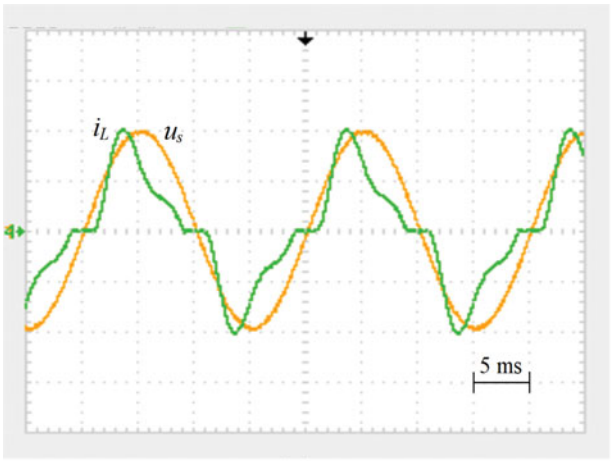
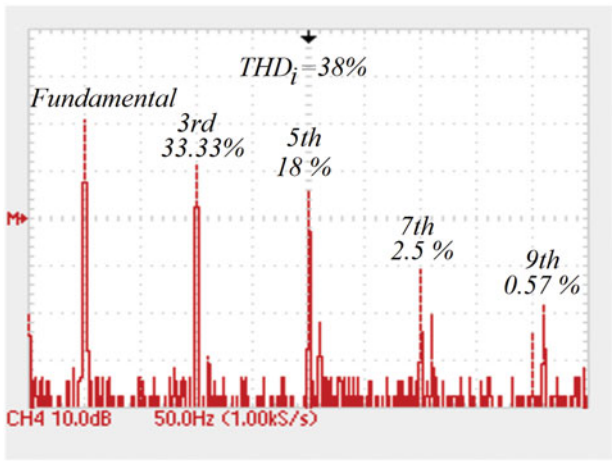


FIGURE 5. Proposed control system.



(a)



(b)

FIGURE 6. (a) Grid voltage, u_s, (170 V/div) and load current, i_L, (10 A/div) and (b) harmonic spectrum of the load current.

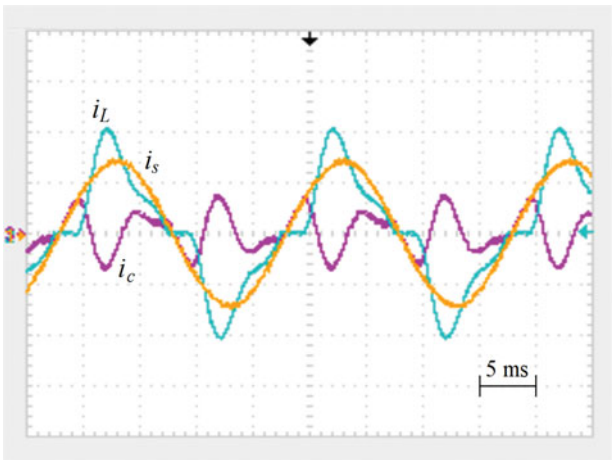


FIGURE 7. Grid current (yellow labeled), i_s, (10 A/div), load current (blue labeled), i_L, (10 A/div), and converter current (purple labeled), i_c, (10 A/div).

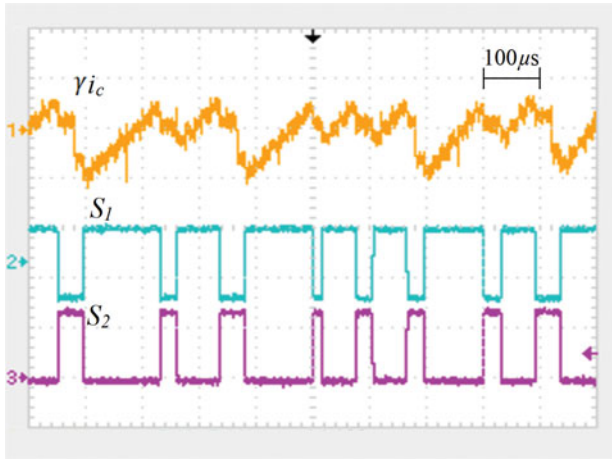
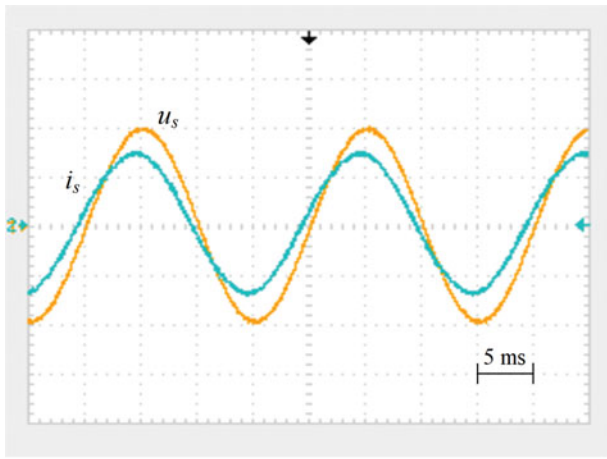
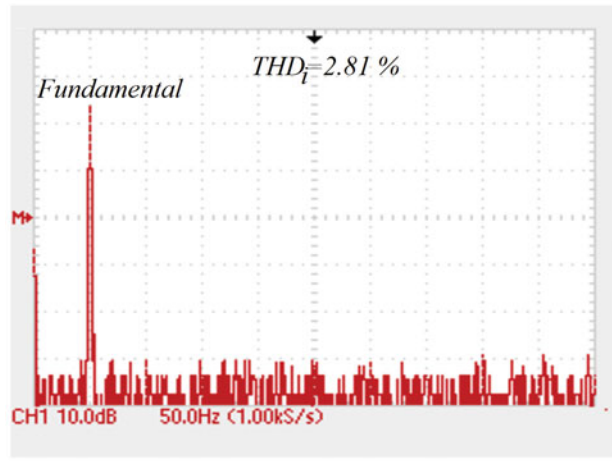


FIGURE 8. Current error, γi_c, and PWM operation in a single-phase half-bridge converter (S_1 and S_2).



(a)



(b)

FIGURE 9. (a) Grid voltage, u_s, (170 V/div) and grid current, i_s, (10 A/div) and (b) harmonic spectrum of the load current.

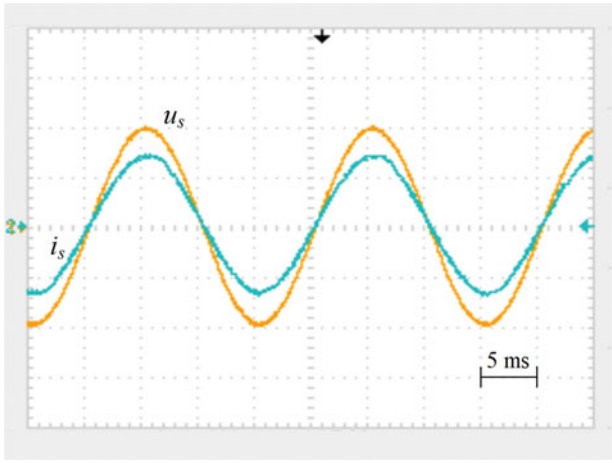


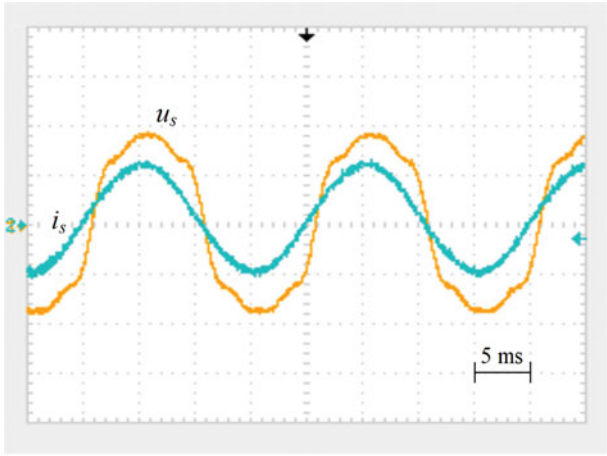
FIGURE 10. Grid voltage, u_s, (170 V/div) and grid current, i_s, (10 A/div).

load 1 is 38.00%, while the RMS current is 9.81 A. In order to observe reaction of the proposed system during dynamic load current change, a second load is used. When the Load 1 and Load 2 are connected together, the total load RMS current increased to 16.38 A and THD is 38.75% on the load terminal. Figure 6(a) shows the grid voltage, u_s, and load current, i_L, waveforms during operation of Load 1, and current harmonic spectrum of the Load 1 is given in Figure 6(b). As can be seen that the load current, i_L, is highly distorted.

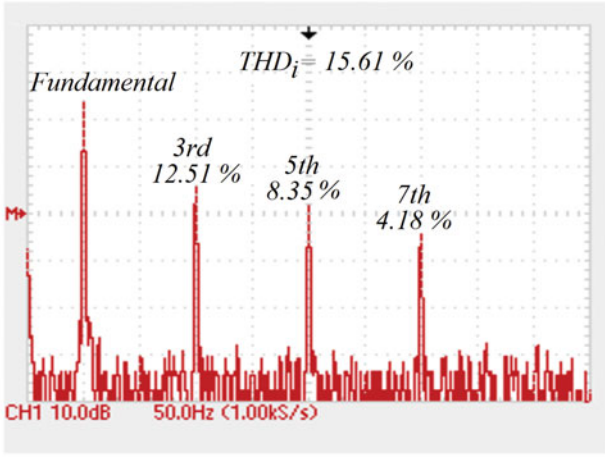
The injected current, i_c, by the half-bridge single-phase converter, can be seen in Figure 7, with the grid and load currents. The current error, λ (t), with switching pulses of S_1 and S_2 can be seen in Figure 8.

As a result of this, undistorted sinusoidal current waveform is obtained at the grid side, as can be seen in Figure 9(a), after effective suppression of the third-, fifth-, seventh-, and ninth-level harmonics (see Figures 6(b) and 9(b)). Current harmonic spectrum of the grid current is given in Figure 9(b). THD measurement shows that the distortion on current reduced to 2.79% during operation of Load 1, and it is suppressed to 2.61% during operation of both loads, which meets the IEEE 519–1992 recommended standard.

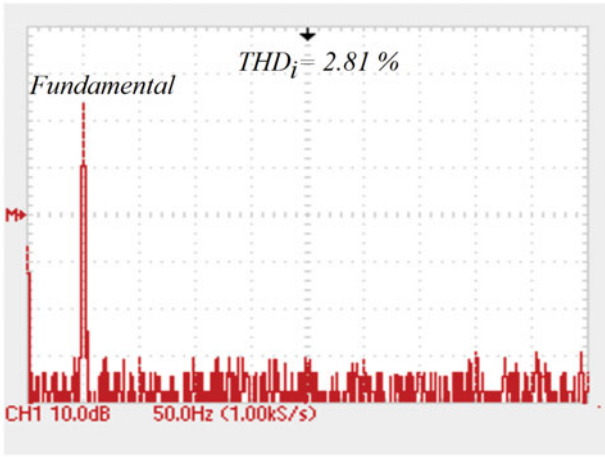
Grid voltage sensorless APF control method for the low-power ratio 1 phase non-linear loads can be a cost-effective solution. On the other hand, proposed single-phase APF is designed for low-power single-phase non-linear loads. Therefore, the compensation of the reactive power is not the aim of this study. As expected, the grid current and voltage waveforms are not in phase, as can be seen in Figure 9(a). Advantage is gained here, the converter power ratio can be designed by only considering power of the harmonic components, which require less power in achieving the goal of harmonic compensation. For this, the proposed control method is,



(a)



(b)



(c)

FIGURE 11. (a) Grid voltage, u_s, (170 V/div) and grid current, i_s, (10 A/div), (b) harmonic spectrum of the distorted grid voltage, and (c) harmonic spectrum of the grid current after filtering.

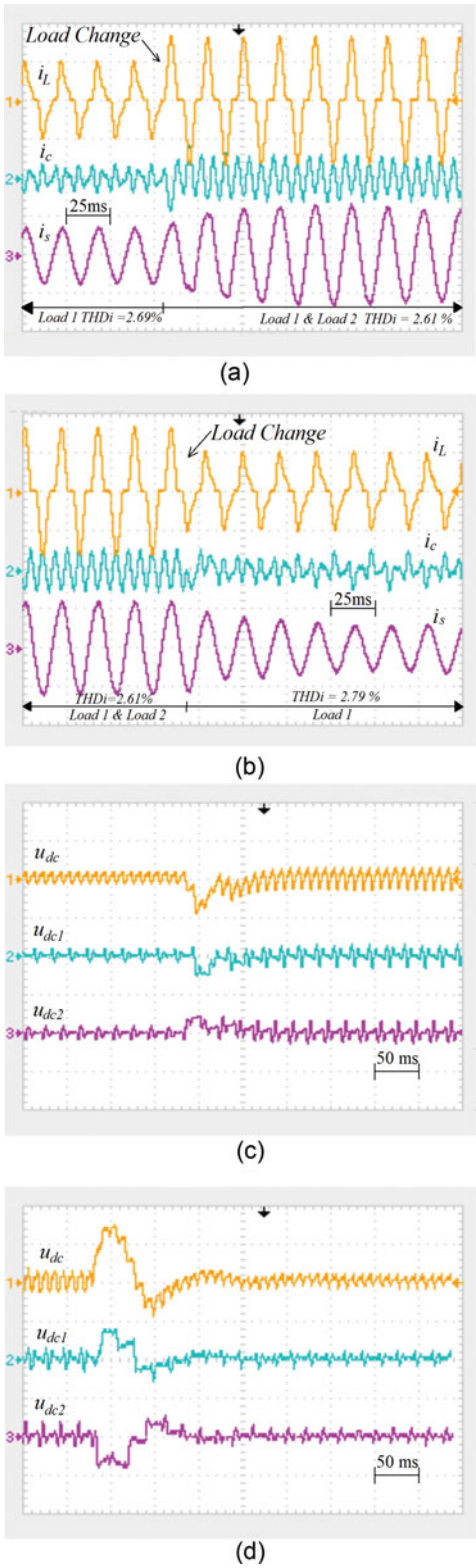


FIGURE 12. System responses during load current changes: (a) filtered grid current during load increasing, (b) filtered grid current during load decreasing, (c) u_{DC}, u_{DC1}, and u_{DC2} voltages during load increasing, and (d) u_{DC}, u_{DC1}, and u_{DC2} voltages during load decreasing.

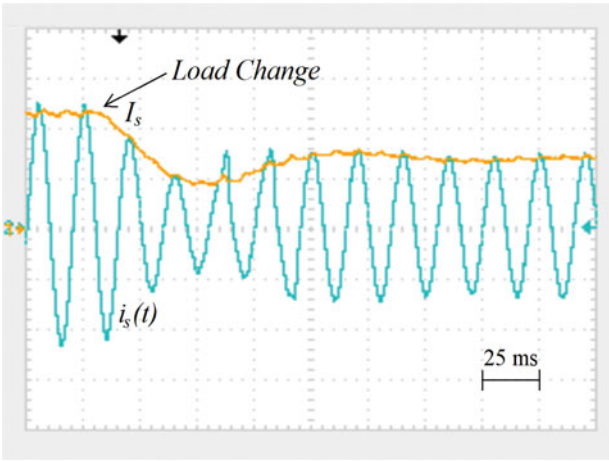


FIGURE 13. Output of the proportional integral (PI) regulator, I_s, and grid current waveform, i_s.

however, not recommended for high-power inductive loads operation or for three-phase APF applications, because power factor of the load will not change at the grid side. This control method can be also applied to the studied topology by adding AC voltage sensor to generate unity sine function as discussed in Section 2.1. In this case, the proposed method will be capable of compensating reactive power with the current harmonics. The viability of the proposed modification is verified by the experimental validation, as seen in Figure 10.

An additional advantage is gained here due to the fact that the problem of grid voltage distortion on the performance of the system is broken. The proposed system is also verified under distorted grid voltage condition to verify the performance of the control system. As can be seen in Figure 11(a), the source voltage, u_s, is highly distorted. The THD of the source voltage is measured as 15.61%. As a result, the grid current, i_s, harmonics are effectively compensated, as can be seen in Figure 11(a). Harmonic spectrum of the grid current after filtering is also given in Figure 11(b).

The dynamic performances of the system during an average load change of 35% are observed. As can be seen in Figures 12(a) and (b), the proposed control method compensated the grid current dynamically under upload and down load changes. Moreover, the DC-link capacitors voltages are maintained with the proposed control method as required during the fast load change and u_{DC1} and u_{DC2} are maintained at equal voltage level. Figures 12(c) and (d) show u_{DC}, u_{DC1}, and u_{DC2} voltage variations during load change. It is also clear that voltages are almost equally distributed among the capacitors ($u_{DC1} \approx u_{DC2}$). Figure 12 also shows that the minimum response time is 50 ms and maximum response time is 150 ms in this study. This response time is comparable to response times observed by relevant systems reported in the literature [19], [22]–[25].

The performance of the studied PI regulator for the half-bridge converter is also presented in Figure 13. The amplitude of the current at the fundamental frequency (yellow labeled), I_s, is obtained properly.

4. CONCLUSION

In this study, a single-phase APF is designed for the low-power single-phase non-linear loads. A cost-effective method is proposed to control grid voltage sensorless half-bridge single-phase active filter to suppress harmonic current pollutions and to balance DC-link capacitor voltages.

This method allows for the design of a simple control circuit, which requires only two offset circuits and two drive signal outputs on the microcontroller. In addition, the switching loss is also reduced by employing a half-bridge voltage source converter, where only two switches and two drive circuits are used. It provides low-cost small-scale APFs with a simple structure but very effective suppression of current harmonic distortions of low-power non-linear loads. An additional advantage is gained here due to the fact that the problem of grid voltage distortion on the system performances is broken. The steady-state and dynamic performance of the system are verified with the experimental study.

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