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An LCL-Filter Design with Optimum Total Inductance and Capacitance

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An *LCL*-Filter Design With Optimum Total Inductance and Capacitance

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***Abstract*—*LCL*-filter is among the best performing filters for grid-connected voltage source inverters. Designing of the filter parameters (grid-side and inverter-side inductors and capacitor), takes an iterative approach due to the coherence between the parameters and design requirements such as IEEE-519 Std for harmonic current limitations, reactive power compensation limit, and maximum allowable voltage drop across the filter to limit the switching losses. Most of the proposed *LCL*-filter optimization strategies emphasize on reducing the total inductance and losses of the filter while meeting the design requirements. There is less emphasis given on the capacitor selection and optimizing its value. Therefore, this paper proposes a method to compute the optimum capacitance requirement of the *LCL*-filter based on reactive power compensation of the filter rather than calculating it as a percentage of base capacitance of the filter as found in the literature. The proposed design methodology compared to the previously proposed designs is capable of reducing filter capacitance by 50% while meeting the harmonic limitation demanded by IEEE-519 Std and also considers the impact of the total inductance on reactive power compensation. Based on the proposed methodology an *LCL*-filter with minimum total inductance and capacitance is realized. Functionality of the proposed *LCL*-filter is verified and validated through simulations and experimental results.**

***Index Terms*—Grid-connected inverter, harmonics, IEEE-519, *LCL*-filter, power quality.**

I. Introduction

MODERN day power electronic systems face the challenge of meeting the volume restrictions demanded by end-users and strict power regulation standards set by bodies such as the IEEE. Among such systems, a passive filter in grid-connected voltage source inverter (VSI) demands small filter size and the harmonic limitations set by IEEE-519 standard. Ideally, the main function of these filters is to attenuate the high-frequency switching components produced during pulse width modulated (PWM) switching to inject harmonic-free current into the grid. Initially, *L*-filters were used to attenuate these harmonics, but recently higher order filters such as an *LCL*-filter is used as it offers substantial advantages over an ordinary *L*-filter [1]–[3]. The primary advantages are reduction in the total inductance requirement, which contributes to improve in output dynamics of the inverter, economical filter design, reduced losses in the filter [2], [4], and higher attenuation of harmonics after the resonance frequency at a rate of 60 dB/decade compared to 20 dB/decade with an *L*-filter [2]. Contrary to advantages, *LCL*-filter possesses a resonance frequency that distorts the grid-injected currents. Therefore, this resonance frequency needs to be mitigated successfully using either passive or active resonance damping methods [5]–[10].

The nature of *LCL*-filter is such that there can be numerous parameter combinations for a given inverter application. However, following benchmark variations define the range of each parameter in an *LCL*-filter:

1) range of capacitance in an *LCL*-filter;
2) based on power factor decrease or based on reactive power compensation limit;
3) range of total inductance in an *LCL*-filter;
4) based on the limit of grid-side (L_g) and inverter-side (L_i) inductance ($\mu = L_g/L_i$);
5) based on IEEE-519 standard for harmonic limitations;
6) based on reactive power compensation;
7) based on the dc bus availability or voltage drop across filter.

As a result, most of the filter designs proposed in the literature take an iterative approach and more often these designs are customized for different operating regions [8], [9] and applications [1]–[4], [12]–[14]. Recently, the filter designers have considered the variation of external parameters such as grid impedance to realize a more robust *LCL*-filter [9] and also designing *LCL*-filters with *LCL* resonance frequencies beyond the Nyquist frequency [11]. Given all these different *LCL*-filter design methodologies, one can identify that common design objective is on reducing the total inductance in an *LCL*-filter in order to reduce the volume of the filter while ensuring minimum losses in the filter. There is hardly any research in optimizing the value of the capacitance and it is generally estimated as a percentage of the base capacitance of the *LCL*-filter [15]–[17]. Furthermore, the impact of total inductance on the reactive power compensation limits is rarely studied. Therefore, in this paper, an approximate mathematical equation is derived to define the reactive power compensation limit of the grid-connected VSI taking into account the effects of both inductive and capacitive elements in an *LCL*-filter. The value of capacitor calculated based on the

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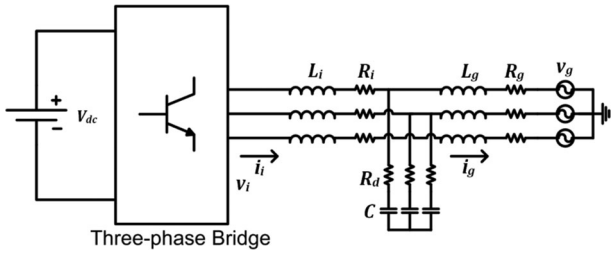


Fig. 1. Grid-connected three-phase VSI with Y-connected *LCL*-filter.

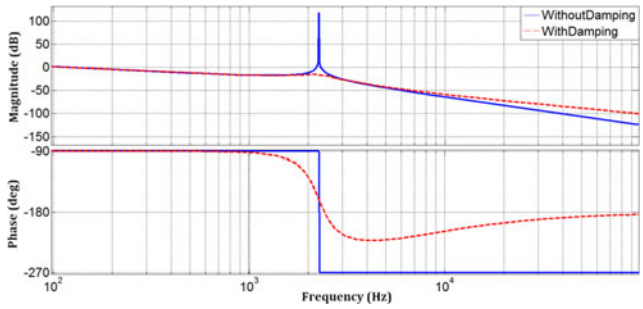


Fig. 2. Bode plot of *LCL*-filter with and without damping.

proposed design procedure is much less than the method based on the percentage of the base capacitance found in the literature [15]–[17]. The reduction of the capacitor was realized by considering the impact of the total inductance on reactive power compensation, which most of the proposed designs in the past failed to identify. The proposed design is also capable of realizing the required attenuation demanded by IEEE-519 with a minimum total inductance and it can also be extended for designing filters for high-power inverters. Furthermore, resulting inductance is minimum when compared to conventional methods, which helps to reduce the overall size of the filter.

The rest of the paper is organized as follows: The basic system description of an *LCL*-filter with the limits of capacitance, reactive power, and total inductance are presented in Section II. The proposed optimum *LCL*-filter design is presented in Section III. Simulations and experimental results are presented in Section IV to validate the efficacy of the proposed optimum *LCL*-filter design.

II. *LCL*-Filter Design

Fig. 1 shows the general structure of the grid-connected three-phase VSI with Y-connected *LCL*-filter, where L_i and L_g are the inverter-side and grid-side inductors, respectively. R_i and R_g are the resistances of the inverter and grid-side inductors, respectively. C is the filter capacitor with series damping resistance R_d.

Grid voltage is assumed to behave as an ideal voltage source at medium and high frequencies, which is capable of sinking all harmonics when deriving the *LCL*-filter transfer function that is responsible for the closed-loop system bandwidth in grid-connected operation of the inverter [13]. All the parasitic resistors (R_d, R_i, and R_g) are neglected to represent the worst case damping performance of the system [13]. For grid-side current control [13], [18]

$$\frac{i_g(s)}{v_i(s)} = \frac{1}{s^3 L_i L_g C + s\left(L_i + L_g\right)} \tag{1}$$

where i_g and v_i are grid-side current and inverter-side voltage, respectively. Resonance frequency (f_{res}) of the *LCL*-filter with Y-connected capacitor is given by [13]

$$f_{\text{res}} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i L_g C}}. \tag{2}$$

Resonant peak at resonance frequency needs to be damped either using active or passive damping to ensure proper operation of the grid-connected VSI. In this paper, passive damping is used due to the ease of controller implementation. Addition of R_d modifies the transfer function in (1) to (3)

$$\frac{i_g(s)}{v_i(s)} = \frac{s R_d C + 1}{s^3 L_i L_g C + s^2\left(L_i + L_g\right) R_d C + s\left(L_i + L_g\right)}. \tag{3}$$

R_d is given by [14]

$$R_d = \frac{1}{3\omega_{\text{res}} C}. \tag{4}$$

Bode plots of the transfer function in (1) without damping and in (3) with damping are shown in Fig. 2.

Equation (2) can be modified to obtain (5) and (6)

$$L_T C = \frac{1}{4\pi^2 f_{\text{res}}^2}\frac{(1+\mu)^2}{\mu} \tag{5}$$

where the total inductance, $L_T = L_i + L_g$ and ratio $\mu = L_g/L_i$.

Per unit derivation of filter passive components are considered in the evaluation to generalize the design for wide range of power levels and to make sure that the filter design procedure complies with the ratings of the grid power system where most impedances are expressed in per unit basis [13]. For a unity system (5) becomes [9]

$$l_T c = \left(\frac{f_b}{f_{\text{res}}}\right)^2 \frac{(1+\mu)^2}{\mu} \tag{6}$$

where l_T is the per unit total inductance, $l_T = 2\pi f_b L_T / Z_b$, c is per unit capacitance, $c = 2\pi f_b C Z_b$, the base impedance of the system, $Z_b = V_{l\text{-}l}^2/P_b$, $f_b = f_g$, where f_g is the grid operating frequency, $V_{l\text{-}l}$ is line to line rms grid voltage, P_b is base power and $P_b = P_r$, where P_r is the rated active power. Equation (1) provides information about the attenuation of an *LCL*-filter, whereas (6) shows the relationship between the factors that determine the passive components l_T and c. In (6), product of $l_T c$ is dependent on the ratio μ and f_{res} and it is always preferable to realize an *LCL*-filter with minimum passive component size [minimum product of $l_T c$ according to (6)] while not compromising the attenuation requirements of (1) according to IEEE-519 harmonic limitations [19] and reactive power compensation limits. The sections below will analyze the range of capacitance and total inductance in an *LCL*-filter.

A. Range of Capacitance in an LCL-Filter

According to the previously proposed designs [2], [4], [14], filter capacitance (C) is selected to limit the overrating of the inverter or reduction in power factor of the inverter. Base impedance of an *LCL*-filter is given by

$$Z_b = \frac{V_{\mathrm{gl}-l}^2}{P_r} \tag{7}$$

where $V_{\mathrm{gl}-l}$ and P_r are line to line grid voltage and rated power, respectively. Base capacitance is given as

$$C_b = \frac{1}{\omega_g Z_b}. \tag{8}$$

Filter capacitance is limited to a maximum of $\lambda\%$ to limit the decrease in power factor. Usually maximum value of $\lambda = 5\%$ is used for grid-connected inverters as reported in [14] and [15]. Filter capacitor becomes [14]

$$C = \lambda\, C_b. \tag{9}$$

As per the literature, this defines the limit of capacitance variation expected around a given resonance frequency and it is always considered to be equal or less than the maximum defined by (9)

$$0 < C \leq \lambda C_b. \tag{10}$$

However, this paper proposes a method to compute the optimum capacitance of the *LCL*-filter by considering the optimum reactive power compensation and total inductance limits of the filter.

B. Limit on Reactive Power (q)

If the active power of the inverter is given by p and the reactive power by q, the power factor (P_{f}) of the inverter output will be

$$P_f = \frac{\text{real power}}{\text{apparent power}} = \frac{p}{\sqrt{p^2+q^2}}. \tag{11}$$

The inverter overrating is given by the apparent power of the inverter and increase in apparent power will reduce the power factor and overrate the inverter according to (11). For an inverter operating at unity power factor, per unit maximum active power will be one ($p = 1$). Minimum limit on the reactive power production will determine the maximum power factor operation of the inverter

$$P_{f\_\max} = \frac{1}{\sqrt{1+q_{\min}^2}}. \tag{12}$$

It is recommended that the operating power factor should be closer to unity in most grid-connected applications [2], [9]. Hence, filter is designed such that it does not exceed a specified limit of reactive power chosen by the designer ($q_{\min}$).

C. Range of Inductance in an LCL-Filter

The choice of total inductance is dependent on:

1) ratio between grid-side (L_g) and inverter-side (L_i) inductance ($\mu = L_g/L_i$);
2) reactive power compensation limit;
3) harmonic attenuation limits specified in IEEE-519 standard;
4) voltage drop across the filter.

Importance of determining the correct ratio between L_g and L_i are extensively investigated in the literature [9]. It can be concluded from those analyses that selecting $\mu = 1$ will result in the minimum inductance and capacitance contributing to minimum voltage drop, moderate switching losses, improved dynamic response, minimum reactive power produced, minimum stored energy in an *LCL*-filter, reasonable attenuation of switching harmonics, economical filter and a robust *LCL*-filter against the variation of grid impedance [9].

Initially, this paper will show how setting a limit on reactive power compensation will define the limits on capacitance and inductance of an *LCL*-filter. Inclusion of capacitor in an *LCL*-filter will alter the control system depending on the position of voltage and current sensing. In other words, inverter needs to compensate the reactive power produced by the filter to operate with unity power factor at the point of common coupling (PCC) [2]. In the literature, many designs consider the amount of reactive power compensated as a percentage of base capacitance as discussed above in Section II-A [2], [14]–[17]. In this paper, a mathematical equation is derived based on the control structure to determine the inductance limit for a given reactive power compensation limit and then to compute the capacitance of the filter by taking into account the inductive effect on reactive power compensation. Since most of the inverters operate by sensing grid-side voltage and controlling grid-side current, here derivation of reactive power is based on it. A similar approach can be used for other control scenarios as well [2]. Output power of the inverter (p) expressed in per unit with active power injected by the converter is 1 p.u. and is given by

$$p \approx 1 - j\,[l_T - c]\,. \tag{13}$$

The proof of (13) is summarized in the Appendix. Where l_T and c are per unit total inductance and capacitance. The per unit reactive power (q) of the inverter can be deduced from (13) as

$$q \approx [l_T - c]\,. \tag{14}$$

In order to avoid the increase in the rating of the inverter, given by (11) or drop in power factor, given by (12) due to reactive power, the reactive component of the filter should be theoretically zero. But this is practically impossible as it will result in higher values of inductances, which will take away the primary advantage offered by low inductance of *LCL*-filters when compared with *L*-filters. This issue is addressed in this paper, by selecting the parameter "c" as small as possible and parameter "l" as high as possible to preserve the minimum limitation on reactive power compensated without overrating the inverter too much. This design methodology will determine the first limit on inductance based on reactive power compensated and also the optimum capacitance. Minimum limitation on q can be set by selecting minimum $c(c_{\min})$ and maximum $l_T(l_{T\max 1})$ to ensure desired reactive power compensation. Equation (14) can be modified to

$$q_{\min} \approx [l_{T\max 1} - c_{\min}]\,. \tag{15}$$

TABLE I
CURRENT HARMONIC LIMITS ACCORDING TO IEEE-519 [19]

	Limits as a percentage of rated current amplitude					
I_{sc}/I_L	$3 \le h \le 11$	$11 \le h \le 17$	$17 \le h \le 23$	$23 \le h \le 35$	$35 \le h \le 50$	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0

Substituting (15) in (6) results in

$$(l_{T\max 1} - q_{\min})\, l_{T\max 1} = \left(\frac{f_b}{f_{\text{res}}}\right)^2 \frac{(1+\mu)^2}{\mu}. \tag{16}$$

Equation (16) simplifies to

$$l_{T\max 1}^2 - q_{\min} l_{T\max 1} - k^2 \left(\frac{f_b}{f_{\text{sw}}}\right)^2 \frac{(1+\mu)^2}{\mu} = 0 \tag{17}$$

where $k\,(= f_{\text{sw}}/f_{\text{res}})$ is the ratio between switching frequency and resonance frequency.

Equation (17) takes the form of a first-order quadratic equation. Solving for $l_{T\max 1}$ will result in two values for total maximum inductance, where the negative value can be ignored as the resulting value is very small and inductance is a positive parameter. Positive $l_{T\max 1}$ defines the first limitation on the total filter inductance requirement. The value of $l_{T\max 1}$ may not necessarily satisfy the harmonic attenuations criterion defined in IEEE-519 standard. Therefore, the role of total inductance in harmonic attenuation needs to be further evaluated.

The second limitation criterion on total inductance requirement is based on the IEEE-519 standard for harmonic limitation [19]. The attenuation of high-frequency switching components by the *LCL*-filter can be evaluated by considering the inverter as a harmonic generator while the grid as a short circuit at high and medium frequencies [2]. The ratio of grid-side current to the inverter-side voltage at switching frequency $s = h = j\omega_{\text{sw}} = j2\pi f_{\text{sw}}$ deduced through (1) can be given as

$$\frac{i_g(h)}{v_i(h)} = \frac{1}{L_T\,(j2\pi f_{\text{sw}})\left(1 - \left(\frac{f_{\text{sw}}}{f_{\text{res}}}\right)^2\right)}. \tag{18}$$

Equation (18) is modified to obtain the minimum per unit total inductance as follows [13]:

$$l_{T\min} = \frac{\left|v_{i(\text{pu})}(h)\right|}{\rho\left|i_{g(\text{pu})}(h)\right|\left|1 - k^2\right|} \tag{19}$$

where $l_{T\min}$ is the per unit total minimum inductance and $\rho = (f_{\text{sw}}/f_b)$ and k is the ratio $f_{\text{sw}}/f_{\text{res}}$, $v_{i(\text{pu})}(h) = v_i(h)/v_g$ (where v_g = grid operating voltage), $i_{g(\text{pu})}(h) = i_g(h)/i_g$ (where i_g = rated grid current). According to IEEE-519 standard listed in Table I, the inverter should not inject harmonic currents (i_g) above 50th harmonic (2500 Hz) that exceed 0.3% of the total demanded current at PCC or rated grid-injected current. In other words, inverter switching at a higher frequency than this particular frequency requires attenuation of switching components to be less than 0.3% ($i_g(h)/i_g \approx 0.003$). Voltage switching ripple component ($v_i(h)$) of the inverter can be evaluated from the Fourier analysis of the inverter voltage or software simulations depending on the modulation strategy used [1], [12] or using simple approximation $V_{\text{dc}}/4$ [13]. It is important to notice that the $l_{T\min}$ will decrease with increase of k or with the drop of resonance frequency ($k = f_{\text{sw}}/f_{\text{res}}$) according to (19). Therefore, $l_{T\min}$ defines a minimum limit on total inductance based on IEEE-519 harmonic standards; the other limits depend on the reactive power compensation at the PCC as shown above and the dc bus availability as shown below.

TABLE II
PARAMETERS FOR EVALUATION OF THE *LCL*-FILTER DESIGN

Parameter	Value
Rated power (P_r)	3 kW
Grid voltage RMS (V_{l_l})	75 V
DC-link voltage (V_{dc})	250 V
Grid frequency (f_g)	50 Hz
Switching frequency (f_{sw})	10 kHz
Sampling frequency (f_s)	20 kHz
Base impedance (Z_b)	5.6250 Ω
Resonance frequency (f_{res})	2.272 kHz
Minimum reactive power $q_{\min}$	0.05
Ratio $\mu(L_i/L_g)$	1
Ratio k	4.40
Inductance, l_T / L_T	0.0756/1.3539 mH
Grid-side/inverter-side inductance	0.67 mH/0.67 mH
Capacitance, c/ C	0.0256/14.5 μF
$u_{i(\text{pu})}$	0.8333
$i_{g(\text{pu})}$	0.003
R_d	1.7 Ω
af	18.856
K_{p_pu}	0.584
K_{I_pu}	250
$l_{T\max}(0.1\,\text{p.u.})$ *or* $L_{T\max}$	1.790 mH
Copper wire size (diameter)	1.80 mm
Number of turns	56
Core geometry	00K130LE026

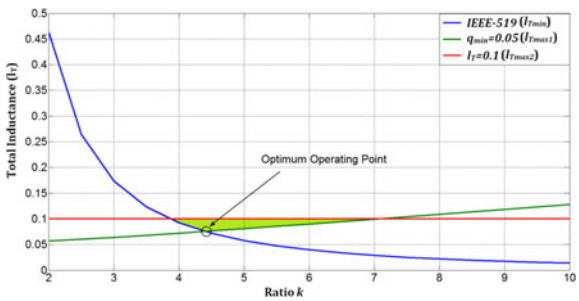


Fig. 3. Variation of total inductance requirement versus ratio k for a given μ ($\mu = 1$).

The variation of the $l_{T\min}$ and $l_{T\max 1}$ against the variation of k for the system parameters listed in Table II is shown in Fig. 3, assuming the minimum reactive power compensated ($q_{\min} = 0.05$) by the filter remains constant and $\mu = 1$ is considered. Total inductance (l_T) should depend on either $l_{T\min}$ or $l_{T\max 1}$, whichever is highest depending on the resonance frequency (ratio k)

$$l_T = \max\ \{l_{T\min}, l_{T\max 1}\}. \tag{20}$$

It can be concluded from Fig. 3 that when $\mu = 1$ the variation of $l_{T\max 1}$ is more dominant than $l_{T\min}$ as the k increase (resonance

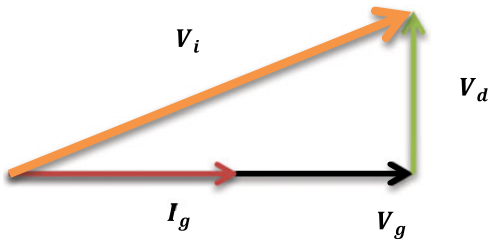


Fig. 4. Vector representation of voltage drop in an inverter system.

frequency decrease). However, it is important to understand, what determines the maximum amount of inductance allowed in a filter connected to an inverter irrespective of the type of the filter utilized or without considering the above-mentioned limitations. It is guided by the dc bus availability in the inverter system.

Maximum limit of L_T ($l_{T\max 2}$), irrespective of the filter type will be based on the ac voltage drop across the total inductance during the inverter operation and anticipated switching losses. Fig. 4 shows the vector representation of voltage drop in an inverter system, where I_g and V_g are grid-injected current and grid voltage, respectively, whereas V_d is the voltage drop across the total inductance of the filter and V_i is the apparent voltage of the inverter. It is always advisable to minimize V_d ($\approx 2\pi f_g L_T I_g$) by reducing L_T to minimize the dc bus requirement; because for an ideal system, the dc bus should be at least equal to $2V_{gpk}$ (for bipolar PWM), where V_{gpk} is the peak grid voltage. However, due to V_d, it should be large enough to compensate for the voltage drop [2] to ensure the current controllability of the inverter and to improve the robustness [2], [20]. For example, an inverter with 0.2 p.u total inductance (l_T) and the grid current (I_g) is in phase with the grid voltage (V_g) and both are 1 p.u. The voltage drop (V_d) of $V_d = j2\pi f l_T I_g = 0.2$ per unit (p.u) is expected. This will result in 1.02-p.u. voltage across the inverter (V_i). Therefore, this requires an increase of the dc bus value to maintain proper operation of the inverter. Since, higher dc bus values give rise to higher switching losses and in order to minimize switching losses, l_T is limited to 0.1 p.u. in grid-connected VSI [4], [15]. But these requirements may vary with STATCOM and inverters that operate with different power factors. The variation of l_T of an *LCL*-filter of a grid-connected inverter should be within the range when considering (20) and dc bus limitation

$$\max\ \{l_{T\min}, l_{T\max 1}\} \leq l_T < l_{T\max 2}. \tag{21}$$

According to above inequality, there will be large number of solutions for l_T of an *LCL*-filter for a given μ (= 1) and $q_{\min}$ limit as shown by the shaded area of Fig. 3. The selected l_T will always comply with the IEEE-519 harmonic attenuation limit and initially anticipated reactive power compensation limit. Any increase in l_T within the shaded area will favorably reduce the initially anticipated reactive power according to (14) and improve the harmonic attenuation level.

LCL-filter introduces resonance phenomena as discussed above and for the proper operation of the inverter, resonance frequency of designed *LCL*-filter should validate the condition $10 f_g < f_{\text{res}} < 0.5 f_{\text{sw}}$ to avoid resonance inside the control bandwidth and for resonance to be visible to the digital controller [4]. Furthermore, when considering the sampling frequency (f_s) of the controller, the above relationship can be modified in terms of ratio $k(= f_{\text{sw}}/f_{\text{res}})$, for double update PWM ($f_s = 2f_{\text{sw}}$)k lies in the range $1 < k < 9.5$ [21]. The section below will briefly discuss the notable *LCL*-filter design methodologies presented in the literature to distinguish the advantages of the proposed method.

TABLE III
COMPARISON OF *LCL* FILTER PARAMETERS BASED ON CONVENTIONAL METHOD [14] AND PROPOSED

Parameter	Value [14]	Proposed
Total inductance, L_T	2.2627 mH	1.3539 mH
Capacitance, C	28.29 μF	14.5 μF
Resonance frequency (f_{res})	4.132 kHz	2.272 kHz

D. Conventional LCL-Filter Designs

LCL-filter-design methods follow two main approaches as presented in the literature. They are classified as designing individual passive components to realize the required attenuation (hereafter referred as design type A) [4], [14], [15] or considering the operation of the *LCL*-filter as a single filtering unit (here after referred as design type B) [8], [9], [13]. Design type A determines the inverter-side inductor (L_i) based on the maximum ripple in the inductor and the grid-side inductor to further attenuate the ripple such that overall ripple is 2% of the output current. Then the capacitor of the *LCL*-filter is selected to limit the overrating of the inverter as discussed in Section II-A.

On the other hand, design type B considers *LCL*-filter as a single filtering unit that determines the required total inductance based on (19) to achieve the attenuation of switching components demanded IEEE-519 standard. Capacitor is selected based on an arbitrary resonance frequency selected to satisfy the condition $10 f_g < f_{\text{res}} < 0.5 f_{\text{sw}}$ or using the same procedure as in the design type A. Design type B uses ratio $\mu = 1$ and design A will not have any of the advantages gained by having equal grid-side and inverter-side inductors as the resulting inverter-side inductor is bigger than the grid-side inductor [14]. However, both of these design methodologies fail to identify the importance of considering the impact of total inductance on the reactive power compensation, which can be used favorably to reduce the capacitance of the *LCL*-filter and also maintain higher power factor while reducing the total inductance simultaneously. Tables III and IV presented under Sections III-B and IV will compare these conventional design methods with proposed method to highlight the uniqueness of the proposed design.

The section below will detail the step by step procedure in realizing the optimum *LCL*-filter design.

III. OPTIMUM *LCL*-FILTER DESIGN

The parameter limitations derived above can be used to realize an optimum *LCL*-filter with optimum capacitance.

TABLE IV
LCL FILTER PARAMETERS BASED ON PROPOSED METHOD AND CONVENTIONAL METHOD [13] FOR A 240-V GRID

Parameter	Proposed	Conventional [13]
Total Inductance, L_T	4.565 mH	6.824 mH
Capacitance, C	4.30 μF	8 μF
THD %	0.63	0.51

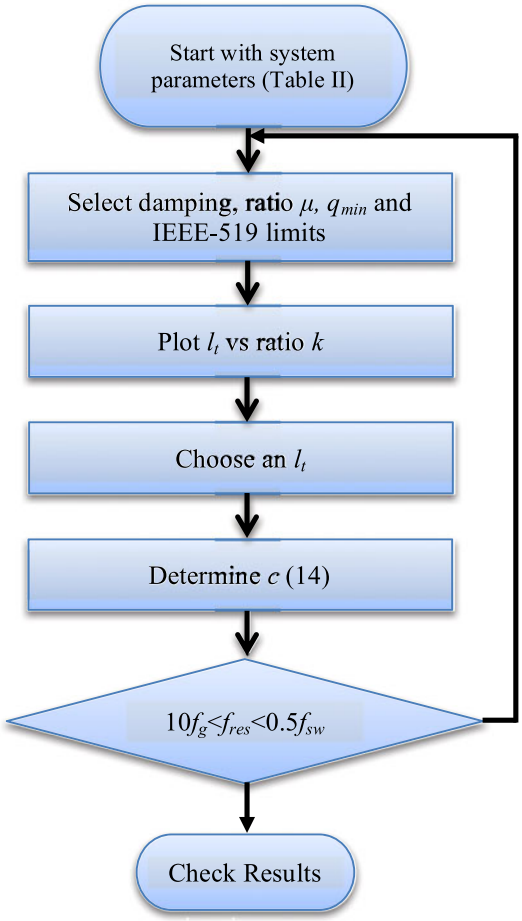


Fig. 5. *LCL*-filter design algorithm.

The step-by-step procedure is shown in Fig. 5 and presented in Section III-A, while a design example is presented in Section III-B.

A. Design Steps for the LCL-Filter With Optimum Capacitance

1) Start with system parameters: The rated power P_r, rated grid voltage V_g, dc-link voltage V_{dc}, rated grid frequency f_g, and switching frequency f_{sw}.
2) Select the damping procedure to damp the resonant peak of the *LCL*-filter (active or passive damping).
3) Set the ratio $\mu = 1$, considering the advantages mentioned above and also in [9], depending on the application (*LCL*-filter is considered as a single filtering unit).
4) Set the limit on the reactive power compensated by the filter defined by (15) or (17).
5) Set the harmonic attenuations limits on (19) based on IEEE-519 Std.
6) Plot the total inductance (l_T) versus ratio k.
7) Select the desired l_T.
8) Compute optimum capacitance c based on (14).
9) Calculate the resonance frequency of the designed *LCL*-filter and validate the condition $10 f_g < f_{\text{res}} < 0.5 f_{\text{sw}}$.
10) Check the results by considering the nonidealities omitted in modeling and experimental variations.

B. Design Example for Low-Power Inverter System (3 kW)

1) Inverter parameters considered for this design are listed in Table II.
2) Passive damping is preferred due to ease of controller implementation.
3) Ratio $\mu = 1$ is selected due to the advantages mentioned above in Section II-C.
4) Reactive power compensated by the filter [in (15) or (17)] is limited to, $q_{\text{min}} = 0.05$.
5) Harmonic limits on (19) are based on IEEE-519 [19] as listed in Table I.
6) Plot the total inductance (l_T) versus ratio k for the system parameters defined in Table II is shown in Fig. 3.
7) There are infinite total inductance values and resonance frequencies that can satisfy the design requirements as seen from Fig. 3. It is always preferable to minimize inductance due to the volume constraints in modern power electronic components. Therefore, minimum inductance ($l_T/L_T = 0.0756/1.3539$ mH) is selected in this design that corresponds to the optimum capacitance as pointed out by Fig. 3.
8) Optimum value of capacitance that corresponds to minimum l_T is ($c/C = 0.0256/14.5\ \mu$F).
9) f_{res} for the selected parameters is 2.272 kHz, which lies in the middle of the range 0.5 kHz $< f_{\text{res}} <$ 5 kHz.
10) Simulation and experimental results of the selected parameters will be shown in Section IV.

It is important to notice in the proposed method, parameter are calculated for $\mu = 1$. It considers *LCL*-filter as a single filtering unit and has the advantages mentioned under Section II-C for $\mu = 1$. For low- and mid-power systems, variation of f_{res} will not have a huge impact due to higher switching frequency and it is also evident from the proposed design by observing the range of ratio k ($\approx 3.9 < k < 7.1$) shown in Fig. 3. But for high power level systems, it becomes a challenging issue as discussed in Section III-D.

In the literature and as discussed in Section II-A, capacitance of the filter is limited to 5% of the base capacitance. Capacitance value calculated based on (7)–(9) for the design parameters listed in Table II is 28.25 μF ($C_b = 1/2\pi f_g Z_b = 0.565$ mF). Therefore, the proposed design has effectively reduced the size of the filter capacitor by 50%, as the capacitance of proposed design is 14.5 μF. *LCL*-filter parameters calculated with a conventional method [14] or design type A are listed in Table III for

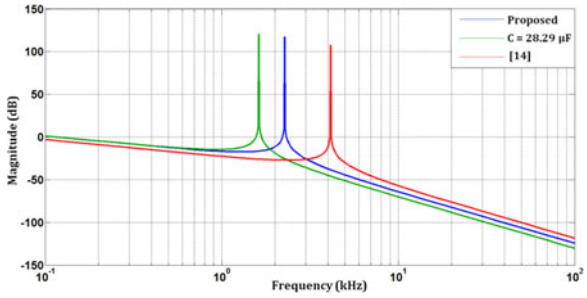


Fig. 6. Bode plots of different *LCL*-filter design listed in Table III.

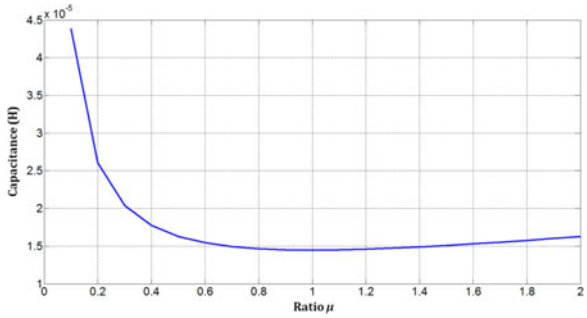


Fig. 7. Variation of the value of optimized capacitor with the ratio μ.

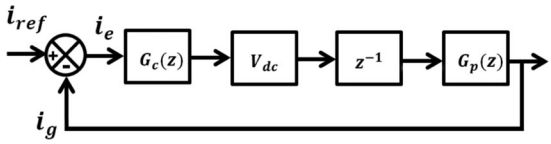


Fig. 8. Control structure for the grid-connected VSI.

comparison. Design type A also utilizes the conventional procedure for calculating the capacitance. Furthermore, the total inductance of the filter is 1.7 times larger than the proposed design. Fig. 6 shows the bode plots of proposed design (1.3539 mH and 14.5 μF), total inductance (proposed design) with capacitance designed using conventional method (1.3539 mH and 28.29 μF) and filter design method presented in [14]. The attenuation of frequency components up to the resonance frequency is higher in the conventional design [14] while lower for the frequencies above resonance frequency than the proposed design. Since switching frequency components are found after resonance frequency, the proposed design provides higher attenuation than the conventional design [14]. Comparing the attenuation with optimum capacitance versus without optimization (maintaining same total inductance 1.3539 mH), the attenuation of high-frequency components are higher for the nonoptimum capacitance (green versus blue in Fig. 6). However, this will not affect the performance of the *LCL*-filter as proposed design effectively satisfies the attenuation requirements defined by IEEE-519.

It can be concluded that the proposed design identifies optimum operating point for the given set of design parameters ($k = 4.40$, when $\mu = 1$ and $q_{\min} = 0.05$) of the *LCL*-filter, which results in minimum inductance and optimum capacitance. Furthermore, a mean (average) value of k (position of resonance frequency compared to switching frequency) is always preferred as it results in an improved filter in terms of total harmonic distortion (THD), passive damping losses, stored energy, and passive component size as detailed in [1], [5], and [9]. It can be noted that $k = 4.40$ lies in the average region facilitating the above-mentioned characteristics. Section below will summarize the impact of variation of μ on the optimized capacitor.

C. Impact of Variation of μ on the Optimized Capacitor Value

The variation of μ on the optimized capacitor value can be analyzed using (5), by keeping the total inductance and resonance frequency of the *LCL*-filter constant as shown in Fig. 7. When the $\mu = 0$, total inductance of the *LCL*-filter is represented by the inverter-side inductor (ratio $\mu = L_g/L_i$ and $L_T = L_g + L_i$). Ratio $\mu = 1$ corresponds to the inverter-side inductance equal to grid-side inductance, whereas ratio μ increases from one to infinity (theoretically), grid-side inductance dominates. However, $\mu = 1$ results in the minimum value of the capacitor and as μ varies from one, the required minimum capacitance of the filter increases.

D. Design Guidelines for High-Power Systems

The proposed design can also be extended to high-power inverters given that the designer carefully chooses the following parameters as they are a function of (19):

1) level of harmonic attenuation defined for high power level inverters based on IEEE-519;
2) voltage switching ripple component of the inverter.

Factor 1 above is a function of maximum demand of load current at PCC as listed in Table I for medium-power systems. Therefore, designer needs to select appropriate attenuation level defined in IEEE-519 as these limits vary with power levels (Refer [19]). Voltage ripple depends on several factors for high-power inverters:

1) number of voltage levels of the inverter output;
2) modulation schemes.

Most often, multilevel inverters are used in high-power applications to reduce switching stress and losses and different modulation schemes such as phase disposition PWM and selective harmonic elimination PWM are used [25]. Therefore, designer needs to estimate the ripple in simulations or mathematically by considering the above-mentioned parameters. Design factor ($10 f_g < f_{\text{res}} < 0.5 f_{\text{sw}}$) for a high-power system is challenging due to lower switching frequencies. Therefore, if the resulting f_{res} fails to satisfy this inequality, the optimum capacitance or optimum total inductance calculated based on the proposed design or ratio μ or combination of any of these parameters may be altered in a way that the resonance frequency lies in the desired region and the attenuation of the filter is within the limits defined by IEEE-519. Bode plots can be effectively utilized to estimate these changes and arrive at an optimized solution.

IV. Simulation and Experimental Verification

Three-phase VSI with *LCL*-filter is simulated in MATLAB Simulink environment where the proportional integral (PI) controller is used to regulate the grid-injected current [18]. A basic block diagram of the entire control system is shown in Fig. 8,

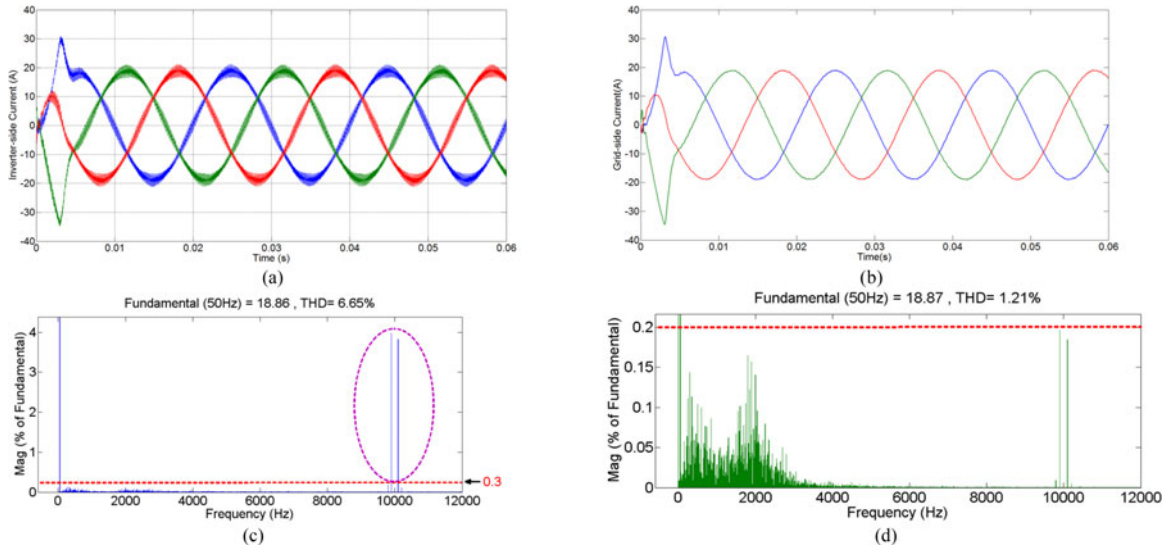


Fig. 9. (a) Inverter-side current, (b) grid-injected current, (c) inverter-side THD plot, and (d) THD plot of grid-injected current for the grid-connected inverter with parameters listed in Table II.

where $G_c(z)$ and $G_p(z)$ are the discrete transfer functions of the PI controller given by (22) and *LCL*-filter given by (1). In simulation, the controller is sampled at 20 kHz (f_s) to mimic the operation inside a real-time digital signal processor, while the rest of the inverter system is sampled at a higher rate (at least $100f_s$) to mimic a real-time system. The controller is tuned according to the guidelines provided in [18] and [22]. The transfer function of the PI controller ($G_{\rm PI}(z) = G_c(z)$) is given by

$$G_{\rm PI}(z) = K_p + K_I T_s \frac{1}{(z-1)}. \tag{22}$$

The proportional and integral gain of the PI controller is given by

$$K_p = \omega_c \left(\frac{L_i + L_g}{V_{\rm dc}} \right) \tag{23}$$

$$K_I = K_p \left(\frac{10}{\omega_c} \right) \tag{24}$$

where $V_{\rm dc}$ is the dc-link voltage of the inverter and ω_c is the crossover frequency. Crossover frequency is approximated to be $0.3\omega_{\rm res}$ ($\omega_{\rm res}$ = resonance frequency) to prevent the interferences between the *LCL* resonant component and the maximum harmonics of the current that needed to be controlled as per [18]. Controllers are synchronized with the grid voltage to achieve unity power factor operation with the use of a PLL. Furthermore, the controller is implemented for the per unit measurements of the grid-injected voltage and current. Therefore, gains are modified using the attenuation factor (af) given by (25) as per [18]

$$\text{af} = \frac{\sqrt{2}P_r}{3V_g} \tag{25}$$

where P_r and V_g are the rated power and the rms value of the grid voltage. Therefore, modified p.u. gains are $K_{p\text{-pu}} = \text{af} * K_p$ and $K_{I\text{-pu}} = \text{af} * K_I$. The calculated p.u. gains for the given system parameters are also listed in Table II. These derived gains are used in both simulations and experimental setup.

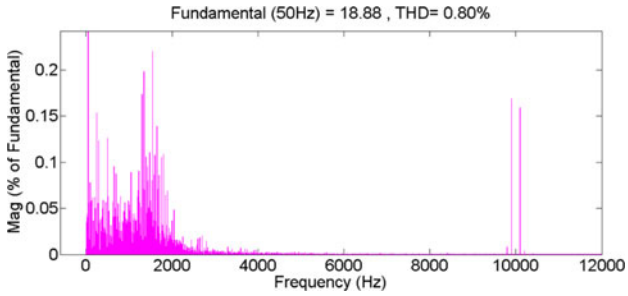


Fig. 10. THD plot of grid-injected current for *LCL*-filter ($L_T = 1.3539$ mH and $C = 28.25\,\mu$F).

Fig. 9(a) and (b) shows the inverter-side and grid-side currents, respectively, while the corresponding THD plots are shown in Fig. 9(c) and (d). Switching components on the inverter-side current as seen from Fig. 9(c) are clearly above 0.3% limit demanded by the IEEE-519. The proposed filter is capable of attenuating them below 0.2% as seen from Fig. 9(d). Another set of simulations were carried out for an *LCL*-filter with the capacitance of 28.25 μF, while keeping the same total filter inductance ($L_T = 1.3539$ mH) and the THD plot of the grid-injected current is shown in Fig. 10. There is a small decrease in the THD compared to the proposed design due to the fact that resonance frequency has decreased to 1627.5 Hz ($k = 6.14$) compared to the proposed design's 2272 Hz ($k = 4.40$). As seen from the bode plot of Fig. 2, reduction in resonance frequency will result in improved attenuation as the 60-dB attenuation slope shifts toward the left of the bode plot. However, the advantage gained is negligible in the context of harmonic attenuation demanded by IEEE-519.

Proposed *LCL*-filter is designed and experimentally validated for a grid voltage of 75 V (other parameters are listed in Table II) due to the safety limitations and limited dc bus voltage

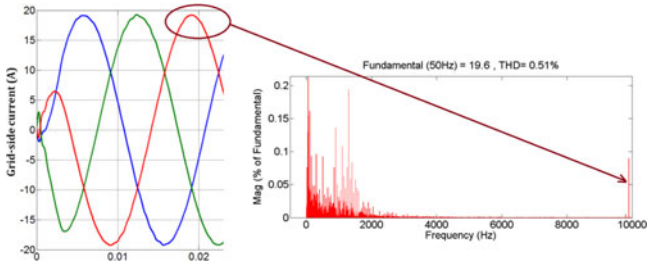


Fig. 11. Grid-injected current and THD plot for *LCL*-filter as per [13] (L_T = 6.824 mH and $C = 8\,\mu$F).

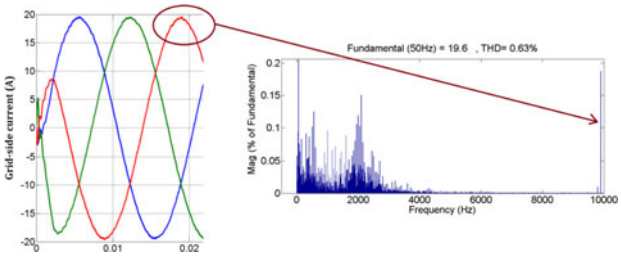


Fig. 12. Grid-injected current and THD plot for proposed *LCL*-filter (L_T = 4.565 mH and $C = 4.3\,\mu$F).

availability in the laboratory. Generally, most of the inverters are connected to a 120 or 240 V (nominal voltage) grid. Therefore, Table IV summarizes the *LCL*-filter parameters calculated using the proposed design for a 240-V system parameters presented in [13] and a comparison is provided with an another conventional method [13] (similar to design type B discussed under Section II-D). Figs. 11 and 12 show the simulations results for the proposed and conventional method. Conventional method has better attenuation of switching frequency components as seen from the THD plot due to higher inductance compared to proposed method. Nevertheless, for the both methods attenuation of switching components is less than 0.2%, which is below the limit demanded by IEEE-519. However, the proposed method is capable of achieving it with a small total inductance and small capacitor.

The proposed filter design can be implemented for a single-phase or a three-phase grid-connected VSI. However, proposed design is verified by a 3-kW three-phase grid interface VSI hardware prototype as shown in Fig. 13. Sinusoidal PWM is utilized for switching power IGBTs of the three-phase inverter. Parameters used for the experimental prototype are listed in Table II. Control algorithm for the grid-connected VSI is implemented in the Texas Instruments TMS320F28335 DSP. Inverter-side and grid-side inductors are implemented using KoolMu powder material, KoolMu core "00K130LE026" is used for the implementation [23], which has a saturation flux density of 1 T [23]. E-core geometry is preferred due to the ease of winding over other core geometries such as toroids. Inductors are designed according to the guidelines provided by magnetic manufacturers [23], [24].

Inverter-side and grid-side currents at rated operating conditions are captured using Yokogawa DL850EV ScopeCoder as shown in Fig. 14(a) and (b), respectively. Experimental results are also consistent with simulations of the proposed filter and

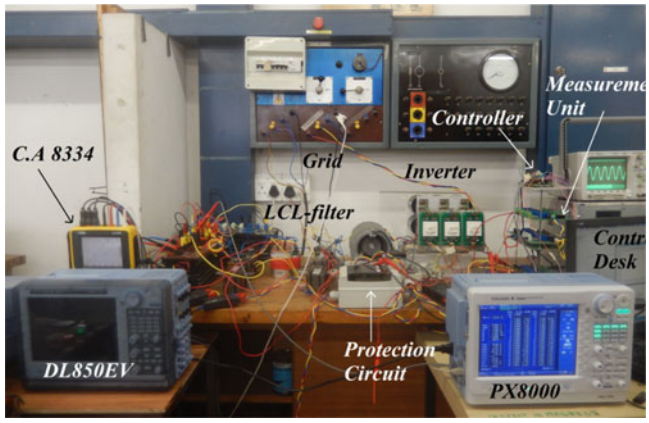


Fig. 13. 3-kW hardware prototype.

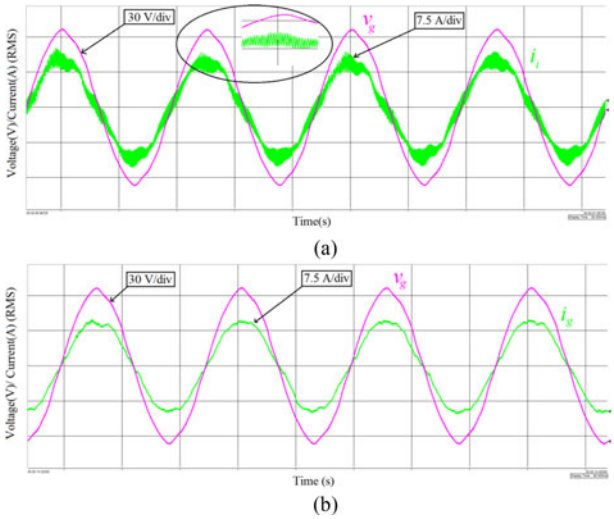


Fig. 14. (a) Inverter-side (i_i) and (b) grid-side current (i_g) waveforms.

the filter is capable of attenuating the high-frequency switching components as seen from THD plots shown in Fig. 15(a) and (b). However, the THD (3.9%) of the grid-injected current of the implemented filter is bit higher than the results from simulations due the nonlinearities such as dead-time, calculation delays, nonideal power devices, etc. However, the proposed filter is in agreement with the 5% THD limit imposed by IEEE-519 standard and most importantly, it has attenuated the switching components completely. Active and reactive power of the inverter are measured using C.A 8334 Power & Quality Analyzer to validate the reactive power compensation by the proposed *LCL*-filter as shown in Fig. 16. Reactive power compensation at different power injection level are listed in Table V. Results confirm that the reactive power of the proposed *LCL*-filter confined to initial designed value.

V. Alternative Filter Optimization Parameters

The proposed *LCL*-filter design primarily focuses on design of total inductance and capacitance for a two level three-phase grid-connected VSI. However, other parameters such as damping, component costs, switching ripple, and switching frequency can

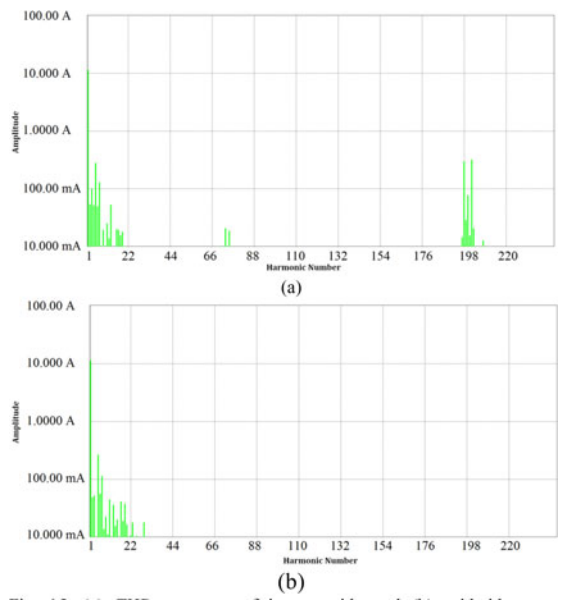


Fig. 15. (a) THD spectrum of inverter-side and (b) grid-side current waveform (THD = 3.9%), where 1(50 Hz)–220(11 kHz) corresponds to harmonic number.

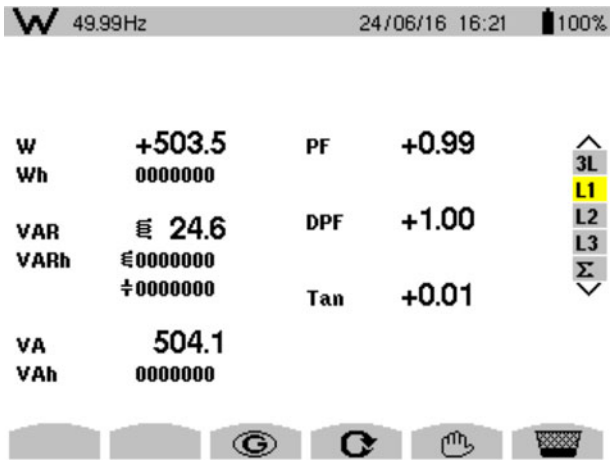


Fig. 16. Active (W), reactive (VAR), apparent (VA) power components, and power factor (PF) at 1/2 rated operating condition (500 W) of one phase of three-phase VSI.

also be considered for optimization. Impact of various passive damping techniques are elaborated in [5] and [15] while active damping can also be used to avoid damping losses at the expense of control complexity. However, passive damping is preferred with stiff grid operating conditions [21].

The proposed design considers the switching ripple of a two-level inverter with sinusoidal PWM scheme in determining the passive components according to (19). However, switching ripple vary with multilevel inverters as discussed under Section III-D and different PWM schemes. As the number of levels increase, switching ripple decreases and it could further reduces the total inductance according to (19). Similarly, switching ripple is smaller with space vector PWM compared to sinusoidal PWM scheme. Switching frequency can also be used as a variable factor according to (19). Higher switching frequencies

TABLE V
POWER AT DIFFERENT PERCENTAGES OF RATED POWER INJECTED TO GRID IN A SINGLE PHASE

% rated = (Active power injected)/(rated power of the inverter = 1 kW) in a single phase				
% rated	25%	50%	75%	100%
Active power	249.2	503.5	752.1	998
Reactive power	11.7	24.6	37.6	50.8
RA ratio*	0.047	0.048	0.049	0.051

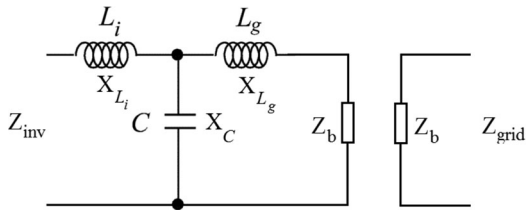
* RA ratio = reactive power/ active power.

result in smaller total inductance at the expense of switching losses. Therefore, an analysis-based switching frequencies and losses can also be used to enhance the performance of the entire system. Furthermore, cost of the passive components can also be incorporated within the design optimization procedure but will increase the complexity. Analysis based on different core materials versus cost or volume for inductors can be used to realize a cost effective *LCL*-filter [23].

VI. CONCLUSION

An optimum capacitance for an *LCL*-filter is derived by considering the impact of total inductance of the filter on reactive power compensation limit. Initially, *LCL*-filter parameter limits and their ranges that are critical for the proper operation of a grid-connected three-phase inverter are analyzed to identify relationship between parameters and design requirements that can lay the foundation to a good *LCL*-filter design. Based on the analysis, an optimum capacitance for an *LCL*-filter is designed by deriving an approximate mathematical equation to define the reactive power compensation. The proposed design is capable of reducing the filter capacitance by 50% compared to the capacitor design that is based on the percentage of base capacitance value and also has the minimum total inductance compared to conventional design methods. The performance of the proposed optimum *LCL*-filter design is both verified in simulations and validated by experimental results

APPENDIX



Impedance of grid

$$Z_{\text{grid}} = Z_b$$

$$\frac{Z_{\text{grid}}}{Z_b} = z_{g\_\text{pu}} = 1.$$

Parallel combination of $(X_{L_g} + Z_b)$ and X_c

$$Z_x = \frac{jX_c\left(jX_{L_g} + Z_b\right)}{jX_c + jX_{L_g} + Z_b}.$$

Impedance of the inverter (Z_{inv})

$$Z_{\text{inv}} = \frac{jX_c\left(jX_{L_g} + Z_b\right)}{jX_c + jX_{L_g} + Z_b} + jX_{L_i}$$

$$Z_{\text{inv}} = \frac{jX_c jX_{L_g}}{jX_c + jX_{L_g} + Z_b} + \frac{jX_c Z_b}{jX_c + jX_{L_g} + Z_b} + jX_{L_i}$$

$$\frac{Z_{\text{inv}}}{Z_b} = \left(\frac{\frac{jX_c jX_{L_g}}{Z_b Z_b}}{\frac{jX_c}{Z_b} + \frac{jX_{L_g}}{Z_b} + \frac{Z_b}{Z_b}} + \frac{\frac{jX_c}{Z_b}}{\frac{jX_c}{Z_b} + \frac{jX_{L_g}}{Z_b} + \frac{Z_b}{Z_b}} + \frac{jX_{L_i}}{Z_b} \right)$$

For a p.u. system ($X_g = \omega L_g$), ($X_i = \omega L_i$) and ($X_c = 1/\omega C$) when expressed with p.u. of the base Z_b, $l_g = X_g/Z_b$, $l_i = X_i/Z_b$, and $c = -Z_b/X_c$

$$z_{\text{inv}} = \left(\frac{-j\left(\frac{1}{c}\right) jl_g}{-j\left(\frac{1}{c}\right) + jl_g + 1} + \frac{-j\left(\frac{1}{c}\right)}{-j\left(\frac{1}{c}\right) + jl_g + 1} + jl_i \right)$$

$$z_{\text{inv}} = \left(\frac{jl_g}{1 - cl_g + jc} + \frac{1}{1 - cl_g + jc} + jl_i \right).$$

If $c < 10\%$ and $l_g < 10\%$ $cl_g < 1\%$ $cl_g \approx 0$

$$z_{\text{inv}} = \left(\frac{jl_g}{1 + jc} + \frac{1}{1 + jc} + jl_i \right).$$

Considering the conjugate

$$z_{\text{inv}} = \left(\frac{jl_g\,(1 - jc)}{1 + c^2} + \frac{(1 - jc)}{1 + c^2} + jl_i \right).$$

If $c < 10\%$ and $c^2 < 1\%$ $c^2 \approx 0$

$$z_{\text{inv}} = \left(jl_g + cl_g + 1 + -jc + jl_i\right)$$

$$z_{\text{inv}} = \left(1 + -jc + jl_g + jl_i\right).$$

If $l_i + l_g = l_T$

$$z_{\text{inv}} = 1 + j\,(l_T - c).$$

Power of the inverter $P_{\text{inv}} = \frac{V_{\text{inv}}^2}{Z_{\text{inv}}}$.

Base power $P_b = \frac{V_b^2}{Z_b}$.

Therefore, for a per unit system (p)

$\frac{P_{\text{inv}}}{P_b} = \frac{V_{\text{inv}}^2}{Z_{\text{inv}}} \frac{Z_b}{V_b^2}$

$$V_{\text{inv}} \approx V_b$$

$$p = \frac{1}{Z_{\text{inv}}/Z_b}.$$

Substituting the inverter per unit impedance derived

$$p = \frac{1}{1 + j\,(l_T - c)}$$

$$p = \frac{1 - j\,(l_T - c)}{1 + (l_T - c)^2}$$

$$(l_T - c)^2 \approx 0$$

$$p \approx 1 + j\,(c - l_T)$$

$$\text{Or } p \approx 1 - j\,(l_T - c).$$

Therefore, (1) corresponds to the unity active power transferred and ($l_T - c$) corresponds to the reactive power transferred.

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REFERENCES

[1] K. Jalili and S. Bernet, "Design of LCL filters of active-front-end two-level voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1674–1689, May 2009.

[2] M. Liserre, F. Blaabjerg, and A. DellAquila, "Step-by-step design procedure for a grid-connected three-phase PWM voltage source converter," *Int. J. Electron.*, vol. 91, no. 8, pp. 445–460, 2004.

[3] R. N. Beres, X. Wang, F. Blaabjerg, M. Liserre, and C. L. Bak, "Optimal design of high-order passive-damped filters for grid-connected applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2083–2098, Mar. 2016.

[4] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep./Oct. 2005.

[5] R. Peña-Alzola, M. Liserre, F. Blaabjerg, R. Sebastián, J. Dannehl, and F. W. Fuchs, "Analysis of the passive damping losses in LCL-filter-based grid converters," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2642–2646, Jun. 2013.

[6] J. Dannehl, F. W. Fuchs, S. Hansen, and P. B. Thøgersen, "Investigation of active damping approaches for pi-based current control of grid-connected pulse width modulation converters with LCL Filters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1509–1517, Jul./Aug. 2010.

[7] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of active damping control for LCL Filters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 424–432, Jan./Feb. 2014.

[8] R. Pena-Alzola, M. Liserre, F. Blaabjerg, R. Sebastian, J. Dannehl, and F. W. Fuchs, "Systematic design of the lead-lag network method for active damping in LCL-filter based three phase converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 43–52, Feb. 2014.

[9] R. Pena-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez, and Y. Yang, "LCL-filter design for robust active damping in grid-connected converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 4, pp. 2192–2203, Nov. 2014.

[10] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414–3427, Jul. 2014.

[11] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Design of LCL filters with LCL resonance frequencies beyond the Nyquist frequency for grid-connected converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 1, pp. 3–14, Mar. 2016.

[12] Q. Liu, L. Peng, Y. Kang, S. Tang, D. Wu, and Y. Qi, "A novel design and optimization method of an LCL filter for a shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4000–4010, Aug. 2014.

[13] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4106–4114, Dec. 2010.

[14] A. Reznik, M. G. Simoes, A. Al-Durra, and S. M. Muyeen, "LCL filter design and performance analysis for grid-interconnected systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1225–1232, Mar./Apr. 2014.

[15] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54–69, Mar. 2016.

[16] M. Sanatkar-Chayjani and M. Monfared, "Design of LCL and LLCL filters for single-phase grid connected converters," *IET Power Electron*., vol. 9, no. 9, pp. 1971–1978, Jul. 27, 2016.

[17] A. Anzalchi, M. Moghaddami, A. Moghadasi, A. Sarwat, and A. Rathore, "A new topology of higher order power filter for single-phase grid-tied voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7511–7522, Dec. 2016.

[18] M. Hanif, V. Khadkikar, X. Weidong, and J. L. Kirtley, "Two degrees of freedom active damping technique for LCL filter-based grid connected PV Systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2795–2803, Jun. 2014.

[19] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Std 519-2014, (Revision of IEEE Std 519-1992), pp. 1–29, Jun. 11, 2014.

[20] H. G. Jeong, K. B. Lee, S. Choi, and W. Choi, "Performance improvement of LCL-filter-based grid-connected inverters using PQR power transformation," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1320–1330, May 2010.

[21] S. Jayalath and M. Hanif, "Generalized LCL-filter design algorithm for grid-connected voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 1905–1915, Mar. 2017.

[22] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Optimized controller design for LCL -type grid-connected inverter to achieve high robustness against grid-impedance variation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1537–1547, Mar. 2015.

[23] "2015 magnetics powder core catalog," Jan. 2016. [Online]. Available: http://www.mag-inc.com/design/technical-documents/powder-core-documents. Accessed on: Jan. 20, 2017

[24] S. Jayalath, D. Ongayo, and M. Hanif, "Modelling powder core inductors for passive filters in inverters using finite element analysis," *Electron. Lett.*, vol. 53, no. 3, pp. 179–181, 2017.

[25] M. Zabaleta, E. Burguete, D. Madariaga, I. Zubimendi, M. Zubiaga, and I. Larrazabal, "LCL grid filter design of a multimegawatt medium-voltage converter for offshore wind turbine using SHEPWM modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1993–2001, Mar. 2016.

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