DC tolerance analysis of electronic circuits by polyhedral circuits

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SUMMARY

Real equilibrium solutions of electronic circuits are affected by deviation of real characteristics of devices from their nominal values, producing the displacement of solution points from their nominal position. In this paper, a method to determine all the equilibrium regions in which real equilibrium points may fall is presented. The analysis is based on the introduction of the so-called strip characteristics that represent the characteristics of devices affected by tolerances. They are modeled by polyhedral characteristics. Different situations may occur as tolerances grow. A nominal solution point may disappear, or on the other end, some solution point not present with nominal characteristics may appear. These possible events call for a classification of the equilibrium regions in either certain or uncertain, depending on the existence or not of an equilibrium point for any choice of real characteristics. The algorithm adopts linear programming techniques and a clustering algorithm. Copyright © 2015 John Wiley & Sons, Ltd.

1. INTRODUCTION

In general, real characteristics of electronic devices are not known exactly because of their dispersions due to aging, environmental effects (temperature), and constructive techniques. Because of production parameter spreads, design verification has to check that both silicon meets the given specifications (at a functional and at a device level), and the whole circuit works within the given tolerances. On the other hand, the aim of fabrication test is to distinguish a faulty circuit from a fault-free one, and this must be done in the shortest time. Therefore, tolerance analysis is an important task faced widely in literature [1–18]. The cited papers consider worst-case analysis of tolerances and are based on deterministic or statistic sensitivity evaluations. Among them, Ref. [2] shows how to find rigorous lower bounds on worst case parameter tolerances in nonlinear resistive circuits. Instead, Refs. [4] and [5] represent the tolerance-dependent parameters by substituting single values by intervals. Ref. [6] analyzes worst case tolerances by means of vertex analysis, while [10] adopts genetic algorithms. Ref. [13] deals with the diagnosis of multiple catastrophic faults, taking into account the deviations of the circuit parameters within their tolerance ranges. Refs. [15–17] are base on the use of set-valued functions, while Ref. [18] adopts integer programming techniques.

The purpose of this paper is to search for the real DC solutions of resistive electronic circuits with tolerances obtained, for example, short-circuiting the inductors and removing the capacitors. A new

approach based on the use of strip characteristics is presented [19]. The real resistive characteristic of a device is assumed to vary in a region around the nominal one: This region, the so-called strip characteristic, is delimited by two boundary characteristics, located above and below the nominal one, in the characteristic plane. In principle, strip characteristics may be introduced for both linear and nonlinear resistors (for example, diodes), as well as for trans-characteristics of controlled sources embedded in bipolar junction transistors and metal-oxide semiconductor field-effect transistors models. As the real characteristics move inside the strip characteristics, the corresponding real equilibrium points move in the so-called equilibrium regions. If, for any choice of real characteristics in the strip characteristics, there is always an equilibrium point in the corresponding equilibrium region, then the equilibrium region is said to be certain. Otherwise, if for some choice of the real characteristics there is no equilibrium point, the equilibrium region is said to be uncertain. Furthermore, there may be uncertain equilibrium regions that are related to more equilibrium points or to none. In this case, equilibrium points may disappear or be multiple for specific real characteristics.

For example, let us consider the simple circuit in Figure 1a. Equilibrium points are given by the intersection between the load line of the real current generator (I_s, R_s) and the tunnel diode D_T characteristic. Current generator I_s is certain without tolerances, while both tunnel diode D_T and resistor R_s are affected by uncertainty in their parameters. So, their 'nominal' characteristics (Figure 1b, dashed lines) cannot describe completely the circuit. Therefore, it is convenient to consider, for each uncertain element, a strip around the nominal characteristic delimited by two boundary characteristics (solid lines), denoted as upper and lower characteristics. The terms 'upper' and 'lower' are conventional; they can be used also if the segments are vertical. Boundary characteristics represent the limit conditions of the uncertain device. These strips representing the characteristics intersect in two distinct 'admissible' equilibrium regions ζ_A^1 and ζ_A^2, the sets containing all the possible equilibrium points obtained under variation of parameters. Equilibrium region ζ_A^2 gives an equilibrium point for any real couple of characteristics belonging to the strips. It is so called 'certain'. Instead equilibrium region ζ_A^1 is called 'uncertain', because a solution point does not exist for all possible choices of characteristics. For example, nominal characteristics intersect in ζ_A^2, but not in ζ_A^1.

In general, the designer wants that only certain equilibrium regions appear in the circuit, because the uncertain regions may generate undesired dynamic behaviors. Clearly, a deeper investigation of the equilibrium points portrait is important for a correct design and working of an electronic (in general nonlinear) circuit. If a classical analysis method (i.e., simulation program SPICE) is used to find all the possible locations of real equilibrium points, each strip characteristic must be substituted by a real characteristic lying inside it. Then, many classical analyses must be repeated, one for each choice of the real characteristics replacing the corresponding strip characteristics. Note that it is not sufficient to analyze all the circuits obtained substituting the upper and lower characteristics of each
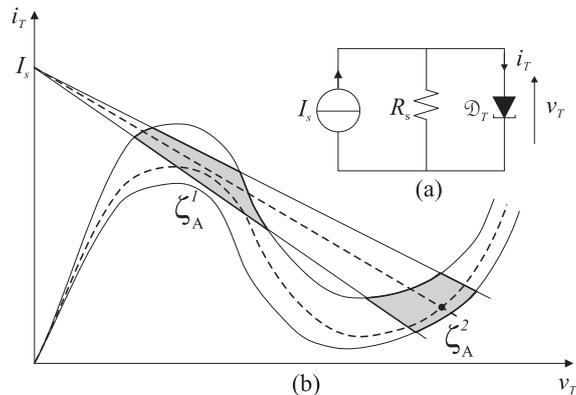

Figure 1. (a) A simple circuit with a tunnel diode; (b) Characteristics with tolerances and equilibrium regions.

strip characteristic to its nominal characteristic, because the results are not resolutive, as it will be pointed out later.

In this paper, strip characteristics are approximated with a method equivalent to piecewise linear (PWL) approximation for nominal nonlinear characteristics. Then, as performed in [20], an algorithm structured as a binary tree and adopting linear programming (LP) techniques is used to find all the admissible unit-rank circuits. An admissible unit-rank circuit has a convex solution domain, and it is the generalization of an equilibrium point in usual PWL circuits. Equilibrium points of real circuits obtained substituting strip characteristics with real characteristics are located inside this convex solution domain. The traditional methods to find all the solutions of a PWL circuit finish their work with the list of the equilibrium points. In this case, the list of admissible unit-rank circuits does not exhaust the work. Indeed, as tolerances grow, equilibrium points can move from one unit-rank circuit to an adjacent one. So, a novel problem has to be faced. The next step of the algorithm consists in clustering suitably adjacent unit-rank circuits with solutions in order to find the so-called equilibrium regions, in which equilibrium points can move. Finally, equilibrium regions have to be classified in certain, therefore robust, or uncertain. An equilibrium region is said to be certain if it gives an equilibrium point whichever is the choice of the real characteristics inside the strip-characteristics. Otherwise, it is said to be uncertain. Moreover, as shown in the examples, more complicated situations may occur as tolerances grow, because equilibrium regions may disappear or new equilibrium regions may appear, or join together to form larger equilibrium regions. These are aspects that can be very important for a designer.

2. PRELIMINARIES

In this paper, the problem of finding all the direct current (DC) solutions of a resistive nonlinear electric circuit with tolerances is tackled. It corresponds to solve a DC-solution problem [19–21] where some elements have tolerances in their characteristics. The circuits considered are assumed to contain, besides linear elements, two-terminal nonlinear resistors and nonlinear controlled sources. The characteristics of resistors with tolerances are said uncertain, the other ones certain.

Let vectors $\mathbf{x}^L$ and $\mathbf{y}^L$ denote the branch voltages and currents involved in linear certain (trans-) characteristics, as linear resistors and ideal transformers, for example. Each of these vectors may contain both voltages and currents, because each linear (trans-) characteristic may link a voltage to a current, link two voltages, or link two currents. The space spanned by $\mathbf{x}^L$ and $\mathbf{y}^L$ is denoted by $\mathscr{L}$. Analogously to $\mathbf{x}^L$ and $\mathbf{y}^L$, vectors $\mathbf{x}$ and $\mathbf{y}$ group the voltages and currents involved in nonlinear, certain, and uncertain, (trans-) characteristics, and in linear uncertain elements. They span space $\mathcal{P}$. The cartesian product of spaces $\mathscr{L}$ and $\mathcal{P}$ constitutes the global space of branch variables $\mathcal{Z}$. The following domains within the previous spaces are defined. Domain $\widetilde{\mathscr{L}}$ denotes the set of vectors $\mathbf{x}^L$ and $\mathbf{y}^L$ satisfying the linear constitutive relations. This domain is an affine subspace of $\mathscr{L}$ when independent voltage and/or current sources are present, otherwise it is a linear subspace. Domain $\widetilde{\mathcal{P}} \subset \mathcal{P}$ denotes the set of vectors $\mathbf{x}$ and $\mathbf{y}$ satisfying the nonlinear (trans-) characteristics. Domain $\mathcal{K}$ denotes the set of vectors $\mathbf{x}^L$, $\mathbf{y}^L$, Z, and $\mathbf{y}$ satisfying Kirchhoff's voltage and current laws. It is a linear subspace of space $\mathcal{Z}$. The configuration domain $\subset Z$ of the resistive circuit, that is, the solution domain of the circuit, can be expressed as

$$\widetilde{\mathcal{Z}} \equiv \widetilde{K} \cap \left[\widetilde{\mathscr{L}} \times \widetilde{\mathcal{P}} \right].$$ (1)

Note that $\widetilde{\mathcal{Z}}$ is in general non-convex and non-connected.

For the sake of clearness, a list with a description of the main symbols used throughout the paper is presented in Section 9 at the end of the paper.

3. PIECEWISE LINEAR AND STRIP PIECEWISE LINEAR CHARACTERISTICS

Nonlinear elements are modeled by a nonlinear function $f(x,y)=0$, involving only two branch variables. This function defines the corresponding domain, that is, the set of values x and y known as the characteristic of the element. Usually, this characteristic is constituted by one or more one-dimensional continuous curves, called branches. For the sake of simplicity, only one-branch continuous infinite characteristics will be considered hereafter. In this paper, usual one-dimensional branch characteristics represent the nominal characteristics of the devices under examination.

A nominal (one-dimensional) characteristic can be approximated [20] by a PWL curve. The number and position of breakpoints may be determined by minimizing the mean square error. Denoted as $\xi(1,H)$, it is composed of H segments $\overline{\xi}(h)$ and $H+1$ breakpoints $B(h_B)$. The extreme segments can be bounded or unbounded. In the last case, the extreme breakpoints supply their direction. In Figure 2, it has shown a PWL characteristic with seven segments and eight breakpoints. Segments $\overline{\xi}(1)$ and $\overline{\xi}(7)$ are infinite. The number H of segments is said to be the rank of the PWL characteristic.

If there is an uncertainty in the parameters of the model, different characteristics where the device may work have to be considered [19]. These characteristics, placed around the nominal characteristic, design a strip on the related characteristic plane K, whose width is determined by the considered amount of tolerance. This strip, delimited by two extreme characteristics called boundary (upper and lower) characteristics, will be denoted as strip (two-dimensional) characteristic. An example is shown in Figure 3. The two boundary characteristics are drawn with a continuous line, while the nominal characteristic in the center of the strip is highlighted with a dashed line. Note that also linear elements can be affected by uncertainty in the model, so suitable strip characteristics can be used to model them, as shown in the succeeding text.

Strip characteristics can be approximated adopting the same approach used for PWL characteristics. The first operation consists of slicing transversally the strip characteristic by means of suitable segments, denoted as one-dimensional (1D-) breakpoints. Their intersections with the lower and upper boundary characteristics are the breakpoints of the induced PWL approximation of the boundary characteristics. They are so-called boundary breakpoints. The second step consists of decomposing and approximating the strip characteristic with a set of convex quadrilaterals, called strip segments, joined in the 1D-breakpoints. Each of them are formed by two 1D-breakpoints and by the segments of the PWL boundary characteristics connecting the breakpoints.

In analogy with usual PWL approximation, the whole approximating strip characteristic is called strip PWL (SPWL) characteristic. An example is shown in Figure 4. If we have chosen $K+1$ 1D-breakpoints, the SPWL characteristic is divided in K strip segments. It is so denoted as $\sigma(1,K)$. It is delimited by two boundary PWL (B-PWL) characteristics denoted as $\sigma^{(u)}(1,K)$ and $\sigma^{(\ell)}(1,K)$. The kth strip segment is denoted as $\overline{\sigma}(k)$, and it is delimited, beside 1D-breakpoints $\overline{B}(k_B)$, by two boundary segments, denoted as $\overline{\sigma}^{(u)}(k)$ and $\overline{\sigma}^{(\ell)}(k)$. Their four boundary breakpoints are denoted as $B^{(\ell)}(k_B)$, $B^{(\ell)}(k_B+1)$, $B^{(u)}(k_B)$, and $B^{(u)}(k_B+1)$.
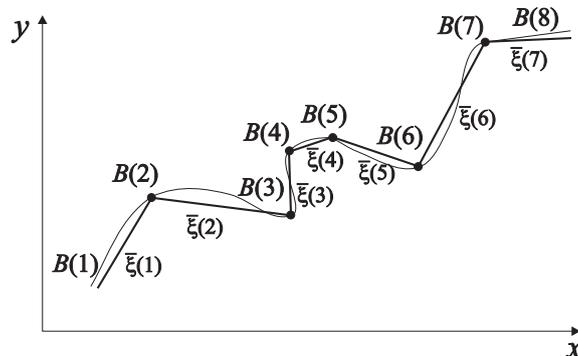

Figure 2. An example of piecewise linear characteristic.
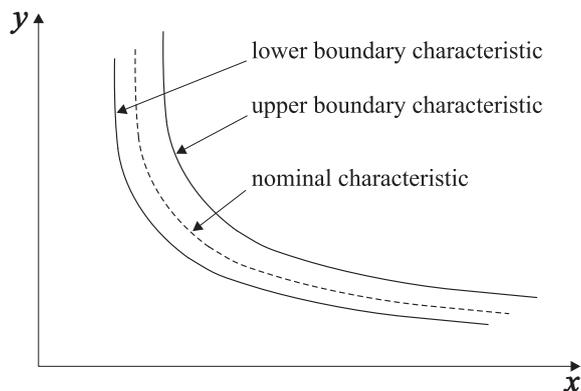
Figure 3. An example of a strip characteristic around the nominal one (dashed line).
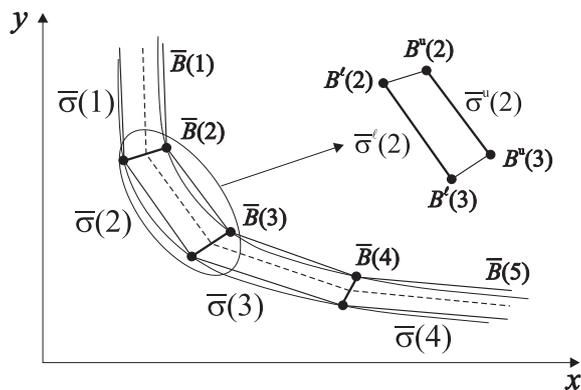

Figure 4. Strip piecewise linear characteristic $\sigma(1,4)$ approximating strip characteristic in Figure 3.

Strip segments will play in the algorithm the same role that linear segments play in the corresponding PWL analysis, that is, they are the fundamental units of a SPWL characteristic. Indeed, the set theoretical union of strip segments $\overline{\sigma}(k)$ supplies the whole SPWL characteristic $\sigma(1,K)$, where K is said to be the rank of the SPWL characteristic.

If a strip characteristic extends to infinite at one side, then an infinite strip segment is introduced. It is delimited by one (finite) 1D-breakpoint and by two parallel or non convergent half-lines; conventionally, their directions are supplied by an infinite 1D-breakpoint (added to the finite 1D-breakpoints). As in PWL approximation, the number and position of 1D-breakpoints may be determined, for example, by minimizing the mean square error between the area of SPWL characteristic and the corresponding original one.

In case of linear resistors with tolerances, the related strip characteristic is shown in Figure 5. It is formed by two triangular strip segments joined in the origin of axis. The nominal characteristic corresponding to value R is drawn with a dashed line.

4. TRUNCATED PIECEWISE LINEAR AND STRIP PIECEWISE LINEAR CIRCUITS

A circuit containing PWL and SPWL resistors is called an SPWL circuit. SPWL circuits contain, besides linear certain elements, M nonlinear certain elements, modeled by PWL ((1)D) characteristics, and N linear and nonlinear uncertain elements, modeled by SPWL ((2)D) characteristics.

Let us introduce the truncated PWL (T-PWL) characteristics associated to PWL characteristic $\xi_m(1,H_m)$. A T-PWL characteristic contains one or more adjacent segments of the original PWL characteristic, and it is denoted as $\xi_m(h_m^1 - h_m^2)$, where h_m^1 and h_m^2 are the first and the last segments.
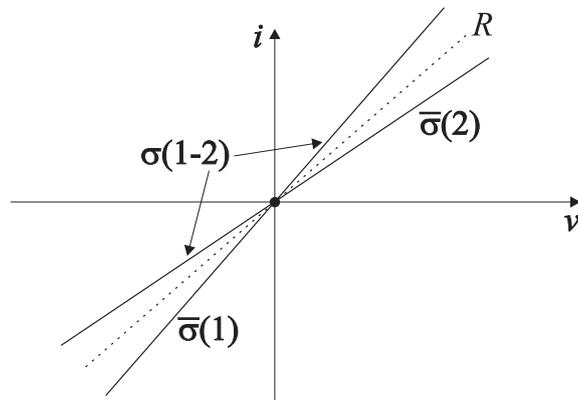
Figure 5. An example of the characteristic of a linear resistor with tolerance.

The number of segments $h_m^2 - h_m^1 + 1$ defines its rank. In Figure 6, the PWL characteristic in Figure 2 is divided in 3 T-PWL characteristics. Analogously, it is possible to define a truncated SPWL (T-SPWL) characteristic associated to a SPWL characteristic $\sigma_n(1, K_n)$. A T-SPWL characteristic $\sigma_n(k_n^1 - k_n^2)$ contains all the strip segments from k_n^1 to k_n^2. The number of segments $k_n^2 - k_n^1 + 1$ defines its rank. Extreme cases are a T-SPWL characteristic coinciding with the original SPWL one and a T-SPWL characteristic composed of one strip segment. An example is shown in Figure 7.

Substituting each $\xi_m(1, H_m)$ and each $\sigma_n(1, K_n)$ with one of their segments $\overline{\overline{\xi}}_m(h_m)$ and, respectively, strip segments $\overline{\sigma}_n(k_n)$, a unit-rank circuit is obtained, a generalization of the linear circuit in a PWL circuit. According to Eq. (1), the configuration domain of a unit-rank circuit is

$$\overline{\zeta}(h_1, ..., h_M, k_1, ..., k_N) \equiv \mathcal{K} \cap \left[\widetilde{\mathcal{L}} \times \lambda(h_1, ..., h_M, k_1, ..., k_N) \right] \subset \widetilde{\mathcal{Z}}, \qquad (2)$$

where

$$\lambda(h_1, ..., h_M, k_1, ..., k_N) \equiv \overline{\overline{\xi}}_1(h_1) \times \cdots \times \overline{\overline{\xi}}_M(h_M) \times$$
$$\times \overline{\sigma}_1(k_1) \times \cdots \times \overline{\sigma}_N(k_N) \subset P$$

is the corresponding unit-rank region.

If $\overline{\zeta}(\cdot)$ is non-empty, the unit-rank region (and circuit) is said to be admissible; otherwise, it is said to be non-admissible. Unlike PWL circuits, where one admissible linear region supplies only one equilibrium point, in SPWL circuits, one admissible unit-rank region supplies a convex set, because strip segments are 2D convex sets.
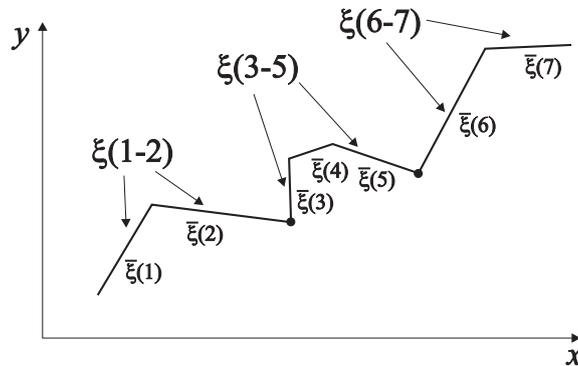

Figure 6. A complete set of three truncated piecewise linear (PWL) characteristics $\xi(1, 2)$, $\xi(3, 5)$, and $\xi(6, 7)$ associated to PWL characteristic $\xi(1, 7)$ in Figure 2.
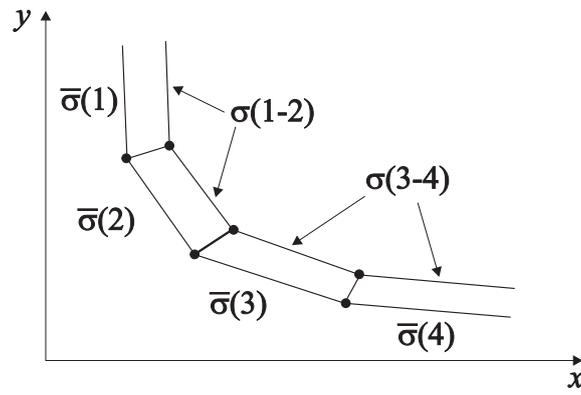
Figure 7. A complete set of two truncated strip piecewise linear (SPWL) characteristics $\sigma(1,2)$ and $\sigma(3,4)$ associated to SPWL characteristic $\sigma(1,4)$ in Figure 4.

The rank L of a SPWL circuit corresponds to the number of unit-rank regions, both admissible and non-admissible, associated to the original circuit, that is,

$$L = \left(\prod_{m=1}^{M} H_m\right)\left(\prod_{n=1}^{N} K_n\right). \tag{3}$$

The configuration domain of the whole SPWL circuit is given by

$$\widetilde{\mathcal{Z}} \equiv \bigcup_{1 \leq h_m \leq H_m} \bigcup_{1 \leq k_n \leq K_n} \overline{\zeta}(h_1, \ldots, h_M, k_1, \ldots, k_N). \tag{4}$$

Generalizing this concept, a T-SPWL circuit is obtained substituting each $\xi_m(1, H_m)$ and each σ_n $(1, K_n)$ with one of the possible $\xi_m\left(h_m^1 - h_m^2\right)$ and, respectively, $\sigma_n\left(k_n^1 - k_n^2\right)$. A T-SPWL region is defined as

$$\tau\left(h_1^1 - h_1^2, \ldots, h_M^1 - h_M^2, k_1^1 - k_1^2, \ldots, k_N^1 - k_N^2\right) \equiv$$
$$\xi_1\left(h_1^1 - h_1^2\right) \times \cdots \times \xi_M\left(h_M^1 - h_M^2\right) \times \sigma_1\left(k_1^1 - k_1^2\right) \times \cdots \times \sigma_N\left(k_N^1 - k_N^2\right) \equiv$$
$$\bigcup_{h_m^1 \leq h_m \leq h_m^2} \bigcup_{k_n^1 \leq k_n \leq k_n^2} \lambda(h_1, \ldots, h_M, k_1, \ldots, k_N) \subset P. \tag{5}$$

It is formed by the union of all unit-rank regions contained in it, whose number constitutes its rank L_τ. The configuration domain of the related T-SPWL circuit is

$$\zeta\left(h_1^1 - h_1^2, \ldots, h_M^1 - h_M^2, k_1^1 - k_1^2, \ldots, k_N^1 - k_N^2\right) \equiv K \cap \left[\widetilde{\mathscr{L}} \times \times \tau\left(h_1^1 - h_1^2, \ldots, h_M^1 - h_M^2, k_1^1 - k_1^2, \ldots, k_N^1 - k_N^2\right)\right]$$

$$\equiv \bigcup_{h_m^1 \leq h_m \leq h_m^2} \bigcup_{k_n^1 \leq k_n \leq k_n^2} \overline{\zeta}(h_1, \ldots, h_M, k_1, \ldots, k_N) \subset \widetilde{\mathcal{Z}}. \tag{6}$$

It corresponds to the union of all the configuration domains of unit-rank regions included in it. Note that, generally, both T-SPWL regions and the related configuration domains are not convex, even if they are formed by the union of convex sets.

A set of T-PWL or T-SPWL characteristics, associated to the same PWL or SPWL characteristic of origin, is said to be complete if each segment or strip segment of the whole characteristic belongs to one and only one T-PWL or T-SPWL characteristic of the set. So, the sum of the ranks of a complete set is equal to the rank of the original characteristic. Examples of complete sets of T-PWL and T-SPWL characteristics are drawn, respectively, in Figures 6 and 7.

Let us partition each PWL and SPWL characteristic of a circuit in a complete set of T-PWL and T-SPWL, respectively, characteristics. The cartesian product of these complete sets yields a set $\mathcal{T}$ of T-SPWL regions that contains all the unit-rank regions of the original SPWL circuit; each one contained in one and only one T-SPWL region of the set. Considering the related T-SPWL circuits and their configuration domains (Eq. (6)), we can state the following 'conservation property':

$$\widetilde{\mathcal{Z}} \equiv \bigcup_{\tau\left(h_1^1 - h_1^2, \ldots, k_N^1 - k_N^2\right) \in T} \zeta\left(h_1^1 - h_1^2, \ldots, h_M^1 - h_M^2, k_1^1 - k_1^2, \ldots, k_N^1 - k_N^2\right) \tag{7}$$

Set $\mathcal{T}$ is said complete because all the unit-rank regions of the original SPWL circuit are contained in one element of $\mathcal{T}$. This property is a generalization of Eq. (4): The original circuit is decomposed in macro-regions, that is, the T-SPWL regions belonging to a complete set. They are, in turn, formed by a union of unit-rank regions.

5. POLYHEDRAL CHARACTERISTICS AND CIRCUITS

Polyhedral characteristics were defined in [20] as convex hulls of T-PWL characteristics. They were generalized in [22]. In the present paper, the original definition of polyhedral characteristic given in [20] is adopted.

A polyhedral characteristic is a convex set of points $[x \; y]^T$ in $\mathcal{R}^2$. It is defined as the linear combination of Q vertices $[\hat{x}^q \; \hat{y}^q]^T$ by parameters $a^q \in \mathcal{R}$. In vectorial notation, it is

$$\begin{bmatrix} x \\ y \end{bmatrix} = a^1 \begin{bmatrix} \hat{x}^1 \\ \hat{y}^1 \end{bmatrix} + a^2 \begin{bmatrix} \hat{x}^2 \\ \hat{y}^2 \end{bmatrix} + \ldots + a^Q \begin{bmatrix} \hat{x}^Q \\ \hat{y}^Q \end{bmatrix}$$

$$\sum_{q=1}^{Q} a^q c^q = 1 \quad \text{with}: \quad \begin{cases} c^q = 1 \;\; \text{for finite vertices} \\ c^q = 0 \;\; \text{for vertices at infinity} \end{cases} \tag{8}$$

$$a^q \geq 0 \quad \forall \; q.$$

The vertices may be finite or at infinity. In the latter case, their coordinates $(\hat{x}^q, \hat{y}^q)$ represent the corresponding directions. Parameters a^q corresponding to infinite vertices are not limited to 1 ($c^h = 0$), because the polyhedron is not bounded. The finite vertices located inside the polyhedron or on a segment of the boundary are called pseudo-vertices: Their only effect is to increase the number of parameters a^q. In any case, a set defined using (8) is always convex, because its boundary is formed only by the external vertices linked by segments.

In [20], a polyhedral characteristic associated to a T-PWL characteristic has been defined as the hull of the T-PWL characteristic, that is, the most restricted convex set containing the T-PWL characteristic. An example of three polyhedral characteristics associated to T-PWL characteristics of Figure 6 is shown in Figure 8. Similarly, a polyhedral characteristic associated to a T-SPWL characteristic is defined as the hull of the T-SPWL characteristic

$$\psi_n\left(k_n^1 - k_n^2\right) \equiv \text{hull}\left[\sigma_n\left(k_n^1 - k_n^2\right)\right], \tag{9}$$

where the boundary breakpoints of T-SPWL characteristics become the vertices of the polyhedral characteristic. In Figure 9, there are three examples of polyhedral characteristics associated to as many T-SPWL characteristics.

The polyhedral characteristic associated to a unit-rank T-SPWL characteristic, that is a strip-segment, coincides with the strip segment itself:
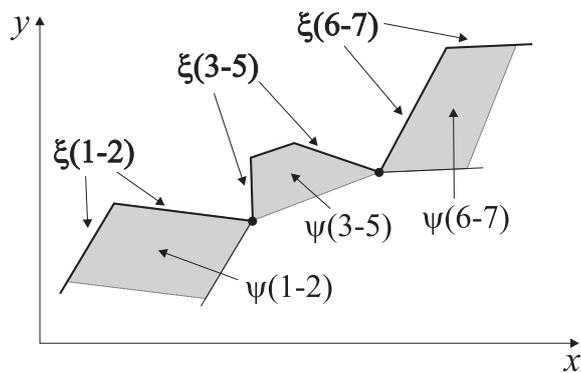
Figure 8. Polyhedral characteristics associated to $\xi(1,2)$, $\xi(3,5)$, and $\xi(6,7)$ in Figure 6.
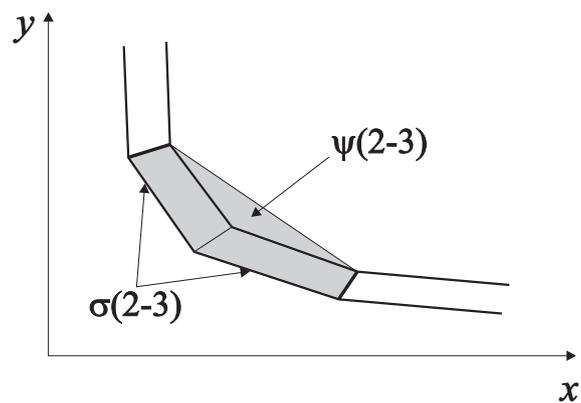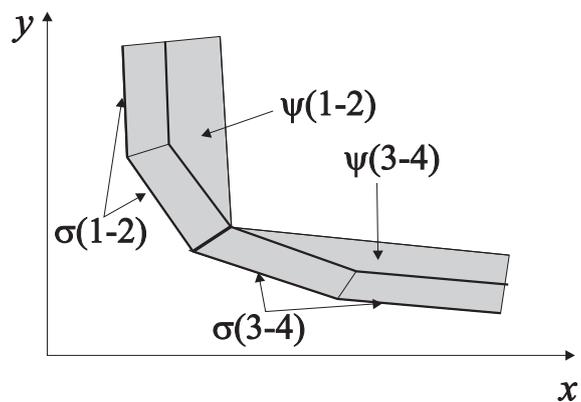
Figure 9. Polyhedral characteristics associated to $\sigma(1,2)$, $\sigma(2,3)$, and $\sigma(3,4)$ of $\sigma(1,4)$ in Figure 4.

$$\psi_n(k_n) \equiv \sigma_n(k_n). \tag{10}$$

It is important to note that polyhedra are a powerful tool that allows one to handle both T-PWL and T-SPWL characteristics with the same approach.

Substituting each T-PWL and each T-SPWL characteristic of a T-SPWL circuit by the corresponding associate polyhedral characteristic, the associate polyhedral circuit is obtained. The related polyhedral region is the hull of the corresponding T-SPWL region. It is defined as

$$\pi\left(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_n^1 - k_n^2, ..., k_N^1 - k_N^2\right) \equiv$$
$$\equiv \psi_1\left(h_1^1 - h_1^2\right) \times \cdots \times \psi_M\left(h_M^1 - h_M^2\right) \times \psi_{M+1}\left(k_1^1 - k_1^2\right) \times \cdots \times \psi_{M+N}\left(k_N^1 - k_N^2\right) \equiv \qquad (11)$$
$$\equiv \mathrm{hull}\tau\left(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_1^1 - k_1^2, ..., k_N^1 - k_N^2\right).$$

So, the configuration domain of a polyhedral circuit is

$$\theta\left(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_1^1 - k_1^2, ..., k_N^1 - k_N^2\right) \equiv \mathcal{K} \cap \left[\widetilde{\mathcal{Z}} \times \times \pi\left(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_1^1 - k_1^2, ..., k_N^1 - k_N^2\right)\right] \subset \widetilde{\mathcal{Z}}.$$
$$(12)$$

The fundamental property of an associate polyhedral circuit is that configuration domain ζ of a T-SPWL circuit is contained in configuration domain θ of the associate polyhedral circuit. The so-called 'inclusion property' states that

$$\zeta\left(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_1^1 - k_1^2, ..., k_N^1 - k_N^2\right) \subset \theta\left(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_1^1 - k_1^2, ..., k_N^1 - k_N^2\right). \quad (13)$$

This property, already valid for T-PWL circuits, retains for T-SPWL circuits, because a polyhedral characteristic is a convex hull for both T-PWL and T-SPWL characteristics.

The configuration domain of a polyhedral circuit may be empty or a convex multidimensional polyhedron. If the configuration domain is empty, the corresponding T-SPWL circuit has an empty configuration domain, because of the inclusion property (13) stated previously. Otherwise, if the configuration domain is non-empty, the T-SPWL circuit may have a non-empty configuration domain. Moreover, the configuration domain of a unit-rank T-SPWL circuit coincides with the configuration domain of the associate polyhedral circuit, because segments and strip-segments are convex sets that coincide with the associate polyhedra.

In Figure 10, an SPWL approximation of strip characteristics in Figure 1b are considered. SPWL characteristic $\sigma_1(1-1)$ is composed of one strip segment $\overline{\sigma}_1(1)$, while SPWL characteristic $\sigma_2(1-8)$ is composed of 8 strip-segments $\overline{\sigma}_2(1), ..., \overline{\sigma}_2(8)$. As it results from figure, there are two T-SPWL regions with solutions, $\tau(1, 2-5) \equiv \overline{\sigma}_1(1) \times \sigma_2(2-5)$ and $\tau(1,7) \equiv \overline{\sigma}_1(1) \times \overline{\sigma}_2(7)$. They give origin to polyhedral regions $\pi(1, 2-5) \equiv \psi_1(1) \times \psi_2(2-5)$ and $\pi(1,7) \equiv \psi_1(1) \times \psi_2(7)$, respectively. Their configurations domains $\theta(1, 2-5)$ and $\theta(1,7)$ are both non-empty and contain (for inclusion property (13)) the related equilibrium regions, that is, configuration domains $\zeta_A(1, 2-5)$ and $\zeta_A(1,7)$, respectively. Configuration domain $\zeta_A(1, 2-5)$ is formed by the union of four unit-rank regions $\overline{\zeta}_A(1,2)$, $\overline{\zeta}_A(1,3)$, $\overline{\zeta}_A(1,4)$, and $\overline{\zeta}_A(1,5)$ (6). Instead $\zeta_A(1,7)$ coincides with $\overline{\zeta}_A(1,7)$.
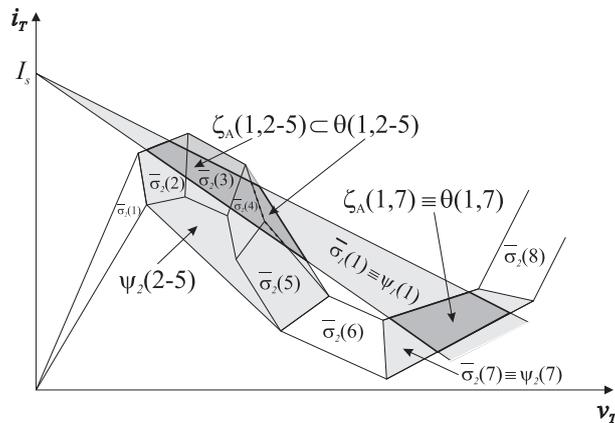
Figure 10. Configuration domains for a strip piecewise linear approximation of strip characteristics in Figure 1b.

5.1. Solution of a polyhedral circuit

To test the configuration domain of a polyhedral circuit, that is, to find if it is empty or not, a suitable LP problem [23] is solved whose feasible domain just coincides with the configuration domain of the related polyhedral region. The related decision variables are all the parameters of polyhedral characteristics, subject to non-negativity constraints. So, with (12) in mind, considering the Kirchhoff's laws, the linear elements equations and the constitutive relations, expressed with (8), of the $M+N$ associate polyhedra, the system of equations/inequalities for describing the configuration domain $\theta(h_1^1 - h_1^2, ..., h_M^1 - h_M^2, k_1^1 - k_1^2, ..., k_N^1 - k_N^2)$ of a polyhedral circuit results to be

$$\mathbf{U}\,\mathbf{x} + \mathbf{V}\,\mathbf{y} = \mathbf{r} \tag{14a}$$

$$x = \left[(\mathbf{a}_1)^T \hat{\mathbf{x}}_1 ... (\mathbf{a}_{M+N})^T \hat{\mathbf{x}}_{M+N}\right]^T \tag{14b}$$

$$\mathbf{y} = \left[(\mathbf{a}_1)^T \hat{\mathbf{y}}_1 ... (\mathbf{a}_{M+N})^T \hat{\mathbf{y}}_{M+N}\right]^T \tag{14c}$$

$$(\mathbf{a}_w)^T \mathbf{c}_w = 1, \qquad \text{for } w = 1, 2, ..., M+N \tag{14d}$$

$$\mathbf{a}_w \geq 0, \qquad \text{for } w = 1, 2, ..., M+N. \tag{14e}$$

Equation (14a) is the implicit representation of the linear $(M+N)$ multi-port obtained by removing the $M+N$ nonlinear elements. It defines sets $\mathcal{K}$ and $\mathcal{L}$. $\mathbf{U}$ and $\mathbf{V}$ are $(M+N) \times (M+N)$ matrices and $\mathbf{r}$ is a $(M+N)$-vector. Equations (14b–d), together with inequalities (14e), describe the polyhedral region π adopting the parametrical notations of (8). Vectors $\hat{\mathbf{x}}_w = \left[\hat{x}_w^1 ... \hat{x}_w^{Q_w}\right]^T$ and $\hat{\mathbf{y}}_w = \left[\hat{y}_w^1 ... \hat{y}_w^{Q_w}\right]^T$ group the cartesian coordinates of vertices of the $(M+N)$ polyhedral characteristics, while $\mathbf{a}_w = \left[a_w^1 ... a_w^{Q_w}\right]^T$, $\mathbf{c}_w = \left[c_w^1 ... c_w^{Q_w}\right]^T$ are Q_w-vectors $(w = 1, 2, ..., M+N)$ grouping the parameters of polyhedral characteristics.

By eliminating vectors $\mathbf{x}$ and $\mathbf{y}$, system (14) is rearranged into the compact form

$$\sum_{w=1}^{M+N} \sum_{q=1}^{Q_w} \left[\hat{x}_w^q u_{jw} + \hat{y}_w^q v_{jw}\right] a_w^q = r_j, \tag{15a}$$
$$\text{where } j = 1, 2, ..., M+N$$

$$\sum_{q=1}^{Q_w} c_w^q a_w^q = 1 \qquad \text{for } w = 1, 2, ..., M+N \tag{15b}$$

$$a_w^q \geq 0 \qquad \text{for } q = 1, 2, ..., Q_w, \ w = 1, 2, ..., M+N. \tag{15c}$$

a_w^q, $q = 1, ..., Q_w$, $w = 1, ..., M+N$, subject to non-negativity constraints (15c).

The tableau of the LP problem has dimensions $2(M+N) \times \left(\sum_{w=1}^{M+N} Q_w + 1\right)$. The number of rows depends only on the number $M+N$ of PWL and SPWL characteristics, while the number of columns is equal to the total number $\sum_{w=1}^{M+N} Q_w$ of breakpoints appearing in the $(M+N)$ T-PWL and T-SPWL characteristics. The emptiness of the configuration domain θ, coincident with the feasible domain of the LP problem in (14), can be tested by means of Phase I, that is the procedure, well known in LP, used for finding if the LP problem has a feasible domain [23].

6. THE ALGORITHM

The algorithm is composed of three steps in cascade. The first step is structured according to a binary tree. It stops when admissible unit-rank regions (AURs) are found [21]. The second step consists in grouping adjacent AURs to form the equilibrium regions, and the third step consists of classifying the equilibrium regions in certain or uncertain.

6.1. Genealogical tree

The first step starts with the main node of the binary tree, corresponding to the original SPWL circuit with rank L, containing all the unit-rank regions and, so, all the possible solution regions. The associate polyhedral circuit is built and tested: If its configuration domain θ is non-admissible, that is, it is empty, domain $\widetilde{\mathcal{Z}}$ of the original SPWL circuit is in turn empty for the inclusion property (13), and so the algorithm stops. The original SPWL circuit has no solutions.

Otherwise, if it is admissible, either one of the M PWL characteristics or one of the N SPWL characteristics is partitioned into a complete set of two T-PWL (T-SPWL) characteristics. The choice of the characteristic to be partitioned and that one of the breakpoint partitioning it has been performed in a heuristic way. Many realistic examples have suggested to choose, during the execution of the algorithm, the characteristic subject to the minimum number of partitions in the previous generations and the breakpoint separating this characteristic in two portions with equal (for even rank) or quasi-equal (for odd rank) number of segments.

By replacing the original PWL (SPWL) characteristic with one of the T-PWL (T-SPWL) characteristics, two new T-SPWL circuits are originated. They represent a complete set of T-SPWL circuits, denoted as the first-generation nodes. In their turn, these first-generation nodes are tested by means of their associate polyhedral circuits to ascertain if they are admissible or non-admissible. A non-admissible node contains only non-admissible unit-rank regions, so it does not generate any other node and can be deleted. Instead, an admissible one generates, in turn, two second-generation nodes with the same rule described previously, and so on. The nodes of the tree are tested one by one in sequence. For increasing level of generation, the rank of the generated T-SPWL regions decreases until unit-rank regions are reached. The first step of the algorithm stops when the tree has been completed, that is, all its branches have arrived at either a non-admissible node or at an AUR. In the sequel, an AUR will be denoted as $\lambda_A(h_1, \ldots, h_M, k_1, \ldots, k_N)$, while its configuration domain as $\overline{\zeta}_A(h_1, \ldots, h_M, k_1, \ldots, k_N)$. Because there is a direct correspondence between λ_A and $\overline{\zeta}_A$, the term AUR will be used indifferently for both, without possibility of confusion.

The simple rule of generating a complete set of two T-SPWL regions at every node implies, for the conservation property (7), that the overall rank, that is, the overall number of unit-rank regions, is conserved during the execution of the algorithm. So, at the end of the tree, the sum of the ranks of all non-admissible T-SPWL regions and of all AURs equals the rank L of the original SPWL circuit. This property guarantees that the AURs found with this algorithm coincide with the AURs of the original SPWL circuit.

In principle, at each generation, the number of nodes increases exponentially, in the worst case by factor 2, but, in circuits of practical interest, many non-admissible T-SPWL regions appear at low generation levels, that is, with high ranks, making so efficient this algorithm. Indeed, T-SPWL circuits with high ranks include inside many unit-rank regions that are deleted all together with only one LP analysis.

6.2. Clustering algorithm

If tolerances are very small, equilibrium regions are expected to be limited to one AUR. But, as tolerances grow, equilibrium regions can become more extended, including more adjacent AURs. The second step of the algorithm consists of grouping together the AURs forming the same equilibrium regions. Let us suppose to have found at the end of the first step of the algorithm AURs $\lambda_A^j(h_1^j, \ldots, h_M^j, k_1^j, \ldots, k_N^j)$, $j = 1, 2, \ldots, J$. In general, the γth admissible T-SPWL region $\tau_A^\gamma(J_\gamma)$ can be formed by the union of several AURs, so it is defined as

$$\tau_A^\gamma(J_\gamma) \equiv \bigcup_{j \in J_\gamma} \lambda_A^j\left(h_1^j, ..., h_M^j, k_1^j, ..., k_N^j\right), \tag{16}$$

where set J_γ contains the indices j of the AURs constituting it. Correspondingly, its configuration domain, that is, the equilibrium region $\zeta_A^\gamma(J_\gamma)$, is a connected, generally non-convex, set obtained by

$$\zeta_A^\gamma(J_\gamma) \equiv \bigcup_{j \in J_\gamma} \overline{\zeta}_A^j\left(h_1^j, ..., h_M^j, k_1^j, ..., k_N^j\right). \tag{17}$$

The AURs forming the same equilibrium region must be adjacent. So, to evaluate their respective distances and state if two unit-rank regions are adjacent or not, and so belong to the same equilibrium region, a metric in the space of unit-rank regions has to be introduced.

Two segments of a PWL or two strip segments of a SPWL characteristic are adjacent if the difference in absolute value of their respective indices is 1. This simple concept can be extended to linear regions. In Figure 10, four adjacent AURs $\overline{\zeta}_A^1(1,2)$, $\overline{\zeta}_A^2(1,3)$, $\overline{\zeta}_A^3(1,4)$, and $\overline{\zeta}_A^4(1,5)$ form equilibrium region $\zeta_A^1(1,2,3,4)$ (according to the last notation introduced). In this case, $J_1 = \{1,2,3,4\}$. Instead, equilibrium region $\zeta_A^2(5)$ is formed by one AUR $\overline{\zeta}_A^5(1,7)$, with $J_2 = \{5\}$. Analyzing the strip segments involved in AURs of $\zeta_A^1(1,2,3,4)$, the first characteristic σ_1 is represented always by the same strip segment $\overline{\sigma}_1(1)$, while σ_2 contributes with the adjacent strip segments $\overline{\sigma}_2(2)$, $\overline{\sigma}_2(3)$, $\overline{\sigma}_2(4)$, and $\overline{\sigma}_2(5)$. So, indices of $\overline{\zeta}_A$s due to σ_1 are equal, while indices due to σ_2 differ of one between each AUR and the adjacent one. Generalizing this example, two unit-rank regions are adjacent if one or more PWL or SPWL characteristics have adjacent segments, that is, one or more indices of PWL and SPWL strip segments have a difference in absolute value not greater than 1. This definition of adjacency of two unit-rank regions implies naturally the choice of the metric to be adopted, that is, the infinite-norm distance or Chebyshev distance. This is not the only possible metric, also the 1-norm distance can be considered, but the infinite-norm is the most effective. Therefore, the distance between two AURs $\lambda_A^{j_1}$ and $\lambda_A^{j_2}$ is calculated with

$$d\left(\lambda_A^{j_1}\left(h_1^{j_1}, ..., h_M^{j_1}, k_1^{j_1}, ..., k_N^{j_1}\right), \lambda_A^{j_2}\left(h_1^{j_2}, ..., h_M^{j_2}, k_1^{j_2}, ..., k_N^{j_2}\right)\right) =$$
$$= max\left(\left|h_1^{j_1} - h_1^{j_2}\right|, ..., \left|h_M^{j_1} - h_M^{j_2}\right|, \left|k_1^{j_1} - k_1^{j_2}\right|, ..., \left|k_N^{j_1} - k_N^{j_2}\right|\right). \tag{18}$$

They are adjacent if the distance is equal to 1. If it is equal or greater to 2, then AURS are non-adjacent.

Basing on this metric, an algorithm of clustering [24], that is, an unsupervised learning algorithm that establishes a classification of points in a given space according to their relative distances, has been adopted. The clustering algorithm implemented in this paper is inspired to density based spatial clustering of applications with noise algorithm [25]. It is a density-based clustering algorithm, that is, clusters are formed starting from the estimated density distribution of corresponding points. In our case, equilibrium regions are sets with a density of 1, with members all adjacent. The algorithm presented here finds the AURs members of each equilibrium region as follows. The first AUR in the list is assigned to the first equilibrium region. Then, all remaining AURs are examined measuring their distances from the first one. Those AURs that result to be adjacent are assigned to the first equilibrium region. The scanning of the list of AURs is repeated, comparing the distances of free AURs with those belonging to the first equilibrium region, until no other adjacent AURs are found. Completed the first equilibrium region, the next free AUR is taken as first element of the second equilibrium region. The scanning of the list of free AURs is repeated in the same way and so on. The clustering algorithm stops when all AURs have been assigned to an equilibrium region.

6.3. Certain and uncertain equilibrium regions

After equilibrium regions are formed, they have to be analyzed to determine if they are certain or uncertain. An equilibrium region is said to be certain if it can produce surely an equilibrium point, whichever is the choice of the parameters for each SPWL characteristic. Otherwise, it is said uncertain.

This purpose can be accomplished by the evaluation of the B-PWL circuits of the SPWL circuit. They are obtained substituting each SPWL characteristic $\sigma_n(1, K_n)$ with one of the two B-PWL characteristics $\sigma_n^{(u)}(1, K_n)$ and $\sigma_n^{(\ell)}(1, K_n)$. Because there are N SPWL characteristics, there are 2^N B-PWL circuits. Each of them can be identified by a label composed of N binary digits, one for SPWL characteristic. The nth digit is '0' if $\sigma_n^{(\ell)}(1, K_n)$ has been chosen, '1' if $\sigma_n^{(u)}(1, K_n)$. The solutions of the B-PWL circuits are denoted as 'effective vertices'. Each effective vertex is a vertex of configuration domains $\zeta_A^\gamma(J_\gamma)$.

The effective vertices can be easily found solving the boundary unit-rank linear circuits associated to each AUR $\lambda_A^j(h_1^j, \ldots, h_M^j, k_1^j, \ldots, k_N^j)$. They are obtained substituting each strip segment $\bar\sigma_n^j(k_m^j)$ with one of the two boundary segments $\bar\sigma_n^{(u)j}(k_m^j)$ and $\bar\sigma_n^{(\ell)j}(k_m^j)$. The effective vertices can so be grouped together in according to the AUR they belong and, as second step, to the related equilibrium region $\zeta_A^\gamma(J_\gamma)$, seen as union of AURs. In general, the effective vertices associated to an equilibrium region $\zeta_A^\gamma(J_\gamma)$ coincide with a subset of vertices of configuration domain $\zeta_A^\gamma(J_\gamma)$. If each one of the 2^N B-PWL circuits associated to $\tau_A^\gamma(J_\gamma)$ admits an effective vertex, then $\zeta_A^\gamma(J_\gamma)$ can be declared certain. This means that it contains at least one certain solution whichever is the choice of the real PWL characteristics. This is because all nonlinear characteristics, both certain and uncertain, have been supposed to be continuous and infinite. But far more complicated situations may occur, as shown in the following example.

In Figure 11a and b, two SPWL characteristics $\sigma_1(1, K_1)$ and $\sigma_2(1, K_2)$ are drawn in the same plane v–i. In both cases, equilibrium region ζ_A (marked with a shadowed area) is formed by the union of AURs $\bar\zeta_A^1(k_1, , k_2)$ and $\bar\zeta_A^2(k_1 + 1, k_2)$. The first AUR $\bar\zeta_A^1(k_1, , k_2)$ is given by the intersection of strip-segments $\bar\sigma_1(k_1)$ and $\bar\sigma_2(k_2)$, the second AUR $\bar\zeta_A^2(k_1 + 1, k_2)$ of $\bar\sigma_1(k_1 + 1)$ and $\bar\sigma_2(k_2)$. The effective vertices (marked with dots), for both AURs and equilibrium region, are found as solutions of the B-PWL circuits obtained substituting SPWL characteristics $\sigma_1(1, K_1)$ and $\sigma_2(1, K_2)$ with their respective B-PWL characteristics. There are 4 B-PWL circuits, denoted as (00), (01), (10), and (1, 1). For example, B-PWL circuit (0, 1) is obtained substituting $\sigma_1(1, K_1)$ with $\sigma_1^{(\ell)}(1, K_1)$ and $\sigma_2(1, K_2)$ with $\sigma_2^{(u)}(1, K_2)$. The number of effective vertices related to each B-PWL circuit for AURs $\bar\zeta_A^1(k_1, , k_2)$ and $\bar\zeta_A^2(k_1 + 1, k_2)$ is shown in Table I, columns 2 and 3. The number of effective vertices for equilibrium region ζ_A (column 4) is obtained summing up the effective vertices of the corresponding AURs.

In case of Figure 11a, it is easy to argue from Figure 11 that there is one certain solution, because any choice of the real characteristics yields surely an equilibrium point in ζ_A. Of course, depending on the real characteristics, the solution may fall either in $\bar\zeta_A^1(k_1, k_2)$ or $\bar\zeta_A^2(k_1 + 1, k_2)$. This situation can be deduced easily from column 4 in Table I. Indeed, there is one effective vertex for each B-PWL circuit. On the contrary, in case of Figure 11b, B-PWL circuit (0, 1) have two effective vertices, while the other ones have 0 effective vertices. This means that there is not a certain solution for any choice of real characteristics, but there may be either two solutions, one for AUR, or no solution at all. Equilibrium region ζ_A is uncertain, and it gives two uncertain solutions.

From this example, we can deduce that both the minimum and maximum number of effective vertices for an equilibrium region are meaningful. Let us define as m_γ^{EV} and M_γ^{EV}, respectively, the minimum and the maximum value of effective vertices of the γth equilibrium region $\zeta_A^\gamma(J_\gamma)$. Because nonlinear characteristics are continuous and infinite, we can easily state that

1. m_γ^{EV} is the number of certain solutions;
2. $\left(M_\gamma^{EV} - m_\gamma^{EV}\right)$ is the minimum number of uncertain solutions (besides certain solutions)

Unlike certain solutions, the actual number of uncertain solutions cannot be determined surely for every circuit. The first of the examples shown in the next section, containing two tunnel diodes, is
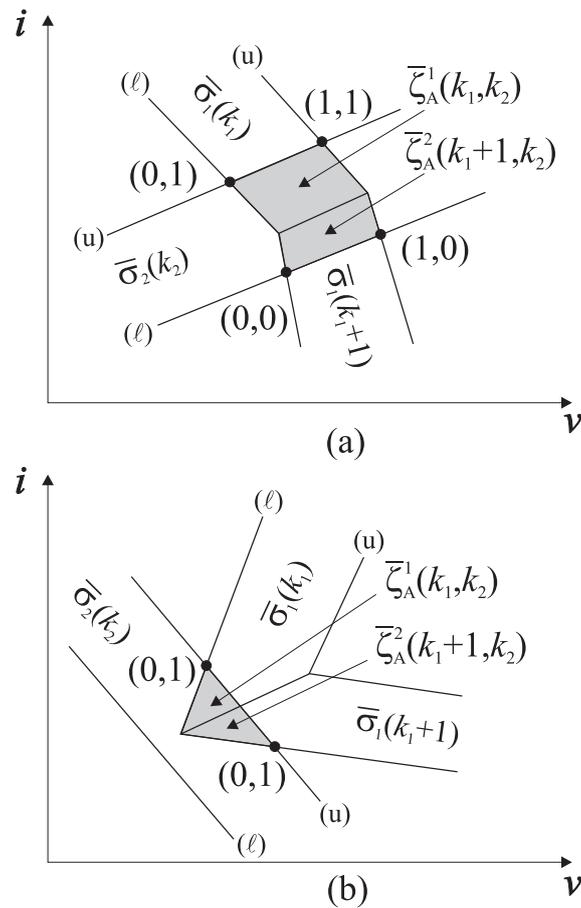
Figure 11. Examples of a certain equilibrium region (a) and an uncertain equilibrium region (b) with their effective vertices.

Table I. Effective vertices of AURS and equilibrium region in Figure 11.

	B-PWL circuit	Effective vertices $\overline{\zeta}_A^1(k_1,,k_2)$	Effective vertices $\overline{\zeta}_A^2(k_1+1,k_2)$	Effective vertices ζ_A
Case (a)	00	0	1	1
	01	1	0	1
	10	0	1	1
	11	1	0	1
Case (b)	00	0	0	0
	01	1	1	2
	10	0	0	0
	11	0	0	0

AURS = admissible unit-rank region; B-PWL = boundary piecewise linear.

explanatory. Only in some particular cases, the number of uncertain solutions can be determined for sure. This is the case of transistors circuits, as those ones presented in the second and third examples in the next section. The reason is that transistors are modeled with Ebers–Moll that adopts exponential diodes. These resistors have a monotone and convex characteristic, without flexes, unlike tunnel diodes. As example, a simple circuit is shown in Figure 12. In case (a), with V_s, $R_s > 0$, there is one certain solution, because any couple of real characteristics cut each other transversally. Instead in case (b), with $V_s > 0$ and $R_s < 0$, there are either two solutions or no solution at all, depending on the choice of real characteristics. Indeed, an SPWL analysis of this circuit, whichever is the number of strip segments used to approximate the strip characteristics,

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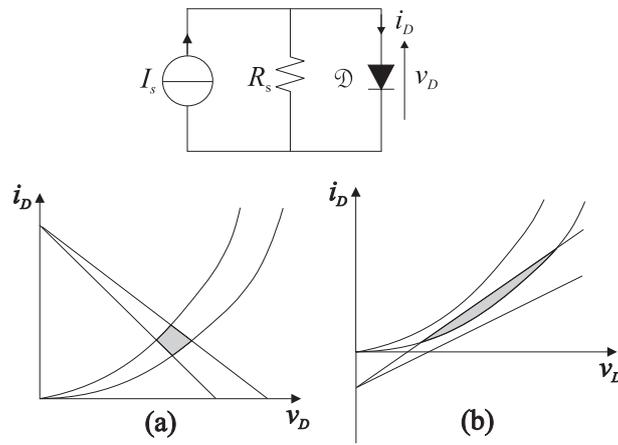
Figure 12. An exponential diode circuit.

would give an equilibrium region with $m^{EV} = 0$ and $M^{EV} = 2$. So, $(M^{EV} - m^{EV})$ represents actually the exact number of uncertain solutions. Furthermore, when the exact number of solutions is known, it is possible to apply another clustering algorithm, a hierarchical one, to identify the AURs where the single solutions, either certain or uncertain, may appear.

Note that it is not possible to reconstruct an equilibrium region from its effective vertices, because not all AURs belonging to an equilibrium region have effective vertices. So the overall algorithm presented here cannot be substituted just by the solution of the 2^N B-PWL circuits.

7. EXAMPLES

The proposed algorithm has been implemented using C++ language on a PC with Intel(R) Core(TM) i5 CPU 2.27 GHz (Santa Clara, CA, USA). The first simple example shows the effects of an expansion of tolerances on equilibrium regions for a tunnel diodes circuit. The second and third examples present two multi-state circuits already analyzed in other papers.

7.1. First example

As first example, let us consider the circuit in Figure 13. Tunnel diodes D_1 and D_2 have the following characteristics [26, 27]:

$$
\begin{aligned}
D_1 &: i = 0.43v_1^3 - 2.69v_1^2 + 4.56v_1 \\
D_2 &: i = 2.5v_2^3 - 10.5v_2^2 + 11.8v_2.
\end{aligned}
\tag{19}
$$

Each of them has been approximated with a 10 segments PWL characteristic equispaced in the range [0,4] V. The ideal current source I_s with value 10 A is certain, while linear resistor in parallel may vary in three different ranges by increasing tolerances, delimited by values $R_a = 0.2\Omega$, $R_b = 0.32\Omega$,
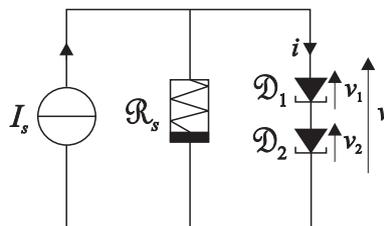

Figure 13. A tunnel diodes circuit.

$R_c = 0.38\Omega$, and $R_d = 0.8\Omega$. Because it is linear but uncertain, it is denoted with symbol $\mathcal{R}_s$. The three ranges are (1) $[R_b, R_c]$, (2) $[R_a, R_c]$, and (3) $[R_a, R_d]$. It is modeled with an SPWL resistor formed by two strip-segments, as shown in Figure 5. The characteristic of the diodes series and the load lines corresponding to boundary resistances R_a, R_b, R_c, and R_d are shown in Figure 14. This circuit has rank 200, that is, it contains $200 = 10 \times 10 \times 2$ linear regions, because each diode has 10 segments and the resistor $\mathcal{R}_s$ has two strip segments. Because $N = 1$, there are two B-PWL circuits per equilibrium region. The number of effective vertices for each possible equilibrium region is shown in Table II. Note that $\zeta_A^3(J_3)$ exists only for the first range $[R_b, R_c]$.

Case $[R_b, R_c]$, the one with the minimum tolerance, yields totally seven AURs divided in three equilibrium regions. One equilibrium region is formed by one AUR, the other two by three AURs each. All B-PWL circuits have one effective vertex, that is, $M^{EV} = m^{EV} = 1$ for all equilibrium regions. This means that the three equilibrium regions are certain and supply one certain solution per each. Case $[R_a, R_c]$, the one with the middle tolerance, yields 11 AURs divided in two equilibrium regions. $\zeta_A^1(J_1)$ (five AURs), related to the butterfly of diodes series, is uncertain, having $M^{EV} = 2$ and $m^{EV} = 0$. So it supplies two uncertain solutions. Instead, $\zeta_A^2(J_2)$ (six AURs), related to the main branch of the diodes series, is certain, because $M^{EV} = m^{EV} = 1$. It supplies one certain solution. At last, case $[R_a, R_d]$, the one with the maximum tolerance, yields 27 AURs divided in two equilibrium regions. Equilibrium region $\zeta_A^1(J_1)$ (12 AURs) is related to the butterfly. It is uncertain, because $M^{EV} = m^{EV} = 0$, but the number of uncertain solutions, that is, equal to 2 as can be deduced easily from Figure 14, is not determined by $M^{EV} - m^{EV}$. Instead, $\zeta_A^2(J_2)$ (15 AURs), related to the main branch of diodes series, gives one certain solution ($M^{EV} = m^{EV} = 1$).
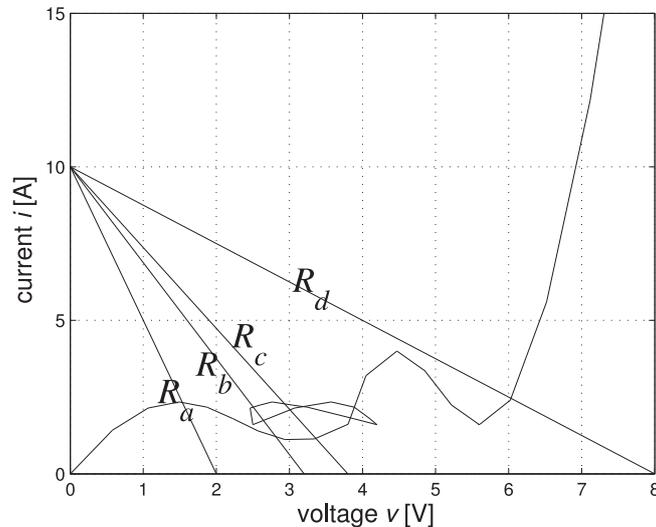

Figure 14. Boundary load lines and characteristic of diodes series for circuit in Figure 13.

Table II. Effective vertices in the first example.

	B-PWL circuit	Effective vertices $\zeta_A^1(J_1)$	Effective vertices $\zeta_A^2(J_2)$	Effective vertices $\zeta_A^3(J_3)$
Case $[R_b, R_c]$	0	1	1	1
	1	1	1	1
Case $[R_a, R_c]$	0	2	1	-
	1	0	1	-
Case $[R_a, R_d]$	0	0	1	-
	1	0	1	-

B-PWL = boundary piecewise linear.

This example is meaningful, because it shows with a very simple circuit the 'structural' effects of increasing tolerances on equilibrium regions. Indeed, the number and properties of equilibrium regions changes when tolerances assume certain values. We pass from three certain equilibrium regions in the first case to two equilibrium regions in the third case. Furthermore, in this third case, the number of uncertain solutions cannot be determined for sure by the analysis of the effective vertices.

7.2. Second example

The four-transistor multi-state circuit shown in Figure 7 of [20] is examined. The same Ebers–Moll model with two diodes and two current-controlled current sources has been adopted for all transistors. Coefficients are $\alpha_F = 0.98$ and $\alpha_I = 0.2$. The exponential nominal characteristic of diodes is $i(t) = 10^{-9}(e^{40v(t)} - 1)$ A, each one approximated with 10 segments, so that the rank of the nominal PWL circuit is 10^8. The nominal circuit has nine exact equilibrium points. Four different cases will be examined. In the first one, only the eight diodes have a tolerance of $\pm 10\%$ in current in comparison with their nominal characteristics. The number of B-PWL circuits is $2^8 = 256$. In the other three cases, a tolerance has been added to the four resistors R_k of nominal value $4k\Omega$. The tolerance is, respectively, of 2%, 5%, and 10%. The rank of these circuits becomes so 1.610^9, because each strip resistance is modeled with two triangular strip segments, as seen in the previous example. The number of B-PWL circuits is $2^{12} = 4096$.

The results for the four cases are shown in Table III. The total number of nodes of the tree (polyhedral circuits) examined during the execution of the algorithm is shown in the second row. It is worth noting that this number is much less that the rank of the circuit. In the third row, it is written that the elapsed time for the complete algorithm included the determination of the certain and uncertain equilibrium regions. Note that the CPU time related to the only genealogical tree plus clustering algorithm takes about 2 s for the 10% case, that is comparable to the time needed for the PWL nominal circuit. The remaining time is due to the classification of equilibrium regions in certain and uncertain, that reveals to be a heavy task. Then, it has shown the number of AURs and equilibrium regions. The equilibrium regions with $M^{EV} = m^{EV} = 1$ supply one certain solution per each. The equilibrium regions with $M^{EV} = 2$ and $= m^{EV} = 0$ supply two uncertain solutions per each. In the case with tolerance of resistors equal to 10%, there is also one equilibrium region with $M^{EV} = 3$ and $= m^{EV} = 1$. This equilibrium region supplies one certain solution and two uncertain solutions. Note that the total number of solutions, both certain and uncertain, is always nine in all cases. If a hierarchical clustering algorithm is applied to the equilibrium regions with more solutions, it is possible to identify suitable clusters of AURs in which only one solution, certain or uncertain, may appear. It is possible to verify that each of them contains one solution of the PWL nominal circuit.

It is remarkable that, as tolerances grow, equilibrium regions expand in number of AURs, until they merge together. Moreover, some certain solutions may become uncertain. Any case, as discussed in Section 3, the examination of effective vertices gives, in this case, the exact number of certain and uncertain solutions.

Table III. Equilibrium regions in the second example.

Case (tolerance of R_k)	0%	2%	5%	10%
Total polyhedral circuits	819	1021	1367	1951
Elapsed time (s)	1.2	12.3	33.6	75.3
Total AURs	16	16	47	107
Equilibrium regions ($M^{EV} = m^{EV} = 1$)	9	9	5	2
Equilibrium regions ($M^{EV} = 2, m^{EV} = 0$)	-	-	2	2
Equilibrium regions ($M^{EV} = 3, m^{EV} = 1$)	-	-	-	1
Total equilibrium regions	9	9	7	5
Total possible solutions	9	9	9	9

AURs = admissible unit-rank regions.

Table IV. Equilibrium regions in the third example.

Case (tolerance of R_k)	0%	2%	5%
Total polyhedral circuits	1277	1881	1955
Tree elapsed time (s)	1.8	4.9	5.1
Total elapsed time (s)	72.3	869.6	1238.9
Total AURs	11	27	39
Equilibrium regions ($M^{EV} = m^{EV} = 1$)	11	11	11
Equilibrium regions ($M^{EV} = 2, m^{EV} = 0$)	—	—	2
Total equilibrium regions	11	11	13
Total possible solutions	11	11	15

AURs = admissible unit-rank regions.

7.3. Third example

The third example is the multi-state circuit shown in Figure 10 of [28]. As in the second example, the same Ebers–Moll model has been adopted, but each exponential nominal characteristic of diodes has been approximated with five segments. The rank of the nominal PWL circuit is $5^{15} \approx 310^{10}$. This circuit, with nominal characteristics for all diodes, has 11 equilibrium points. Three different cases will be examined. In the first one, the 15 diodes have tolerances of $\pm 10\%$ in current respect to their nominal characteristics. The rank is $10^{15} \approx 3.051765^{15}$, and the number of B-PWL circuits is $2^{15} = 32768$. As for the nominal circuit, 11 AURs have been found coinciding with 11 convex and certain equilibrium regions. In the second and third cases, it has added a tolerance to the two resistors of nominal value 2700Ω. Two values of tolerance have been taken into account, 2% and 5%. The rank of the circuit becomes about 1.2210^{11}, and the number of B-PWL circuits is $2^{17} = 131072$. The results are summarized in Table IV.

The total number of nodes of the tree (polyhedral circuits) examined during the execution of the algorithm is shown in the second row. It is worth noting that, in this case too, this number is much less than the rank of the circuit. In the third row, it has written the elapsed time for the tree plus clustering algorithm, while in the fourth row, the elapsed time for the complete algorithm included the determination of the certain and uncertain equilibrium regions. In the 2% case, there are 27 AURs grouped in 11 certain equilibrium regions, of which nine are composed of one AURs, one of five AURs, and 1 of 13 AURs. In the 5% case, there are 39 AURs, but besides the same certain equilibrium regions of the previous case, two uncertain equilibrium regions formed by six AURs each appear, both with $M_{EV} = 2$ and $m_{EV} = 0$. So they bear two further uncertain solutions per each, besides the nominal 11 certain solutions. This example shows clearly how the presence of tolerances in elements may cause the appearance of solutions not present with the nominal values.

The certain–uncertain analysis is very heavy from a computational point of view, because of the high number of B-PWL circuits to be examined, especially when the number of SPWL characteristics grow. If one is interested in only one of the possible equilibrium regions, then the certain–uncertain analysis can be limited only to that equilibrium region, limiting the CPU time. However, even if the aim of this work is to present a method to determine the equilibrium regions of a resistive circuit with tolerances, including their certainty, it is important to note that the efficiency of the program can be surely improved.

8. CONCLUSIONS

The here proposed algorithm investigates the robustness of the equilibrium points of a nonlinear circuit with respect to device tolerances. It is based on the introduction of strip characteristics and polyhedral characteristics. It is so possible to find equilibrium regions in which the equilibrium points may fall as characteristics varies. The distinction between certain and uncertain equilibrium regions allows the designer to check possible undesired behaviors of the circuit because of deviation of real characteristics from nominal ones. By repeating these analyses, the designer can

determine the maximum acceptable tolerances for assuring a correct behavior of the circuit. The algorithm adopts LP techniques and a clustering algorithm. The possible improvements of this algorithm regards the optimization of the routines used to classify the equilibrium regions in certain and uncertain. Not only, but also, a new approach can be searched for. Instead, a real challenge can be the extension of this approach to the analysis of dynamic circuits, at least of their steady state.

9. LIST OF MAIN SYMBOLS

- $\mathcal{L}$: Space spanned by variables of linear elements;
- $\mathcal{P}$: Space spanned by variables of nonlinear elements;
- $\mathcal{Z}$: Space spanned by all branch variables;
- $\widetilde{\mathcal{L}}$: Affine subspace of $\mathscr{L}$ satisfying linear certain relations;
- $\widetilde{\mathcal{P}}$: Subset of $\mathcal{P}$ satisfying nonlinear and linear uncertain relations;
- $\mathcal{K}$: Subspace of $\mathcal{Z}$ satisfying Kirchhoff's equations;
- $\widetilde{\mathcal{Z}}$: Configuration domain of circuit (subset of $\mathcal{Z}$);
- ξ_m: piecewise linear (PWL) or truncated PWL (T-PWL) certain characteristic;
- $\overline{\xi}$: Segment of a PWL certain characteristic;
- σ_n: Strip PWL (SPWL) or truncated SPWL (T-SPWL) characteristic;
- $\overline{\sigma}$: Strip segment of an SPWL characteristic;
- $\sigma_n^{(u)}, \sigma_n^{(\ell)}$: boundary (upper and lower) PWL or T-PWL characteristics;
- ψ: Polyhedral characteristic;
- λ: Unit-rank region;
- τ: T-SPWL region;
- π: Polyhedral region;
- $\overline{\zeta}$: Configuration domain of a unit-rank region;
- ζ: Configuration domain of a T-SPWL region;
- Θ: Configuration domain of a polyhedral region;
- λ_A: Admissible unit-rank region (AUR);
- τ_A: Admissible T-SPWL region;
- $\overline{\zeta}_A$: Configuration domain of an AUR;
- ζ_A: Configuration domain of an admissible T-SPWL region or equilibrium region.

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