SKRIPSI

PERANCANGAN DAN PEMBUATAN SISTEM MONITORING PADA JALUR KERETA API DENGAN MENGGUNAKAN GELOMBANG ULTRASONIK DAN GELOMBANG RADIO BERBASIS MIKROKONTROLER AT89C51

Disusun Oleh :

ZIKI ZAULIA PANDUWINATA

01.17.032

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

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LEMBAR PERSETUJUAN

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN SISTEM MONITORING PADA JALUR KERETA API DENGAN MENGGUNAKAN GELOMBANG ULTRASONIK DAN GELOMBANG RADIO BERBASIS MIKROKONTROLER AT89C51

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Abstrak

Pada saat kereta api beroperasi, informasi mengenai letak/posisi kereta api sangatlah penting untuk diketahui bagi para petugas kereta api, agar para petugas dapat mengatur jalannya lalulintas kereta api. Teknologi penyampaian informasi posisi kereta api pada saat ini masih menggunakan pesawat telepon, sehingga masih banyak terjadi kesalahan (human error) dalam penyampaian informasi posisi kereta api. Salah satu akibat dari kesalahan dalam memberikan informasi posisi kereta api adalah dapat menimbulkan terjadinya kecelakaan.

Dengan disusun dan dirancangnya alat ini diharapkan dapat membantu dan memudahkan para petugas untuk mengetahui letak/posisi kereta api pada saat kereta api beroperasi hanya dengan melihat tampilan LED indicator posisi kereta api dan LCD. Pada perancangan alat ini menggunakan media komunikasi gelombang ultrasonic dan gelombang radio sebagai media penghantar informasi posisi kereta api. Dengan didirikan beberapa transceiver di setiap stasiun KA maupun disepanjang jalur kereta api dengan skala jarak tertentu dan dengan mengunakan data DTMF untuk membedakan menara transceiver sebagai pemosisi kereta api, maka sistem monitoring posisi kereta api yang berbasis mikrokontroler AT89C51 dapat beroperasi.

Kata Kunci : sistim monitoring posisi kereta api, gelombang ultrasonic, gelombang radio, DTMF, mikrokontroler AT89C51

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DAFTAR ISI

DAFTAR GAMBAR

DAFTAR TABEL

DAFTAR GRAFIK

INSTITUT TEKNOLOGI NASIONAL MALANG

BAB I

PENDAHULUAN

1.1. Latar Belakang

Dalam kehidupan sehari-hari kereta api merupakan salah satu transportasi darat yang sering digunakan, karena transportasi ini lebih ekonomis dibandingkan dengan transportasi darat yang lain. Dalam penggunaan alat transportasi kereta api saat ini banyak sekali terjadi kesalahan-kesalahan dalam menginformasikan letak/posisi kereta api pada saat kereta api sedang melaju.

Seiring dengan perkembangan ilmu pengetahuan dan teknologi, mulai dikembangkan alat bantu yang dapat menginformasikan posisi dan letak alat transportasi maupun benda seperti *SONAR*, *RADAR*, dan *GPS*. Sedangkan pada unit kereta api pada saat ini kita menggunakan media komunikasi pesawat telepon untuk menginformasikan posisi atau letak dari kereta api tersebut. Karena kurang tepatnya informasi yang kita berikan banyak sekali terjadi kesalahan-kesalahan dalam memberikan informasi posisi kereta api sehingga menimbulkan terjadinya kecelakaan.

Di sini akan dicoba memperkenalkan sebuah sistem monitoring yang digunakan pada alat transportasi darat salah satunya yaitu kereta api, dimana sistem ini dapat membantu kita untuk mengetahui posisi kereta api sehingga dapat mengurangi terjadinya kesalahan dalam memberikan informasi posisi pada kereta api.

1.2. Perumusan Masalah

Berdasarkan latar belakang, maka untuk perumusan masalahnya adalah bagaimana merancang suatu alat yang dapat mengetahui letak atau posisi kereta api yang sedang melaju dengan menggunakan sistem komunikasi gelombang ultrasonik dan gelombang radio.

Oleh karena itu dalam perumusan masalah skripsi ini diberi judul :

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1.3. Tujuan Pembahasan

Tujuan dari penyusunan skripsi ini adalah untuk merancang sistem monitoring kereta api yang dapat mengetahui letak atau posisi dari kereta api berdasarkan perbedaan sinyal *DTMF* yang dihasilkan pada menara yang ditempatkan di sepanjang jalur kereta api dengan media penghantar melalui udara (Gelombang Ultrasonic dan Gelombang Radio) yang berbasiskan Mikrokontoler AT89C51.

1.4. Batasan Masalah

Dalam menyusun skripsi ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya :

1. Alat ini bekerja pada jalur Low Frekuensi untuk transduser ultrasonik dan Very High Frekuensi untuk modul *wireless microphone* .

2. Jalur dan penempatan menara tidak berdasarkan pada jarak yang sesungguhnya.
3. Tidak membahas gangguan frekuensi yang disebabkan dari luar.
4. Tidak membahas daya dan jarak jangkau pancaran.
5. Tidak membahas kecepatan sistem transmisi.
6. Tidak membahas catu daya dan final amplifier.
7. Tidak membahas masalah antena dan saluran transmisi.
8. Hanya membahas masalah perancangan perangkat kerasnya.

1.5. Metodologi Penelitian

Metodologi yang digunakan dalam penulisan skripsi ini adalah sebagai berikut :

1. Studi *literature* tentang cara kerja *transmitter/receiver* gelombang *ultrasonic*, DTMF, gelombang radio dan mikrokontroler AT89C51 yang meliputi pengumpulan dan analisa data.
2 Perancangan dan Pembuatan Alat meliputi :
   - Sistem *transmitter* dan *receiver* dari gelombang *ultrasoni*c.
   - Rangkaian Pengkondisi Sinyal, DTMF *Encoder* dan *Decoder*
   - Pemrograman Mikrokontroler AT89C51.
3. Pengujian alat yang meliputi :
   a. Sinyal yang dihasilkan *transmitter/receiver* (baik gelombang *ultrasonic* maupun gelombang radio).
   b. Rangkaian Pengkondisi Sinyal , DTMF *Encoder* dan *Decoder.*

c. Mikrokontroler AT89C51.

d. Sistem monitoring posisi kereta api yang ditampilkan pada LED *display* dan LCD.

1.6. Sistematika Penulisan

Sistematika dari penulisan Skripsi ini adalah sebagai berikut :

- **Bab I** merupakan Pendahuluan yang berisi latar belakang, perumusan masalah, tujuan, batasan masalah, metodologi penelitian serta sistematika penulisan.
- **Bab II** membahas tentang Teori Penunjang yang membahas tentang teori dasar transduser ultrasonik, DTMF, gelombang radio dan mikrokontroler AT89C51.
- **Bab III** membahas tentang Perancangan dan Pembuatan Alat yang meliputi: Osilator gelombang ultrasonik pada *transmitter* transduser ultrasonik dan filter pada *receiver* transduser ultrasonik, Rangkaian Pengkondisi Sinyal, DTMF, pemrograman mikrokontroler AT89C51 dan penjelasan tentang cara kerja dari sistem monitoring pada LED *display.*
- **Bab IV** membahas tentang Pengujian Alat yang mencakup tentang pembahasan yang akan menampilkan hasil pengamatan dan analisa dari hasil pengujian. Dan menguji sejauh mana alat tersebut berfungsi.
- **Bab V** merupakan bagian Penutup yang meliputi kesimpulan dan saran.

Daftar Pustaka

Lampiran

BAB II

TEORI PENUNJANG

2.1. Pendahuluan

Dalam bab ini akan dibahas mengenai teori penunjang dari perencanaan dan pembuatan alat. Teori penunjang ini akan membahas tentang komponen dan peralatan pendukung dari alat yang akan kita buat, hal tersebut guna memudahkan dalam memahami cara kerja rangkaian maupun dasar-dasar perencanaan hingga terciptanya alat ini.

Bagian pokok dalam teori penunjang ini akan membahas secara garis besar tentang transduser ultrasonik, DTMF, gelombang radio dan mikrokontoler AT89C51. Untuk lebih jelasnya akan dijelaskan di bawah ini.

2.2. Gelombang Ultrasonik

Gelombang Ultrasonik adalah salah satu bagian dari gelombang suara/akustik yang mempunyai daerah frekuensi di atas batas kemampuan pendengaran manusia yaitu di atas 20 KHz [1]. Gelombang ultrasonik sering digunakan pada bidang maritim dengan istilah SONAR *(sound navigation and ranging)* dimana fungsi dari SONAR adalah sebagai komunikasi antar kapal, pendeteksi atau untuk mengetahui posisi benda dalam air seperti ranjau dan kapal selam. SONAR juga berfungsi sebagai pengukur jarak suatu benda maupun kedalaman lautan berdasarkan waktu antara pancaran dengan pantulan gelombang

[1] http://en.wikipedia.org/wiki/Ultrasound

yang diterima *(echo)*. Jarak yang dapat dipancarkan dalam air dengan gelombang ultrasonik adalah antara 1 sampai dengan kurang lebih 10 Km. Sedangkan pada media udara SONAR hanya digunakan untuk jarak yang pendek.[2]

Nama	Frekwensi
Infrasonik	Dibawah 20Hz
Audibel	20 – 20.000 Hz
Ultrasonik	Diatas 20.000Hz

Tabel 2 -1. Kategori Suara Menurut Frekwensi.[3]

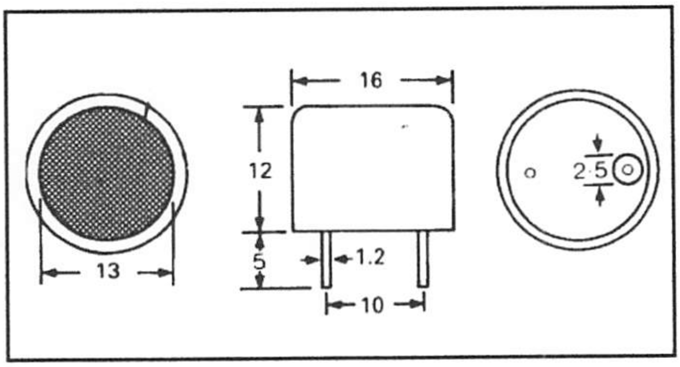
2.2.1. Tranducer Ultrasonik

Tranduser adalah suatu alat yang dapat merubah energi dari suatu energi kebentuk energi yang lain. Sedangkan Tranduser ultrasonik adalah suatu alat yang dapat merubah energi elektrik menjadi energi akustik (gelombang ultrasonik).[4]

Tranduser yang digunakan dalam peencanaan ini adalah jenis tranducer *Piezzoelektrik* yang dapat merubah energi elektrik menjadi suara, dimana dalam perancangan ini berfungsi sebagai pemancar dan penerima gelombang ultrasonik yang bekerja pada frekuensi 40 KHz. Tujuan dari penggunaan transduser ultrasonik ini selain dalam teknologi saat ini gelombang ultrasonik digunakan dalam SONAR sebagai pendeteksi atau posisi suatu benda. Sedangkan pada perencanaan ini pemakaian ultrasonik adalah untuk mengetahui kereta api pada

[2] http://en.wikipedia.org/wiki/Sonar
[3] http://en.wikipedia.org/wiki/Ultrasound
[4] http://en.wikipedia.org/wiki/Transducer

saat melintas *(transmitter dan receiver transducer ultrasonic)*, selain itu juga untuk menghindari terjadinya gangguan frekuensi pada saat pengiriman dan penerimaan sinyal.



Gambar 2-1. *Transducer Ultrasonic.*[5]

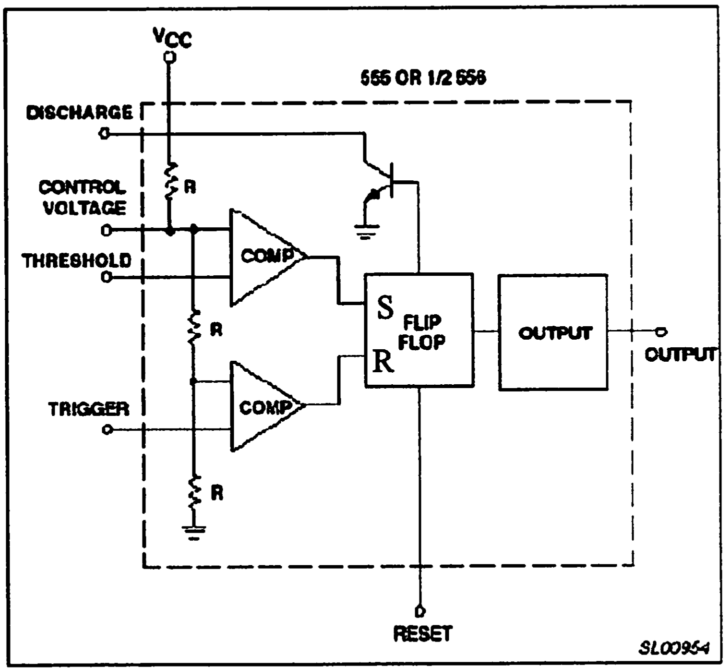
2.2.2. Transmitter Transducer Ultrasonik

Transmitter Transducer Ultrasonik adalah suatu alat yang dapat mengirimkan energi elektrik melalui medium udara dengan transducer ultrasonik. Untuk membangkitkan getaran elektrik pada transmitter maka diperlukan suatu komponen elektronik yang dapat membangkitkan frekuensi sebesar 40 KHz.

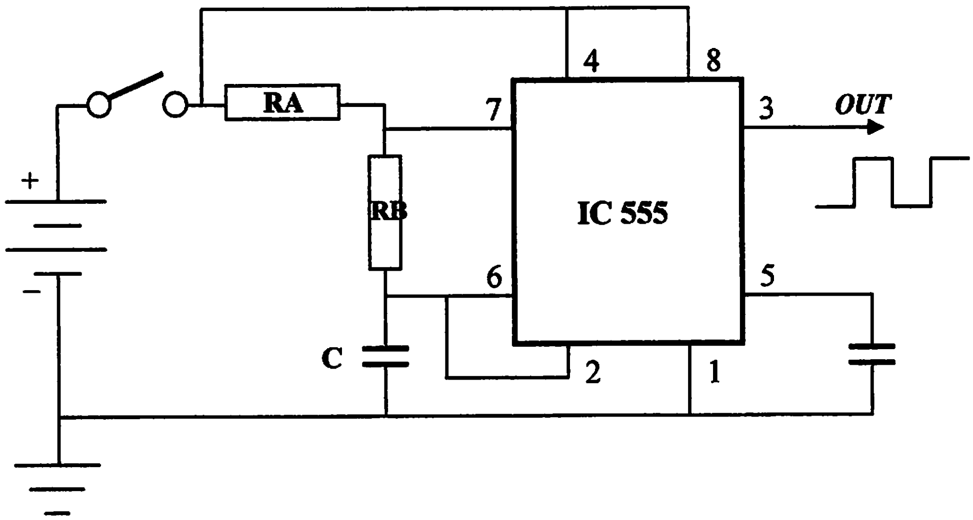
Pada transmitter transducer ultrasonik komponen elektronik yang digunakan adalah IC 555 sebagai pembangkit gelombang ultrasonic. IC 555 bekerja dengan mode astabil multivibrator, hal tersebut dikarenakan pada mode astabil multivibrator IC 555 akan membangkitkan pulsa/gelombang kotak (osilator *relaksasi*) secara berulang.

[5] Data Sheet Ultrasonic Transducers

Untuk bentuk blok diagram IC 555 dan rangkaian skematik IC 555 yang bekerja pada mode astabil multivibrator dapat kita lihat pada gambar di bawah ini :



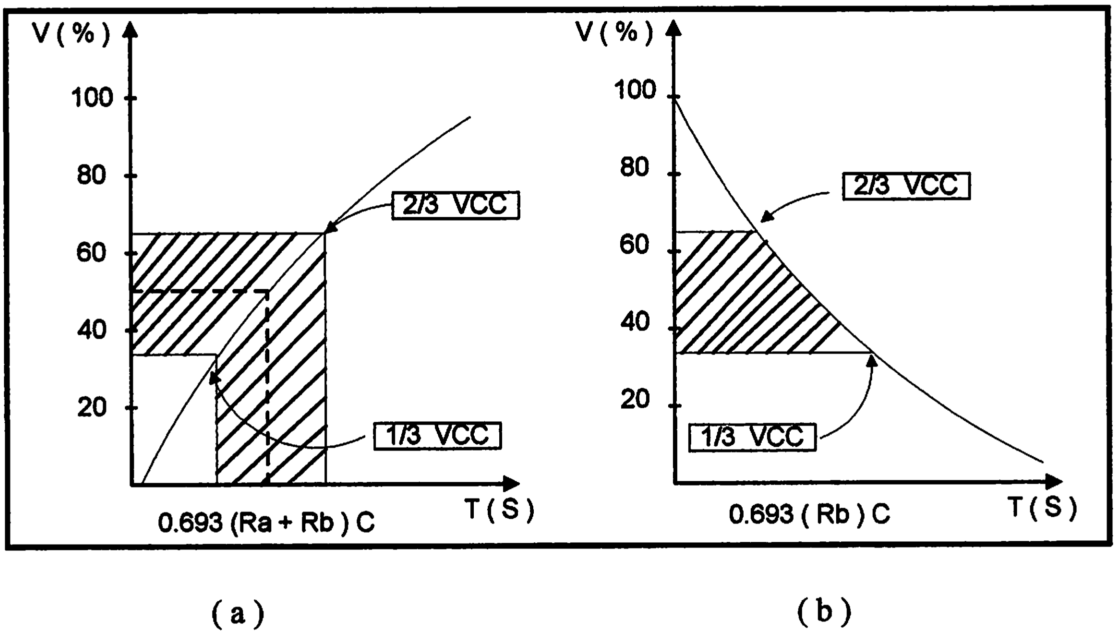
Gambar 2-2. Diagram Blok IC 555.[6]



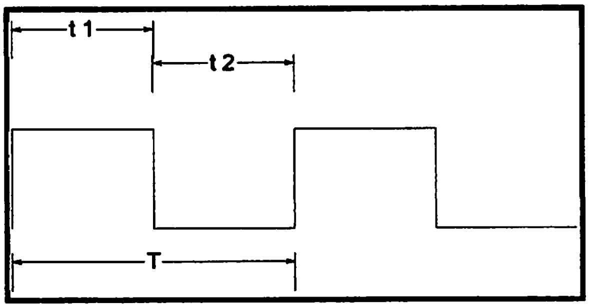
Gambar 2-3. *Oscillator Astabil Multivibrator*

[6] Philip Semiconductor NE 555 And 556 Application Note, page 2

Rangkaian astabil multivibrator bekerja pada saat terjadi proses pengisian dan pengosongan pada komponen luar. Pada saat pengisian nilai tegangan pada pin 6 (enam) *(threshold)* dan pin 2 (dua) (trigger) akan lebih besar dari 2/3 VCC selama 0.693 (Ra + Rb) C, dan setelah 0.693 (Ra + Rb) C rangkaian IC akan menset flip flop RS dan keluaran flipflop RS akan menjadi 1 (Q=1). Pada saat Q=1 rangkain dalam IC akan mengaktifkan transistor sehingga arus yang melintas pada pin 7 *(discharge)* akan langsung ditanahkan, dalam keadaan ini rangkaian akan terjadi pengosongan dengan waktu sebesar 0.693 (Rb) C. Nilai tegangan akan terus turun sampai lebih kecil dari 1/3VCC, dan membuat keadaan pada *output trigger* menjadi 1 (R=1) sehingga membuat Q=0, dan membuat transistor menjadi jenuh, dan proses pengisian akan terjadi lagi dan terus berulang selama rangkaian dalam keadaan aktif.



Grafik 2-1. (a) Waktu Pengisian Kapasitor, (b) Waktu Pengosongan Kapasitor



Gambar 2-4. Bentuk Gelombang Keluaran Pewaktu 555

Untuk perumusan astabil multivibrator adalah sebagai berikut :

- Pada waktu pengisian :

  t1 = 0,693 (Ra + Rb) C.[7]

- Pada waktu pengosongan

  t2 = 0,693 (Rb) C.[8]

- Sehingga untuk waktu keseluruhan adalah :

  T = t1 + t2 = 0,693 (Ra + 2Rb) C.[9]

- Untuk persamaan umum dari frekuensi adalah :

$$f = \frac{1}{T} = \frac{1}{0,693(Ra + 2Rb)C} = \frac{1,44}{(Ra + 2Rb)C}$$ [10]

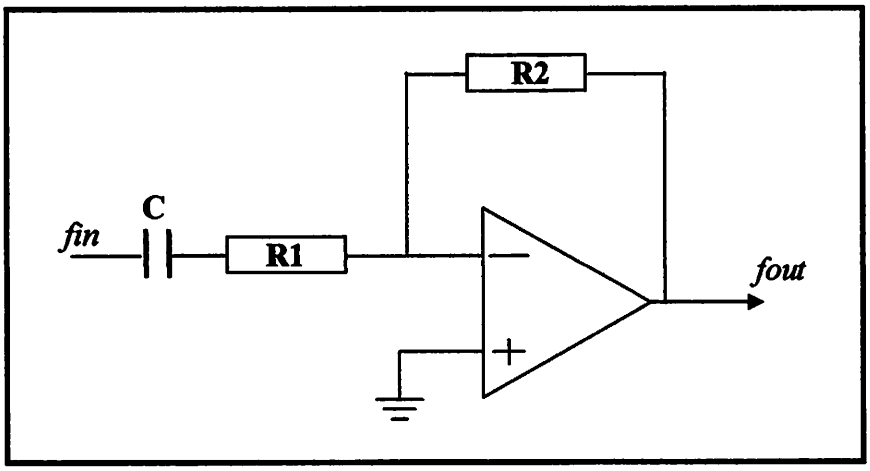
2.2.3. Receiver Transducer Ultrasonik

Untuk menghasilkan kembali frekuensi yang dihantarkan melalui media udara maka diperlukan suatu alat penerima yang mempunyai frekuensi kerja yang

[7] Natioanal Semiconductor LM555 Data Sheet, 2000, Page 8
[8] Ibid. Page 8
[9] Ibid. Page 8
[10] Ibid. Page 8

sama yaitu sebesar 40 Khz. Agar pada penerimaan gelombang ultrasonic dapat bekerja pada frekuensi 40 KHz, maka diperlukan sebuah filter yang berfungsi untuk meluluskan frekuensi kerja dari alat. Dalam hal ini filter yang digunakan adalah jenis High Pass Filter dimana prinsip kerja dari High Pass Filter adalah untuk meloloskan frekuensi yang kita tentukan. Untuk membentuk High Pass Filter digunakan rangkaian Op-Amp sehingga selain sebagai HPF OP-Amp juga sebagai penguat dari gelombang yang dihasilkan.

Untuk bagian skematik dari High Pass Filter dapat dilihat pada gambar di bawah ini beserta perumusannya :



Gambar 2-5. High Pass Filter.[11]

Dari rangkaian di atas untuk perumusannya adalah sebagai berikut :

$A = -\frac{R2}{R1} atau = -\frac{V_o}{Vi}$ dimana C akan terhubung singkat pada frekuensi sebesar :

[11] Wasito S, VADEMEKUM ELEKTRONIKA EDISI KEDUA, PT Gramedia. Jakarta, 1995, hal 362

$fc = \frac{1}{2.\pi.R1.C}$, sehingga penguatan akan terjadi pada saat harga f_c terpenuhi.

Dan apabila nilai frekuensi masuk lebih kecil dari harga f_c maka A = 0.[12]

2.3. DTMF

DTMF (*Dual Tone Multi Frequency*) merupakan frekuensi isyarat yang biasa digunakan dalam pesawat telekomunikasi yang berfungsi untuk membentuk nada yang mengisyaratkan nomor pada tombol pesawat telepon di dalam jaringan telekomunikasi.

Dalam perancangan ini DTMF difungsikan sebagai isyarat untuk membedakan menara yang satu dengan yang lain sesuai dengan nomor dan nada pembentuk pada DTMF tersebut. Setiap isyarat angka/nomor DTMF pada pesawat telepon terbentuk dari dua frekuensi audio yang berbeda, untuk lebih jelasnya akan dijelaskan pada gambar dan sub bab di bawah ini :

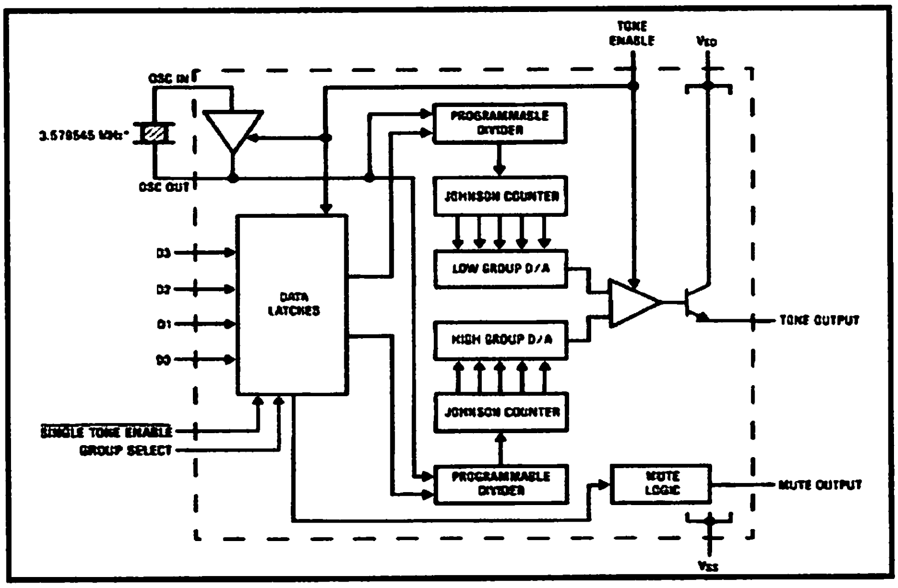
	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

Tabel 2-2. Frekuensi DTMF Pada Keypad.[13]

[12] Ibid. Hal. 362
[13] http://en.wikipedia.org/wiki/Dual-tone_multi-frequency

2.3.1 DTMF Generator

Dalam rangkaian terintegrasi (*Integrated Circuit*) generator *tone* banyak didapatkan di pasaran. Salah satunya adalah IC TP5088. DTMF Generator TP5088 merupakan jenis IC CMOS yang dapat menghasilkan *tone-dialling* yang dalam aplikasinya biasa digunakan pada hubungan telepon. IC ini dapat dikontrol oleh mikrokontroller atau secara manual kontrol/*switch*. Data *input* yang berupa 4 (empat) data biner akan diuraikan secara langsung sehingga membentuk 2 (dua) bagian yaitu FL dan FH untuk mensimulasikan *input switch* yang dibutuhkan oleh pembangkit DTMF



Gambar 2-6. Diagram Blok DTMF Generator.[14]

IC TP5088 ini merupakan DTMF *generator* yang menghasilkan *tone dialing*. Di mana *Input* dari TP5088 ini berupa 4 (empat) data *biner* (D0 sampai

[14] National Semiconductor IC TP5088 Data Sheet, October 1991, Page 1

dengan D3) yang selanjutnya akan diuraikan menjadi sinyal DTMF tergantung kepada kode sinyal yang dimasukkan. IC ini akan bekerja apabila *Tone Enable* berlogika tinggi sehingga *clock* yang berasal dari *oscillator crystal* 3.579545 MHz akan aktif. 4 (empat) data biner ini (D0-D3) masuk dan diterima oleh *Data Latches* untuk menjaga inputan data biner ini tetap, sampai ada inputan data baru yang masuk. Selanjutnya data dibagi dan dipecah melalui *programmable divider*, masuk ke dalam *Johnson Counter* yang akan mengurut data ke dalam dua buah kelompok *Digital to Analog Converter* sehingga terbentuk kelompok sinyal frekuensi tinggi dan rendah melalui *High Group D/A* dan *Low Group D/A*. Kedua nada (*tone*) frekuensi tinggi dan rendah kemudian dicampur menggunakan *mixer amplifier*, lalu *Tone Out* keluar melalui kaki emitor sebuah transistor NPN dengan kaki kolektor dihubungkan V_{DD}. IC TP5088 ini akan menghasilkan *tone* sampai *tone enable low* kembali. Jadi pembacaan terhadap *input* akan dimulai pada saat transisi *tone enable* dari *low* ke *high*.

Keyboard Equivalent	Data Inputs				TONE ENABLE	TONES OUT		MUTE
	D3	D2	D1	D0		f_L (Hz)	f_H(Hz)	
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	_/‾	697	1209	O/C
2	0	0	1	0	_/‾	697	1336	O/C
3	0	0	1	1	_/‾	697	1477	O/C
4	0	1	0	0	_/‾	770	1209	O/C
5	0	1	0	1	_/‾	770	1336	O/C
6	0	1	1	0	_/‾	770	1477	O/C
7	0	1	1	1	_/‾	852	1209	O/C
8	1	0	0	0	_/‾	852	1336	O/C
9	1	0	0	1	_/‾	852	1477	O/C
0	1	0	1	0	_/‾	941	1336	O/C
*	1	0	1	1	_/‾	941	1209	O/C
#	1	1	0	0	_/‾	941	1477	O/C
A	1	1	0	1	_/‾	697	1633	O/C
B	1	1	1	0	_/‾	770	1633	O/C
C	1	1	1	1	_/‾	852	1633	O/C
D	0	0	0	0	_/‾	941	1633	O/C

Tabel 2-3. Tabel Kebenaran DTMF TP5088.[15]

[15] Ibid. Page 4

Secara keseluruhan fungsi dari masing-masing pin TP5088 adalah :

a) Vdd dan Vss. Merupakan pin catu daya, V_{dd} dihubungkan dengan catu daya positif (+) dan Vss dihubungkan dengan catu daya negatif (-).

b) Osc *In* dan Osc *Out.* Pin ini dihubungkan dengan kristal atau *oscillator* dari luar.

c) *Tone Enable Input. Input* ini mempunyai sebuah resistor *pull-up internal.* Ketika *Tone enable* dalam kondisi *low, oscillator* akan diberhentikan sehingga *tone generator* dan *output* lain akan mati. Perubahan logika "0" ke logika "1" akan menahan data dari D0-D3 dan *oscillator* akan mulai bekerja dan tone generator kontinyu sampai *tone enable* kembali ke keadaan *low.*

d) *Mute. Output* ini berfungsi untuk mengalirkan arus ke Vss pada saat *tone enable low* dan tidak ada *tone* yang dibangkitkan dan rangkaian ini dimatikan saat *tone enable high.*

e) D0-D3. Pin untuk *input* data biner yang dikodekan, yang ditahan pada sisi naik *tone enable.*

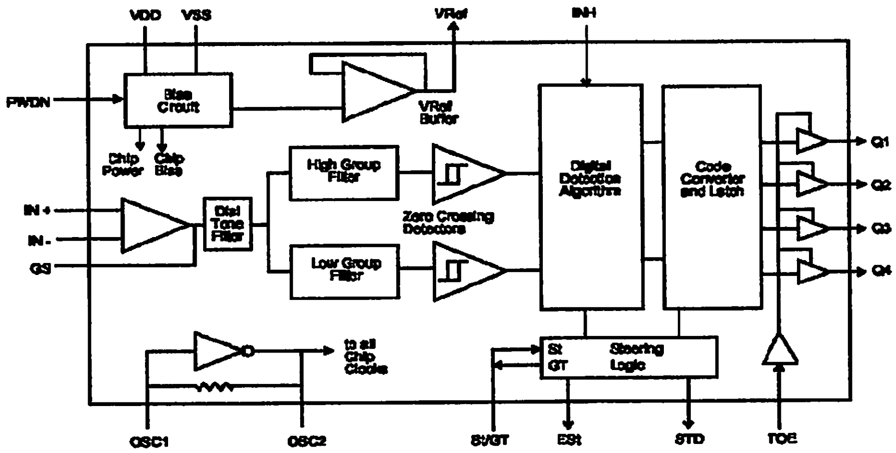
f) *Tone Out. Output* ini merupakan *open* emitor dari transistor NPN, kolektor secara *internal* dihubungkan ke V_{dd}. Ketika beban resistor *eksternal* dihubungkan *Tone out* ke Vss, maka tegangan pada kaki ini merupakan penjumlahan dari *group tone low* dan *high.* Pada saat tidak membangkitkan *tone output*, transistor ini mati.

g) *Single Tone Enable.* Pada keadaan normal kaki ini- dihubungkan ke Vdd.

h) *Group Select.* Kaki ini digunakan untuk menyeleksi *group* frekuensi atas atau bawah. Ketika perangkat ini dalam mode tunggal.

2.3.2. DTMF Receiver.

IC MT8870 adalah IC terpadu penerima/ pengkonversi DTMF yang merupakan salah satu IC produksi *Mitel, Inc.* Fungsi dari DTMF ini adalah untuk menterjemahkan masukkan berupa sinyal frekuensi menjadi data biner. IC MT8870 ditunjukkan pada gambar 4 rangkaian terintegrasi yang di dalamnya dilengkapi dengan filter digunakan frekuensi tinggi dan rendah serta sebuah decoder *digital.* Pada bagian *filter* digunakan teknik *switch* kapasitor untuk membedakan pasangan frekuensi yang masuk. Sedang untuk dekoder digunakan teknik pencacahan *digital* untuk mendeteksi dan mengkode 16 buah pasangan frekuensi DTMF menjadi kode 4 bit. MT8870 juga dilengkapi dengan rangkaian-rangkaian *internal* penguat *differendsial, clock oscillator* dan sebuah rangkaian *latch* 3-*state* pada bagian *output.*



Gambar 2-7. Diagram Blok DTMF *Receiver.*[16]

[16] Zarlink Semiconductor IC MT8870D/MT8870D-1 Data Sheet, march 1997, Page 1

Secara keseluruhan, fungsi masing-masing pin MT8870 adalah :

a) IN+ dan IN-. Merupakan pin *input*, IN+ merupakan *non inverting input op-amp* dan IN- merupakan *inverting input op-amp.*

b) GS (*gain select*). Pemilihan besarnya *gain* (penguatan) untuk sinyal dari luar.

c) Vref. *Voltage* referensi, biasanya besarnya $V_{DD}/2$ (output).

d) INH. Berfungsi untuk mengeluarkan data DTMF A,B,C,D.

e) PWDN. *Power down* (input), aktif tinggi.

f) OSC1 dan OSC2. Pin ini dihubungkan dengan kristal sebesar 3,579545 MHz. OSC1 merupakan *Clock input* dan OSC2 merupakan *Clock output.*

g) Vss dan Vdd. Merupakan pin catu daya. Vss dihubungkan dengan *ground.* Sedangkan Vdd dihubungkan dengan catu daya *positif.*

h) St/GT. *Steering/Guard Time*, menentukan kecepatan nada yang dapat diterjemahkan.

i) Est. Saat nilai *input* benar maka akan mengeluarkan logika tinggi.

j) StD. Jika logika tinggi pada pin ini maka data yang akan dikeluarkan adalah *valid.*

k) Q1-Q4. *Output* data yang akan dikeluarkan

l) TOE. *Tristate output enable*, untuk mengaktifkan tidak ada keluaran data.

2.4. Gelombang Radio

Gelombang Radio adalah gelombang elekromagnetik yang dihasilkan oleh suatu rangkain/komponen elektronika dimana media penghantar yang biasa digunakan adalah udara [17]. Salah satu pengembangan dari gelombang radio untuk menentukan letak atau lokasi suatu daerah adalah dengan adanya RADAR (*Radio Detection and Ranging*) dan GPS (*Global Positioning System*)

Karena pada perencanaan untuk membentuk gelombang radio menggunakan suatu modul, maka untuk gelombang radio hanya akan dijelaskan secara garis besar mengenai system dasar dari system komunikasi frekuensi radio. Dalam perencanaan ini modul gelombang radio menggunakan sistem komunikasi frekuensi radio analog yaitu dengan menggunakan modul wireless microphone yang bekerja pada jalur *Very High Frequency (VHF)* yaitu sebesar 100 MHz – 120 MHz. Sedangkan untuk pembagian jalur gelombang radio dapat dilihat pada table di bawah ini.

Band name	Abbr	ITU band	Frequency and Wavelength in air	Example uses
			< 3 Hz > 100,000 km	
Extremely low frequency	ELF	1	3–30 Hz 100,000 km – 10,000 km	Communication with submarines
Super low frequency	SLF	2	30–300 Hz 10,000 km – 1000 km	Communication with submarines
Ultra low frequency	ULF	3	300–3000 Hz 1000 km – 100 km	Communication within mines
Very low frequency	VLF	4	3–30 kHz 100 km – 10 km	Submarine communication, avalanche beacons, wireless heart rate monitors, geophysics
Low frequency	LF	5	30–300 kHz 10 km – 1 km	Navigation, time signals, AM longwave broadcasting
Medium frequency	MF	6	300–3000 kHz 1 km – 100 m	AM (Medium-wave) broadcasts

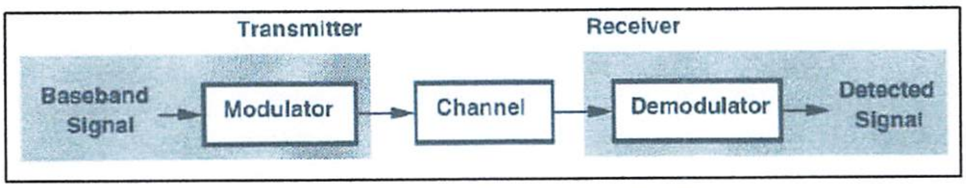
[17] http://en.wikipedia.org/wiki/Radio_wave

High frequency	HF	7	3–30 MHz 100 m – 10 m	Shortwave broadcasts, amateur radio and over-the-horizon aviation communications
Very high frequency	VHF	8	30–300 MHz 10 m – 1 m	FM, television broadcasts and line-of-sight ground-to-aircraft and aircraft-to-aircraft communications
Ultra high frequency	UHF	9	300–3000 MHz 1 m – 100 mm	television broadcasts, microwave ovens, mobile phones, wireless LAN, Bluetooth, GPS and Two-Way Radios such as FRS and GMRS Radios
Super high frequency	SHF	10	3–30 GHz 100 mm – 10 mm	microwave devices, wireless LAN, most modern Radars
Extremely high frequency	EHF	11	30–300 GHz 10 mm – 1 mm	Radio astronomy, high-speed microwave radio relay
			Above 300 GHz < 1 mm	

Tabel 2-4. Tabel Klasifikasi Frekuensi Radio.[18]

2.4.1. Sistem Dasar Perencanaan dan Perancangan Frekuensi Radio

Dasar dari system komunikasi frekuensi radio terbagi menjadi dua system yaitu system komunikasi radio analog dan digital, berikut bentuk dari masing – masing system komunikasi radio :



Gambar 2-8. Blok Sistem Komunikasi Sederhana.[19]

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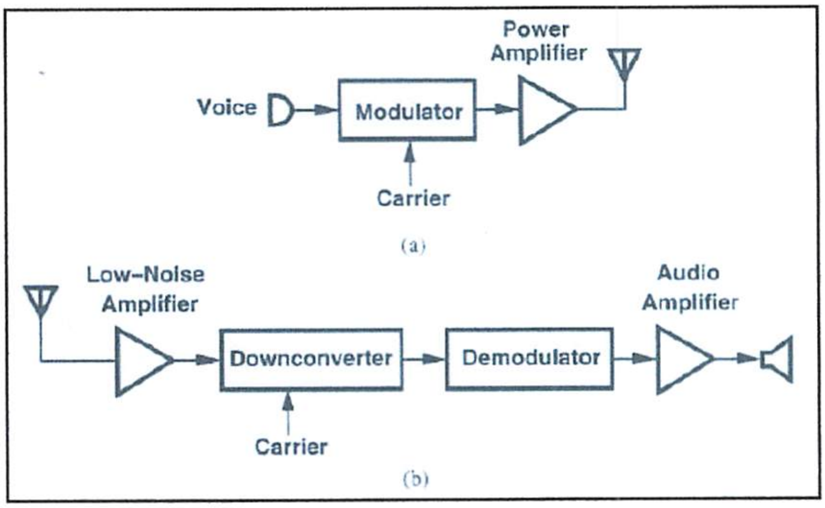
[18] Ibid

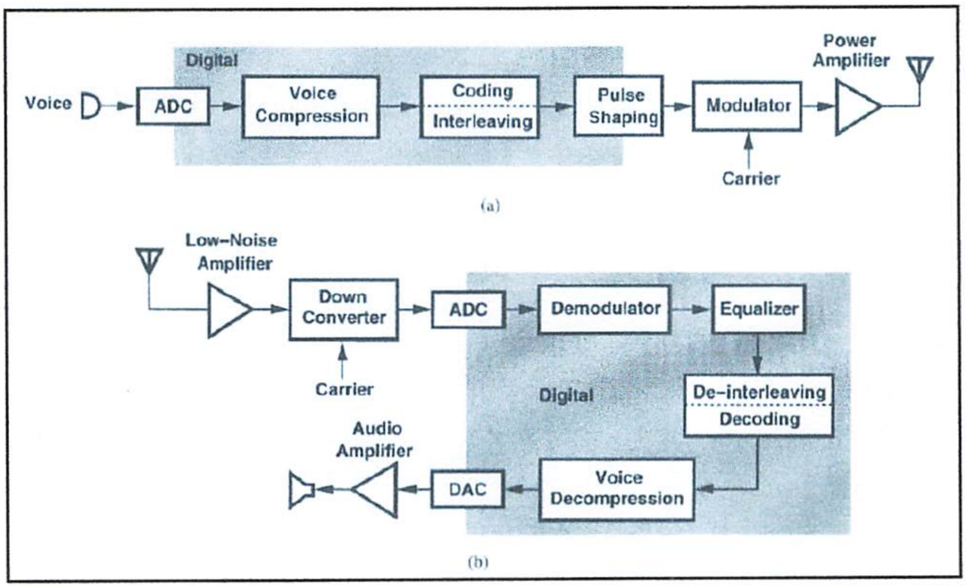
[19] BEHZAD RAZAVI. RF MICROELECTRONICS, PRENTICE HALL PTR, University Off California, Los Angeles, 1998, Page 55

a. Komunikasi Frekuensi Radio Analog



Gambar 2-9. Sistem Komunikasi Fekuensi Radio Analog.[20]

b. Komunikasi Frekuensi Radio Digital



Gambar 2-10. Sistem Komunikasi Fekuensi Radio Digital.[21]

[20] Ibid, page 7
[21] Ibid, Page 8

Yang menyamakan dari system komunikasi analog dan digital adalah data/informasi yang dikirim dan yang diterima tidak berubah. Seperti yang terlihat pada gambar 2-9 sistem komunikasi radio terdiri dari 3 (tiga) bagian terpenting yaitu transmitter, receiver dan media penghantar, Sedangkan untuk masing-masing bagian terdiri dari beberapa rangkaian, diantaranya yaitu :

1. **Osilator**

   Osilator berfungsi sebagai pembangkit gelombang yang digunakan untuk membentuk frekuensi isyarat maupun frekuensi pembawa.

2. **Modulator**

   Modulator adalah suatu rangkaian yang berfungsi untuk menggabungkan antara frekuensi isyarat/informasi dengan frekuensi pembawa (*Carrier*) sebelum ditransmisikan atau dikirim melalui gelombang radio (udara).

3. **Demodulator**

   Demodulator adalah suatu rangkaian yang berfungsi untuk memisahkan antara frekuensi isyarat dengan frekuensi pembawa sehingga hanya frekuensi isyarat/informasi yang diambil.

4. **Transmitter**

   Transimiter adalah suatu perangkat elektronik yang pada umumnya berupa antena dalam komunikasi udara dan berupa kabel dimana keduannya berfungsi sebagai penghantar media komunikasi atau sebagai pengirim sinyal.

5. **Receiver**

Receiver adalah suatu rangkaian elektronik yang berfungsi menerima sinyal atau gelombang yang dipancarkan dari pemancar radio.

2.4.2. Modulasi dan Demodulasi

Seperti pada sub bab sebelumnya, untuk system modulasi dan demodulasi pada suatu system komunikasi juga terbagi menjadi 2 (dua) yaitu Analog dan Digital. Berikut akan dijelaskan secara garis besar mengenai system komuniksai tersebut.

2.4.2.1 Modulasi

Modulasi adalah proses pencampuran 2 (dua) frekuensi yang berbeda yaitu antara frekuensi rendah sebagai informasi dan frekuensi tinggi sebagai frekuensi pembawa (carrier) menjadi 1 (satu) bentuk gelombang frekuensi radio.[22] Berikut penjelasannya :

a Modulasi Analog

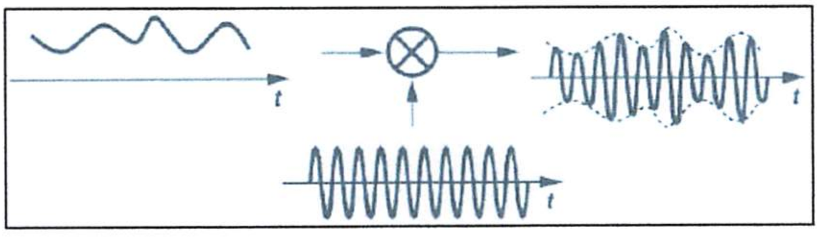
Modulasi Analog adalah salah satu teknik modulasi dimana sinyal informasinya berupa sinyal analog. Pada umunnya modulasi analog terbagi menjadi 3 (tiga) yaitu :

[22] http://en.wikipedia.org/wiki/Modulation

- AM (*Amplitudo Modulation*) adalah teknik modulasi analog berdasarkan besar kecilnya anplitudo pada frekuensi rendah mengendalikan amplitude frekuensi tinggi. Sedangkan phase dan fekuensinya tidak berubah.

  Penggolongan AM :

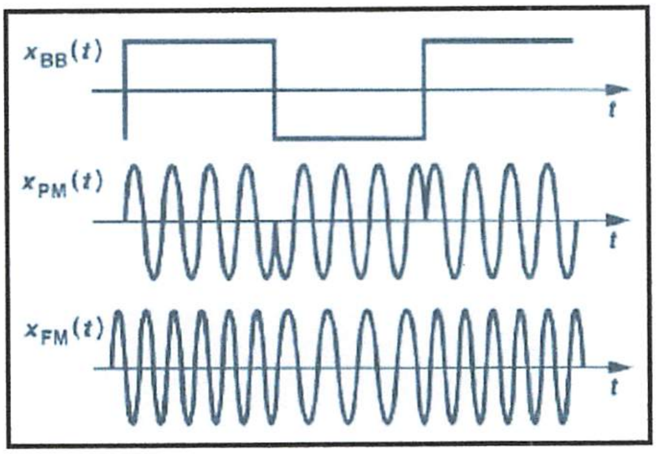
  - *Double-sideband modulation* (DSB).
    - *Double-sideband modulation with unsuppressed carrier* (DSB-WC) (*used on the AM radio broadcasting band*)
    - *Double-sideband suppressed-carrier transmission* (DSB-SC)
    - *Double-sideband reduced carrier transmi*ssion (DSB-RC)
  - *Single-sideband modulation* (SSB, or SSB-AM).
    - SSB with carrier (SSB-WC)
    - SSB suppressed carrier modulation (SSB-SC)
  - *Vestigial sideband modulation* (VSB, or VSB-AM)
  - *Quadrature amplitude modulation* (QAM)



Gambar 2-11. Amplitude Madulation Methode.[23]

[23] BEHZAD RAZAVI. RF MICROELECTRONICS, PRENTICE HALL PTR, University Off California, Los Angeles, 1998, Page 57

- PM (*Phase Modulation*) adalah teknik modulasi analog terjadi apabila fasa frekuensi rendah mengendalikan fasa frekuensi tinggi. Sedangkan amplitude dan fekuensinya tidak berubah.
- FM (*Frequency Modulation*) adalah modulasi frekuensi dimana frekuensi rendah mengendalikan frekuensi tinggi. Sedangkan amplitude dan fasanya tidak berubah.



Gambar 2-12. Phase Madulation and Frequency Modulation Methode.[24]

b. Modulasi Digital

Modulasi digital adalah salah satu teknik modulasi dimana sinyal informasinya berupa data digital (*bit*). Pada umumnya data/informasi digital dirubah ke dalam bentuk sinyal analog sebelum dimodulasikan dengan frekuensi pembawa (*carrier*). Untuk dasar modulasi digital dibedakan menjadi 3 yaitu:[25]

- ASK (*Amplitude Shift Keying*)
- PSK (*Phase Shift Keying*)

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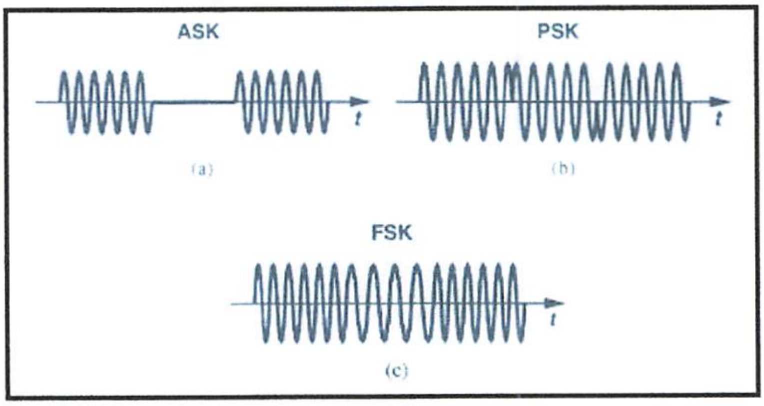
[24] Ibid, Page 59
[25] Ibid. Page 63

- FSK (*Frequency Shift Keying*)



Gambar 2-13. (a) Amplitude, (b) Phase, dan (c) Frequency Shift Keying.[26]

2.4.2.2. Demodulasi

Demodulasi adalah proses pemisahan antara frekuensi pembawa dengan frekuensi isyarat (data) sehingga hanya frekuensi informasi yang diambil/diloloskan. Sama halnya dengan modulasi, untuk penggolongan demodulasi pada umunya dibedakan menjadi 3 yaitu :[27]

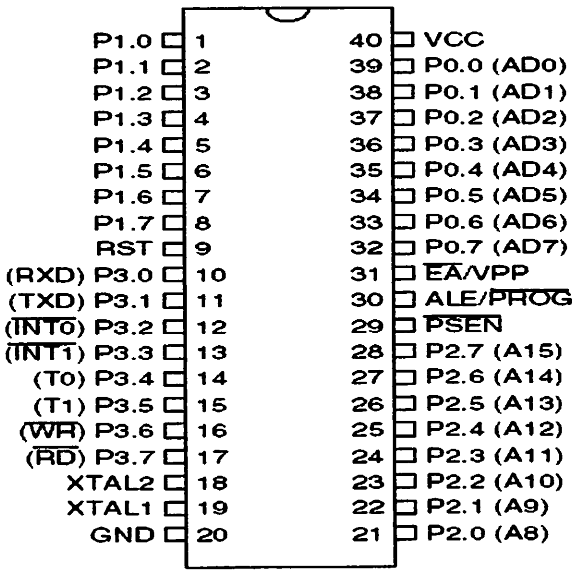
- AM Demodulasi
- FM Demodulasi
- PM Demodulasi

Salah satu bentuk proses modulasi dan demodulasi pada perencanaan ini adalah dengan digunakannya IC DTMF TP5088 sebagai pembentuk frekuensi informasi (data) dan MT8870 sebagai demodulator seperti yang sudah dijalaskan pada sub-bab sebelumnya..

[26] Ibid Page 64
[27] http://en.wikipedia.org/wiki/Demodulation

2.5. Mikrokontroler AT89C51

Mikrokontroller AT89C51 adalah Mikrokontroller ATMEL yang kompatibel penuh dengan Mikrokontroller keluarga MCS-51, yang membutuhkan daya yang rendah,memiliki performance yang tinggi, dan merupakan Mikrokomputer 8 bit yang dilengkapi 4 Kbyte EPROM (*Erasable and Programable Read Only*) dan 128 byte RAM internal. Program memory dapat di program ulang dalam sistem atau dengan *Nonvalately Memory Konvensional.* Adapun untuk Mikrokontroller AT89C51 (*produksi ATMEL*) dibandingkan dengan Mikrokontroller lainnya (*produksi INTEL*) perbedaannya terletak pada memory program yang digunakannya. Jika Mikrokontroller 8031 menggunakan memory luar, 8051 menggunakan ROM, 8751 menggunakan EPROM, maka Mikrokontroller AT89C51 menggunakan EEPROM (mengisi EPROM langsung tanpa dihapus terlebih dahulu).



Gambar 2-14. Konfigurasi Pin AT89C51.[28]

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[28] AT89C51 Data Sheet

Fungsi tiap – tiap pin adalah sebagai berikut :

1. GND (*ground*)

   Dihubungkan dengan ground rangkaian.

2. VCC (*power supply*)

   Dihubungkan dengan sumber tegangan.

3. Port 0 (P0.0 – P0.7)

   Port 0 merupakan port I/O 8 bit dua arah. Port ini digunakan sebagai multipleks bus alamat rendah (A0 –A7) dan data selama pengaksesan program memory dan data memory eksternal.

4. Port 1 (P1.0 –P1.7)

   Port 1 dapat berfungsi sebagai input atau oautput dan bekerja baik untuk operasi bit maupun *byte,* tergantung dari pengaturan *software.*

5. Port 2 (P2.0 – P2.7)

   Merupakan port input output dengan internal *pull-up.* Port 2 mengeluarkan high *order address byte* selama pengambilan *(fatch)* program memory eksternal dan selama pengaksesan data memory eksternal. Port 2 juga menerima *high order address bit* dan beberapa sinyal control selama pemrograman dan *verifikasi.*

6. Port 3 (P3.0 – P3.7)

   Port 3 selain mempunyai fungsi sebagai I/O juga mempunyai fungsi khusus sebagai berikut :

   ➢ RD (P3.7)

Strobe tulis data memori eksternal (sinyal pembacaan memory data luar).

- WR (P3.6)

  Sinyal penulisan memory luar data.

- T1 (P3.5)

  Masukan dari pewaktu / pencacah 1

- T0 (P3.4)

  Masukan dari pewaktu / pencacah 0

- *INT*1 (P3.3)

  Interupt 1 eksternal.

- *INT*0 (P3.2)

  Interupt 0 eksternal.

- *TXD* (P3.1) (port ouput serial)

  Keluaran pengiriman data untuk serial port (*asinkron*) atau sebagai keluaran clock (*sinkron*).

- RXD (P3.0) (port input serial)

  Masukan penerimaan data serial (*asinkron*) atau sebagai masukan / keluaran data (*sinkron*).

7. RST

   Merupakan pin input yang aktif tinggi, pin ini aktif tinggi selama dua siklus mesin ketika osilator bekerja akan me – reset peralatan.

8. ALE (*Address Latch Enable*)/ PROG

Pin ALE (*Address Latch Enable*) aktif tinggi mengeluarkan pulsa output untuk me – latch satu byte alamat rendah selama pengaksesan ke memory luar. ALE dapat mengendalikan 8 beban TTL. Pin ini juga merupakan input pulsa program yang aktif rendah selama pemrograman. Pada operasi normal, ALE dikeluarkan pada suatu kecepatan yang konstan, yaitu 1/6 dari frekuensi osilator, dan dapat digunakan untuk timing eksternal atau untuk tujuan pen-*clock*-an.

9. PSEN (*Program Strobe Enable*)

   Pin ini aktif rendah yang merupakan *Strobe* pembacaan ke program memory eksternal.

10. XTAL1 dan XTAL2

    Pin XTAL1 merupakan pin input ke penguat osilator pembalik dan pin XTAL2 merupakan pin output dari penguat osilator pembalik.

11. EA / Vpp (*External Acces / Programming Supply Voltage*).

    Pin EA harus di hold rendah secara eksternal atau dihubungkan ke ground agar Mikrokontroller AT89C51 dapat mengakses kode mesin dari program memory eksternal dengan lokasi 0000H sampai 0FFFH.

INSTITUT TEKNOLOGI NASIONAL

ITN

MALANG

BAB III

PERENCANAAN PERANCANGAN DAN PEMBUATAN ALAT

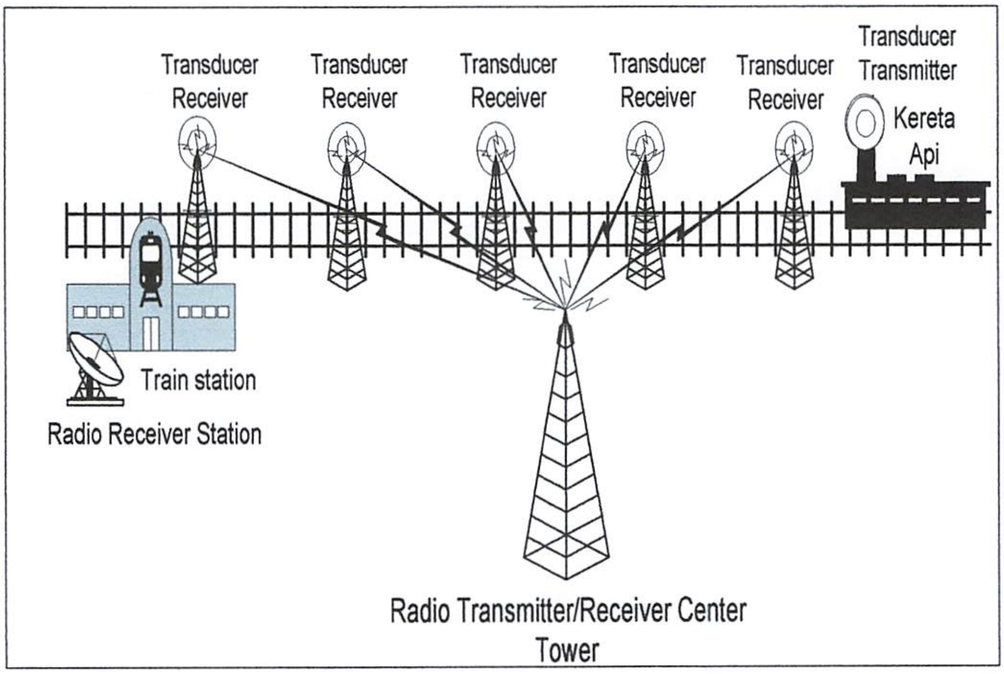
3.1. Gambaran Umum Alat

Adapun gambaran umum mengenai sistem monitoring ini adalah memanfaatkan sistem pemancar (transmitter) dan penerima (receiver) dimana sistem monitoring ini terdiri dari 5 bagian utama yaitu transmitter ultrasonic dan receiver ultrasonic sebagai pemicu sinyal, DTMF transmitter gelombang radio, DTMF receiver gelombang radio dan mikrokontroler AT89C51 yang digunakan sebagai pengolah data akhir dimana data yang diterima akan ditampilkan pada lampu indikator letak menara sebagai penentu posisi kereta api.

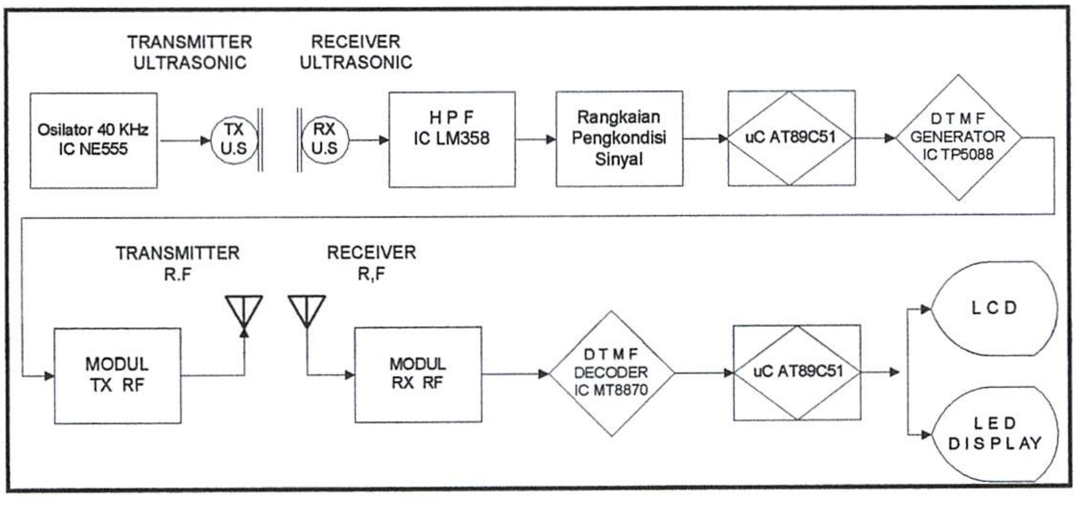
Pada perencanaan, perancangan dam pembuatan system monitoring ini digunakan transmitter ultrasonik (pada Kereta Api) dan receiver ultrasonik (pada Menara) yang bekerja pada frekuensi 40 KHz sebagai media penghantarnya sehingga jika transmitter transduser ultrasonic melintasi menara receiver ultrasonic kemudian diterima oleh receiver yang didirikan di samping rel kereta api atau di sepanjang rel kereta api dengan skala jarak tertentu kita dapat mengetahui bahwa kereta api tersebut telah melintasi atau sedang berada di posisi tempat kita mendirikan receiver. Sinyal yang diterima pada receiver ultrasonic tersebut akan memicu sinyal DTMF dimana pada perancangan ini data DTMF yang dihasilkan digunakan untuk membedakan menara yang satu dengan yang lain.sehingga jika pada setiap stasiun atau sepanjang rel kereta api dengan skala jarak tertentu kita dirikan menara, maka perbedaan data DTMF yang digunakan pada setiap menara tersebut digunakan sebagai isyarat penentu dari posisi kereta api.

Gelombang radio pada perancangan ini digunakan untuk menghindari terjadinya frekuensi silang, karena dalam miniatur sistem monitoring ini jarak antar penerima yang satu dan yang lain berdekatan sehingga guna mengurangi terjadinya kesalahan pengiriman dan penerimaan sinyal, oleh karena itu dalam perancangan ini menggunakan 2 (dua) sistem pemancar dan penerima (transducer ultrasonik dan gelombang radio). Karena pada perancangan untuk gelombang radio menggunakan modul yang ada di pasaran maka untuk modul gelombang radio akan dijelaskan secara garis besar.

Untuk mendapatkan tampilan secara visual dan sebagai pengolah akhir dari penerimaan sinyal DTMF maka dalam perancangan dan pembuatan ini perancang menggunakan mirokontroler type AT89C51, sehingga setelah sinyal DTMF diterima, sinyal tersebut dapat ditampilkan pada lampu indikator, begitu dengan seterusnya sampai kereta api sampai pada tujuan..Untuk memahami lebih jelasnya berikut gambaran mengenai alat dan blok diagram dalam perencanaan, perancangan pembuatan sistem monitoring pada jalur kereta api :



Gambar 3-1. Miniatur Sistem Monitoring
Posisi Kereta Api Pada Jalur/Rel Kereta Api



Gambar 3-2. Blok Diagram Sistem Monitoring

3.2. Perancangan dan Pembuatan Alat

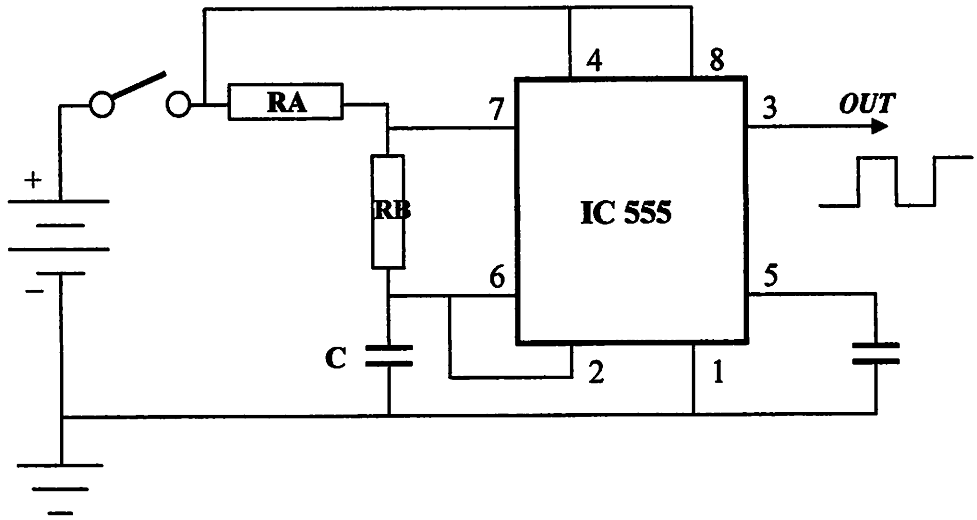
Pada sistem monitoring ini ada 5 hal pokok penting yang hendak dirancang, yaitu Transmitter Ultrasonic, Receiver Ultrasonic, DTMF Transmitter RF, DTMF Receiver RF dan Pemrograman Mikrokontroller.

Untuk sub-sub bagian dari masing-masing perancangan adalah sebagai berikut :

1. Pada Transmitter Ultrasonic terdiri dari : :
   - Osilator Astabil Multivibrator 40 KHz
2. Pada Receiver Ultrasonic dan Transmitter RF terdiri dari 4 bagian yaitu:
   - High Pass Filter
   - Rangkaian Pengkondisi sinyal
   - Mikrokontroler AT89C51
   - DTMF Generator IC TP5088
3. Pada Receiver RF :
   - DTMF Demodulator IC MT8870
   - Mikrokontroler AT89C51
   - LED Display dan LCD

3.2.1. Perancangan dan Pembuatan Transmitter Ultrasonik

Seperti yang dijelaskan di atas bahwa untuk transmitter digunakan osilator astabil multivibrator dengan menggunakan IC 555. yang bekerja pada frekuesi 40 KHz. Berikut bentuk rangkaian skematik dan perhitungan nilai komponennya :



Gambar 3-3. Rangkaian Skematik Osilator Astabil Multivibrator

Dengan ditentukan nilai komponen pembanding Rb = 18 KΩ, C = 680 pF dan frekuensi kerja sebesar 40 Khz. Maka untuk menentukan besarnya nilai komponen Ra adalah sebagai berikut

$$f = \frac{1{,}44}{(Ra + 2Rb)C}$$

$$40.000 = \frac{1{,}44}{(Ra + 2.18.10^3)680.10^{-12}}$$

$$(Ra + 2.18.10^3) = \frac{1,44}{40.000x680.10^{-12}}$$

$$= 52.941,2$$

$$Ra = 52.941,2 - 36.000$$

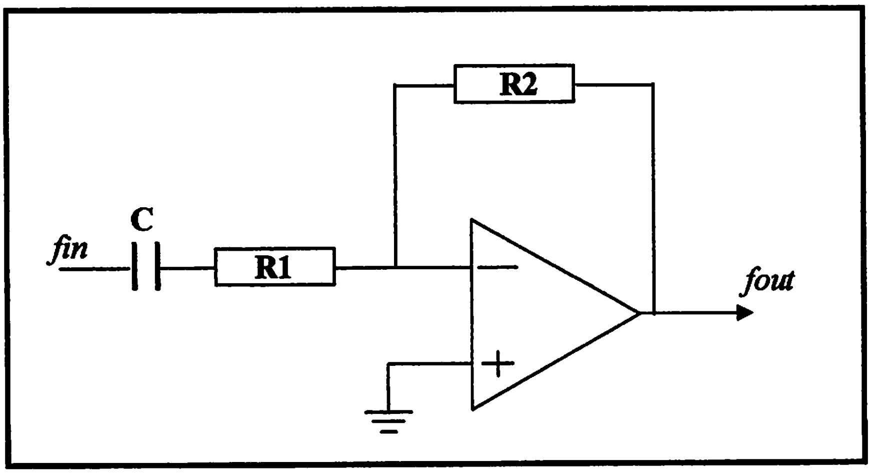
$$= 16.941,2$$

$$= 17\,K\Omega$$

3.2.2. Perancangan dan Pembuatan Receiver Ultrasonik dan DTMF Generator

3.2.2.1. High Pass Filter

Pada perancangan ini digunakan High Pass Filter untuk meloloskan frekuensi 40 Khz. Untuk rangkaian skematik dan perhitungannya adalah sebagai berikut :



Gambar 3-4. Rangkaian Skematik High Pass Filter

Sedangkan untuk perhitungan nilai komponennya adalah sebagai berikut Dengan ditentukan frekuensi cutt off sebesar 37 KHz dan R1 = 1,3 KΩ maka untuk mencari nilai C:

$$f_c = \frac{1}{2.\pi.R1.C}$$

$$37.0000 = \frac{1}{2x3{,}14x1.300xC}$$

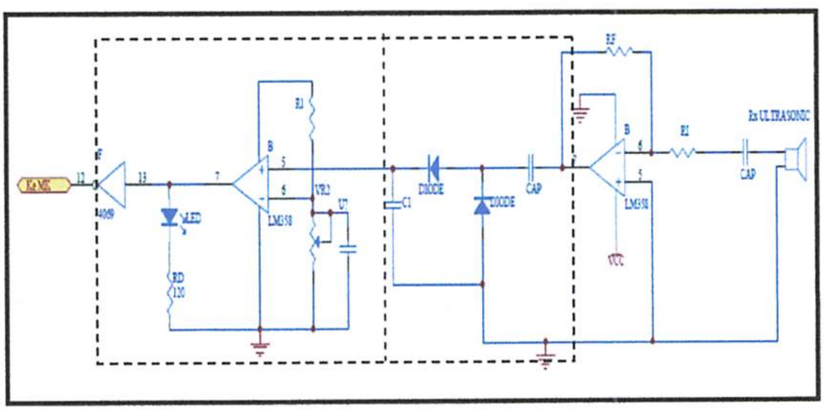
$$37.000 = \frac{1}{8.164xC}$$

$$8.164 \text{ x C} = \frac{1}{37.000}$$

$$\text{C} = 3{,}31\ 10^{-9}$$

3.2.2.2. Pengkondisi Sinyal

Rangkaian pengkondisi sinyal terdiri dari detector peak to peak sebagai penyearah frekuensi yang dihasilkan dari frekuensi keluaran pada saat receiver ultrasonic menerima sinyal, sedangkan comparator dan inverter digunakan untuk menghasilkan tegangan keluaran menjadi 0 V dan 5 V (*high* dan *Low*)



Gambar 3-5. Rangkaian Skematik Pengkondisi Sinyal

Untuk comparator digunakan tegangan referensi sebesar 0,7 volt, sehingga jika pada saat receiver menerima sinyal dari transmitter tegangan keluaran yang dihasilkan kurang dari 0,7 volt maka output comparator akan berlogika low dan akan berlogika high apabila Vin > Vref, oleh karena itu jarak penerimaan pada receiver ultrasonic dapat dibatasi dengan mengatur besar kecilnya tegangan referensi pada comparator.

Untuk perhitungan dari tegangan referensi adalah sebagai berikut :

Ditentukan nilai Vcc : 5 Volt, R1 = 10 KΩ dan besarnya Vref yang diinginkan sebesar 0,7 Volt, maka nilai R2 adalah :

$$V = \frac{R2}{R1 + R2} Vcc$$

$$0{,}7 = \frac{R2}{10.10^3 + R2} 5$$

$$0{,}7\,(10.10^3 + R2) = 5R2$$

$$7.000 + 0{,}7R2 = 5R2$$

$$5R2 - 0{,}7R2 = 7.000$$

$$4{,}3R2 = 7.000$$

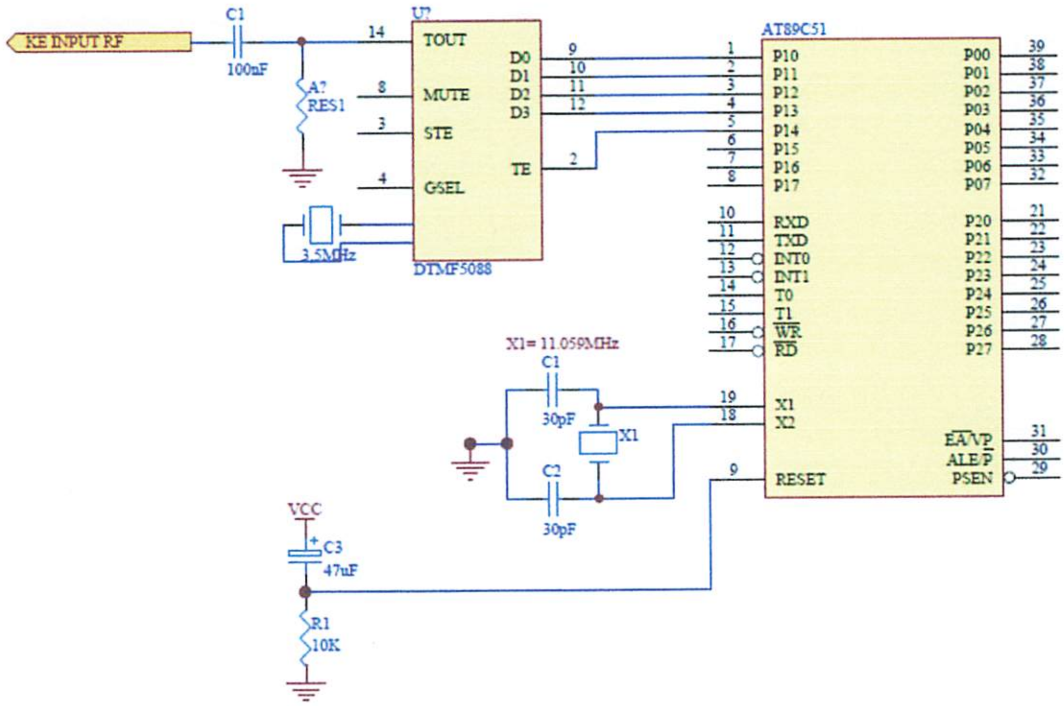
$$R2 = \frac{7.000}{4{,}3}$$

$$R2 = 1.627{,}8$$

$$R2 = 1{,}6\ K\Omega$$

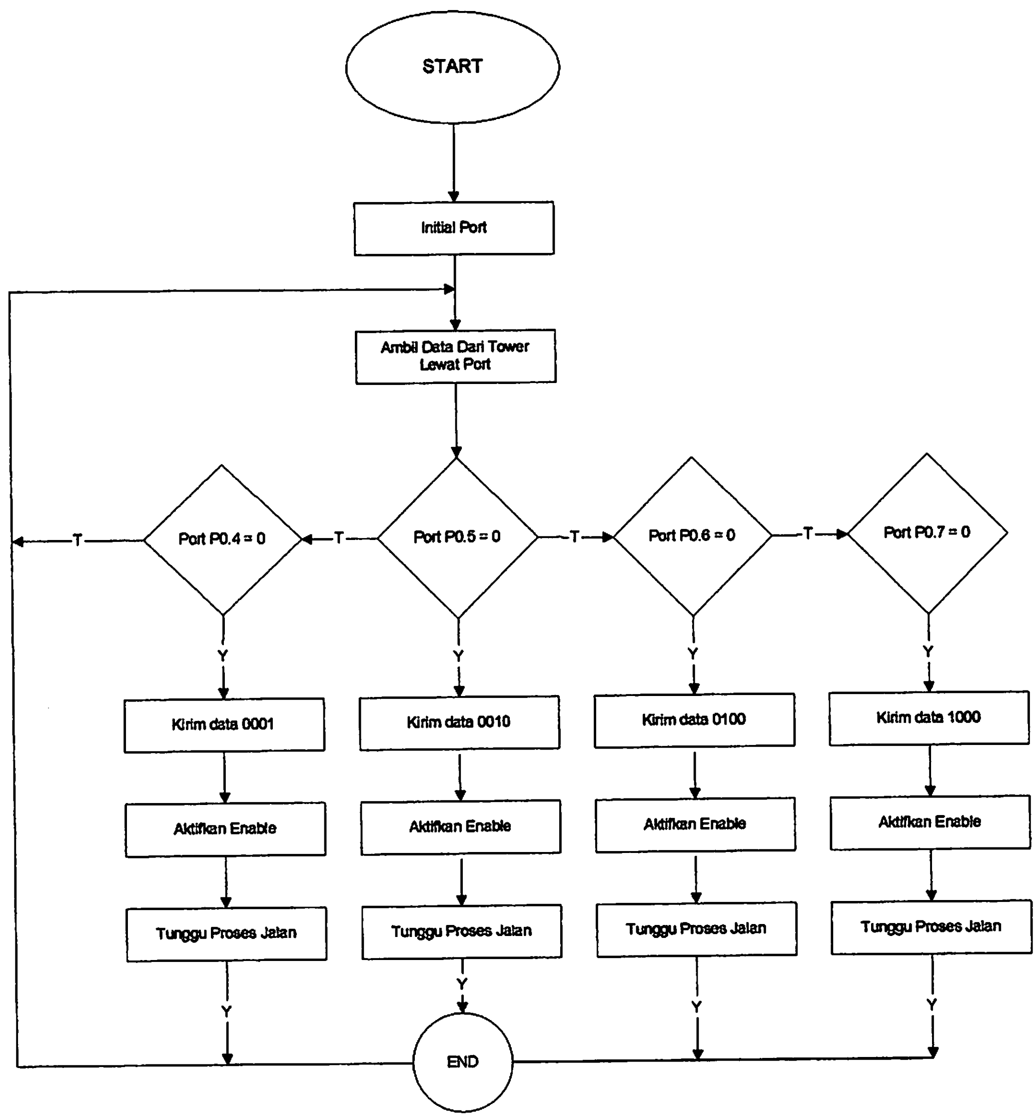
3.2.2.3. AT89C51 dan DTMF Generator TP5088

Tujuan penggunaan mikrokontroler adalah untuk pemilih 4 (empat) bit data DTMF pada IC TP5088 dan untuk memudahkan pada perancangan alat. Untuk bentuk rangkaian skematiknya adalah sebagai berikut :



Gambar 3-6. Rangkaian DTMF dan Mikrokontroler AT89C51

Flowchart AT89C51 sebagai pemilih informasi data DTMF adalah sebagai berikut :



Gambar 3-7. Flowchart DTMF Input

Sedangkan untuk Data DTMF yang digunakan adalah sebagai berikut :

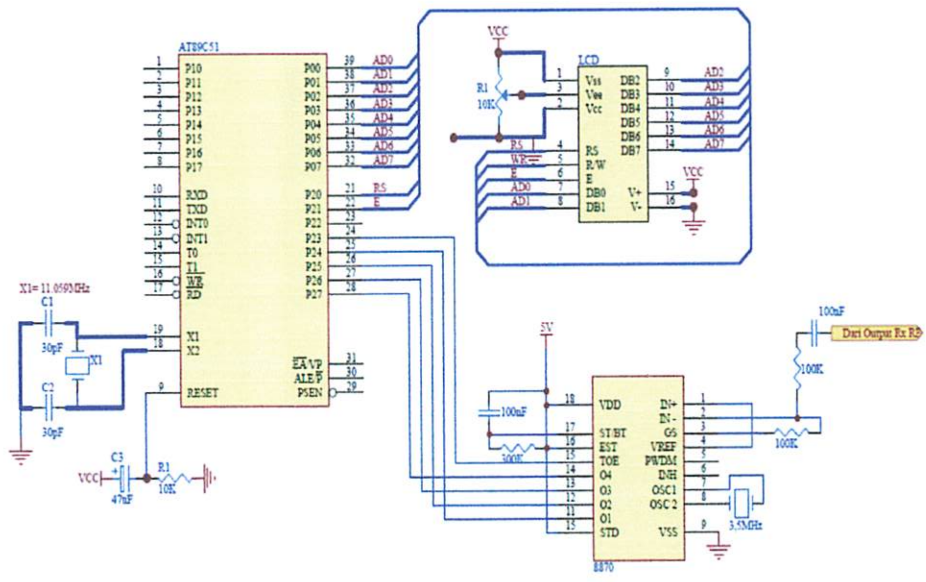
- Informasi menara 1 digunakan input data DTMF 1
- Informasi menara 2 digunakan input data DTMF 2
- Informasi menara 3 digunakan input data DTMF 4
- Informasi menara 4 digunakan input data DTMF 8

Sedangkan untuk 4 (empat) bit data DTMF yang digunakan pada masukkan pin D0-D3 selengkapnya dapat dilihat pada tabel 2-3 (hal.14).

3.2.3. Perancangan dan Pembuatan Demodulator DTMF dan Tampilan Posisi Kereta Api.

Pada perancangan receiver RF digunakan modul wireless yang bekerja pada jalur VHF dengan frekuensi sebesar 120 MHz. Karena pada perancangan ini untuk receiver RF menggunakan modul maka pada sub-bab ini hanya akan dijelaskan pada perancangan Demodulator DTMF dan AT89C51 sebagai pengolah data akhir yang akan dtampilkan pada LED *display*.

Agar data DTMF yang diterima pada receiver RF yang ditransmisikan dari modul wireless microphone transmitter dapat dihasilkan kembali maka diperlukan sebuah komponen demodulator yang mampu mendemodulasikan data DTMF. Maka pada perancangan ini digunakan IC MT8870 yang biasa digunakan pada penerima DTMF. Untuk rangkaian skematik dapat dilihat pada gambar di bawah ini.



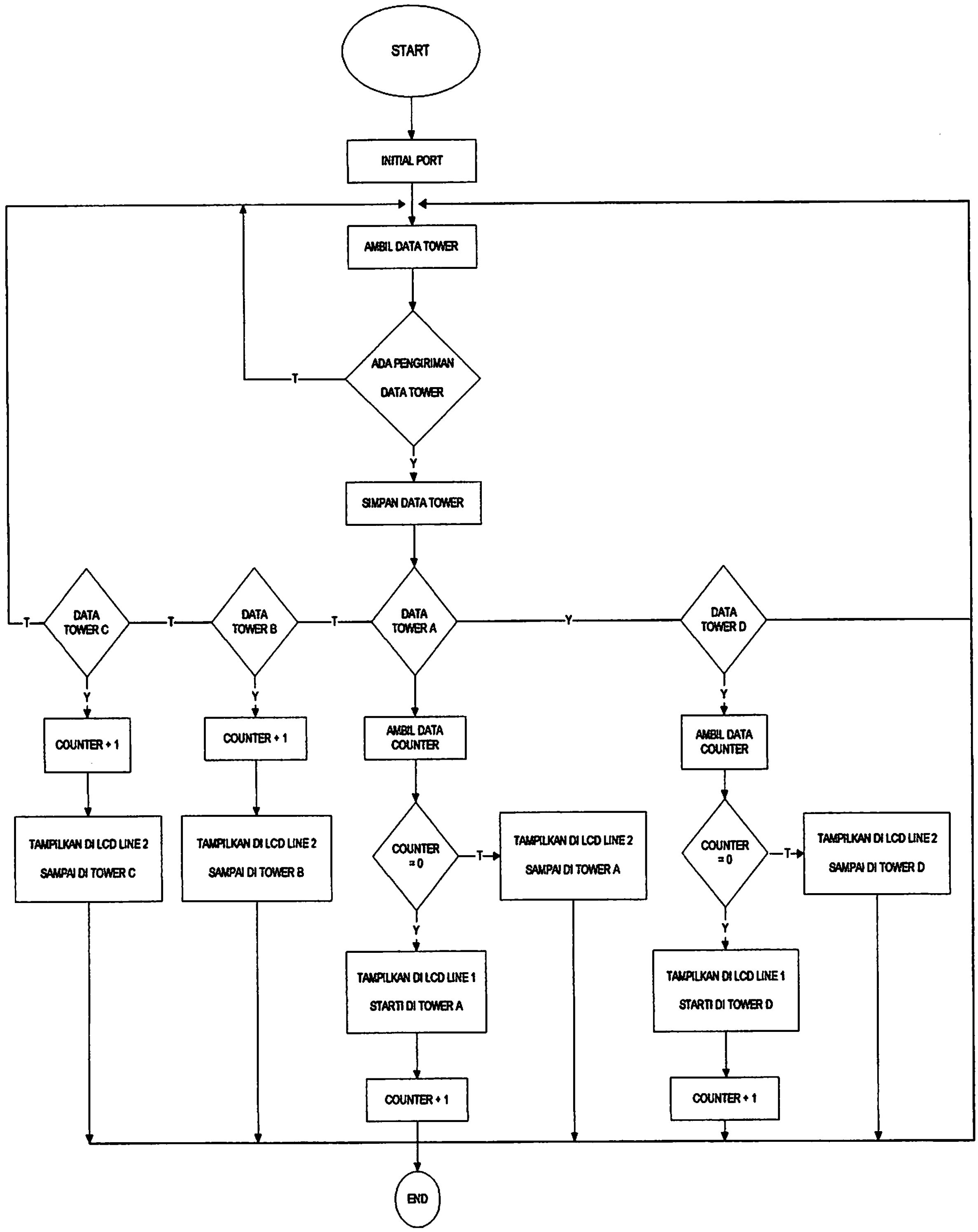
Gambar 3-8. Rangkaian Demodulator DTMF dan AT89C51

Sedangkan untuk frekuensi demodulasi yang digunakan sebagai data output dari IC MT8870 dapat dilihat pada tabel di bawah ini :

f_{LOW}	f_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1209	0	1	1	0	1	0
941	1336	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0
-	-	ANY	0	Z	Z	Z	Z

Tabel 3-1. Tabel Kebenaran Output MT8870

Flowchart AT89C51 sebagai pengolah data DTMF untuk ditampilkan pada LED display dan LCD adalah sebagai berikut :



Gambar 3-9. Flowchart Untuk Menampilkan Posisi Kereta Api

BAB IV

PENGUJIAN ALAT

4.1. Tujuan

Bab ini membahas tentang pengujian alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah rancangan yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi perencanaan yang telah ditetapkan. Pengujian rancangan ini dilakukan dalam dua tahap. Pertama, dilakukan pengujian terhadap hardware pada masing-masing blok diagram penyusun sistem antara lain :

a. Transmitter Transduser Ultrasonik
   - Bentuk Gelombang Keluaran Osilator Astabil Multivibrator IC555
b. Receiver Transducer Ultrasonik
   - Hasil Gelombang keluaran High Pass Filter dan
   - Rangkaian Pengkondisi Sinyal
c. Modulasi dan Demodulasi DTMF

Dan untuk Pengujian kedua dilakukan pada sistem secara keseluruhan untuk mengetahui sejauh mana alat ini bekerja.

4.2. Peralatan Yang Digunakan

Peralatan yang dipergunakan dalam pengukuran dan pengujian rangkaian antara lain adalah :

1. Analog Oscilloscope
2. Digital Multimeter HB DT-9205A
3. Analog Multimeter Sanwa YX-360TRN $_{LED}$

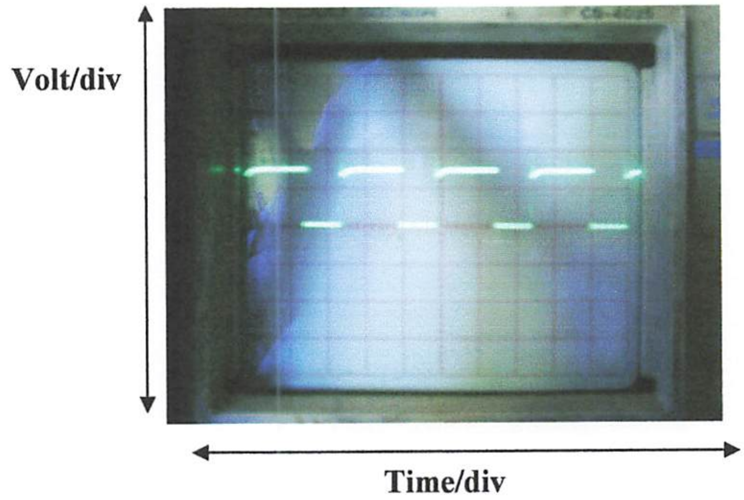
4.3. Prosedur Pegujian

Pada rangkaian transmitter ultrasonic dicatu/dihubungkan dengan tegangan DC sebesar 9 Volt dimana tegangan catu didapat dari baterai 9 Volt DC yang kemudian untuk menguji hasil frekuensi keluaran pada tiap-tiap bagian transmitter harus dalam keadaan hidup/On. Sedangkan untuk bagian penerima ultrasonic, pemancar RF, penerima Rf dan mikrokontroler harus selalu dalam keadan On (Stand-by) dengan cara memasang tegangan DC 5 Volt ke tegangan catu.

4.3.1. Pengujian Rangkaian Transmiter Ultrasonik

Pengukuran ini dilakukan untuk mengetahui besarnya frekuensi yang dihasilkan dari osilator astabil multivibrator pada transmitter ultrasonic, dan untuk melihat bentuk gelombang keluarannya , berikut hasil dari pengujian transmitter ultrasonic :

- Pengujian dilakukan dengan mengatur Time/Div dan Volt/Div dari Osiloskop yaitu sebesar T/div = 10 us dan V/div = 5 V.



Gambar 4-1. Bentuk Gelombang Hasil Pengujian Osilator Astabil Multivibrator

Untuk hasil percobaan didapatkan perhitungan untuk mengetahui frekuensi yang dihasilkan berdasarkan besarnya Time/div pada pengaturan osiloskop. Dari gambar di atas dapat dilihat untuk mencapai 1 (satu) gelombang penuh dibutuhkan waktu sebesar 25 us dan tegangan peak to peak sebesar 7,5 Volt. Dari hasil di atas dapat dihitung besarnya frekuensi yang dihasilkan, yaitu sebesar :

$$f = \frac{1}{T}$$

$$= \frac{1}{25.10^{-6}}$$

$$= 40 \text{ KHz}$$

Time/Div	Volt/Div	Time	V p-p	Frekuensi
10 us	5 Volt	25 us	7,5 Volt	40 KHz

Tabel 4-1. Data Hasil Pengujian Rangkaian Frekuensi Modulasi

Dari hasil perhitungan pada bab 3 (tiga) dan hasil percobaan di atas didapat frekuensi error sebesar 0 %, untuk perumusan dalam menghitung besarnya error adalah sebagai berikut:

$$\% \text{ error} = f_{Pengujian} - f_{Perhitungan} \text{ x } 100\%$$

$$= 40KHz - 40KHz \text{ x } 100\%$$

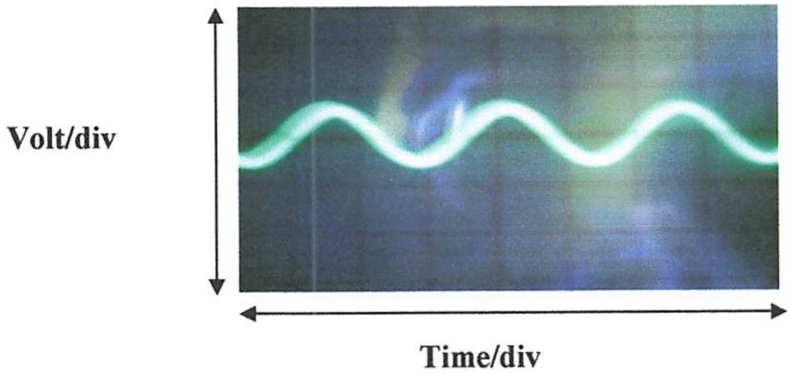
$$= 0\,\%$$

4.3.2. Pengujian Rangkaian Receiver Ultrasonik dan Pengkondisi Sinyal

4.3.2.1. Pengujian Receiver Ultrasonik

Pada pengujian ini dilakukan untuk mengetahui besarnya frekuensi yang dihasilkan, bentuk gelombang dari receiver ultrasonic dan sejauh mana receiver ultrasonic bekerja, untuk bentuk gelombang dari hasil pengujian adalah sebagai berikut :

- pengujian dilakukan dengan mengatur Time/div pada osiloskop yaitu sebesar 10 us, Volt/div sebesar 2 Volt.



Gambar 4-2. Bentuk Gelombang Hasil Pengujian Receiver Ultrasonik

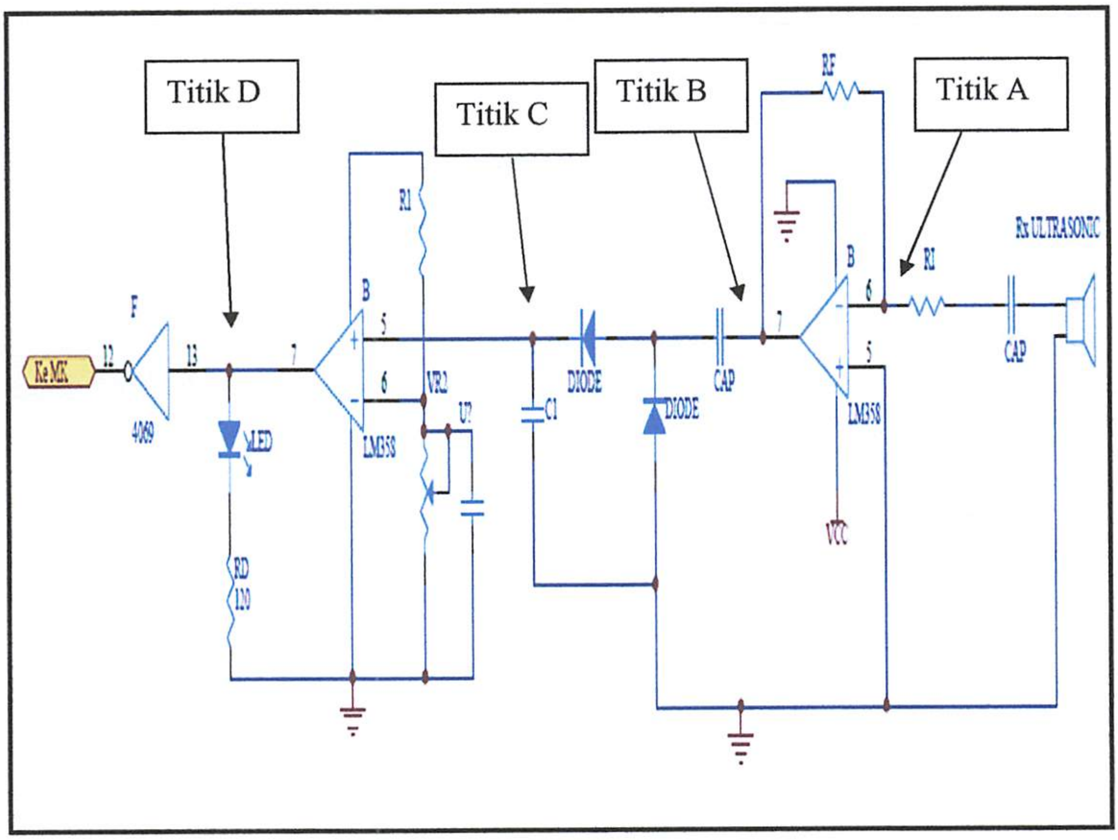
Pada gambar 4-2 hasil pengujian penerimaan frekuensi ultrasonic waktu yang dibutuhkan untuk mencapai 1 (satu) gelombang penuh adalah sebesar 25 us, sehingga sama halnya dengan perhitungan frekuensi pada pengujian transmitter ultrasonic bahwa frekuensi yang dihasilkan pada receiver ultrasonic adalah sebesar 40 KHz.

Time/Div	Volt/Div	Time	V p -p	Frekuensi
10 us	2 Volt	25 us	3 Volt	40 KHz

Tabel 4-2. Data Hasil Pengujian Rangkaian Receiver Ultrasonik.

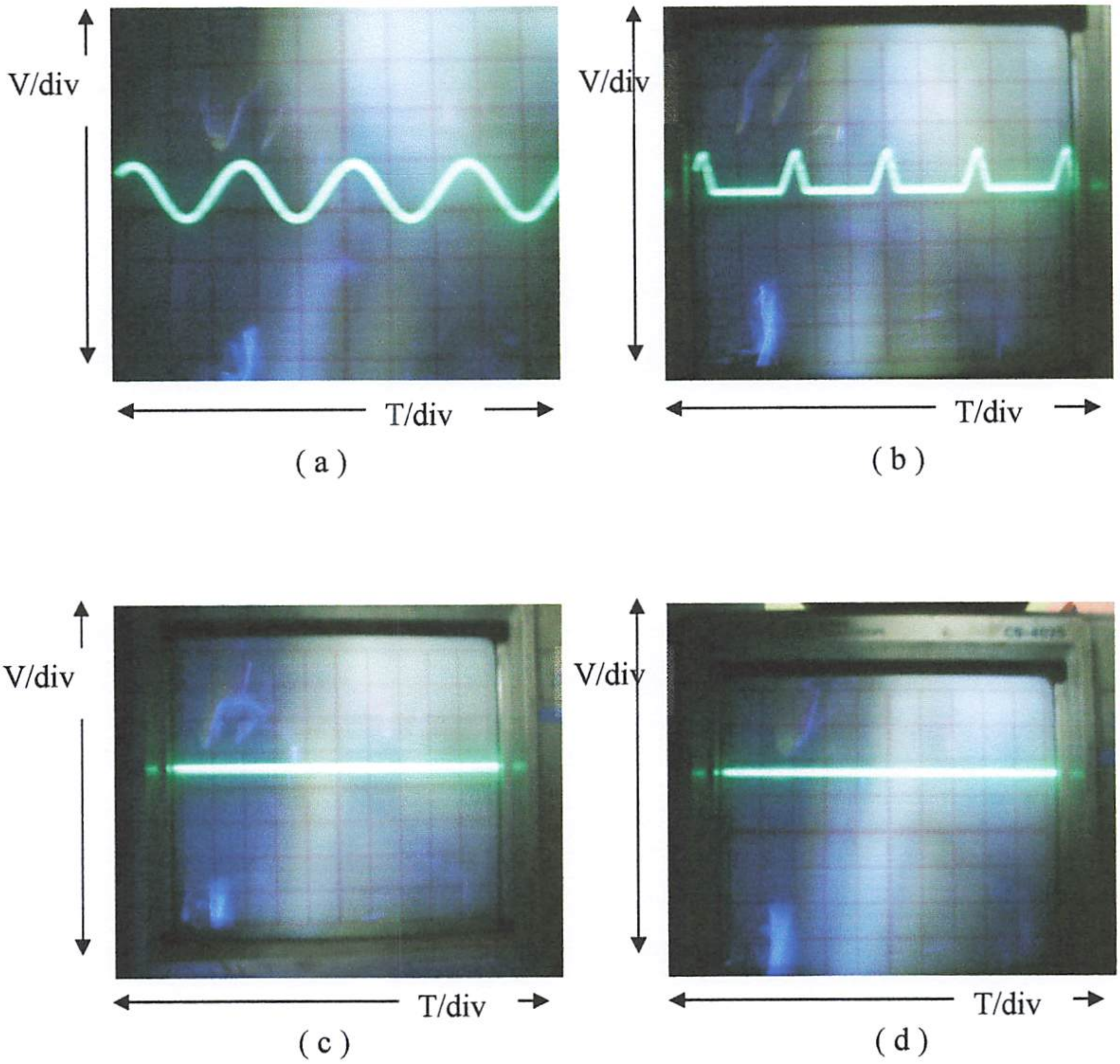
4.3.2.2. Pengujian High Pass Filter dan Rangkaian Pengkondisi Sinyal

Pada pengujian ini ditampilkan 4 (empat) hasil pengujian sekaligus.Tujuannya adalah untuk memudahkan dalam memahami, menganalisa suatu rangkaian percobaan dan sejauh mana alat ini dapat bekerja. Sedangkan letak titik pengujian adalah sebagai berikut :



Gambar 4-3. Letak Titik-Titik Pengujian High Pass Filter dan Pengkondisi Sinyal

Untuk pengaturan Time/div dan Volt/div pada pengujian setiap titik adalah sama, yaitu untuk Time/div diatur sebesar 10 us dan Volt/div sebesar 2 Volt.



Gambar 4-4. Bentuk Gelombang Hasil Pengujian (a) Input HPF, (b) Output HPF dan Clamping, (c) output Detektor Puncak dan (d) Output Comparator

Dari hasil percobaan HPF dan Rangkaian pengkondisi sinyal dapat dilihat bahwa nilai frekuensi pada input HPF dan pada Output HPF mempunyai besar yang sama yaitu sebesar 25 us (lihat gambar 4-4. (a) dan (b)), sehingga seperti pada perumusan sebelumnnya bahwa nilai frekuensinya yaitu sebesar 40 Khz.

Perbedaan dari masing-masing gambar pengujian diatas dapat dilihat bahwa pada masing-masing titik percobaan mempunyai bentuk gelombang yang berbeda. Hal tersebut dikarenakan pada masing-masing titik percobaan mempunyai karakteristik tersendiri yaitu :

Titik A : adalah membuktikan bahwa pada input HPF frekuensi inputan tidak berubah yaitu sebesar 40 KHz.

Titik B : adalah hasil keluaran dari HPF dan Clamping, pada titik dapat kita lihat (gambar 4-4. (b)) terjadi pemotongan bentuk gelombang, hal tersebut dikarenakan sesuai dengan fungsi dari rangkaian clamping yaitu menambahkan komponen dc kepada suatu isyarat.

Titik C : adalah hasil keluaran dari Detektor puncak yang sebesar 40 Khz mempunyai tegangan keluaran sebesar 1,2 Volt.

Titik D : adalah hasil keluaran dari comparator, dimana dari hasil pengujian (gambar 4-4. (d)) dapat dilihat bahwa komparator akan berlogika high apabila nilai tegangan input lebih besar dari tegangan referensi yang ditentukan yaitu 0,7Volt pada perancangan

Titik Percobaaan	Time/Div	Volt/Div	Time	V p-p	Frekuensi
Titik A	10 us	2 Volt	25 us	3 Volt	40 KHZ
Titik B	10 us	2 Volt	25 us	3 Volt	40 KHz
Titik C	10 us	2 Volt	-	1,2 Volt	-
Titik D	10 us	2 Volt	-	3,8 Volt	-

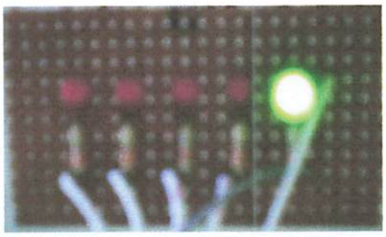
Tabel 4-3. Data Hasil Pengujian Rangkaian HPF dan Pengkondisi Sinyal

4.3.3. Pengujian Modulasi dan Demodulasi DTMF

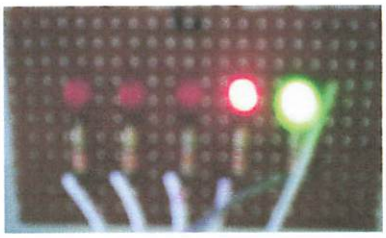
Tujuan dari percobaan ini adalah untuk mengetahui apakah data output DTMF demodulasi (IC MT8870) yang dihasilkan pada penerima wireless microphone sama dengan data yang ditransmisikan dari DTMF Generator (IC TP5088). Data pengujian sesuai dengan perancangan adalah sebagai berikut :

- Informasi menara 1 digunakan input data TP5088 DTMF 1 = 0001
- Informasi menara 2 digunakan input data TP5088 DTMF 2 = 0010
- Informasi menara 3 digunakan input data TP5088 DTMF 4 = 0100
- Informasi menara 4 digunakan input data TP5088 DTMF 8 = 1000

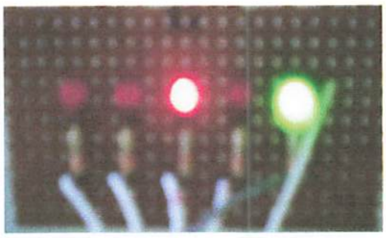
Pengujian dilakukan dengan cara memberikan LED pada pin Q1-Q4 di IC MT8870, sehingga dengan mengetahui nyala LED di tiap pin Q1-Q4 dapat diketahui data DTMF yang digunakan sebagai data informasi.Berikut hasil dari pengujian :



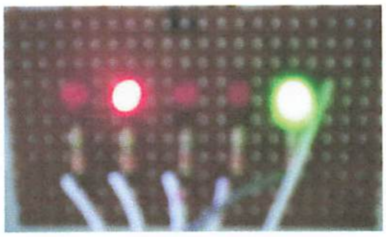
(a)



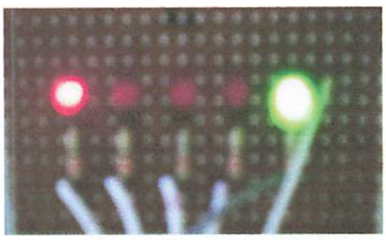
(b)



(c)



(d)



(e)

Gambar 4-5. Hasil Demodulasi IC MT8870

Keterangan gambar LED dari kiri ke kanan

Q4, Q3 ,Q2, Q1 dan TO = Tone Enable

Gambar (a) menunjukan kondisi rangkaian sebelum data diterima

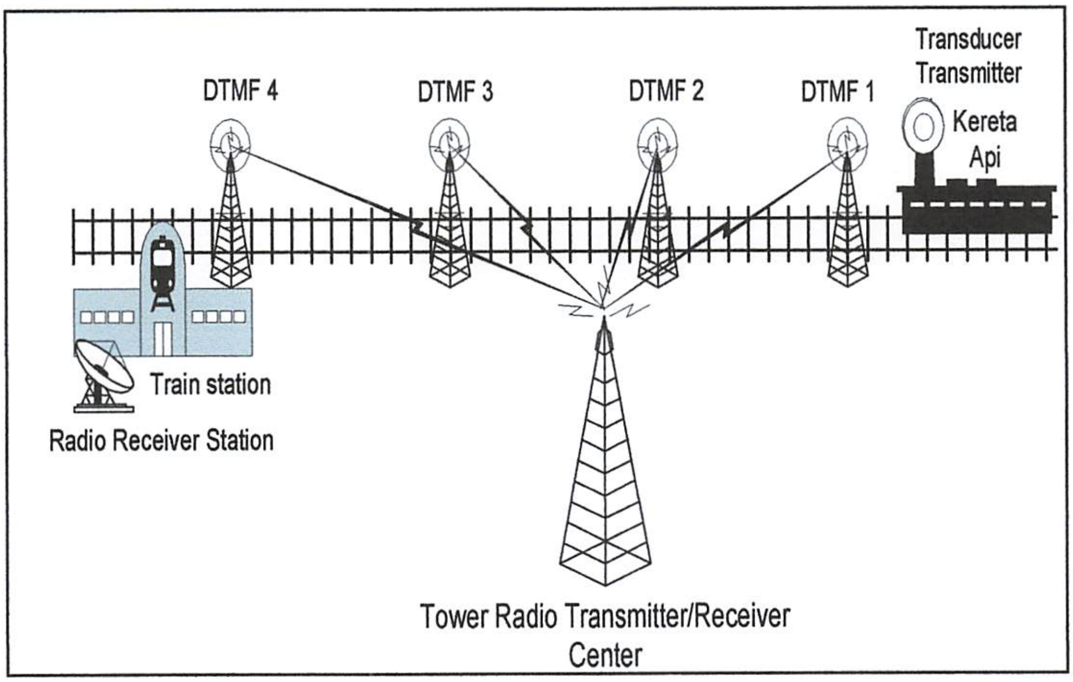
Gambar (b) menunjukan data hasil demodulasi MT8870 dari tower 1 = 0001

Gambar (c) menunjukan data hasil demodulasi MT8870 dari tower 2 = 0010

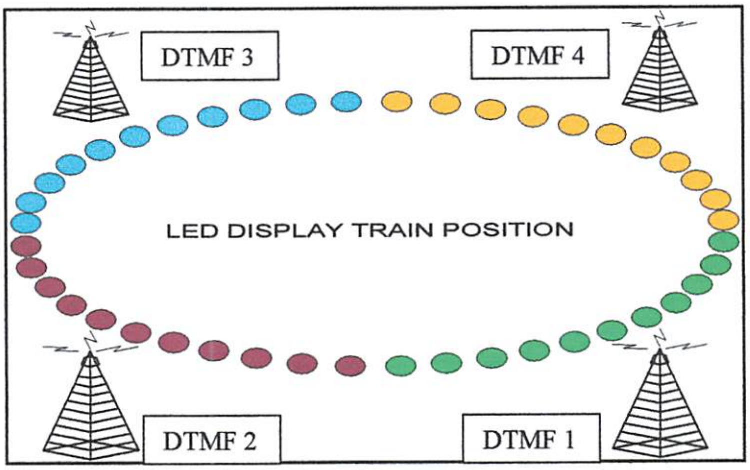
Gambar (d) menunjukan data hasil demodulasi MT8870 dari tower 3 = 0100

Gambar (e) menunjukan data hasil demodulasi MT8870 dari tower 4 = 1000

Data - data yang diterima kemudian ditampilkan dengan menggunakan LED yang menginformasikan posisi kereta api..



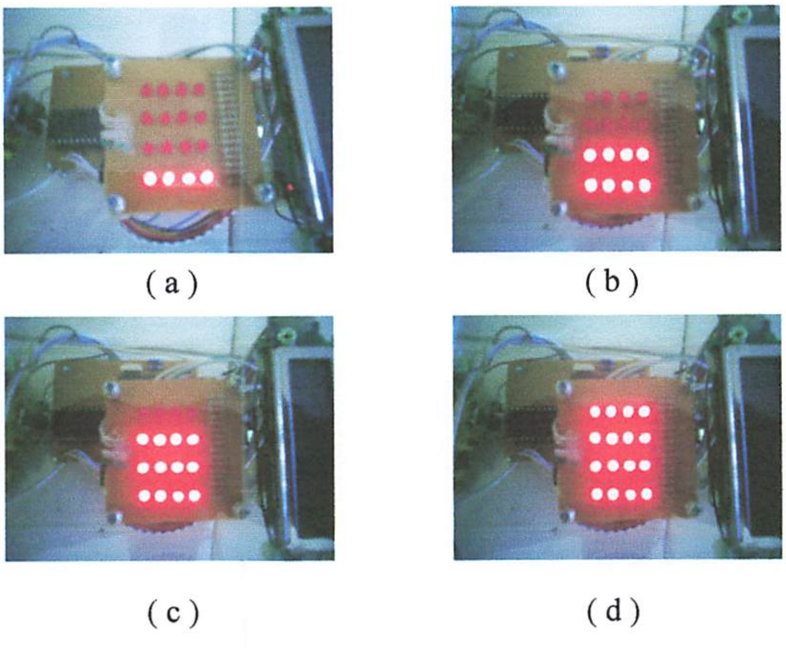
Gambar 4–6. Data DTMF pada Tower yang Digunakan Sebagai Posisi Kereta Api



Gambar 4–7. Tampilan Posisi Kereta Api

4.4. Hasil Pengujian Alat Secara Keseluruhan

Dari masing – masing pengujian di atas dapat diuji secara keseluruhan dengan melihat hasil akhir pada pengujian yaitu dengan cara melihat tampilan posisi kereta api pada *LED Display Train Position*..



(a) (b) (c) (d)

Gambar 4–8. Tampilan Posisi Kereta Api pada LED yang Ditampilkan Berjajar

Keterangan gambar 4 – 8 :

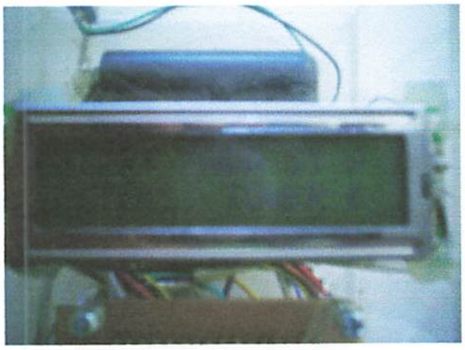
Gambar (a) menunjukan kereta api berada pada posisi Tower A ditempatkan.

Gambar (b) menunjukan kereta api berada pada posisi Tower B ditempatkan.

Gambar (c) menunjukan kereta api berada pada posisi Tower C ditempatkan.

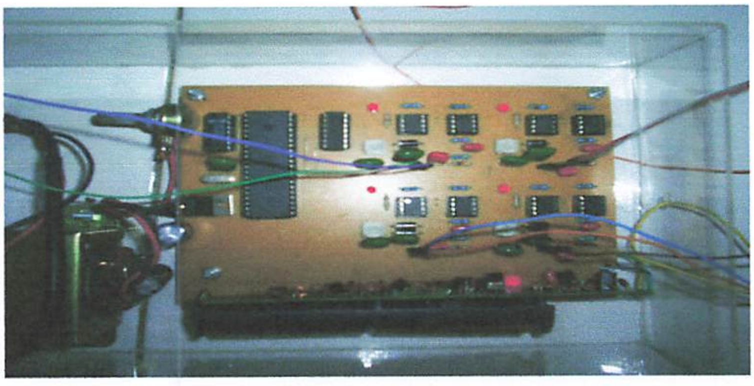
Gambar (d) menunjukan kereta api berada pada posisi Tower D ditempatkan.

Untuk memudahkan pada pembacaan posisi kereta api, maka pada perancangan ini ditambahkan sebuah LCD untuk menampilkan posisi kereta api berbentuk text.



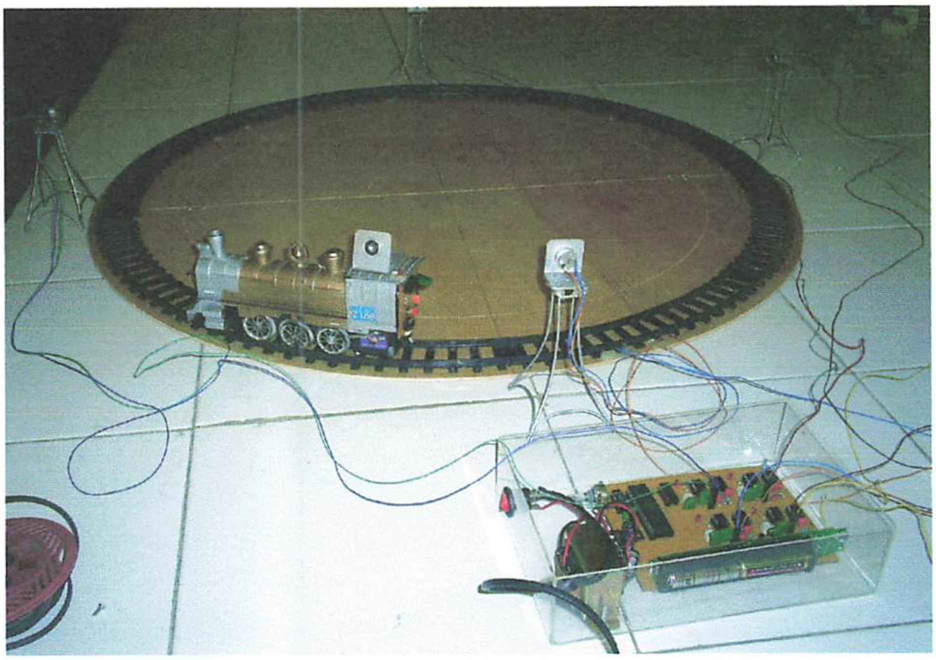
Gambar 4–9. Tampilan Posisi Kereta Api pada LCD Berbentuk Text

Sedangkan untuk gambar hasil perancangan alat keseluruhan dapat dilihat pada foto alat di bawah ini :



Gambar 4-10. Foto Alat Receiver Ultrasonik dan Transmitter Modul RF

Gambar 4-11 Foto Alat Modul Receiver RF dan Posisi Kereta Api



Gambar 4-12. Foto Alat Keseluruhan

BAB V

PENUTUP

5.1. Kesimpulan

Dari hasil pengujian alat system monitoring kereta api dapat diambil beberapa kesimpulan

1. Sistem monitoring pada perencanaan ini menggunakan 2 (dua) jalur frekuensi yaitu Low Frekuensi untuk transduser ultrasonic dan Very High Frekuensi pada modul *wireless microphone.*
2. Pada hasil perancangan alat ini penggunaan gelombang ultrasonic sebagai media penghantar melalui udara mempunyai hasil sesuai dengan perancangan dimana pada perancagan ini gelombang utrasonik Dengan menggunakan gelombang ultrasonic dan gelombang radio sistem monitoring posisi kereta api berjalan sesuai dengan perencanaan dan perancangan.
3. Data yang digunakan sebagai informasi posisi kereta api adalah perbedaan data DTMF yang digunakan pada setiap menara. Sehingga pada perencanaan system monitoring ini, penentuan posisi kereta api berdasarkan dari perbedaan data DTMF dan penempatan menara pada jalur kereta api dengan skala jarak tertentu yang mengisyaratkan letak atau posisi kereta api.
4. Pada alat sistem monitoring ini hanya dapat mengetahui letak/posisi kereta api.

5. Sistem monitoring ini belum dapat mengetahui posisi kereta api apabila kereta api.kereta api berada diantara menara.
6. Sistem komunikasi gelombang radio mempunyai aplikasi yang sangat beragam, salah satunya adalah dengan dirancangnya alat ini.

5.2. Saran

1. Informasi yang dapat di monitoring hendaknya lebih beragam. Salah satunya adalah dengan ditambahkan informasi nama kereta api dan informasi yang lain.
2. Pada perancangan alat ini untuk gelombang ultrasonic hendaknya tidak meggunakan transduser ultrasonic, hal tersebut dikarenakan transducer ultrasonic mempunyai kelemahan apabila osilator frekuensi yang sebesar 40 KHz dimodulasikan dengan frekuensi rendah, Oleh karena itu hendaknya transducer ultrasonic dapat digantikan dengan menggunakan komponen lain atau bisa juga dengan merubah daerah frekuensinya dengan menggunakan gelombang radio
3. Agar alat ini dapat terealisasi hendaknya daya pancar/jarak jangkau pada transmitter dan receiver diperhitungkan. Begitu juga dengan gangguan frekuensi yang disebabkan dari luar.
4. Jika diperbolehkan, penggunaan DTMF sebagai data/informasi pada perancangan alat ini mempunyai data/informasi yang sangat beragam, hal tersebut dikarenakan selain dalam perancangan alat ini bahwa

data DTMF mempunyai 16 (enam belas) bit data yang dapat dikombinasikan untuk dijadikan sebagai informasi.

5. Pada perancangan alat ini agar bisa terealisasi hendaknya dalam pembuatannya lebih baik dikerjakan secara kelompok (*teamwork*), karena pada system ini mempunyai permasalahan yang cukup beragam.

Daftar Pustaka

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- http://en.wikipedia.org

LAMPIRAN

FORMULIR PERBAIKAN SKRIPSI

Nama	:	ZIKI ZAULIA PANDUWINATA
NIM	:	01.17.032
Jurusan	:	Teknik Elektro S-1
Konsentrasi	:	Teknik Elektronika

No.	Materi Perbaikan	Paraf
1.	Bab IV - Penjelasan Pada Penguijian	
2.	Lampiran - Rangkaian Skematik	

Telah diperiksa dan disetujui,

Penguji I

Sotyohadi, ST, MSc.

Penguji II

Joseph Dedy Irawan, ST, MT.
NIP 132315178

Mengetahui,

Dosen Pembimbing

Ir. Sidik Noertjahjono, MT
NIP.P. 102 870 0163

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

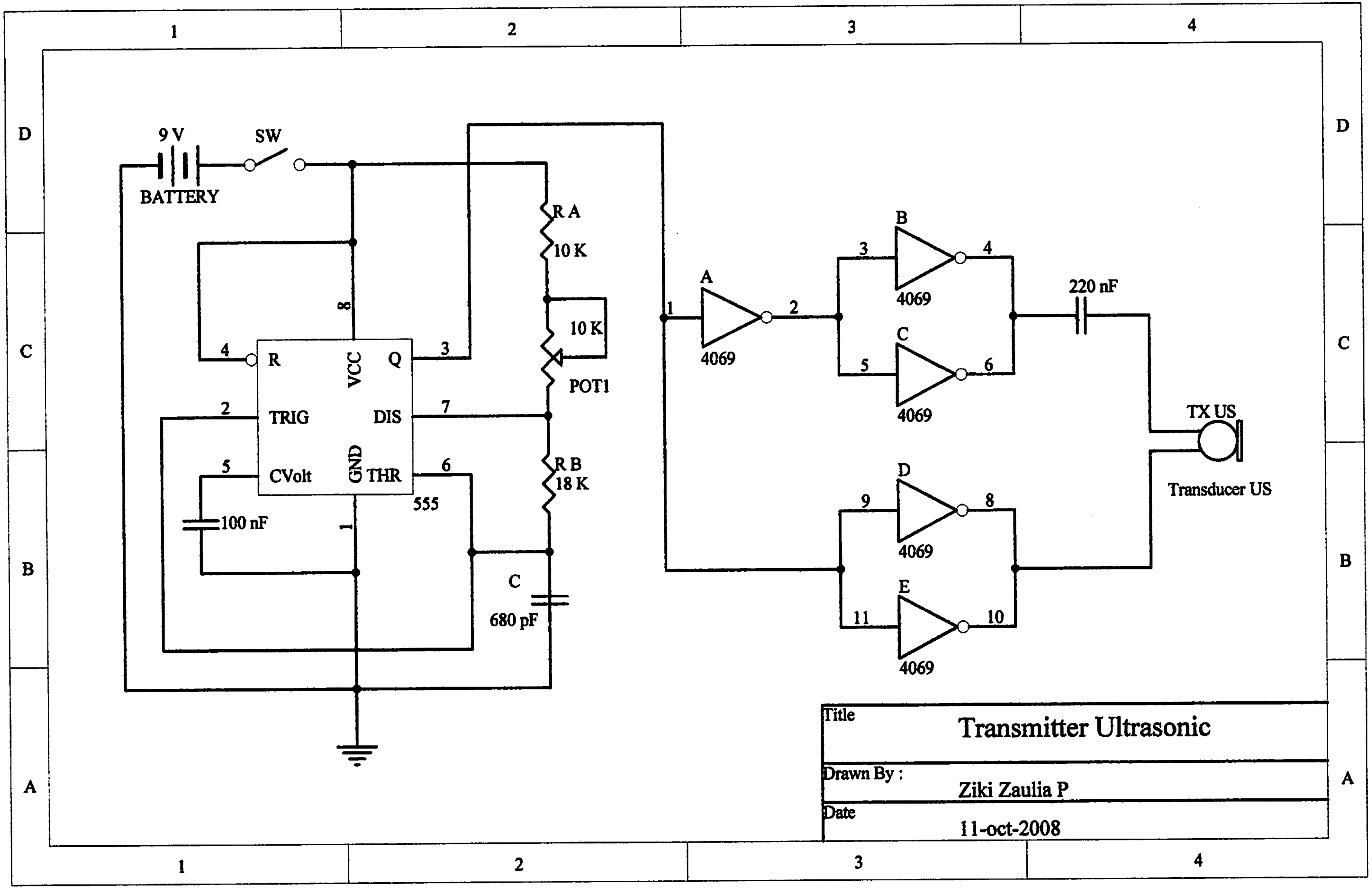
Nama : Ziki Zaulia Panduwinata
Nim : 0117032
Masa Bimbingan : 11-Jun-2005 s/d 12-Dec-2005
Judul Skripsi : Perancangan dan pembuatan sistem monitoring pada jalur kereta api dengan menggunakan gelombang Ultrasonik dan gelombang radio berbasis Mikrokontroller AT899C51

NO	Tanggal	Uraian	Paraf Pembimbing
1.	14 Mei 2005	Konsultasi Judul.	[signature]
2.	28/5 -2005.	Konsultasi Ringkasan	[signature]
3.	5/11 - 06.	Konsultasi Bab IV.	[signature]
4.	10/4 - 07.	Konsultasi Makalah Prop.	[signature]
5.	12/5 - 08.	Konsultasi Bab Teori	[signature]
6.	8/7 - 08.	Konsultasi Bab Peren.	[signature]
7.	13/9 08.	Konsultasi Seminar Hasil	[signature]
8.	17/9 08.	Konsultasi seluruhnya.	[signature]
9.	22/9 08.	Pengecekan Kesiapan.	[signature]
10.			

Malang, 2005
Dosen Pembmbing
[signature] 20/9 08.

Ir. Sidik Noertjahjono, MT

Form. S-4a


1
2
3
4
D
C
B
A
9 V
BATTERY
SW
R A
10 K
10 K
POT1
R B
18 K
C
680 pF
100 nF
R
VCC
Q
TRIG
DIS
CVolt
GND
THR
555
4
8
3
2
7
5
6
1
A
4069
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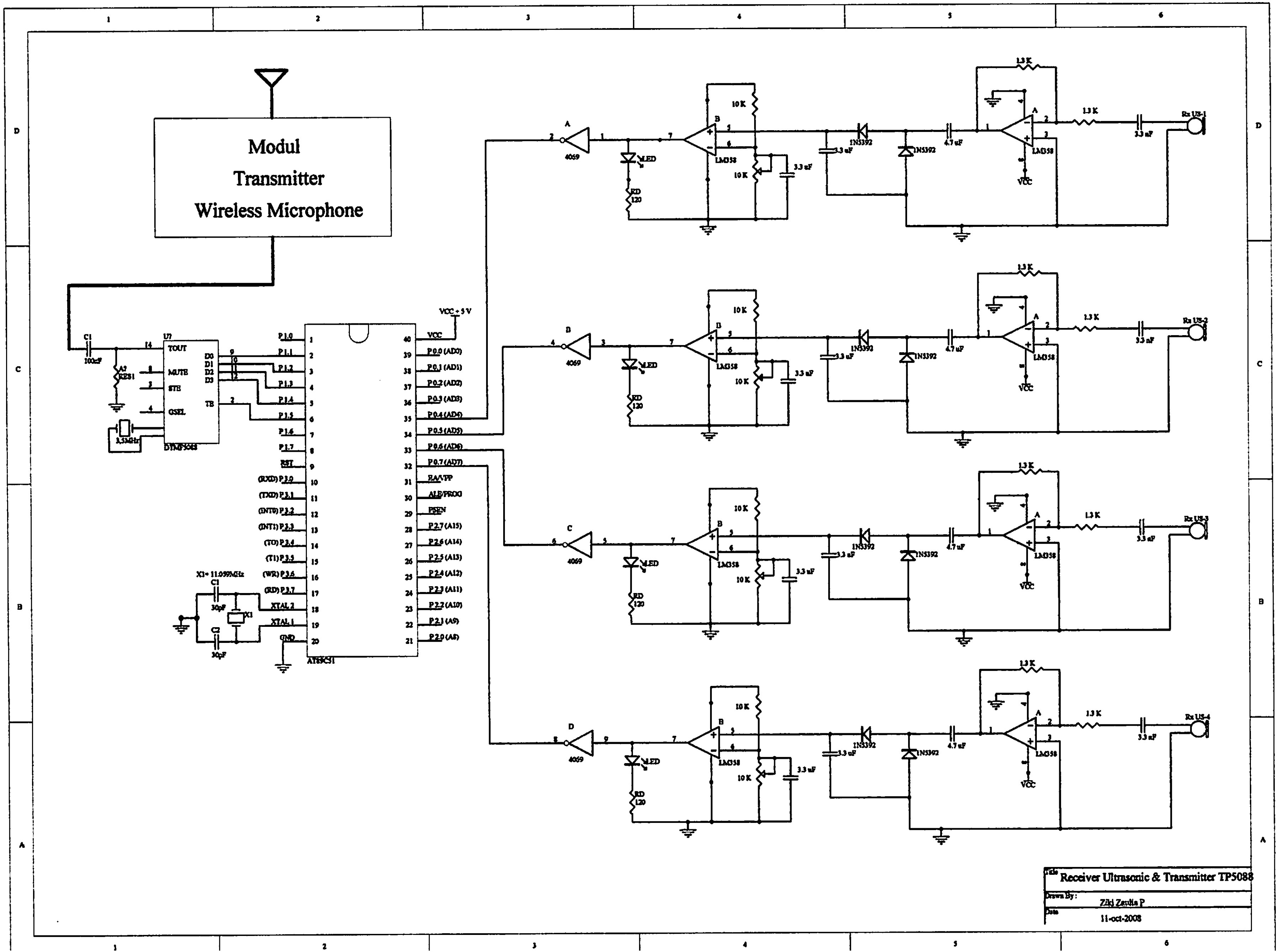
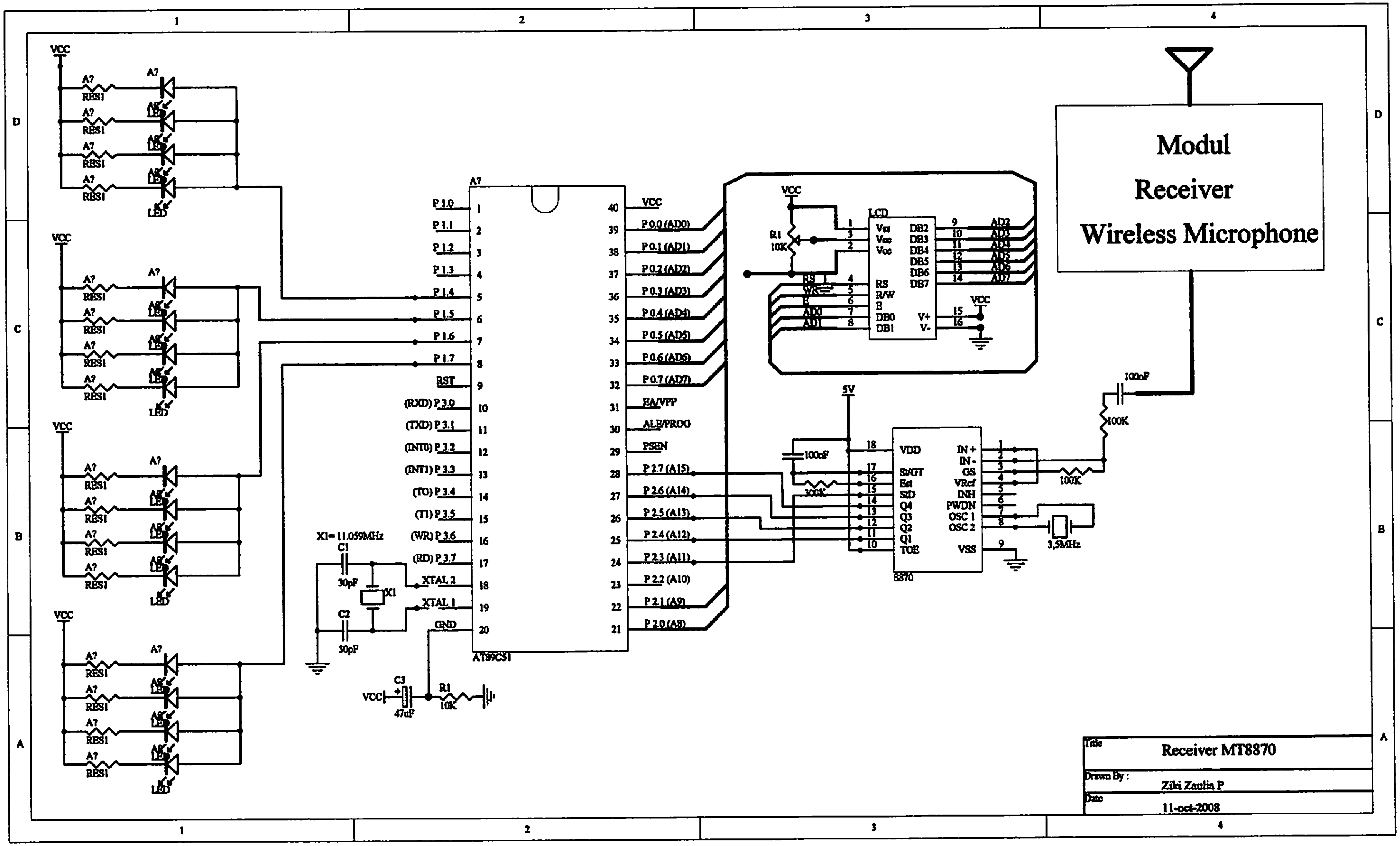
4069
1
2
3
4
5
6
9
8
11
10
220 nF
TX US
Transducer US
Title
Transmitter Ultrasonic
Drawn By :
Ziki Zaulia P
Date
11-oct-2008


Modul
Transmitter
Wireless Microphone
DTMF5088
AT89C51
VCC + 5 V
X1= 11.059MHz
30pF
3,58MHz
100nF
4069
LED
LM358
10 K
3.3 uF
4.7 uF
1N5392
1.3 K
3.3 nF
VCC
Rx US-1
Rx US-2
Rx US-3
Rx US-4
Receiver Ultrasonic & Transmitter TP5088
Drawn By :
Zikri Zaulia P
11-oct-2008


Modul
Receiver
Wireless Microphone
AT89C51
LCD
8870
X1= 11.059MHz
3,5MHz
VCC
5V
Title
Receiver MT8870
Drawn By :
Ziki Zaulia P
Date
11-oct-2008

Data Sheet

Ultrasonic transducers

RS stock numbers 307-351, 307-367

A range of two transducers operating at 40kHz approximately and designed for ultrasonic transmission and reception. The ultrasonic transmitter, 307-351 is capable of emitting 106dB (0dB = 2 × 10^{-4}μbar) and the receiver 307-367 has a sensitivity of –65dB (0dB = 1/μbar/V/metre).

These units can be used for the transmission of continuous wave ultrasonic sound or for pulsed sound applications

Characteristics

Item		Unit	307-351	307-367
Transmitting sensitivity	Sv	dB*1	106	-
Receiving sensitivity	Mv	dB*2	-	–65
Resonant frequency (transmitting)	Frsv	kHz*3	40±1	-
Resonant frequency (receiving)	Frmv	kHz*4	-	40±1
Directional angle	$\theta^1/_2$	°	20	
Maximum input voltage		Vrms	20	-
Impedance		Ω	Approx. 500	Approx. 30k
Capacitance		pF	1100±20%	
Pulse rise time		msec.	2.0	0.5
Maximum input voltage for pulse operation		Vp.p	60	-
Temperature range		°C	–20 to +60	
Transmitting selectivity	Qsv		Approx. 70	-
Receiving selectivity	Qmv			Approx. 60

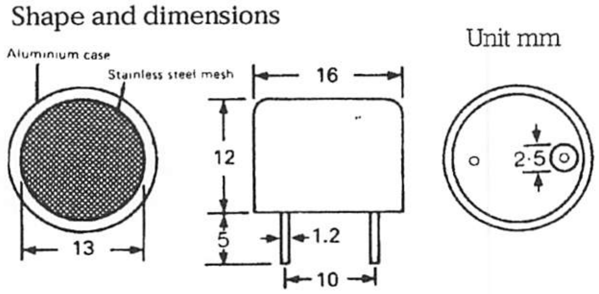
*1 0dB = 2 × 10^{-4}μbar

*2 0dB = 1V/μbar

*3 Frequency where transmitting sensitivity is maximum

*4 Frequency where receiving sensitivity is maximum

Shape and dimensions



Applications

Burglar alarm systems

Proximity switches

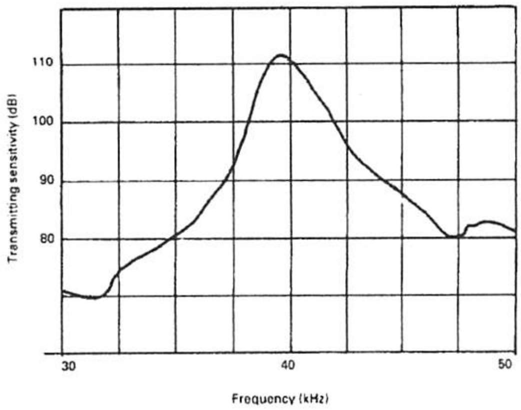
Liquid level meters

Anti-collision devices

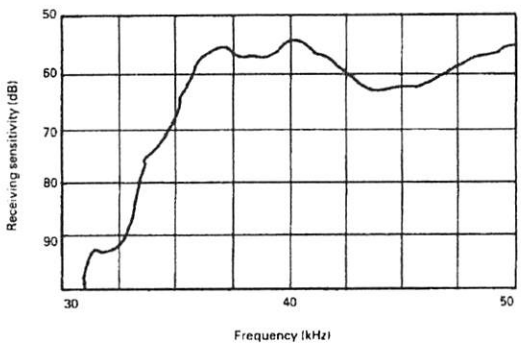
Counters for moving objects

TV remote control systems.

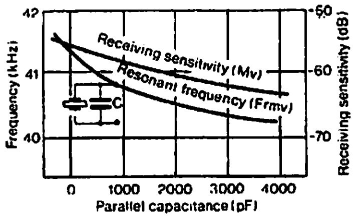
Frequency response (transmitting)



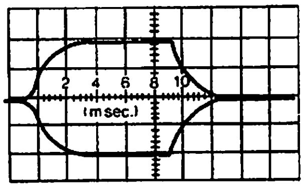
Frequency response (receiving)



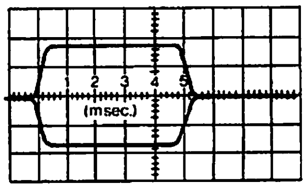
Effect of parallel capacitance



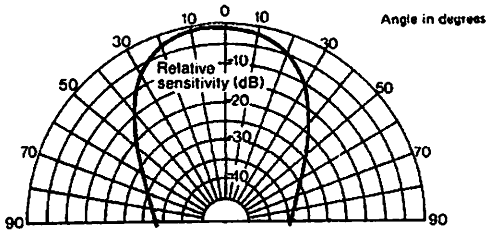
Pulse response (transmitting)



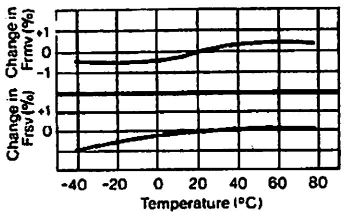
Pulse response (receiving)



Directional radiation pattern



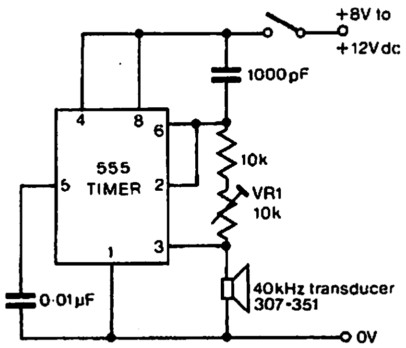
Temperature characteristics TRANSMITTER & RECEIVER



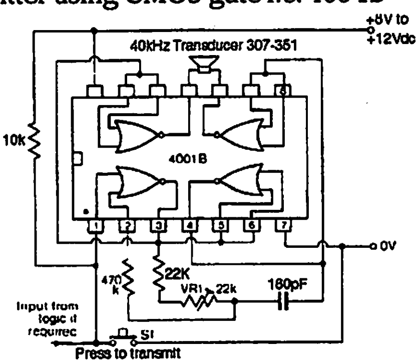
he following circuits show how the transducers may e used in remote control applications. Either of the ansmitter circuits may be used with the receiver. The equency of oscillation is adjusted by means of VR1 or maximum sensitivity. The CMOS circuit llows direct interfacing with logic circuitry. In the eceiver VR2 is adjusted for maximum sensitivity.

Note: The relay energises when a signal is received from the transmitter.

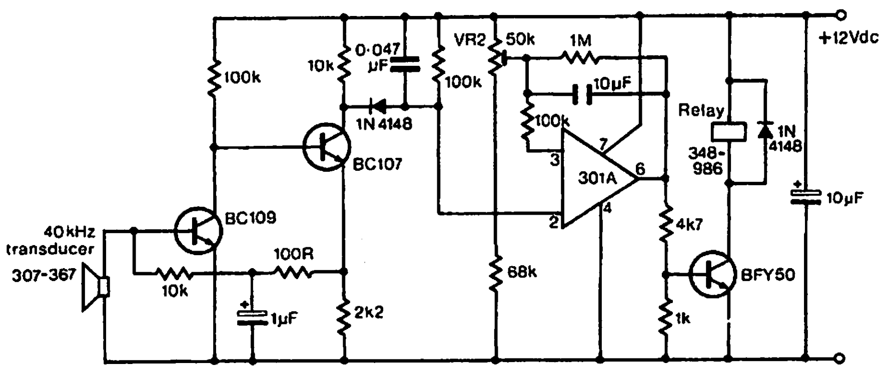
Transmitter using 555 timer i.c.



Transmitter using CMOS gate i.c. 400 1B



Receiver



RS Components, PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Company
Telephone: 01536 201234

National Semiconductor

October 1991

TP5088 DTMF Generator for Binary Data

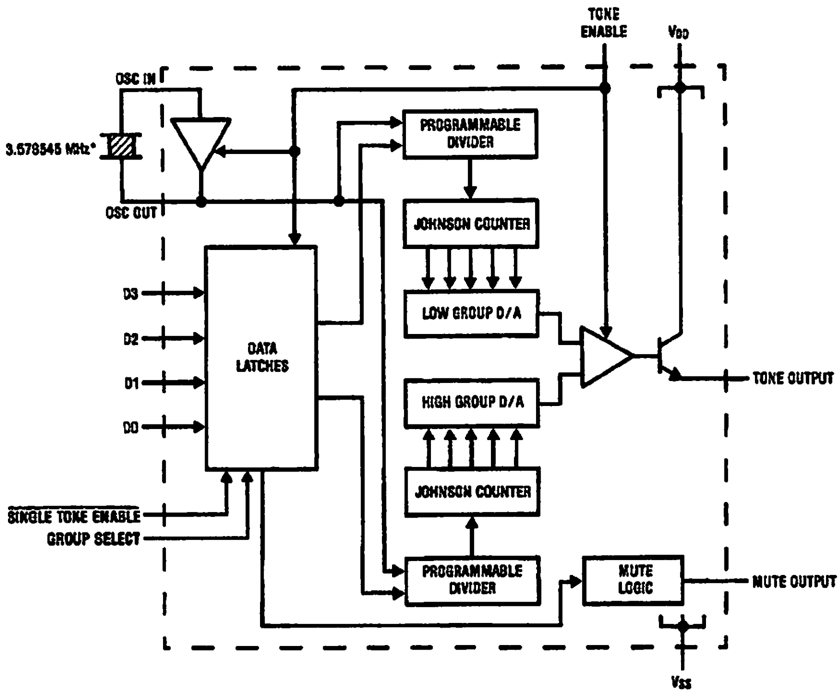
General Description

This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. 4-bit binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, data is latched into the device and the selected tone pair from the standard DTMF frequencies is generated. An open-drain N-channel transistor provides a MUTE output during tone generation.

Features

- Direct microprocessor interface
- Binary data inputs with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Better than 0.64% frequency accuracy
- High group pre-emphasis
- Low harmonic distortion
- MUTE output interfaces to speech network
- Low power idle mode
- 3.5V–8V operation

Block Diagram



TL/H/5004–1

*Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD}-V_{SS}$)	12V
$\overline{MUTE}$ Voltage	12V
Maximum Voltage at Any Other Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature, T_A	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics

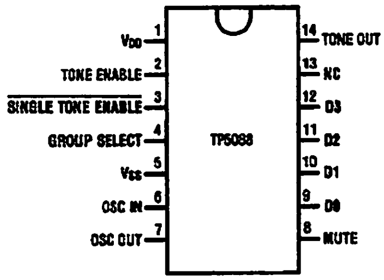
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 8V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage, V_{DD} (min)	Generating Tones	**3.5**			V
Minimum Supply Voltage for Data Input, TONE ENABLE and MUTE Logic Functions		2			V
Operating Current Idle Generating Tones	 R_L = ∞, D0–D3 Open V_{DD} = 3.5V, Mute Open		 55 1.5	 **350** **2.5**	 μA mA
Input Pull-Up Resistance D0–D3 TONE ENABLE			 100 50		 kΩ kΩ
Input Low Level TONE ENABLE, D0–D3				**0.2 V_{DD}**	V
Input High Level TONE ENABLE, D0–D3		**0.8 V_{DD}**			V
MUTE OUT Sink Current (TONE ENABLE LOW)	V_{DD} = 3.5V V_o = 0.5V	**0.4**			mA
MUTE OUT Leakage Current (TONE ENABLE HIGH)	V_{DD} = 3.5V V_o = V_{DD}		1		μA
Output Amplitudes Low Group High Group	R_L = 240 Ω V_{DD} = 3.5V T_A = 25°C	 **130** **180**	 170 230	 **220** **310**	 mVrms mVrms
Mean Output DC Offset	V_{DD} = 3.5V V_{DD} = 8V		1.2 3.6		V V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth, V_{DD} = 5V R_L = 240Ω	**−20**			dB
Start-Up Time (to 90% Amplitude), t_{OSC}			4		ms
Data Set-Up Time, t_S (*Figure 2*)	V_{DD} = 5V	100			ns
Data Hold Time, t_H	V_{DD} = 5V	280			ns
Data Duration t_W	V_{DD} = 5V	600			ns

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Connection Diagram

Dual-In-Line Package



TL/H/5004-2

Top View

Order Number TP5088WM or TP5088N
See NS Package M14B or N14A

Functional Description

With the TONE ENABLE pin pulled low, the device is in a low power idle mode, with the oscillator inhibited and the output transistor turned off. Data on inputs D0–D3 is ignored until a rising transition on TONE ENABLE. Data meeting the timing specifications is latched in, the oscillator and output stage are enabled, and tone generation begins. The decoded data sets the high group and low group programmable counters to the appropriate divide ratios. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}.

Table I shows the accuracies of the tone output frequencies and Table II is the Functional Truth Table.

TABLE I. Output Frequency Accuracy

Tone Group	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low	697	694.8	−0.32
Group	770	770.1	+0.02
f_L	852	852.4	+0.03
	941	940.0	−0.11
High	1209	1206.0	−0.24
Group	1336	1331.7	−0.32
f_H	1477	1486.5	+0.64
	1633	1639.0	+0.37

Pin Descriptions

V_{DD} (Pin 1): This is the positive supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is also connected to this pin.

V_{SS} (Pin 5): This is the negative voltage supply. All voltages are referenced to this pin.

OSC IN, OSC OUT (Pins 6 and 7): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 6 and 7. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator is stopped when the TONE ENABLE input is pulled to logic low.

TONE ENABLE Input (Pin 2): This input has an internal pull-up resistor. When TONE ENABLE is pulled to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on TONE ENABLE latches in data from D0–D3. The oscillator starts, and tone generation continues until TONE ENABLE is pulled low again.

MUTE (Pin 8): This output is an open-drain N-channel device that sinks current to V_{SS} when TONE ENABLE is low and no tones are being generated. The device turns off when TONE ENABLE is high.

D0, D1, D2, D3 (Pins 9, 10, 11, 12): These are the inputs for binary-coded data, which is latched in on the rising edge of TONE ENABLE. Data must meet the timing specifications of *Figure 2*. At all other times these inputs are ignored and may be multiplexed with other system functions.

TONE OUT (Pin 14): This output is the open emitter of an NPN transistor, the collector of which is connected internally to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group tones superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

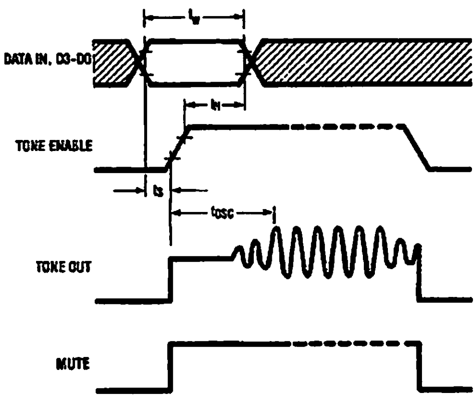
$\overline{\text{SINGLE TONE ENABLE}}$ (Pin 3): This input has an internal pull-up resistor. When pulled to V_{SS}, the device is in single tone mode and only a single tone will be generated at pin 14 (for testing purposes). For normal operation, leave this pin open-circuit or pull to V_{DD}.

GROUP SELECT (Pin 4): This pin is used to select the high group or low group frequency when the device is in single tone mode. It has an internal pull-up resistor. Leaving this pin open-circuit or pulling it to V_{DD} will generate the high group, while pulling to V_{SS} will generate the low group frequency at the TONE OUT pin.

TABLE II. Functional Truth Table

Keyboard Equivalent	Data Inputs				TONE ENABLE	TONES OUT		MUTE
	D3	D2	D1	D0		f_L (Hz)	f_H(Hz)	
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	_/‾	697	1209	O/C
2	0	0	1	0	_/‾	697	1336	O/C
3	0	0	1	1	_/‾	697	1477	O/C
4	0	1	0	0	_/‾	770	1209	O/C
5	0	1	0	1	_/‾	770	1336	O/C
6	0	1	1	0	_/‾	770	1477	O/C
7	0	1	1	1	_/‾	852	1209	O/C
8	1	0	0	0	_/‾	852	1336	O/C
9	1	0	0	1	_/‾	852	1477	O/C
0	1	0	1	0	_/‾	941	1336	O/C
*	1	0	1	1	_/‾	941	1209	O/C
#	1	1	0	0	_/‾	941	1477	O/C
A	1	1	0	1	_/‾	697	1633	O/C
B	1	1	1	0	_/‾	770	1633	O/C
C	1	1	1	1	_/‾	852	1633	O/C
D	0	0	0	0	_/‾	941	1633	O/C

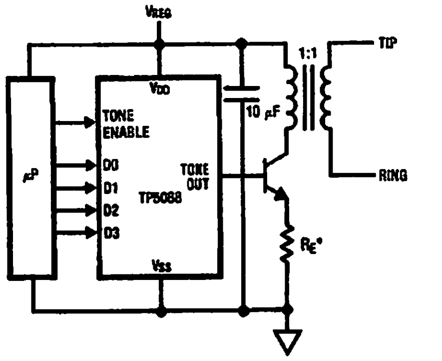
Timing Diagram



TL/H/5004-3

FIGURE 2

Typical Application

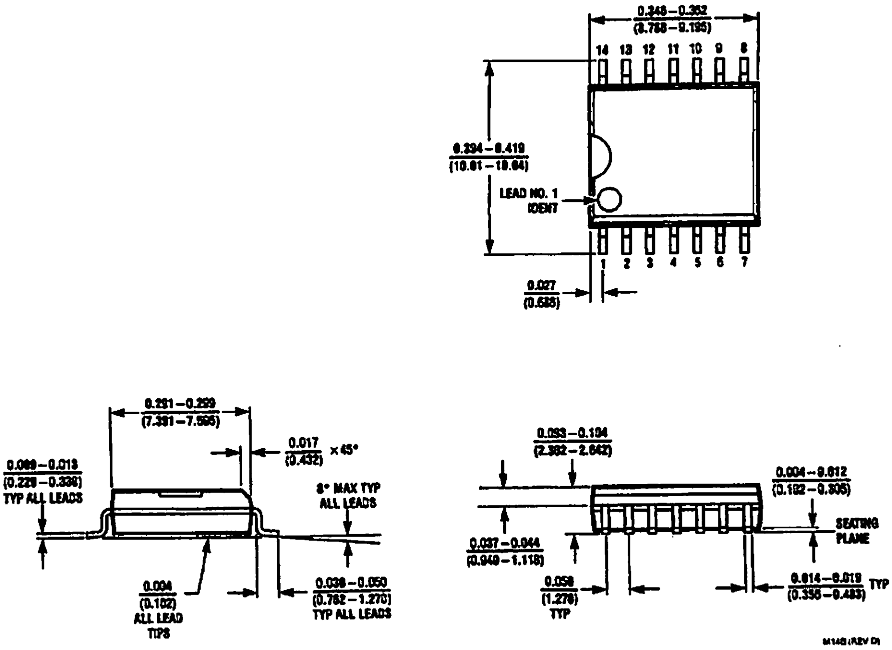


TL/H/5004-4

*Adjust R_E for desired tone amplitude.

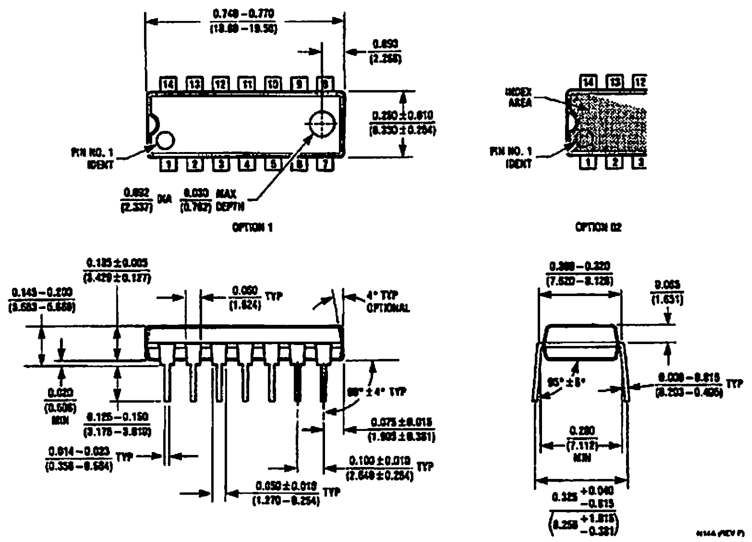
FIGURE 3

Physical Dimensions inches (millimeters)



Order Number TP5088WM
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line (N)
Order Number TP5088N
NS Package Number N14A

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Application Note **MSAN-108**

Applications of The MT8870 Integrated DTMF Receiver

MITEL®

ISSUE 1 June 1983

Contents

- DTMF Receiver Development
- Mobile Radio Applications
- Inside The MT8870
- Distributed Control Systems
- DTMF Receiver Application
- Data Communication Using DTMF

Introduction

The purpose of this Application Note is to provide information on the operation and application of DTMF Receivers. The MT8870 Integrated DTMF Receiver will be discussed in detail and its use illustrated in the application examples which follow.

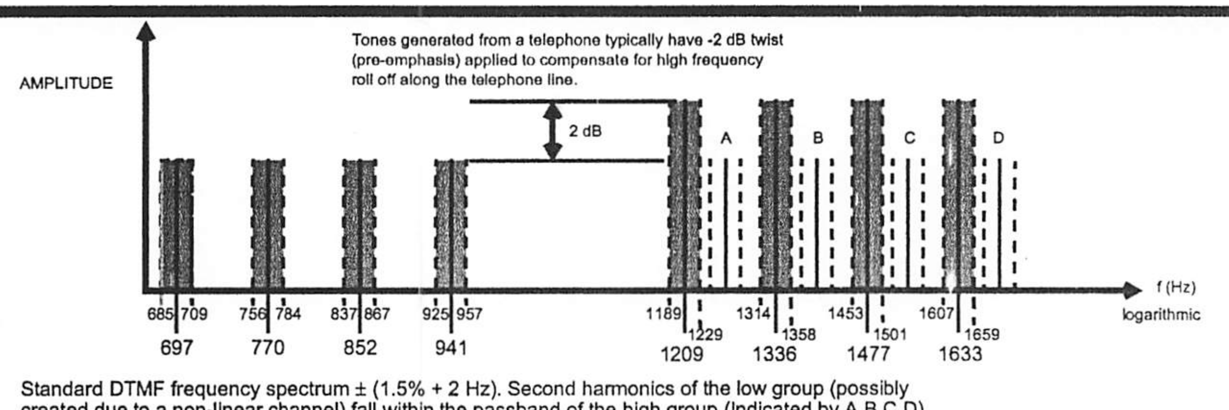
More than 25 years ago the need for an improved method for transferring dialling information through the telephone network was recognized. The traditional method, Dial pulse signalling, was not only slow, suffering severe distortion over long wire loops, but required a DC path through the communications channel. A signalling scheme was developed utilizing voice frequency tones and implemented as a very reliable alternative to pulse dialling. This scheme is known as DTMF (Dual Tone Multi-Frequency), Touch-Tone™ or simply, tone dialling. As its acronym suggests, a valid DTMF signal is the sum of two tones, one from a low group (697-941Hz) and one from a high group (1209-1633Hz) with each group containing four individual tones. The tone frequencies were carefully chosen such that they are not harmonically related and that their intermodulation products result in minimal signalling impairment (Fig. 1a). This scheme allows for 16 unique combinations. Ten of these codes represent the numerals zero through nine, the remaining six (*,#,A,B,C,D) being reserved for special signalling. Most telephone keypads contain ten numeric push buttons plus the asterisk (*) and octothorp (#). The buttons are arranged in a matrix, each selecting its low group tone from its respective row and its high group tone from its respective column (Fig. 1b).

The DTMF coding scheme ensures that each signal contains one and only one component from each of the high and low groups. This significantly simplifies decoding because the composite DTMF signal may be separated with bandpass filters, into its two single frequency components each of which may be handled individually. As a result DTMF coding has proven to provide a flexible signalling scheme of excellent reliability, hence motivating innovative and competitive decoder design.

Development

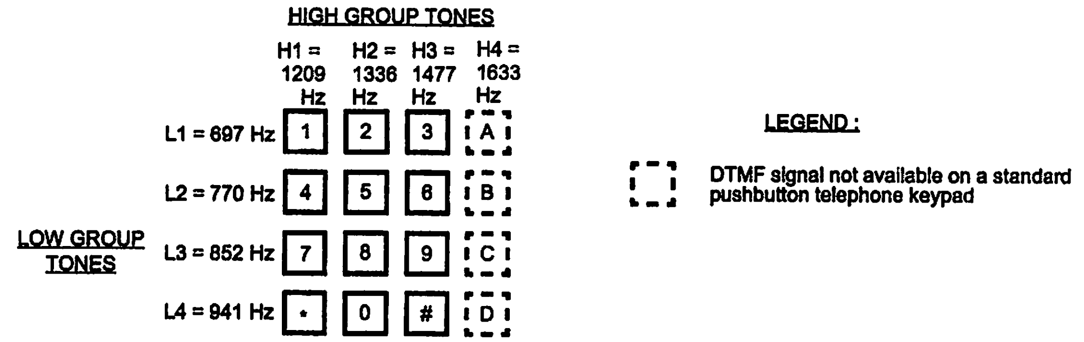
Early DTMF decoders (receivers) utilized banks of bandpass filters making them somewhat cumbersome and expensive to implement. This generally restricted their application to central offices (telephone exchanges).

The first generation receiver typically used LC filters, active filters and/or phase locked loop techniques to



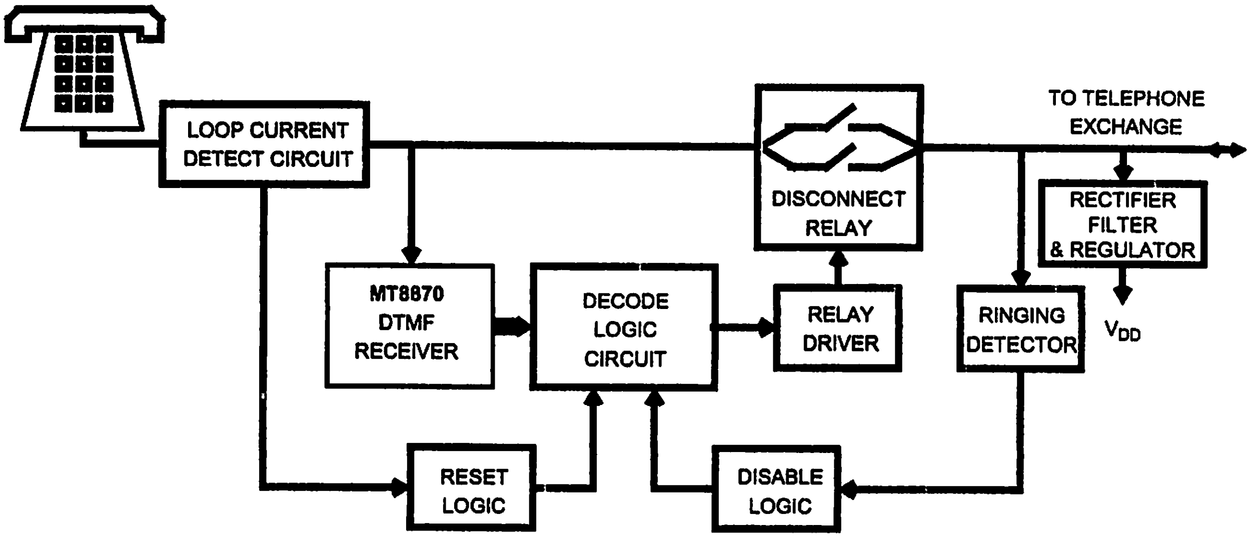
Standard DTMF frequency spectrum ± (1.5% + 2 Hz). Second harmonics of the low group (possibly created due to a non-linear channel) fall within the passband of the high group (Indicated by A,B,C,D). This is a potential source of interference.

Figure 1a - The Dual Tone Multifrequency (DTMF) Spectrum

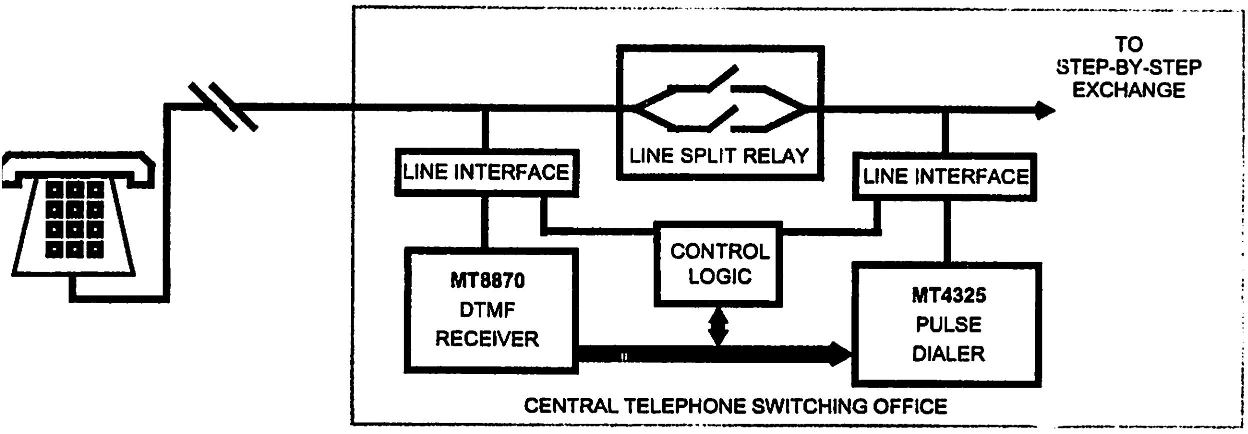


Telephone DTMF keypad matrix. Column H_4 is normally not available on a telephone keypad and is reserved for special signalling.

Figure 1b - The Dual Tone Multifrequency (DTMF) Keypad



a) Block diagram of a toll call restrictor. This could be implemented on a small pc board and installed in a telephone to disallow long distance calling.



b) Block diagram of a simple tome to pulse converter to allow TOUCH-TONE dialing into a step-by-step or crossbar exchange.

Figure 2 - Typical DTMF Receiver Applications

receive and decode DTMF tones. Initial functions were, commonly, phone number decoders and toll call restrictors. A DTMF receiver is also frequently used as a building block in a tone-to-pulse converter which allows Touch-Tone dialling access to mechanical step-by-step and crossbar exchanges (Fig. 2).

The introduction of MOS/LSI digital techniques brought about the second generation of tone receiver development. These devices were used to digitally decode the two discrete tones that result from decomposition of the composite signal. Two analog bandpass filters were used to perform the decomposition.

Totally self-contained receivers implemented in thick film hybrid technology depicted the start of third generation devices. Typically, they also used analog active filters to bandsplit the composite signal and MOS digital devices to decode the tones.

The development of silicon-implemented switched capacitor sampled filters marked the birth of the fourth and current generation of DTMF receiver technology. Initially single chip bandpass filters were combined with currently available decoders enabling a two chip receiver design. A further advance in integration has merged both functions onto a single chip allowing DTMF receivers to be realized in minimal space at a low cost.

The second and third generation technologies saw a tendency to shift complexity away from the analog circuitry towards the digital LSI circuitry in order to reduce the complexity of analog filters and their inherent problems. Now that the filters themselves can be implemented in silicon, the distribution of complexity becomes more a function of performance and silicon real estate.

Inside The MT8870

The MT8870 is a state of the art single chip DTMF receiver incorporating switched capacitor filter technology and an advanced digital counting/averaging algorithm for period measurement. The block diagram (Fig. 3) illustrates the internal workings of this device.

To aid design flexibility, the DTMF input signal is first buffered by an input op-amp which allows adjustment of gain and choice of input configuration. The input stage is followed by a low pass continuous RC active filter which performs an antialiasing function. Dial tone at 350 and 440Hz is then rejected by a third order switched capacitor notch filter. The signal, still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor and pass filters. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator.

The two resulting rectangular waves are applied to digital circuitry where a counting algorithm measures and averages their periods. An accurate reference clock is derived from an inexpensive external 3.58MHz colourburst crystal.

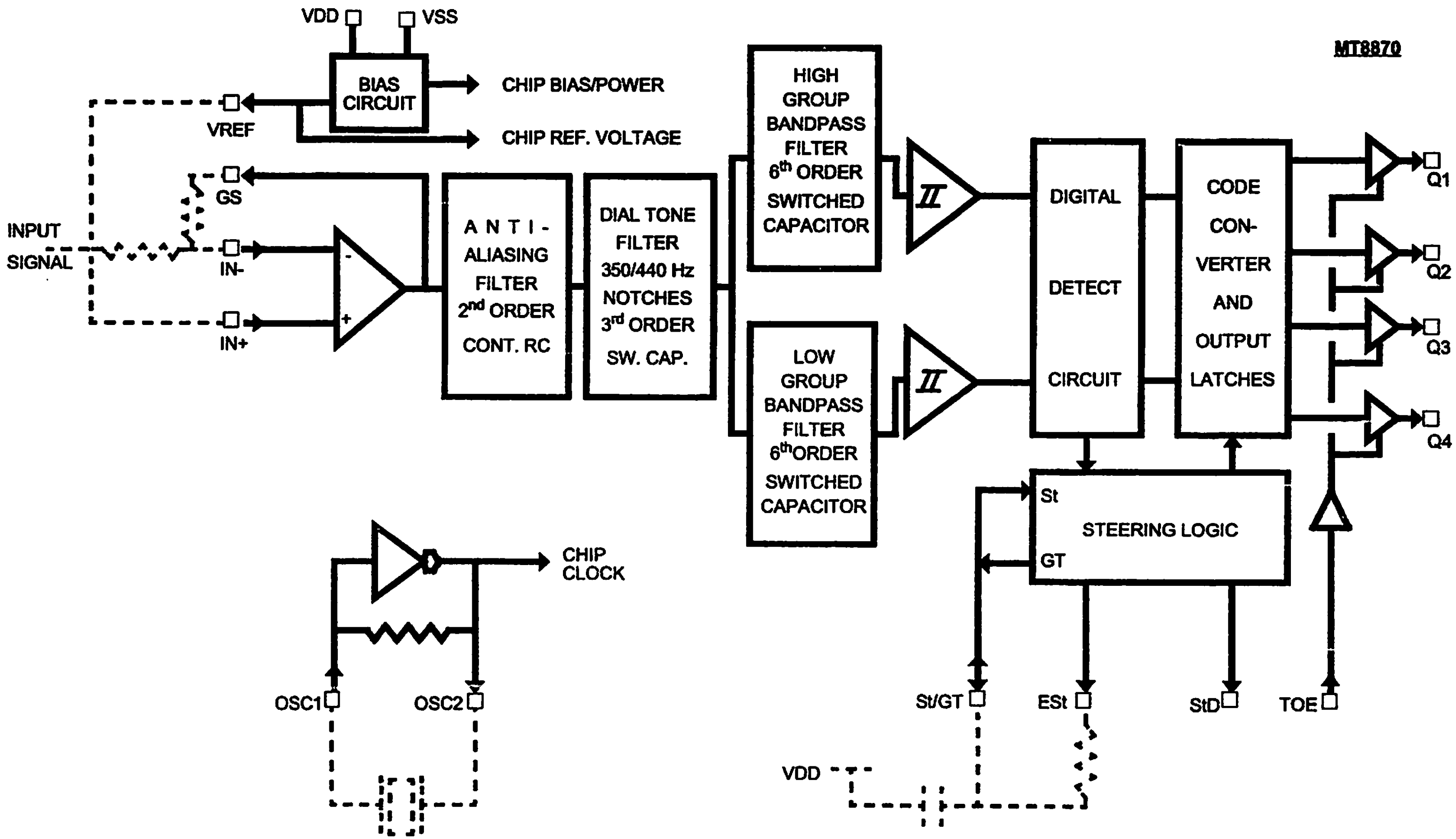
The timing diagram (Fig. 4) illustrates the sequence of events which follow digital detection of a DTMF tone pair. Upon recognition of a valid frequency from each tone group the Early Steering (ESt) output is raised. The time required to detect the presence of two valid tones, t_{DP} is a function of the decode algorithm, the tone frequency and the previous state of the decode logic. ESt indicates that two tones of proper frequency have been detected and initiates an RC timing circuit. If both tones are present for the minimum guard time, t_{GTP} which is determined by the external RC network, the DTMF signal is decoded and the resulting data (Table 1) is latched in the output register. The Delayed Steering (StD) output is raised and indicates that new data is available. The time required to receive a valid DTMF signal, t_{REC}, is equal to the sum of t_{DP} and t_{GTP}

f_{LOW}	f_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1209	0	1	1	0	1	0
941	1336	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0
-	-	ANY	0	Z	Z	Z	Z

Table 1. MT8870 Output Truth Table

0=LOGIC LOW 1=LOGIC HIGH Z :HIGH IMPEDANCE
Output truth table. Note that key "0" is output as "1010_2 (ie:10_{10})" corresponding to standard telephony coding.

A simplified circuit diagram (Fig. 5) illustrates how the chip's steering circuit drives the external RC network to generate guard times. Pin 17, St/GT (Steering/Guard Time), is a bidirectional signal pin which controls StD, the output latches, and resets the timing circuit. When St/GT is in its input mode (St function) both Q_1 and Q_2 are turned off and the voltage level at St/GT is compared to the steering threshold voltage V_{TSt}. A transition from below to above V_{TSt} will switch the comparator's output from



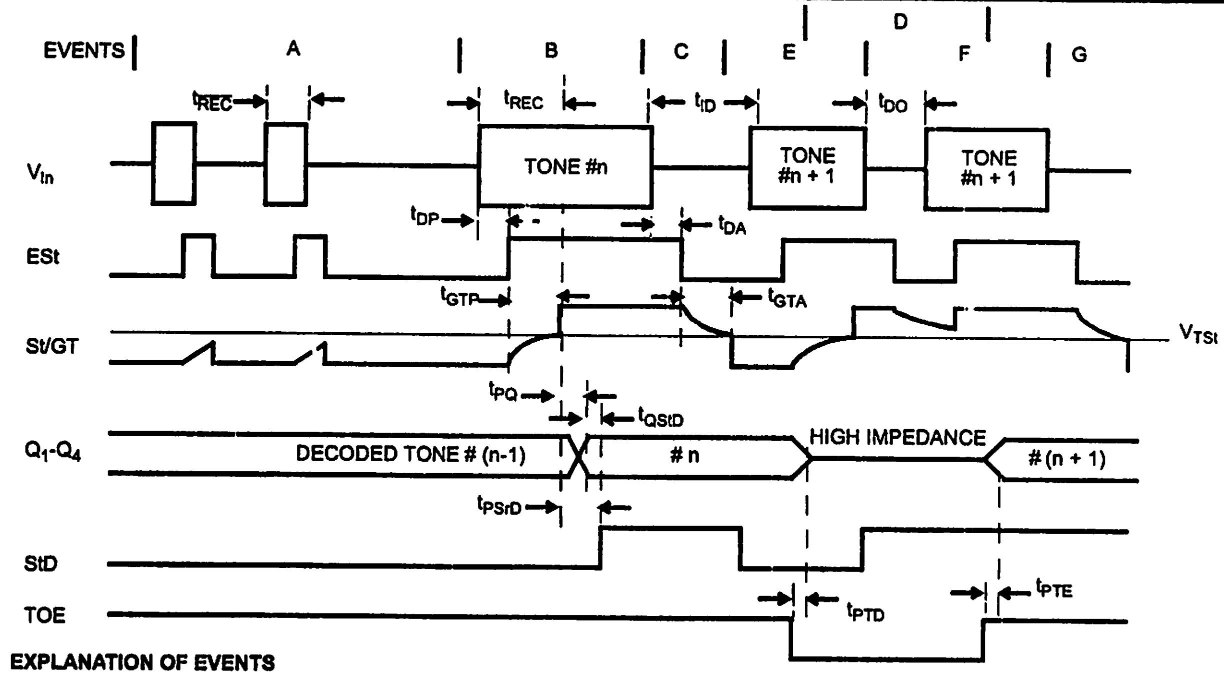
External guard time, input, and clock components (dashed) are included for clarity.

Figure 3 - MT8870 Functional Block Diagram

low to high strobing new data into the output latches, and raising the StD output. As long as an input level above V_{TSt} is maintained StD will remain high indicating the presence of a valid DTMF signal.

Initially, when no valid tone-pairs are present, capacitor C is fully charged applying a low voltage to St/GT. This causes a low at the comparator's output and since ESt is also low, Q_2 turns on ensuring that C is completely charged. In this condition St/GT is in its output mode (GT function). When a valid tone-pair is received ESt is raised turning off Q_2 which puts St/GT in its high impedance input mode and allows C to discharge through R. If this condition persists for the tone-present guard time, t_{GTP}, the voltage at St/GT rises above V_{TSt} raising StD which indicates reception of a valid DTMF signal. If the tone pair drops out before the duration of t_{GTP}, ESt is lowered turning on Q_2 which charges C resetting the tone-present guard time.

Once a DTMF signal is recognized as valid both ESt and the comparator output are high. This turns on Q_1 which discharges C and initializes the tone-absent guard time, t_{GTA}. After the DTMF signal is removed, ESt is lowered, Q_1 turns off placing St/GT in its input mode and C begins to charge through R.



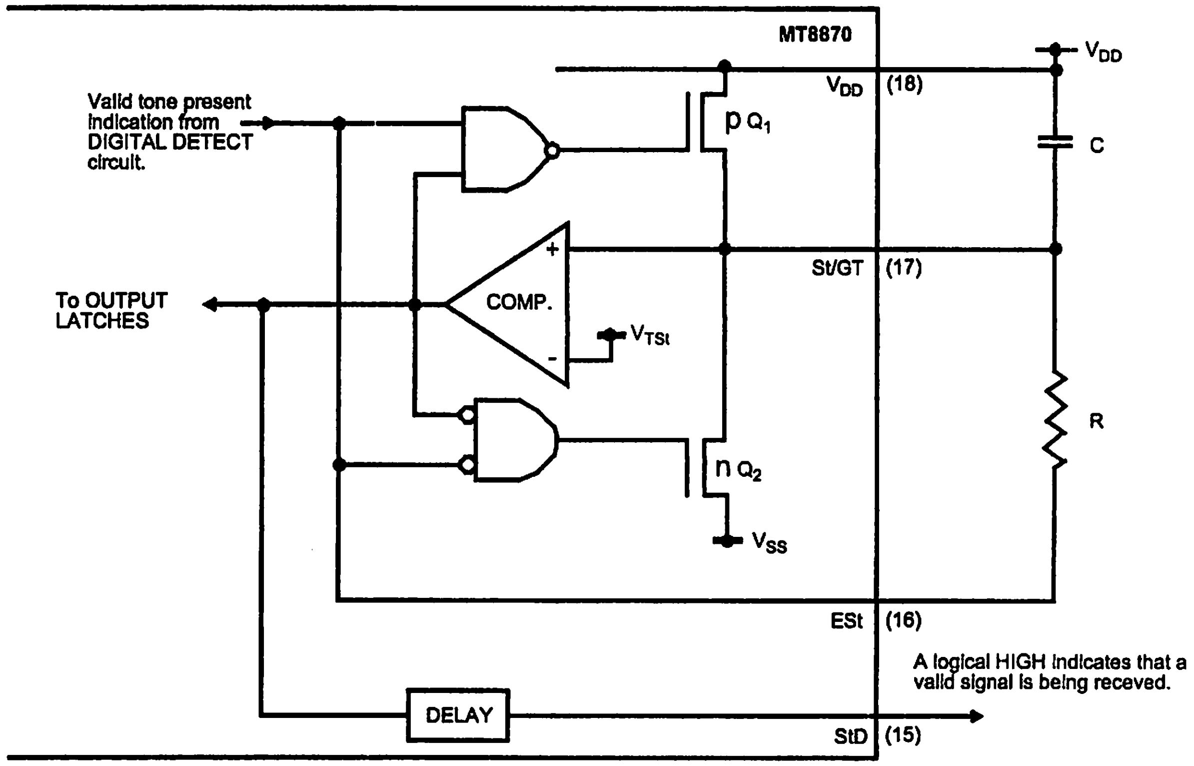
EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.
E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).
F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.
G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT.
StD	DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION
t_{ID}	MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.
t_{DA}	TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 4 - MT8870 Timing Diagram



Simplified steering circuit. Initially ESt is low, C is fully charged applying 0V to St/GT and Q_2 is on. Upon reception of a valid tone pair ESt is raised turning off Q_2 and allowing C to discharge through R which increases the voltae at St/GT. When VTSt is reached the comparator output goes high indicating a valid signal, latches the outputs and turns on Q_1 which discharges C. When the tone pair is lost ESt goes low Q_1 turns off and C charges through R decreasing the voltage at St/GT. When V_{TSt} is reached StD goes low and Q_2 turns on resetting the timing circuit.

STEERING TRUTH TABLE

ESt	St(/GT)	(St/)GT	StD
0	$<V_{TSt}$	0	0
0	$>V_{TSt}$	Z	1
1	$<V_{TSt}$	Z	0
1	$>V_{TSt}$	1	1

0 - LOGIC LOW
1 = LOGIC HIGH
Z = HIH IMPEDANCE
V_{TSt} = Threshold Voltqae (typically 1/2 V_{DD})

Steering circuit truth table. Note that pin 17 (St/GT) acts as both an input and an output depending on the relative states of ESt and the comparator output.

Figure 5 - MT8870 Steering And GuardTime Circuit Operation

the same valid tone-pair does not reappear before $_{TA}$ then the voltage at St/GT falls below V_{TSt} which esets the timing circuit via Q_2 and prepares the evice to receive another signal. If the same valid ne-pair reappears before t_{GTA}, ESt is raised turning n Q_1 and discharging C which resets t_{GTA}. In this ase StD remains high and the tone dropout is sregarded as noise.

) provide good reliability in a typical telephony nvironment, a DTMF receiver should be designed to cognize a valid tone-pair greater than 40mS in uration and, to accept as successive digits, tone-airs that are greater than 40mS apart. However in other environments, such as two-way radio, the optimum tone duration and intra-digit times may differ due to noise considerations.

By adding an extra resistor and steering diode (Fig. 6b, 6c) t_{GTP} and t_{GTA} can be set to different values. Guard time adjustment allows tailoring of noise immunity and talk-off performance to meet specific system needs.

Talk-off is a measure of errors that occur when the receiver falsely detects a tone pair due to speech or background noise simulating a DTMF signal. Increasing t_{GTP} improves talk off performance since

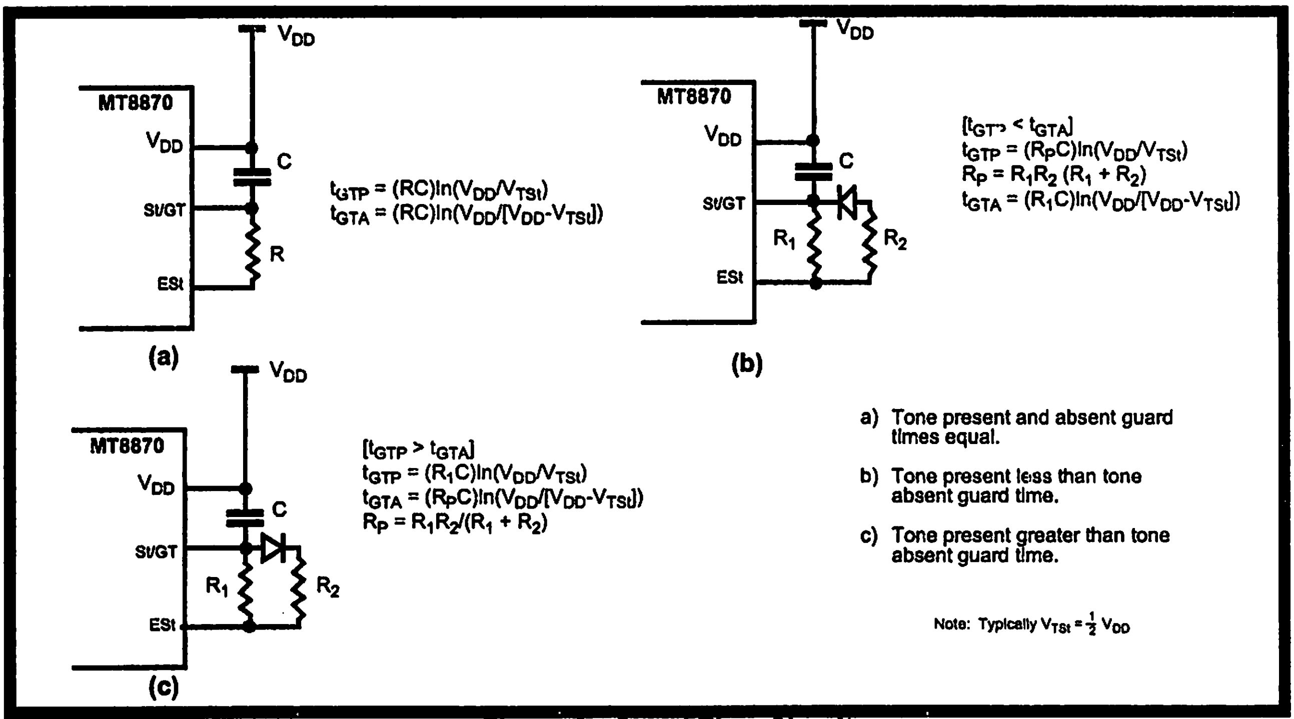


Figure 6 - Guard Time Circuits

it reduces the probability that speech will maintain DTMF simulation long enough to be considered valid. The trade-off here is decreased noise immunity because dropout (longer than t_{DA}) due to noise pulses will restart t_{GTP}. Therefore, for noisy environments, t_{GTP} should be decreased. The signal absent guard time, t_{GTA}, determines the minimum time allowed between successive DTMF signals. A dropout shorter than t_{GTA} will be considered noise and will not register as a successive valid tone detection. This guards against multiple reception of a single character. Therefore, lengthening t_{GTA} will increase noise immunity and tolerance to the presence of an unwanted third tone at the expense of decreasing the maximum signalling rate.

The intricacies of the digital detection algorithm have a significant impact on the overall receiver performance. It is here that the initial decision is made to accept the signal as valid or reject it as speech or noise.

Trade-offs must be made between eliminating talk off errors and eliminating the effects of unwanted third tone signals and noise. These are mutually conflicting events. On one hand valid DTMF signals present in noise must be recognized which requires relaxation of the detection criteria. On the other hand, relaxing the detection criteria increases the probability of receiving "hits" due to talk off errors.

Many considerations must be taken into account in evaluating criteria for noise rejection. In the telephony environment two sources of noise are predominant. These are, third tone interference, which generally comes from dial tone harmonics, and band-limited white noise . In the MT8870 a complex digital averaging algorithm provides excellent immunity to voice, third tone and noise signals which prevail in a typical voice bandwidth channel.

The algorithm used in the MT8870 combines the best features from two previous generations of Mitel digital decoders with improvements resulting from years of practical use within the telephone environment. The algorithm has evolved through a combination of statistical calculations and empirical "tweaks" to result in the realization of an extremely reliable decoder.

Applications

The proven reliability of DTMF signalling has created a vast spectrum of possible applications. Until recently, many of these applications were rendered ineffective due to cost or size considerations. Now that a complete DTMF receiver can be designed with merely a single chip and a few external passive components one can take full advantage of a highly developed signalling scheme as a small, cost-effective signalling solution.

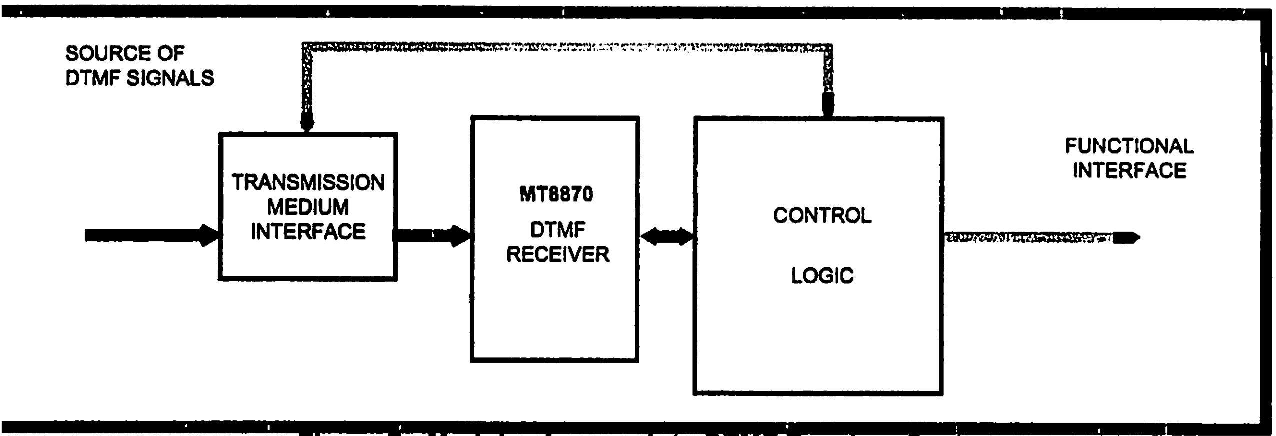


Figure 7 - Modular Approach to DTMF Receiver Systems

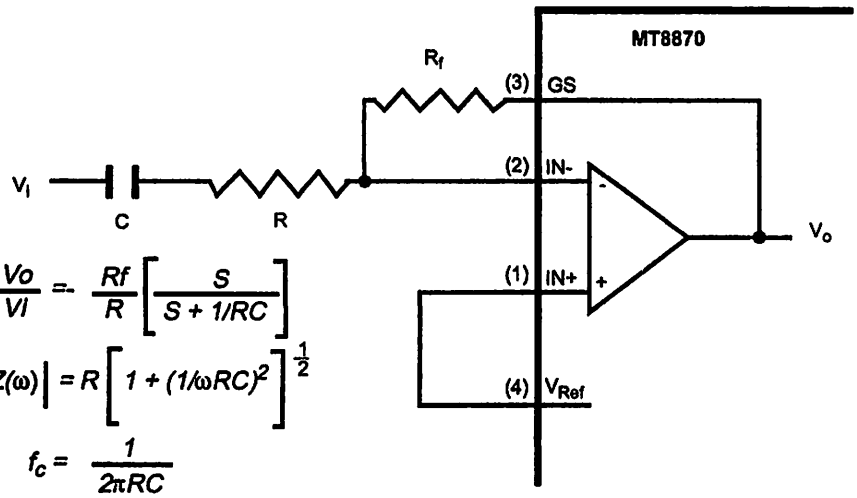
'he design of a DTMF receiving system can enerally be broken down into three functional locks (Fig. 7). The first consideration is the iterface to the transmission medium. This may be s simple as a few passive components to dequately configure the MT8870's input stage or as omplex as some form of demodulation, multiplexing r analog switching system. The second functional lock is the DTMF receiver itself. This is where the eceiving system's parameters can be optimized for ie specific signal conditions delivered from the ront end" interface. The third, and perhaps most idely varying function, is the output control logic. 'his may be as simple as a 4 to 16 line decoder, ontrolling a specific function for each DTMF code, r as complex as a full blown computer handling ystem protocols and adaptively varying the tone eceiver's parameters to adjust for changing signal onditions. Several currently applied and onceptually designed applications are described ubsequently but first let's consider the design of a ypical input stage.

The input arrangement of the MT8870 provides a differential input op amp as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail. The output of this op amp is available to provide feedback for gain adjustment.

A typical single ended input configuration having unity gain is shown in Figure 8.

For balanced line applications good common mode rejection is offered by the differential configuration (Fig. 9). In both cases, the inputs are biased to 1/2 V_{DD} by V_{Ref}. Consider an input stage which will interface to a 600Ω balanced line. To reject common mode noise signals, a balanced differential amplifier input provides the solution.

With the input configured for unity gain the MT8870 will accept maximum signal levels of +1 dBm (into 600Ω). The lowest DTMF frequency that must be detected is approximately 685Hz. Allowing 0.1dB of



Voltage Gain; $AV = \frac{Vo}{VI} = -\frac{Rf}{R}\left[\frac{S}{S + 1/RC}\right]$

Input Impedance; $\left|Z(\omega)\right| = R\left[1 + (1/\omega RC)^2\right]^{\frac{1}{2}}$

3dB Cutoff Frequency; $f_c = \frac{1}{2\pi RC}$

Figure 8 - Single Ended Input Configuration

attenuation at 685Hz, the required input time constant may be derived from;

$$M(\omega)_{dB} = 20\ log_{10}\frac{R_f}{R} + 20\ log_{10}\frac{\omega\tau}{\left\{(\omega\tau)^2+1\right\}^{1/2}}$$

where $M(\omega)_{dB}$ *is the amplifier gain in decibels*

ω *is the radian frequency*

τ *is the input time constant*

$$Therefore\quad -0.1 = 20\ log_{10}\frac{(2\pi)685\tau}{\left\{[(2\pi)685\tau]^2+1\right\}^{1/2}}$$

$$or\ \tau = 1.52mS$$

Now, choosing R=220K gives a high input impedance (440K in the passband) and C= τ/R=6.9nF (use a standard value of 10 nF). For unity gain in the passband we choose R_f=R. R_a and R_b are biasing resistors. The choice of R_a is not critical and could be set at, say... 68K. Bias resistor R_a adds a zero to the non-inverting path through the differential amplifier but has no affect on the inverting path. This zero can be exactly cancelled by the added pole due to R_b if R_b is chosen as;

$$R_b = \frac{R_aR_f}{R_a+R_f}\ .$$

With appropriate input transient protection, this circuit will provide an excellent bridging interface across a properly terminated telephone line for end-to-end or key system applications. Transient protection may be achieved by splitting the input resistors and inserting zener diodes to achieve voltage clamping (Fig. 10). This allows the transient energy to be dissipated in the resistors and diodes and limits the maximum voltage that may appear at the op-amp inputs.

It is important to consider the amount of shunt capacitance introduced by the protection devices. In this case the parasitic capacitances of the zener diodes are in series which reduces their effect. Relatively large shunt capacitances will attenuate the high group frequencies causing the input signal to "twist" which degrades receiver performance.

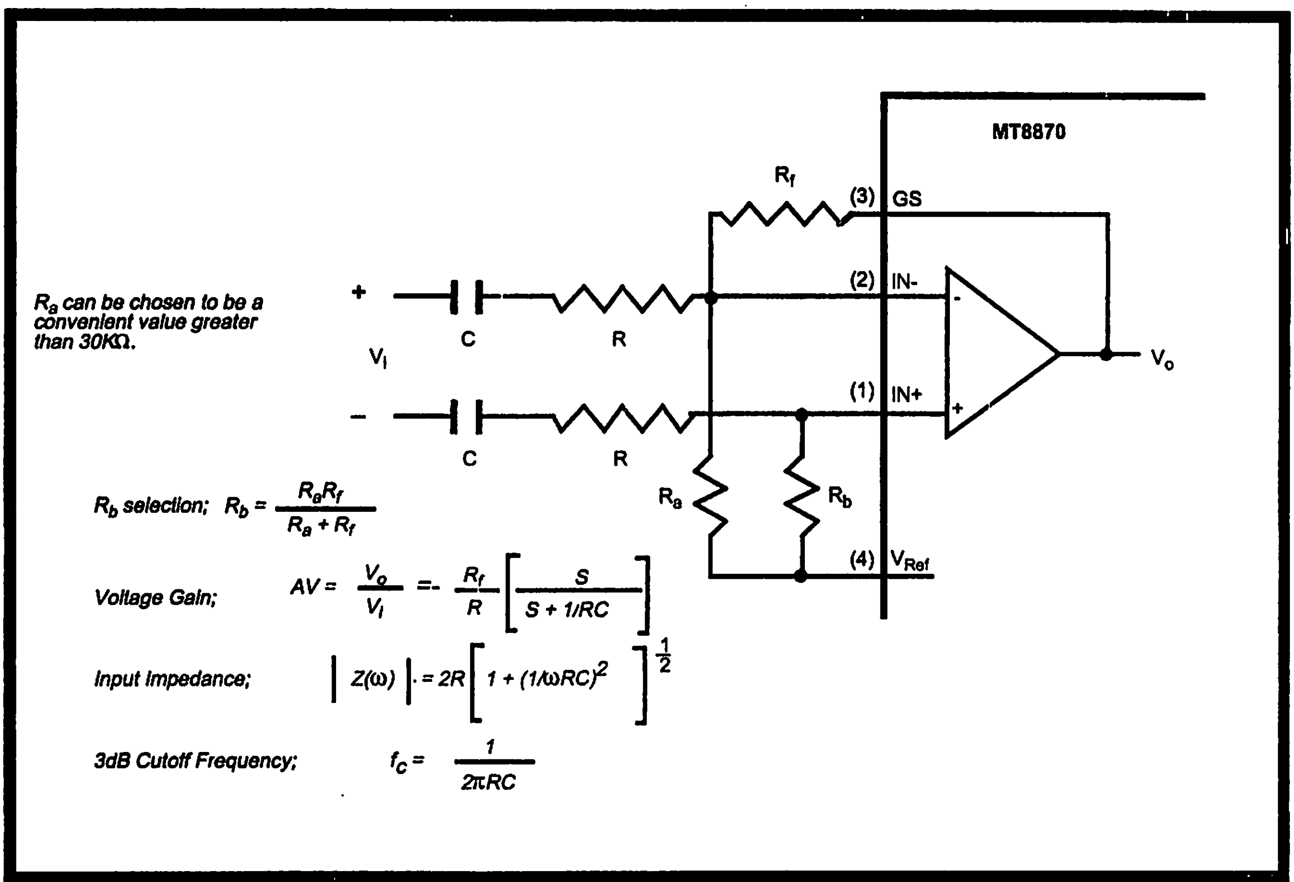


Figure 9 - Differential Input Configuration

Twist" is known as the difference in amplitude)etween the low and high group tones. It is specified n dB as:

$$TWIST = 20log_{10}\frac{V_L}{V_H}$$

where V_L is the amplitude of the low frequency tone

and V_H is the amplitude of the high frequency tone.

Twist is usually caused by the frequency response :haracteristic of the communication channel. Along a elephone line higher frequencies tend to roll off aster than the lower ones so the line response is ısually compensated for by applying pre-emphasis negative twist) to the originating DTMF signal. In ıxtreme cases the receiver may require ompensation. This could be realized with a filter ırrangement utilizing the input op amp.

ıny communication path that can pass the human oice spectrum is eligible for DTMF signalling. 'herefore a variety of "front-end" interfaces may be ıpplicable in a given control system. More ommonly used media are copper wire and RF hannels. An optical fibre could carry a light beam ıodulated by DTMF. Although this would incur a ırge overhead in terms of bandwidth utilization, ıptical fibres do offer isolation from external electro-ıagnetic interference. For example, if control or lata signals must be sent near a high power ·ansmission line environment, strong electric and ıagnetic fields could have a devastating effect on ignals transmitted over wires. DTMF over fibre-optics could easily be employed as a highly reliable communications method in a harsh interference infested environment.

In modern digital switching equipment the MT8870 can easily be interfaced to a digital PCM line by using a codec as an input interface (Fig. 11). Actually, all that is required for the interface is a PCM decoder. In fact, the output filter that normally is associated with PCM decoders is not required since the high group DTMF bandpass filter has an upper cutoff frequency low enough to meet the required roll-off of the PCM filter.

DTMF In Mobile Radio Applications

DTMF signalling plays an important role in distributed communications systems, such as multi-user mobile radio (Fig. 12). It is a "natural" in the two-way radio environment since it slips neatly into the center of the voice spectrum, has excellent noise immunity and highly integrated methods of implementation are currently available. It is also directly compatible with telephone signalling, simplifying automatic phone patch systems.

Several emergency medical service networks currently use DTMF signals to control radio repeaters. Functions are, typically, mobile identification, selection of appropriate repeater links, selection of repeater frequencies, reading of repeater status, and for completing automatic phone patch links.

If available in a system of this type, audio from a long distance communications link (microwave,

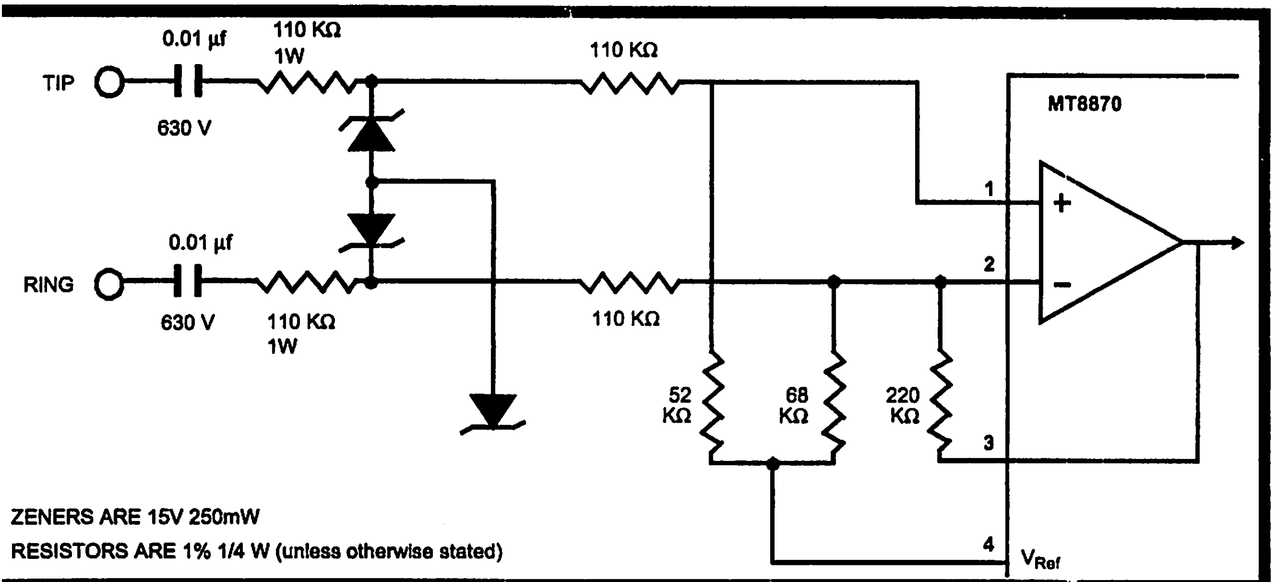


Figure 10 - MT8870 Front End Protection Circuit

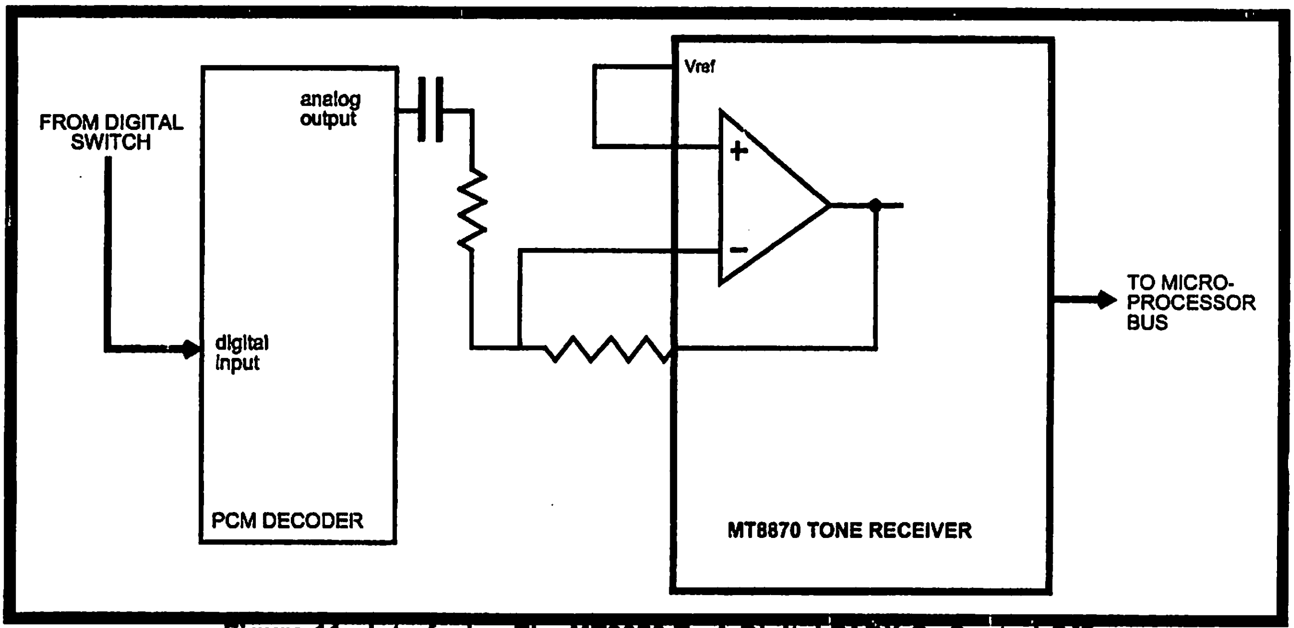


Figure 11 - Interfacing The MT8870 To A Digital PABX Or Central Office

satellite, etc.) could be switched, via commands from the user's DTMF keypad, into the local repeater. This would offer the mobile user a variety of paths for communication without the assistance of a human operator.

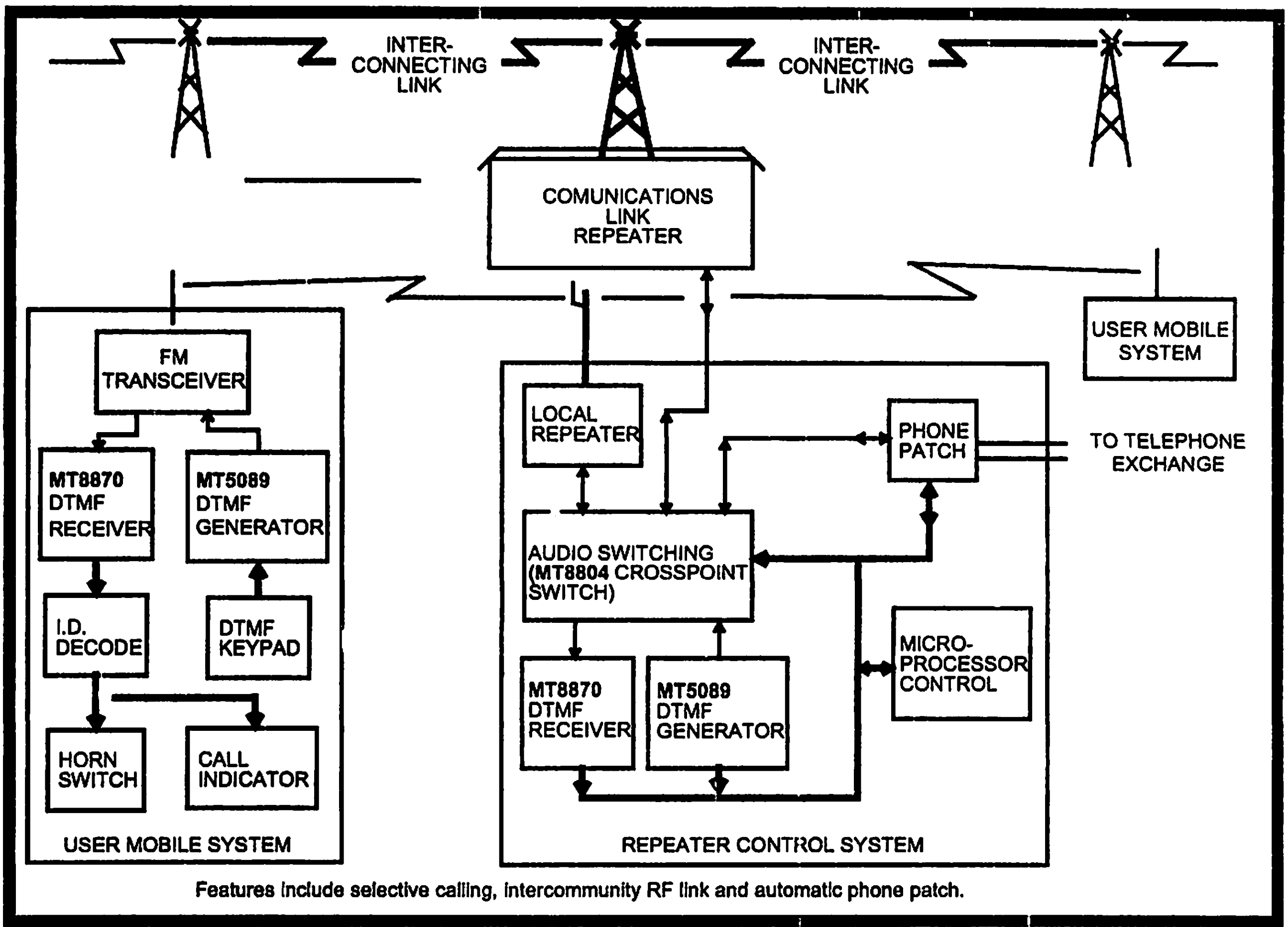


Figure 12 - DTMF Controlled Radio Repeater

multi-channel repeater system serving a multitude user groups may be found to achieve its most fective performance in the "trunked" mode. In this ise, one RF channel is reserved for system gnalling. System operation could be achieved as llows.

ich mobile plus the repeater system contain a TMF receiver, DTMF generator and appropriate introl logic. Mobiles are assigned individual DTMF). codes and always monitor the signalling channel hen idle. An originating mobile automatically sends DTMF sequence containing its own I.D. and the). of the called party. This is recognized by the peater control which retransmits the called party's). The answering mobile returns a DTMF indshake indicating to the repeater control that it is ailable to accept a call. At this time the repeater introl sends a DTMF command sequence to both e originating and answering mobiles which structs their logic circuits to switch to a specific, ailable channel. If all channels are busy the peater control could send DTMF sequences to put oth mobiles on "hold" and add their I.D.'s to a hannel-request" queue. This arrangement would allow users to access any available frequency and converse privately instead of being restricted to one assigned channel which is shared among several user groups.

As well as an individual I.D., each mobile belonging to a particular organization could also have a common group I.D. This would allow dispatch messages to be sent to all company mobiles simultaneously. Since mobiles would be under DTMF control, messages could be sent to an unattended vehicle and, at the user's convenience, displayed on a readout .

Each radio link either established or attempted would result in DTMF I.D. codes being sent to the repeater control. These occurrences could easily be collected by a computer for statistical analysis or billing information. Customers who have defaulted on rental payments could be denied access to the system.

Simplified block diagrams of the control systems for both the repeater and mobiles are shown in Figures 13 and 14 respectively.

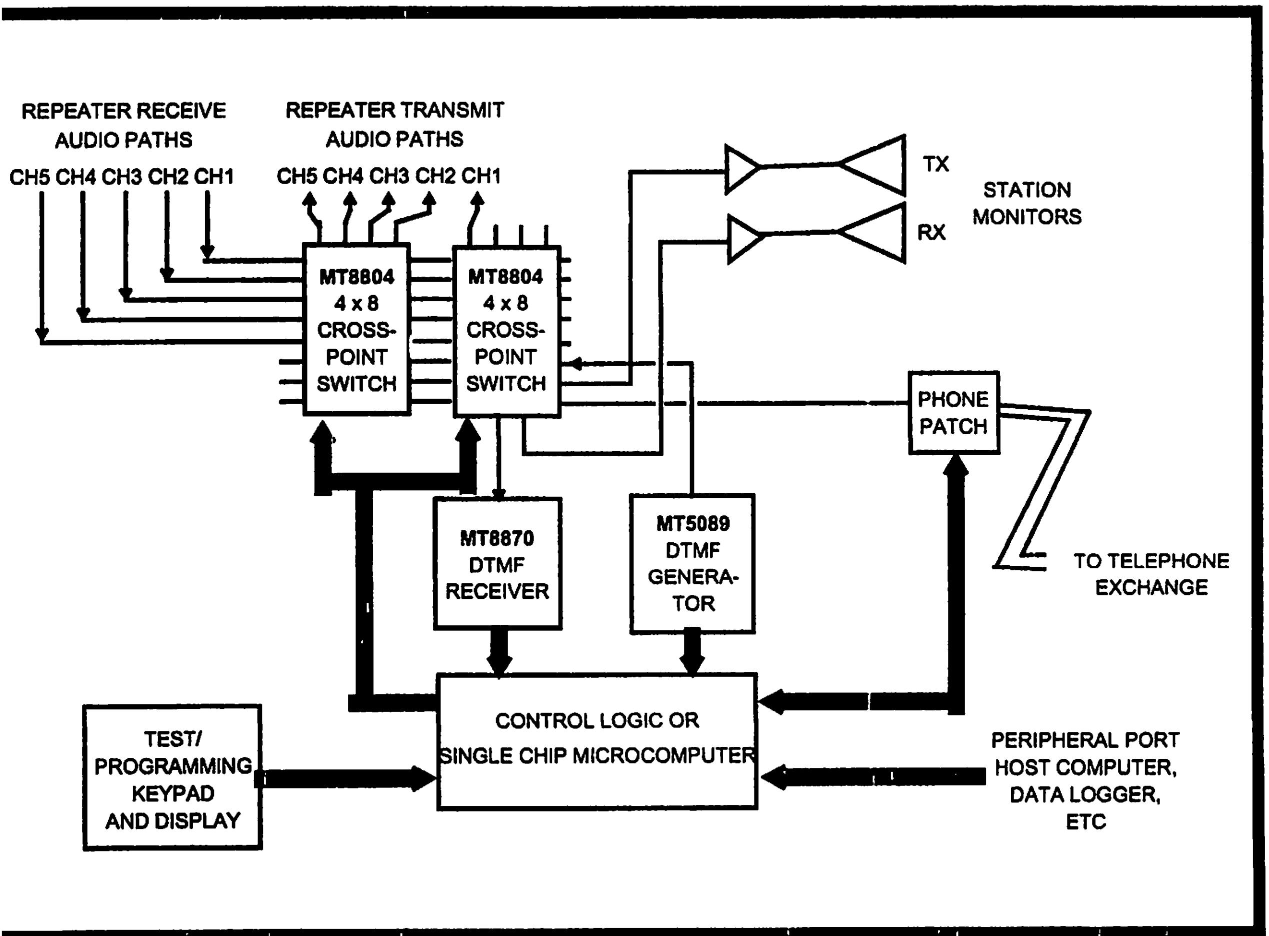


Figure 13 - Block Diagram of Control for "Trunked" Repeater System"

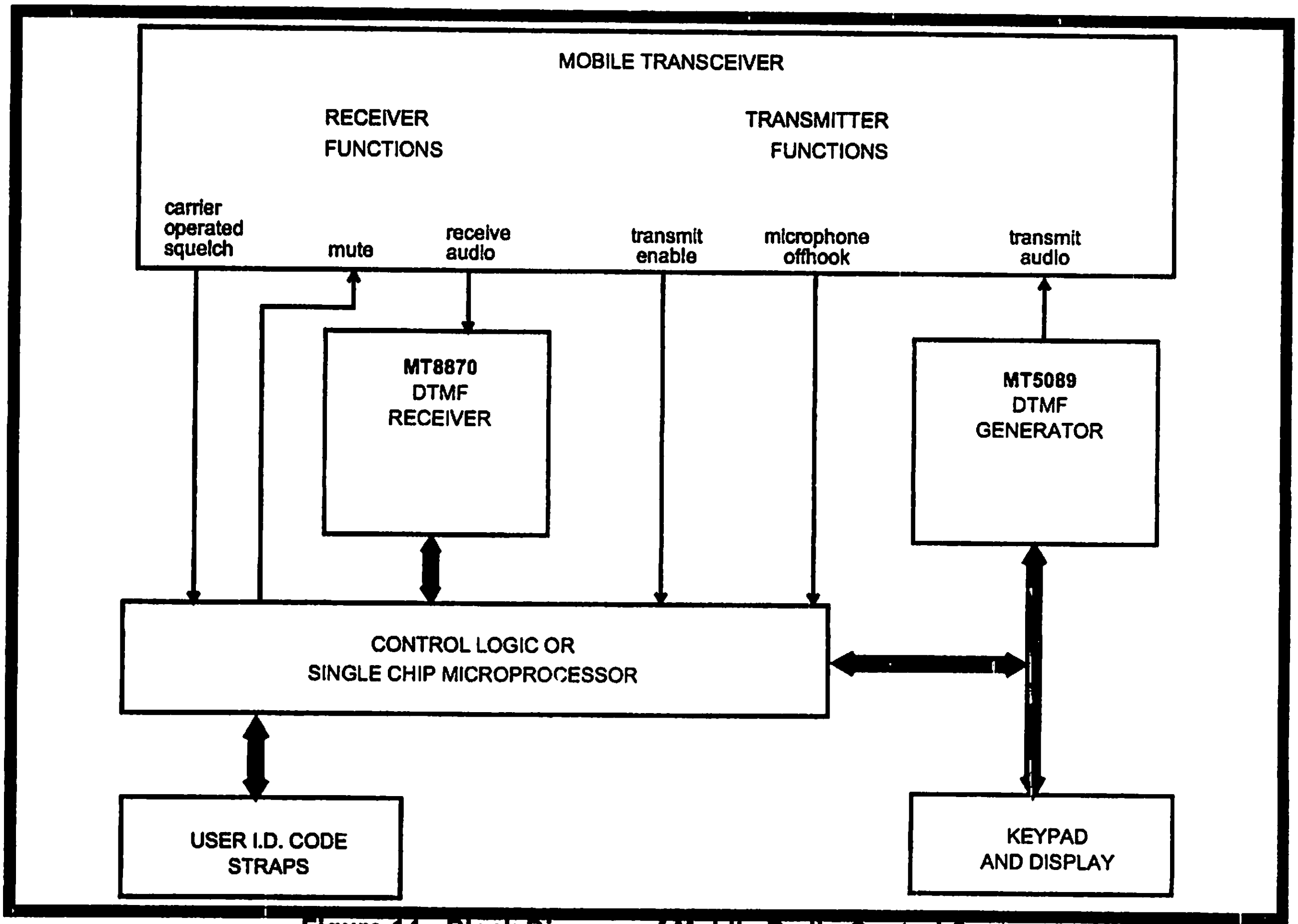


Figure 14 - Block Diagram of Mobile Radio Control System

Distributed Control Systems

There are many other applications which also fall into the distributed communications/control class. That is, several devices being controlled via a common communications medium whether it be RF, copper wire or optical fibres, etc.

Consider, for example, an existing pair of wires circulating throughout a plant. By connecting DTMF receivers at strategic points along this path one could conceivably control the whole plant from a single DTMF transmitter (Fig. 15). Each DTMF receiver would monitor the common line until its specific I.D. was received, at which time it would transfer data to its functional control logic.

With some simple logic a circuit can be devised to recognize a sequence of programmed DTMF code. Figure 16 illustrates a method of detecting a DTMF code sequence of arbitrary length, N. The object is to compare N sequential 4-bit DTMF data words to N preprogrammed 4-bit I.D. words. Programming the I.D. code is accomplished by applying the desired logic levels to the inputs of N 4-bit bus buffers. This may be achieved with straps as shown, dipswitches or thumbwheels. Pull-up resistors should be applied to the buffer inputs. Initially, after a RESET has occurred, Q_0 of the presettable shift register is set logically high, the remaining outputs are reset. This activates the first bus buffer which applies its outputs to the Y inputs of a 4-bit comparator.The "LAST DIGIT" latch is reset, the "ERROR-" flip-flop and "VALID DIGIT" latch are set. These three signals are ANDed indicating a "no-match" condition. When a valid DTMF signal is received its data appears at the comparators "X" inputs, a comparison occurs and the result appears at the "X=Y" output. After 3.4 µS (typical) Std rises indicating that the MT8870 output data is valid and strobes "X=Y" into the "VALID DIGIT" latch. The shift register advances one position which enables the next bus buffer. If the result of the comparison was true then the "VALID DIGIT" output is high. If all digits of the sequence match then the high output from the shift register "wraps around" from Q_{N-1} to Q_0, which strobes the "LAST DIGIT" latch high. This activates the three input AND gate indicating a "match" condition. If non-matching data is received any time during the detection sequence the "ERROR-" flip-flop is reset which disables the AND gate until a system "RESET" occurs. "RESET" may be generated in a variety of ways depending on the

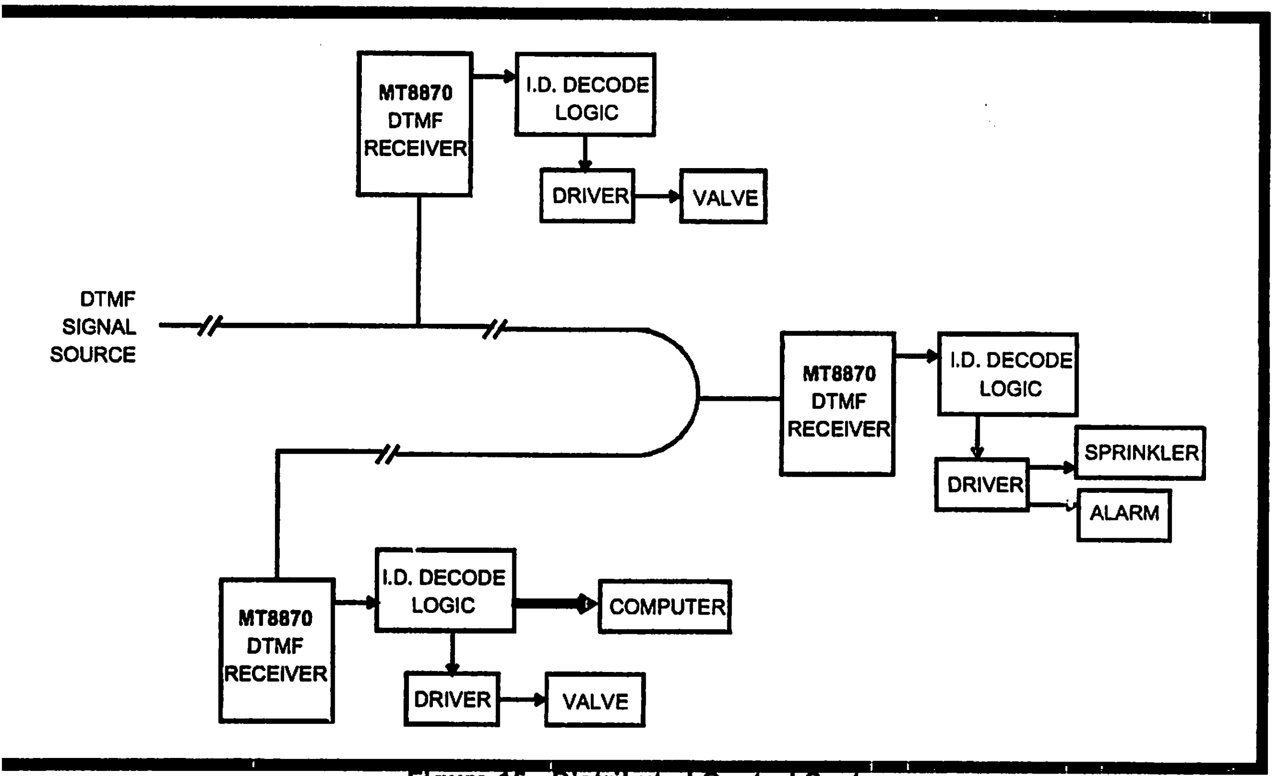


Figure 15 - Distributed Control System

ystem design objective. If one DTMF code is served exclusively for the "RESET" function then e MT8870 outputs can be decoded directly. This quires that the controller send a "RESET" ommand prior to sending an I.D. sequence. lternatively a "time-out" timer, triggered by StD, ould serve to generate a system reset if a certain ne lapse occurs between received signals. This ethod places time constraints on the system but liminates the need to consume a DTMF command r the "RESET" function.

he concept of using a common transmission edium for control signalling applies to several ossible situations. Plant process control, remote easurement control, selective intercom call ystems, institutional intercom systems, two way dio control, pocket pagers and model car or boat mote control, just to mention a few.

onversely, data could be collected from distributed urces. Implemented on a circulating wire or an RF annel, as illustrated in Figure 17, information could e collected by a central unit which individually polls ach monitor to ask for data. Alternatively, the stem could be interrupt driven (Fig.18). In this se each monitor, when ready to send data, enerates an interrupt request by sending a DTMF D. sequence followed by a data stream. Interrupt asking or prioritizing could be achieved from the e central control end by applying DC levels across a wire pair or sending a pilot tone in an RF system. Remote data collection units would monitor this signal to detect when a higher priority interupt is being handled or the communications channel is busy.

Data Communication Using DTMF

There is a vast array of potential applications for DTMF signalling using the existing telephone network. Considering that there are millions of ready-made data sets installed in convenient locations (i.e. the Touch Tone telephone) remote control and data entry may be performed by users without requiring them to carry around bulky data modems.

Potential applications include:

- home remote control
- remote data entry from any Touch-Tone keypad
- credit card verification and inquiry
- salesman order entry
- catalogue store (stock/price returned via voice synthesis)
- stock broker buy/sell/inquire -using stock exchange listing mnemonics
- answering machine message retrieval
- automatic switchboard extension forwarding

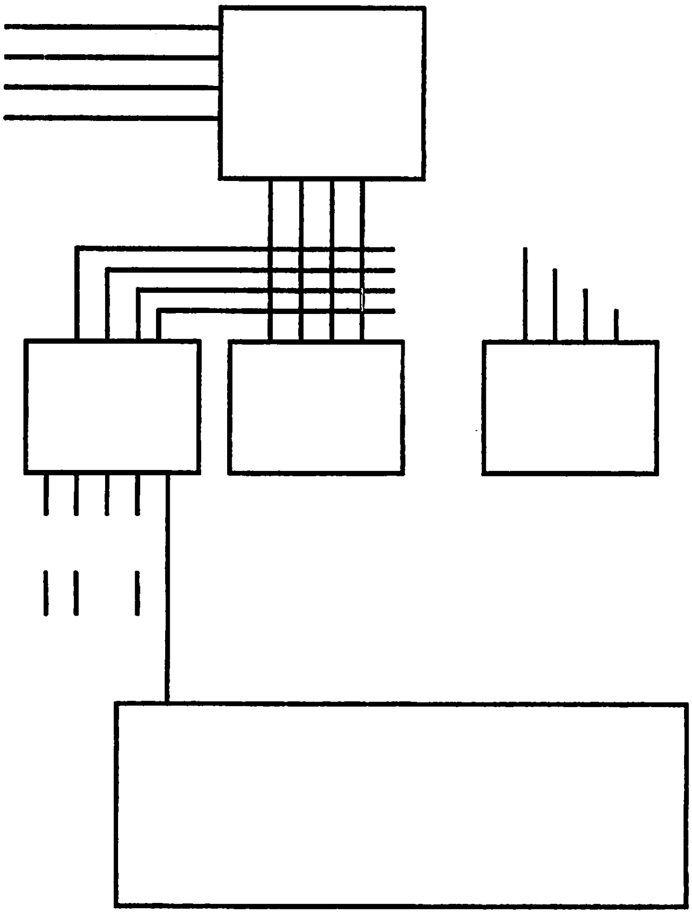
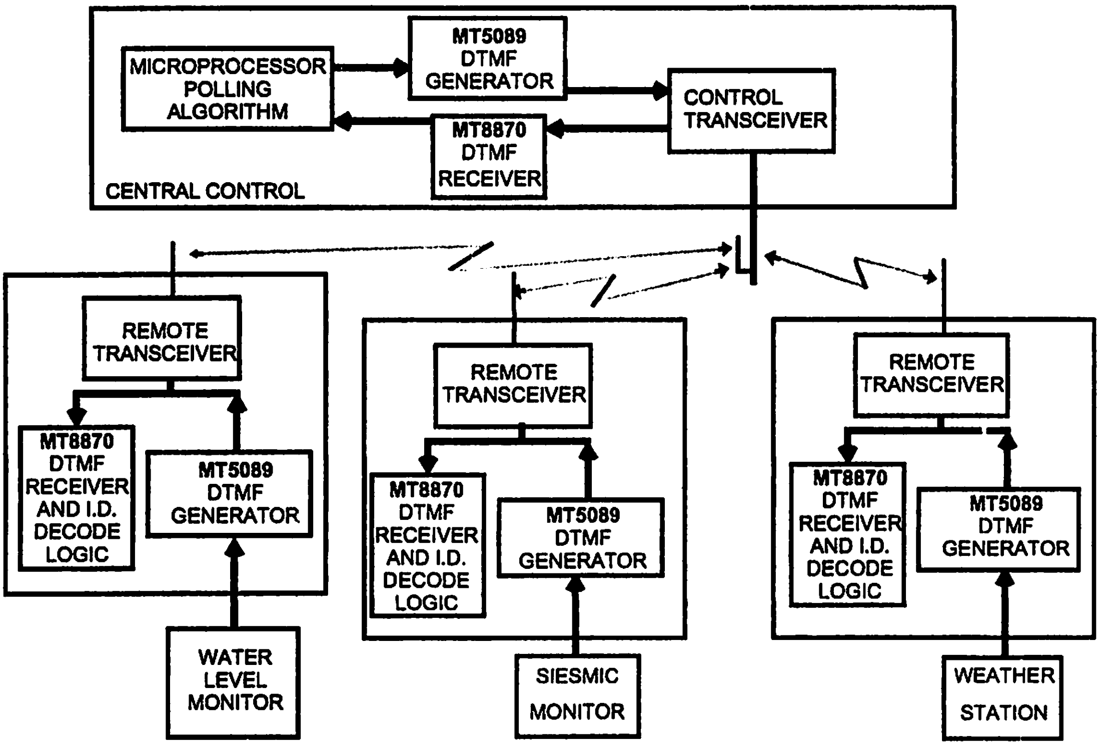
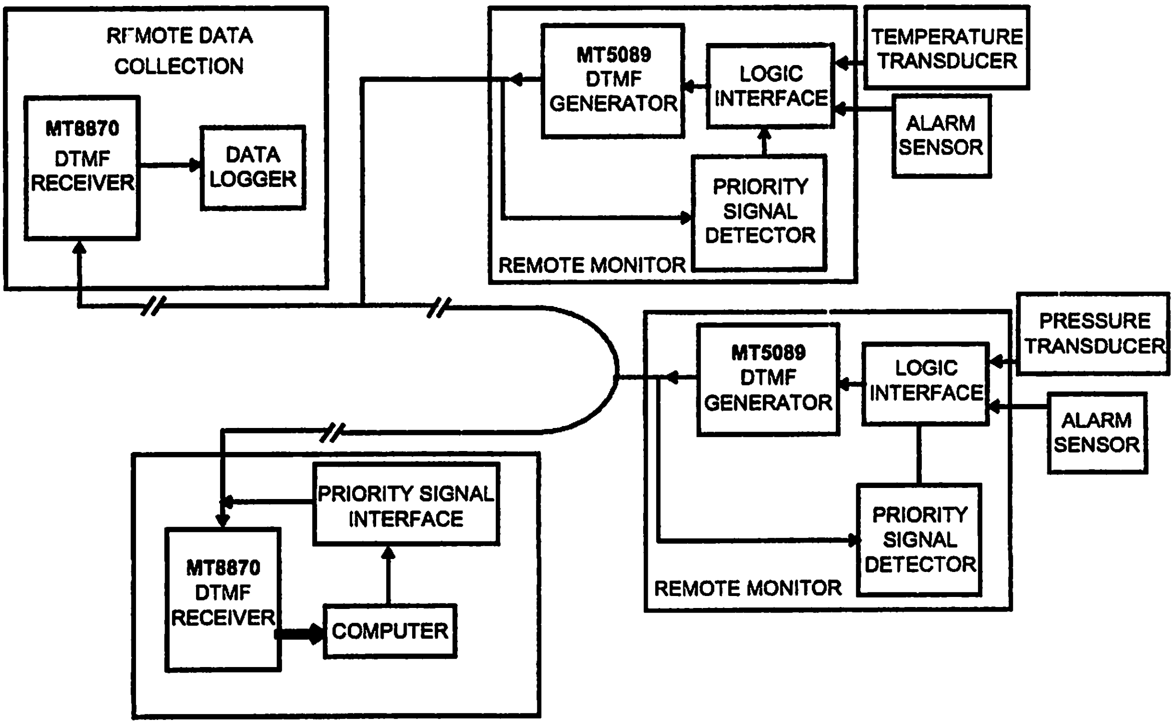


Figure 16 - N-Character Sequence Identifier



Polling system for multiple location remote data collection.

Figure 17 - DTMF Controlled Data Collection



Remote monitors send data while the interconnecting pair of wires is clear of other interrupts.

Figure 18 - Interrupt Driven Data Collection System

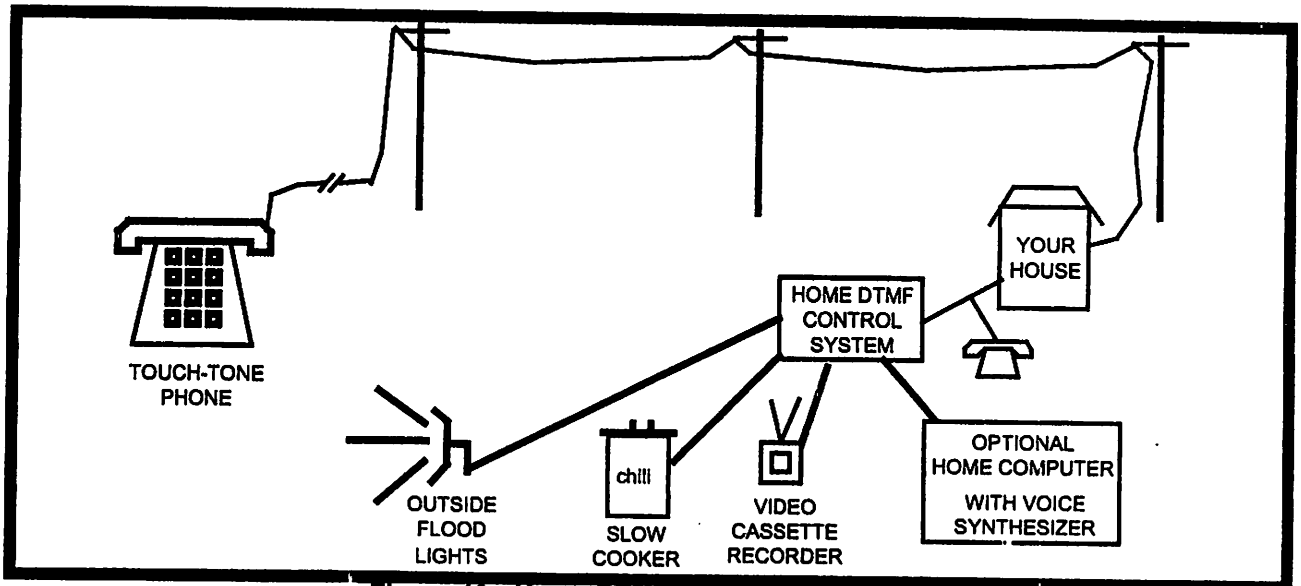
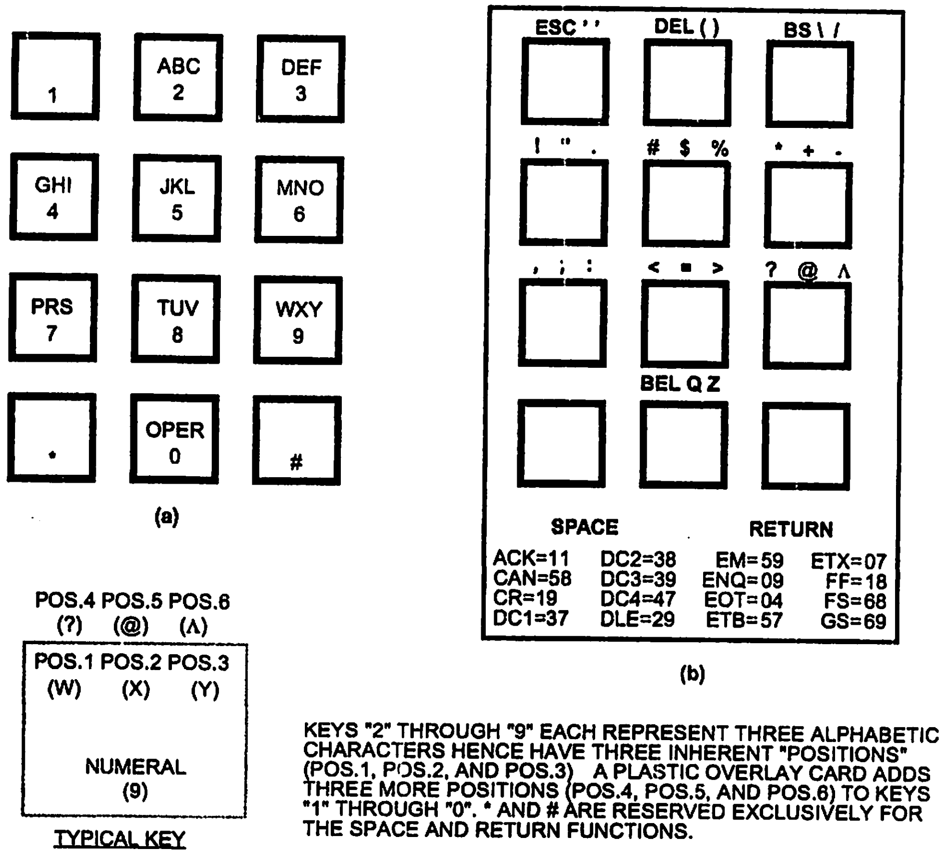


Figure 19 - Home DTMF Remote Control System



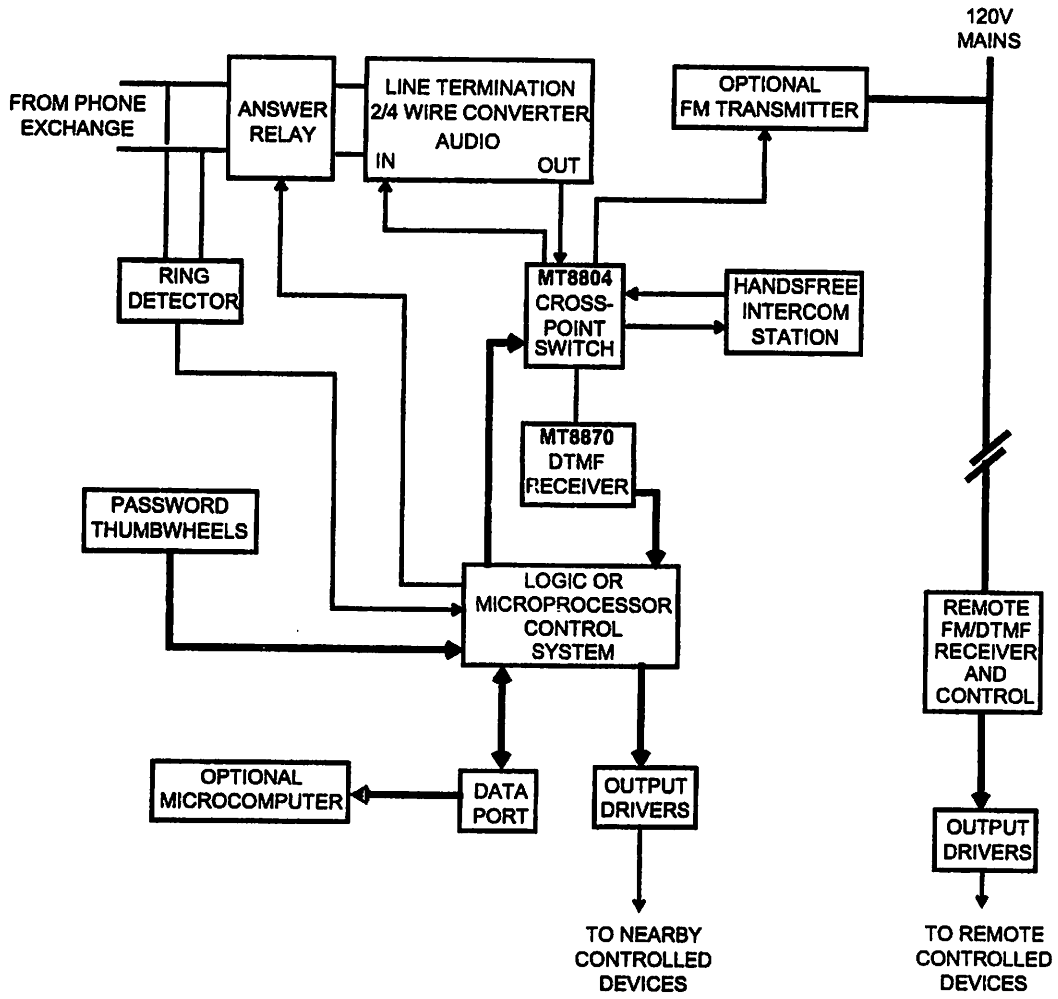
a) Layout of a standard telephone keypad showing inherent character positions for coding purposes.
b) Credit card size overlay expands each keys function by adding three more character positions.
The * and # are reserved to send "SPACE" and "RETURN" as single key operations. Each other ASCII code requires two keystrokes. To send a character simply push the button on or over which it appears, then push the numeral corresponding to its position. For example, to send a "T" push '8' followed by '1', to send "%" push '5' followed by '6'.

Figure 20 - Using A Pushbutton Phone As A Data Terminal

A scheme for coding ASCII characters using one and two digit DTMF signals is outlined in the appendix. Notice that on a telephone keypad keys 2 through 9 are represented by three alpha-characters as well as a numeral. To send an alpha-character, using this scheme, first press the key on which the character appears then press the key corresponding to the position in which the character appears on its key (1, 2 or 3). Numerals are sent by touching the desired number followed by a zero. The asterisk (*) and octothorp (#) have been reserved for "space" and "return" respectively. A plastic overlay the size of a credit card expands the number of useable "positions" on each button (Fig. 20). This serves as a guide for sending other ASCII codes and fits snug into a credit card wallet. ASCII control characters that are not commonly used could be listed at the bottom of the card. This user-friendly algorithm eliminates the need to memorize conversion codes and allows significant functionality even without the overlay reference.

A simple block diagram shows how this scheme may be implemented for a home DTMF control system (Fig. 21). A ringing voltage detector signals the microprocessor of an incoming call. The microprocessor, after the prescribed number of rings, closes the answer relay engaging the proper terminating impedance. A two-to-four wire converter splits bidirectional audio from the balanced telephone line into separate single ended transmit and receive paths.

Receive audio is then switched to the DTMF receiver through the crosspoint switch. Upon receiving a valid DTMF signal, the microprocessor is alerted by



An FM transmitter could be used to couple control signals for distribution over existing power lines. This would eliminate the need for installing wires between the DTMF control unit and remote controlled devices.

Figure 21 - Block Diagram of Home DTMF Remote Control System

the rising edge of StD. The microprocessor then checks for a valid password sequence and decodes subsequent commands. A command can be entered to put the system into remote-control mode. In this case the crosspoint switch is configured to route DTMF signals into the FM-over-mains transmitter as well as the system tone receiver. Forwarding of control signals is accomplished by applying an FM carrier to the power line. This eliminates the need to string control wires haphazardly about the house. The appropriate device is selected by its unique DTMF I.D. code. The microcomputer keeps track of all device locations and their I.D. codes since it must decide when to supply function outputs to the "nearby" devices and when to let the "remote" receivers handle the data. Subsequent data is transmitted to a selected device until a 'reset' command is entered.

Upon receiving any DTMF signal, answer back tones are returned by the microprocessor to acknowledge valid or invalid operations and to indicate the state of an interrogated device. For example, a low to high tone transition could indicate that a particular device is on, a high to low transition indicating the off state. A command could be entered to put the system in an 'external' mode which would allow communications through the data port. A host computer could be connected to this port to broaden the scope of the system.

The resident microprocessor unit contains the software and hardware to control ringing verification, password and command decoding, answer back tone generation, audio routing, output function latches and an optional data port. Output drivers buffer the latches and switch relays or SCRs to control peripheral devices.

An infinite variety of devices could be controlled by such a system, the spectrum of which is limited only by the ability to provide appropriate interfacing. This system could also be the heart of a DTMF intercom system allowing intercommunication, "phone-patching", and remote control from varied household locations. This type of system concept is, of course, anything but limited to home use. Many applications can provide conveniences to consumers, salespeople and executives.

For example, a merchant could verify credit card accounts quickly utilizing only a telephone keypad for data entry (Fig. 22). Each credit card company could reserve one or more telephone lines to provide this function, reducing the human effort required. The receiving end system would be required to answer the call, provide a short answer back tone or message, receive and decode the credit card account number, verify it, verify the owner's name and give a go/no-go authorization. This return data could easily be provided with the aid of a voice synthesizer. An auto-dialler containing appropriate phone numbers could be installed at the merchant end as an added time saver.

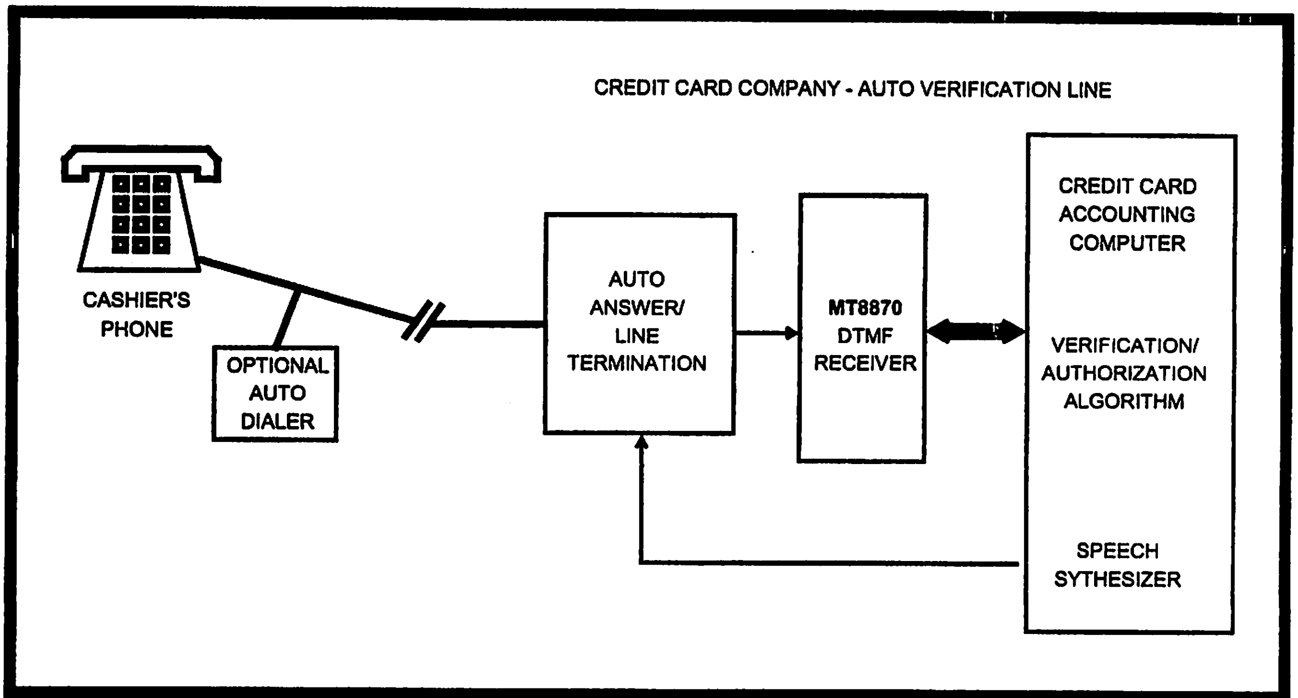


Figure 22 DTMF Data Communications For An Auto Verification Line

With a similar arrangement, a travelling salesman could access price, delivery and customer status, enter or delete merchandise orders and retrieve messages all from the comfort of the customer's office (Fig. 23a). A department store could provide shop-by-phone service to its customers using telephone keypad data entry (Fig. 23b). Brokerage firms, utilizing the stock exchange mnemonic listings could provide trading price information and buy/sell service via telephone keypad entry. A voice synthesizer could provide opening and current trading price, volume of transactions and other pertinent data. A telephone answering system manufacturer could apply this technique, allowing users to access and change outgoing and incoming messages from a Touch-Tone phone.

A PBX manufacturer could offer a feature that relieves the switchboard attendant from unneccesary interaction. A call could be answered automatically and a recording may reply "Thank you for calling XYZ. Please dial the extension you wish to contact or zero for the switchboard". If the caller knows the called party's extension in advance it is not neccesary to wait for the switchboard attendant to forward the call. The attendant could be notified to intervene if there is no action by the caller say, ten seconds after the recording ends. This provides a similar function to a "Direct Inward Dialling" (DID) trunk but without the additional overhead incurred with renting a block of phone numbers as in the DID case.

Now that a DTMF receiver is so easy and inexpensive to implement there are many simple dedicated uses that become attractive. A useful home and office application for DTMF receivers is in a self-contained telephone-line-powered toll call restrictor similar to the block diagram in Fig. 2a. This could be installed in an individual telephone or at the incoming main termination depending on which phone or phones are to be restricted. While disallowing visitors from making unauthorized long distance calls, the owner may still desire access to toll dialling. This could be provided by adding a logic circuit that disables the toll restrictor upon receiving a predetermined sequence of DTMF characters (Fig. 16). In this case, the user must enter his password before dialling a long distance number.

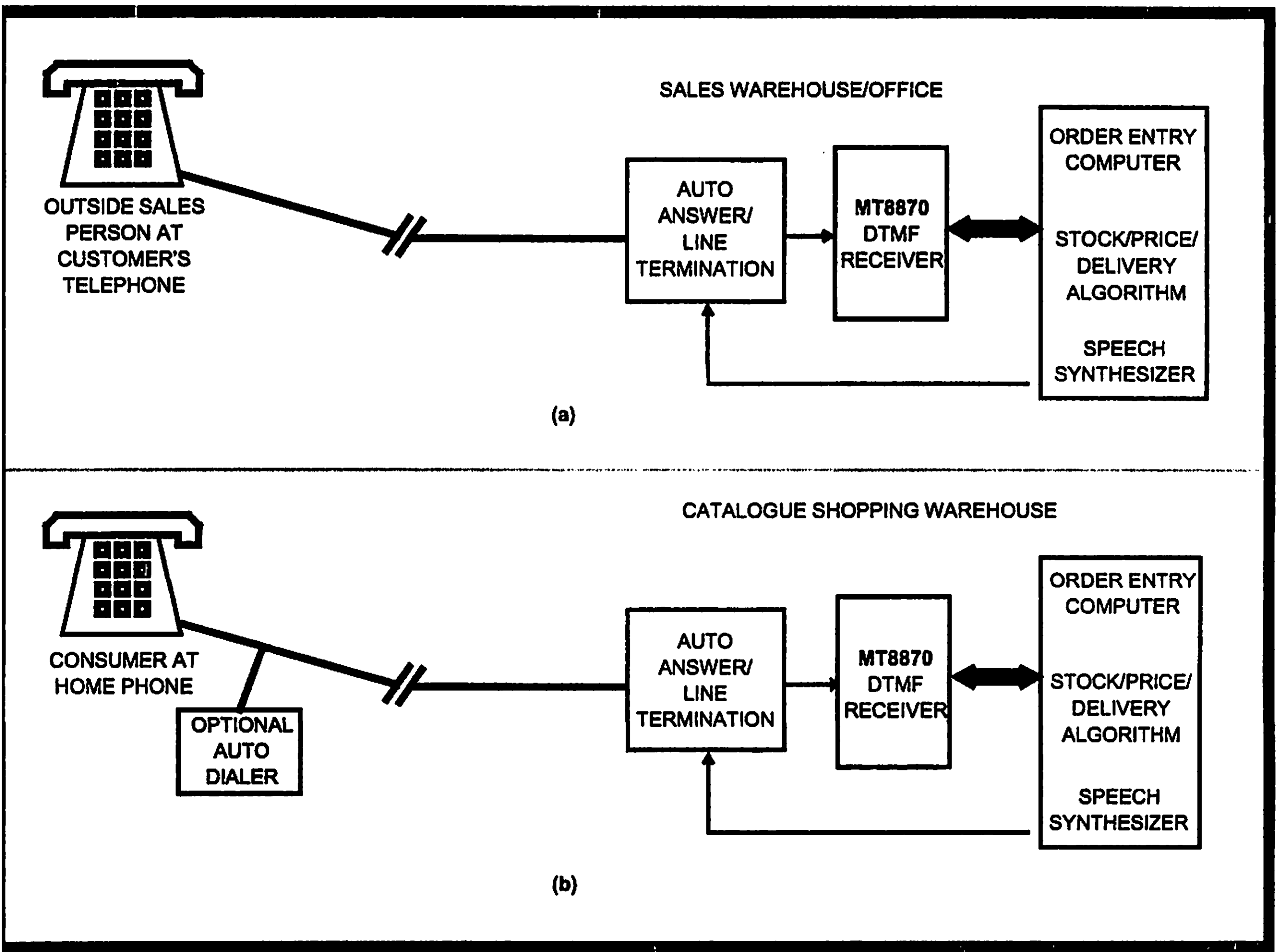


Figure 23 - Two Applications Of DTMF Data Communications

Conclusion

The applications for DTMF signalling are tremendous and due to innovative technological advances its use is increasingly widespread. DTMF offers highly reliable, cost effective signalling solutions which require no development effort on the user's part. The advent of single chip receivers has allowed many products that were previously not cost-effective to be manufactured in production quantities.

DTMF signalling was originally designed for telephony signalling over voice quality telephone lines. This signalling technique has been applied to a multitude of control and data communications systems. All that is required is a voice quality communication channel with appropriate interfacing. The applications are limited only by one's imagination.

Appendix

ASCII TO DTMF CONVERSION

Partial ASCII coding and conversion to 2 sequential DTMF signals

ASCII	HEX	DTMF	ASCII	HEX	DTMF	ASCII	HEX	DTMF
ACK	06	11	!	21	44	A	41	21
BEL	07	01	"	22	45	B	42	22
BS	08	34	#	23	54	C	43	23
CAN	18	58	$	24	55	D	44	31
CR	0D	19	%	25	56	E	45	32
DC1	11	37	&	26	79	F	46	33
DC2	12	38	'	27	16	G	47	41
DC3	13	39	(	28	25	H	48	42
DC4	14	47	)	29	26	I	49	43
DEL	7F	24	*	2A	64	J	4A	51
DLE	10	29	+	2B	65	K	4B	52
EM	19	59	,	2C	74	L	4C	53
ENQ	05	09	-	2D	66	M	4D	61
EOT	04	08	.	2E	46	N	4E	62
ESC	1B	14	/	2F	36	O	4F	63
ETB	17	57	0	30	00	P	50	71
ETX	03	07	1	31	10	Q	51	02
FF	0C	18	2	32	20	R	52	72
FS	1C	68	3	33	30	S	53	73
GS	1D	69	4	34	40	T	54	81
HT	09	12	5	35	50	U	55	82
LF	0A	13	6	36	60	V	56	83
NAK	15	48	7	37	70	W	57	91
NUL	00	04	8	38	80	X	58	92
RS	1E	77	9	39	90	Y	59	93
S0	0E	27	:	3A	76	Z	5A	03
S1	0F	28	;	3B	75	[	5B	87
SOH	01	05	<	3C	84	\	5C	35
SP	20	*	=	3D	85	]	5D	88
STX	02	06	>	3E	86	^	5E	96
SUB	1A	67	?	3F	94		5F	89
SYN	16	49	@	40	95	`	60	15
US	1F	78				DEL	7F	24
VT	0B	17						

National Semiconductor

February 2000

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

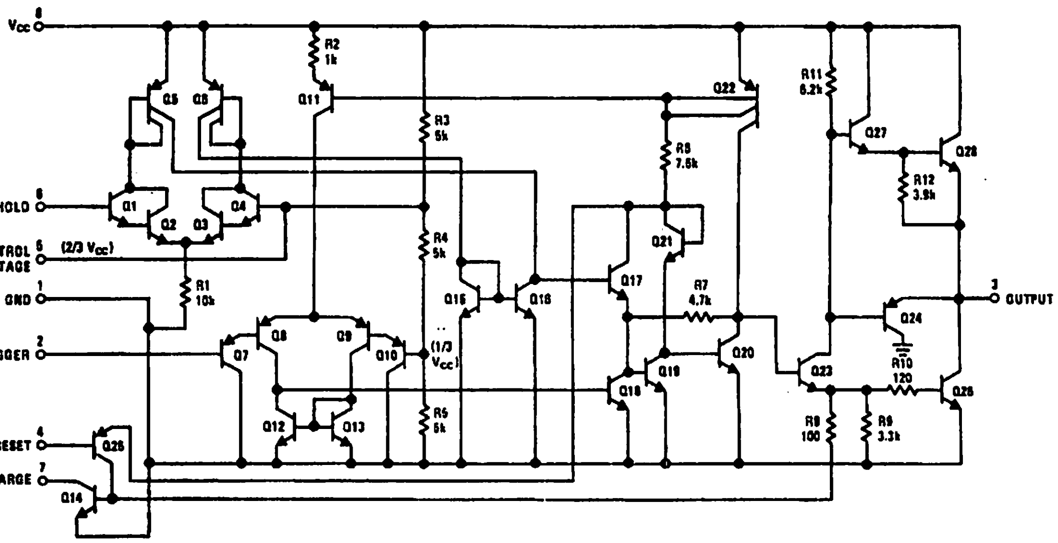
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



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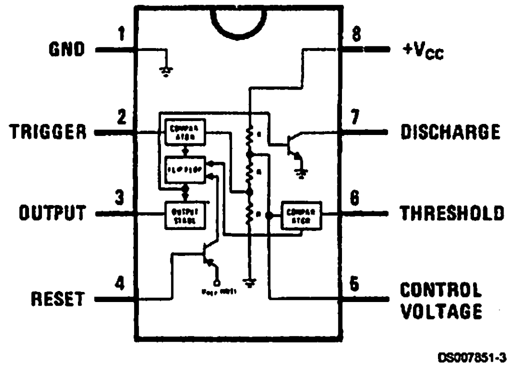
Connection Diagram

Dual-In-Line, Small Outline
and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits LM555C Min	Limits LM555C Typ	Limits LM555C Max	Units
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		3 10	6 15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1μF, (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1μF, (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9 2.6	10 3.33	11 4	V
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a −150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

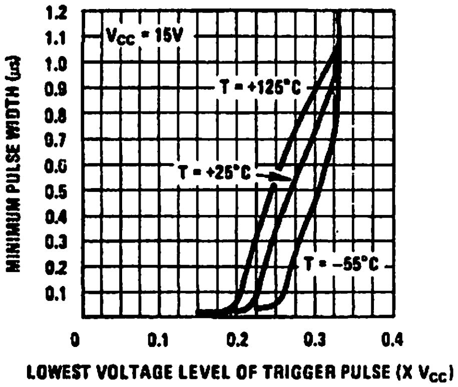
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

Minimum Pulse Width Required for Triggering



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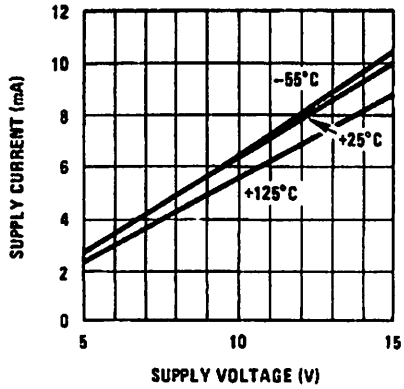
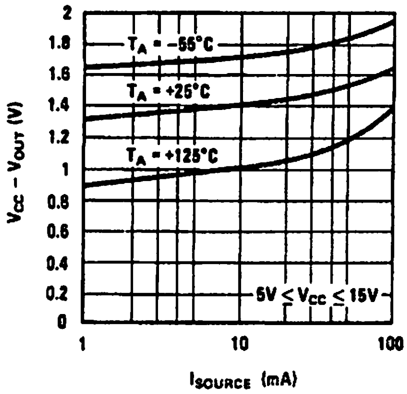
Supply Current vs. Supply Voltage



DS007851-19

High Output Voltage vs. Output Source Current



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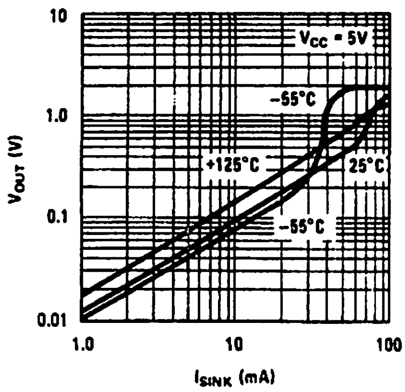
Low Output Voltage vs. Output Sink Current



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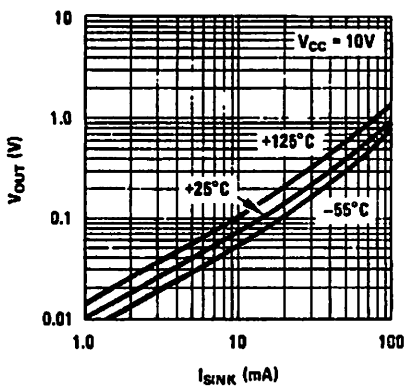
Low Output Voltage vs. Output Sink C. rrent



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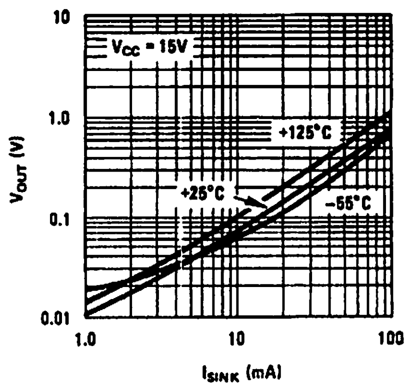
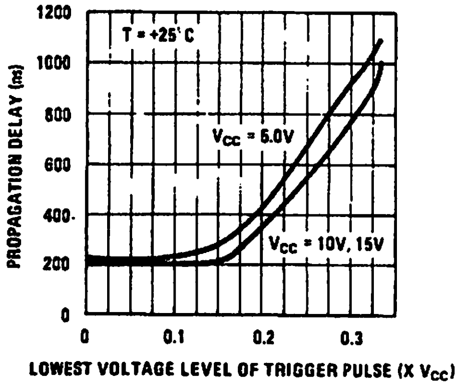
Low Output Voltage vs. Output Sink Current



DS007851-23

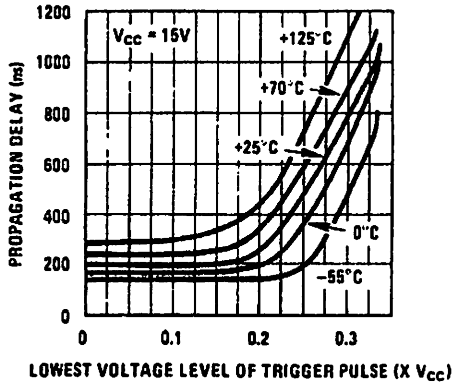
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



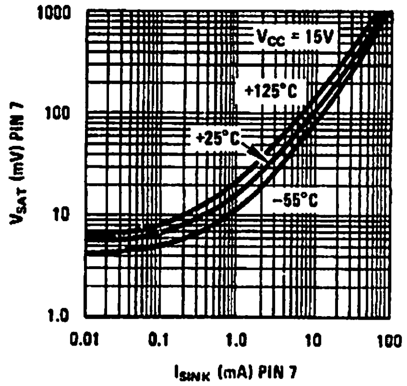
DS007851-24

Output Propagation Delay vs. Voltage Level of Trigger Pulse



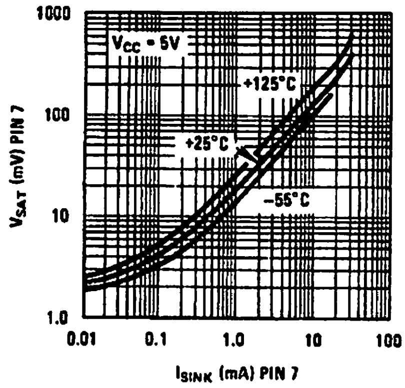
DS007851-25

Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-26

Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-27

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

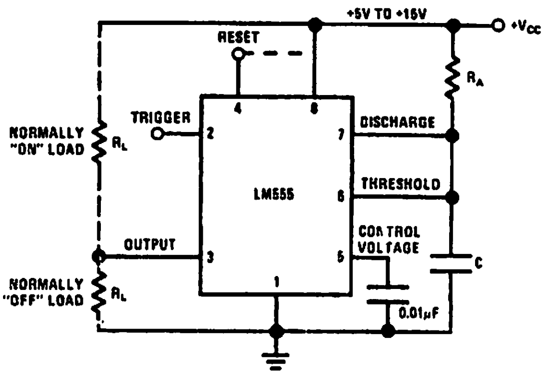
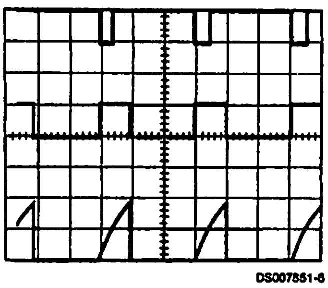


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

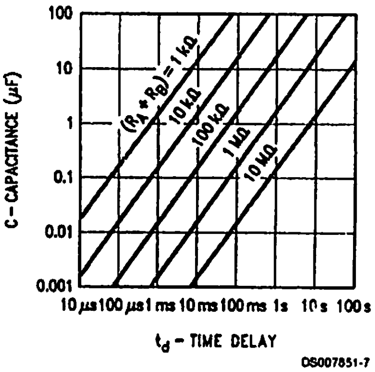


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

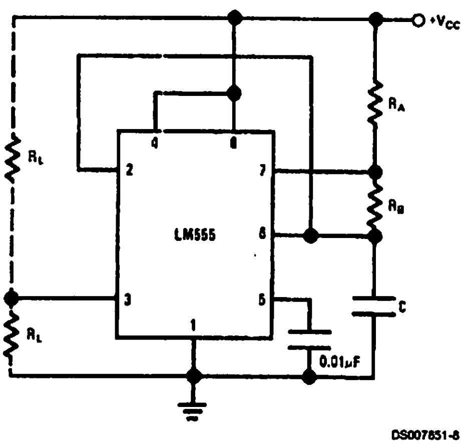
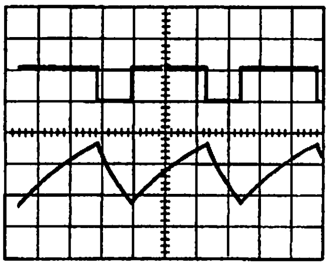


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



DS007851-9

V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

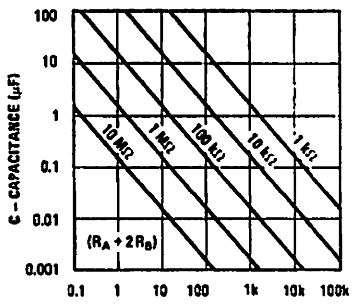
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

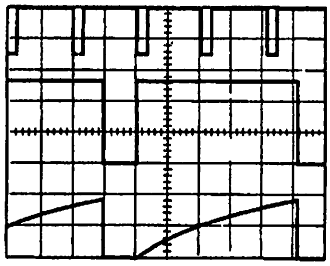


DS007851-10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



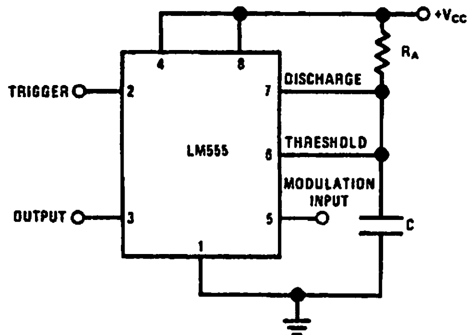
DS007851-11

V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

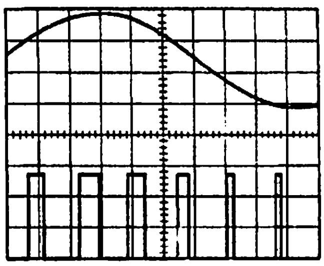
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



DS007851-12

FIGURE 8. Pulse Width Modulator



DS007851-13

V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

Applications Information (Continued)

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

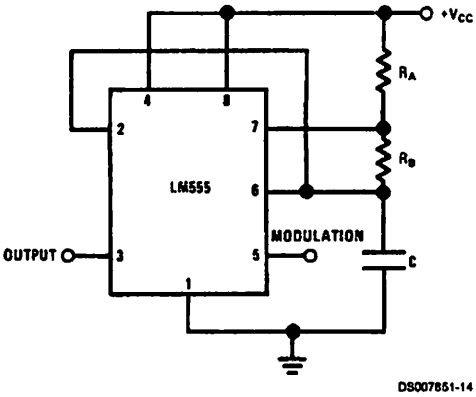
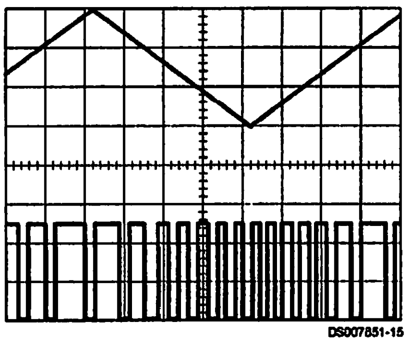


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

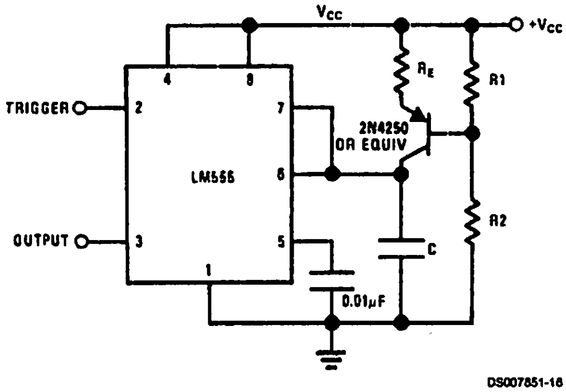


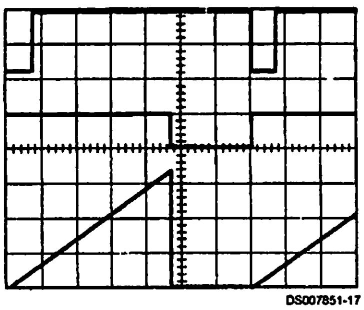
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} = 0.6V$$



V_{CC} = 5V
TIME = 20µs/DIV.
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14.* The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

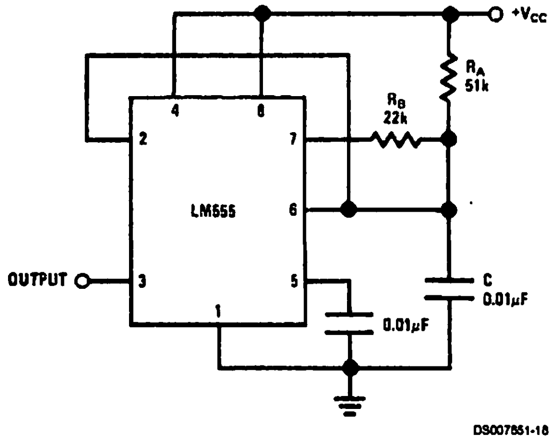


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

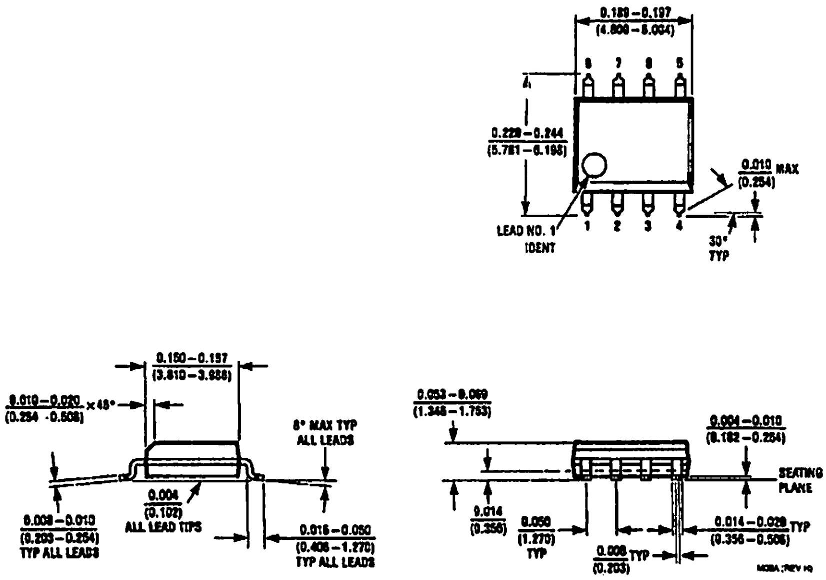
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

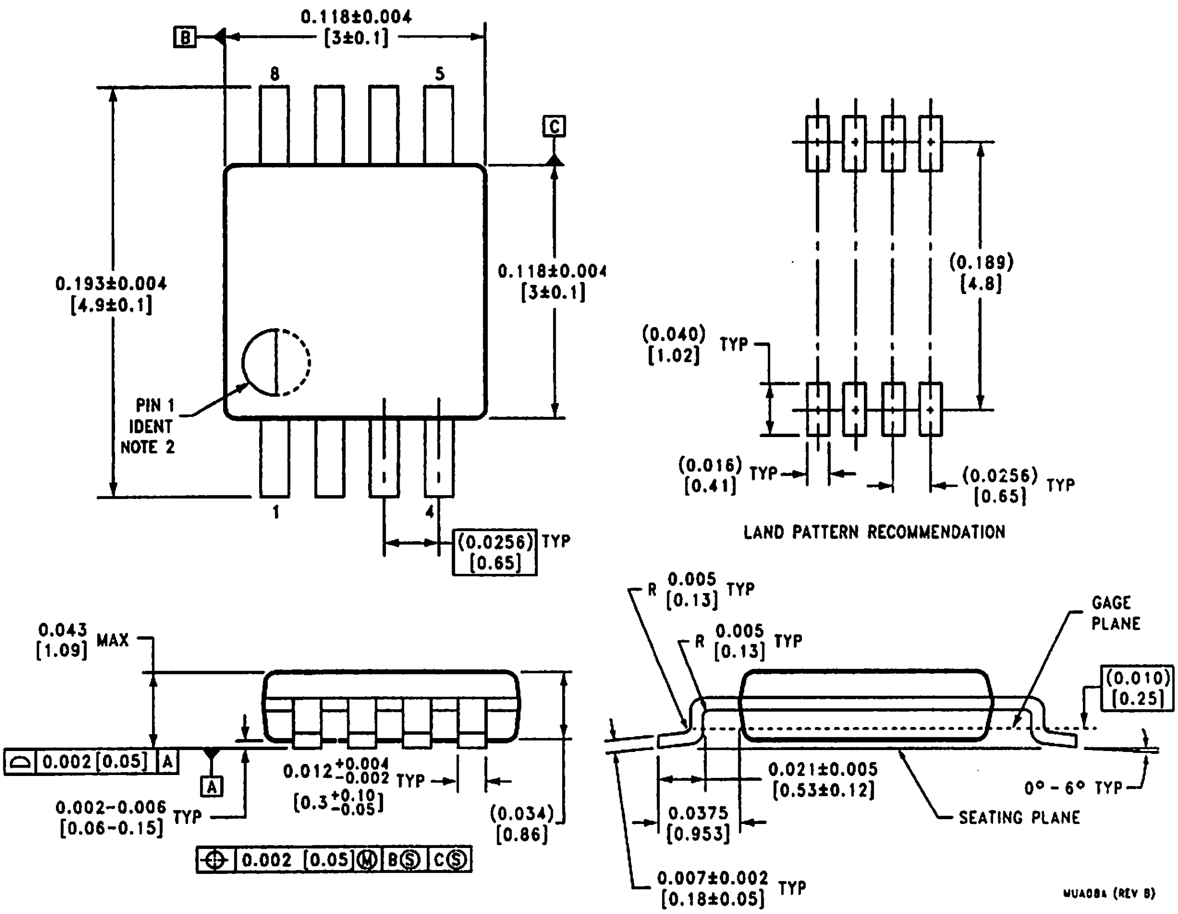
Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

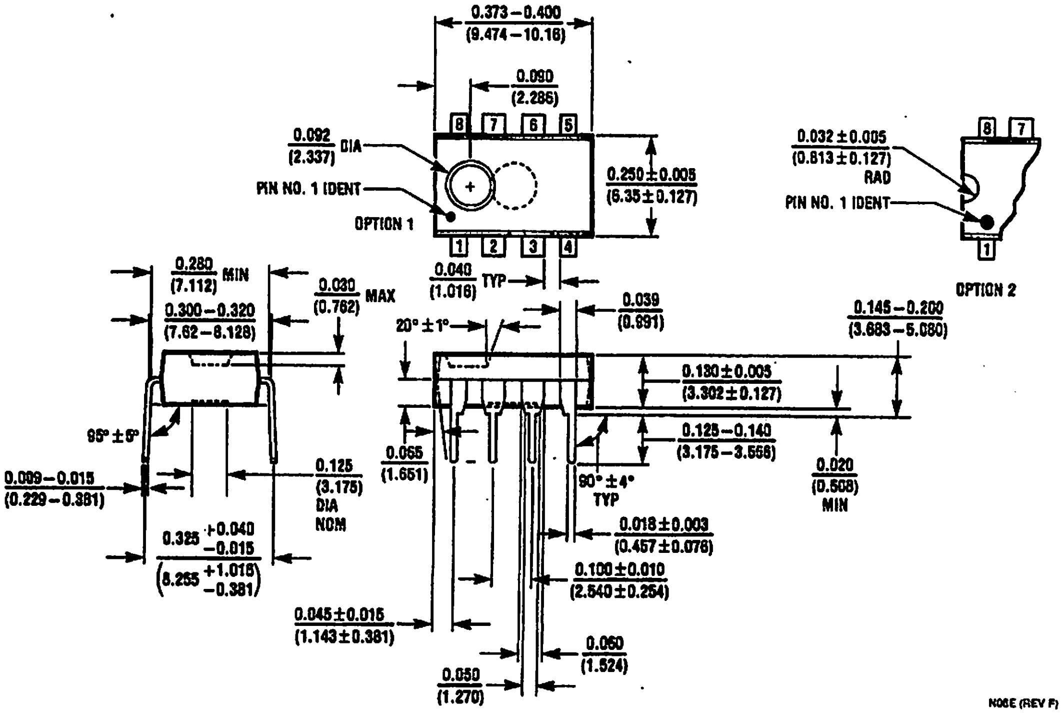


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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National Semiconductor

December 1994

LM158/LM258/LM358/LM2904 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

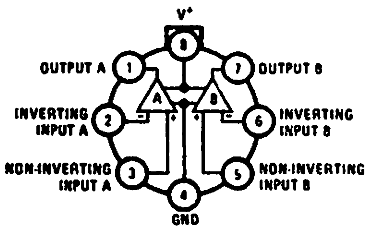
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^{+} − 1.5V

Connection Diagrams (Top Views)

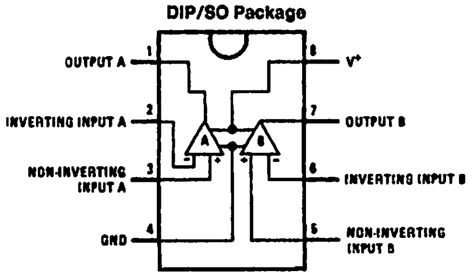
Metal Can Package



TL/H/7787-1

Order Number LM158AH, LM158AH/883*, LM158H, LM158H/883*, LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787-2

Order Number LM158J, LM158J/883*, LM158AJ or LM158AJ/883*
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2)		
$V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$		1	2		2	3		2	5		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)		20	50		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps $V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2		1	2		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2		0.5	1.2		0.5	1.2		0.5	1.2	mA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1V$ to 11V)	50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5V$	70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to 30V (LM2904, $V^+ = 5V$ to 26V), $T_A = 25°C$	65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling		$f = 1$ kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $T_A = 25°C$, $V_O = 200$ mV, $V^+ = 15V$	12	50		12	50		12	50		12	50		12	50		μA
Short Circuit to Ground		$T_A = 25°C$, (Note 2), $V^+ = 15V$		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7			7			7		μV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300		40	500		40	500	nA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range		$V^+ = 30$ V, (Note 7) (LM2904, $V^+ = 26V$)		0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V
Large Signal Voltage Gain		$V^+ = +15V$ (V_O = 1V to 11V) $R_L \geq 2\,k\Omega$		25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	$R_L = 2\,k\Omega$	26			26			26			26			22			V
			$R_L = 10\,k\Omega$	27	28		27	28		27	28		27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10\,k\Omega$			5	20		5	20		5	20		5	20		5	100	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		10	20		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		10	15		5	8		5	8		5	8		5	8		mA

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed
4 circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \approx 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

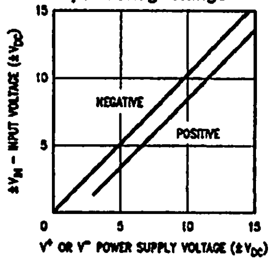
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

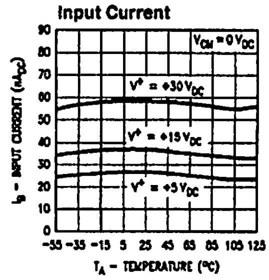
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

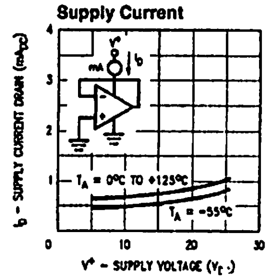
Input Voltage Range



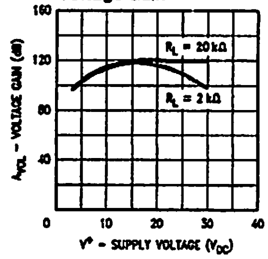
Input Current



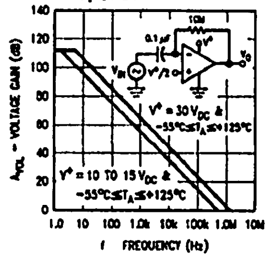
Supply Current



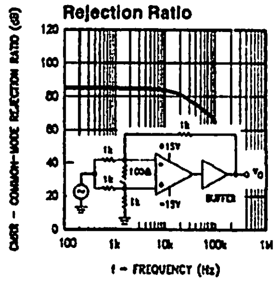
Voltage Gain



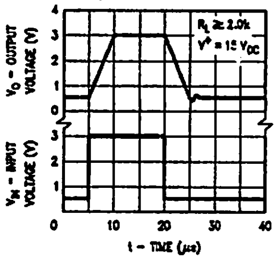
Open Loop Frequency Response



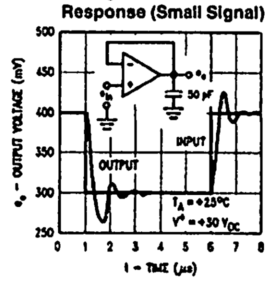
Common-Mode Rejection Ratio



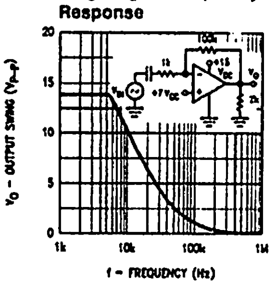
Voltage Follower Pulse Response



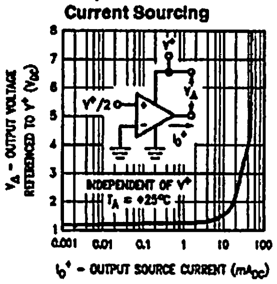
Voltage Follower Pulse Response (Small Signal)



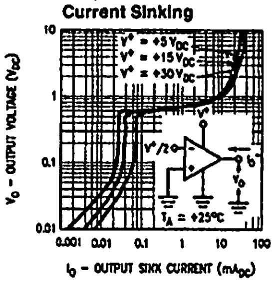
Large Signal Frequency Response



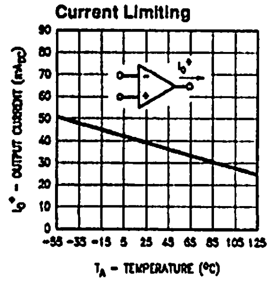
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



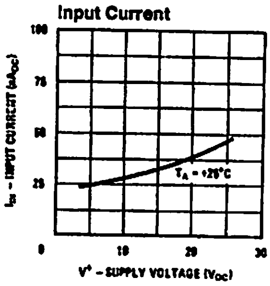
Current Limiting



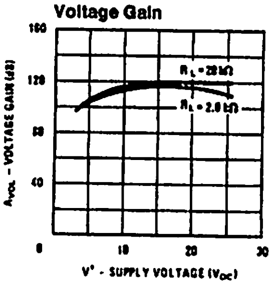
TL/H/7787–4

Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



TL/H/7787-5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers ope:ate over a wide range of power supply voltage with little change in performance chara teristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

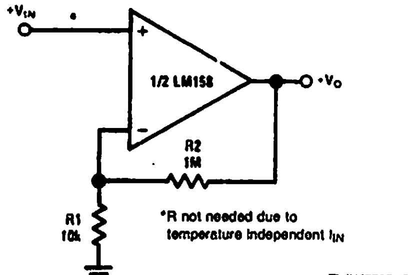
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

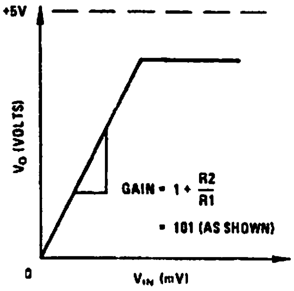
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

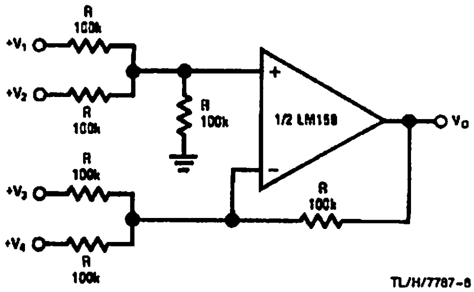


TL/H/7787-6



TL/H/7787-7

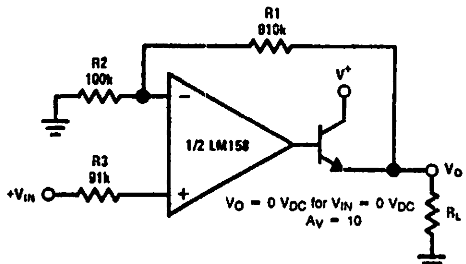
DC Summing Amplifier
(V_{IN}'s ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



TL/H/7787-8

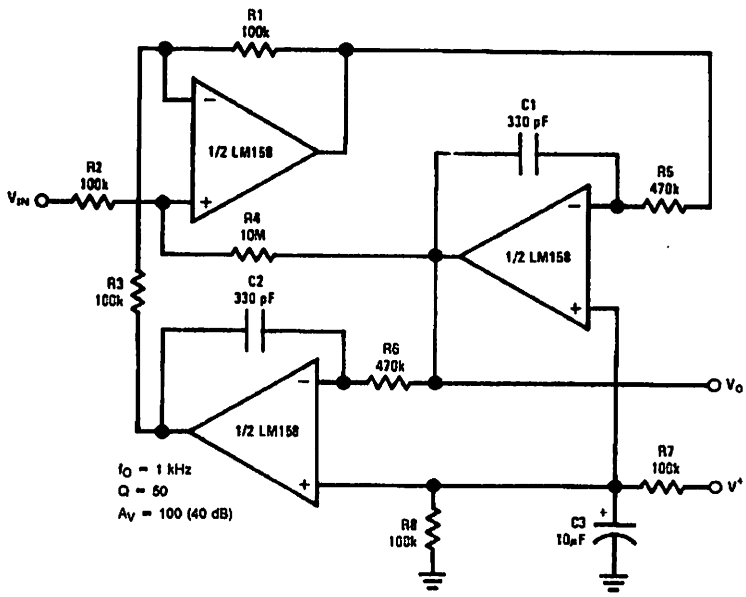
Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier



TL/H/7787-9

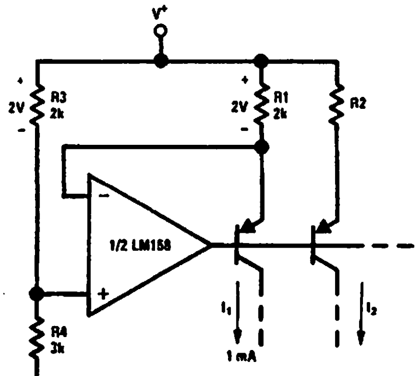
"BI-QUAD" RC Active Bandpass Filter



TL/H/7787-10

Typical Single-Supply Applications $(V^{+} = 5.0\ V_{DC})$ (Continued)

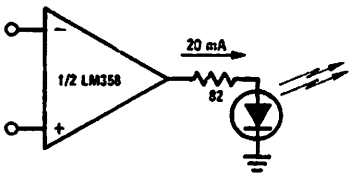
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

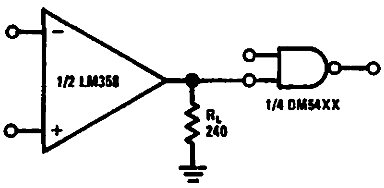
TL/H/7787-11

LED Driver



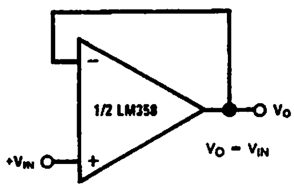
TL/H/7787-13

Driving TTL



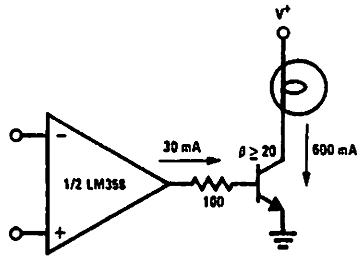
TL/H/7787-15

Voltage Follower



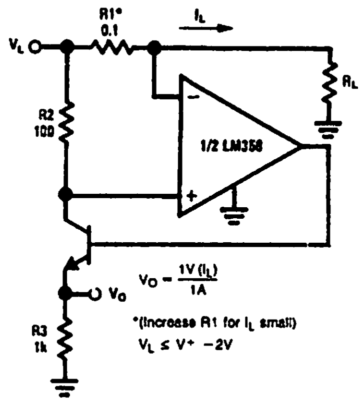
TL/H/7787-17

Lamp Driver



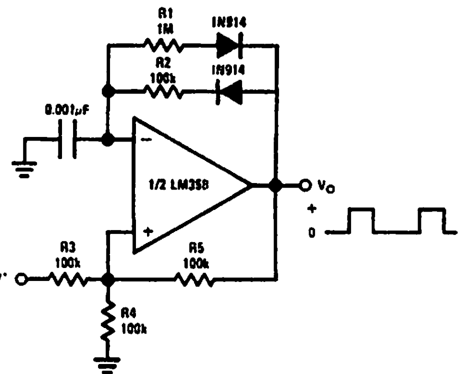
TL/H/7787-12

Current Monitor



TL/H/7787-14

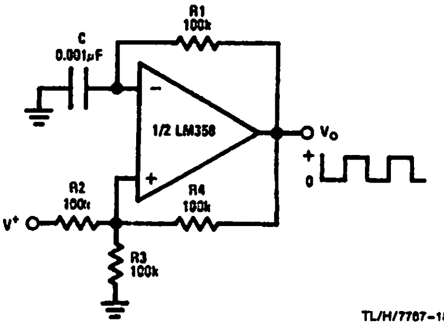
Pulse Generator



TL/H/7787-16

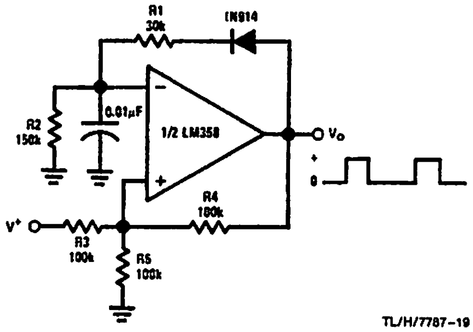
Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



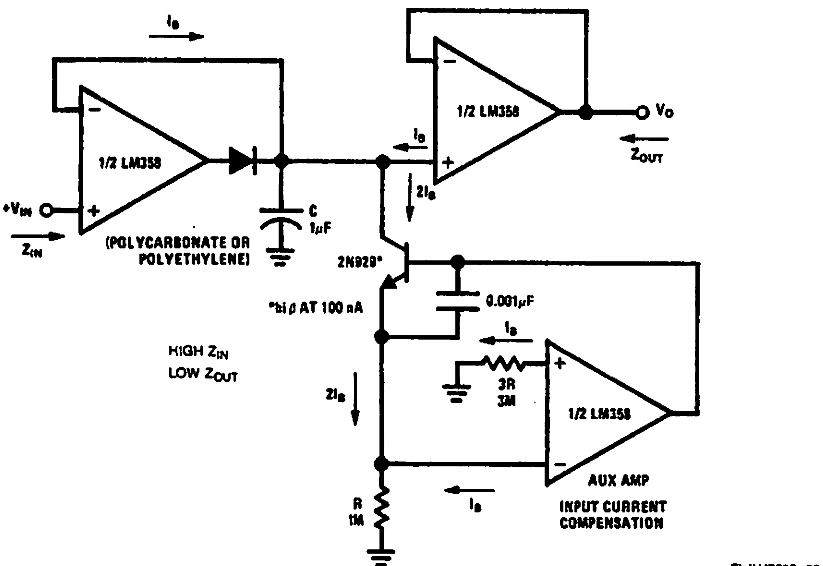
TL/H/7787-18

Pulse Generator



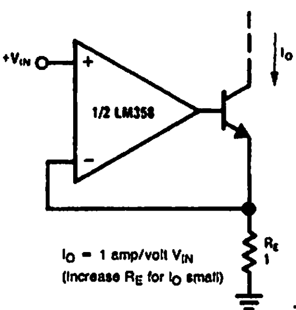
TL/H/7787-19

Low Drift Peak Detector



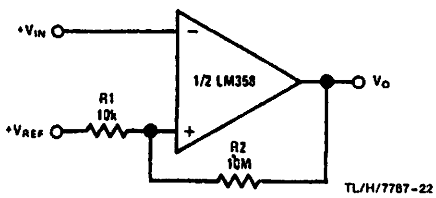
TL/H/7787-20

High Compliance Current Sink



TL/H/7787-21

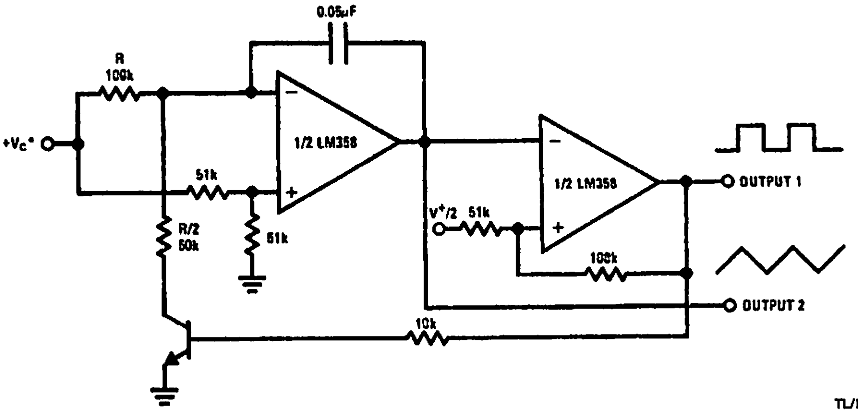
Comparator with Hysteresis



TL/H/7787-22

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

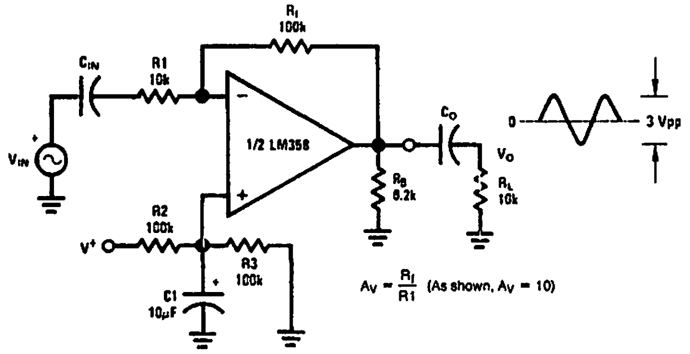
Voltage Controlled Oscillator (VCO)



TL/H/7787–23

*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

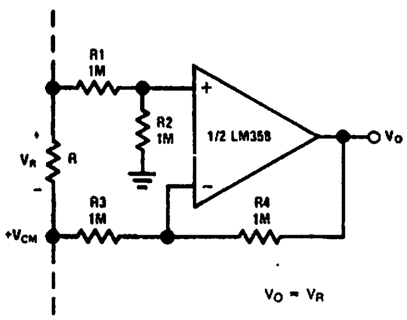
AC Coupled Inverting Amplifier



$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

TL/H/7787–24

Ground Referencing a Differential Input Signal

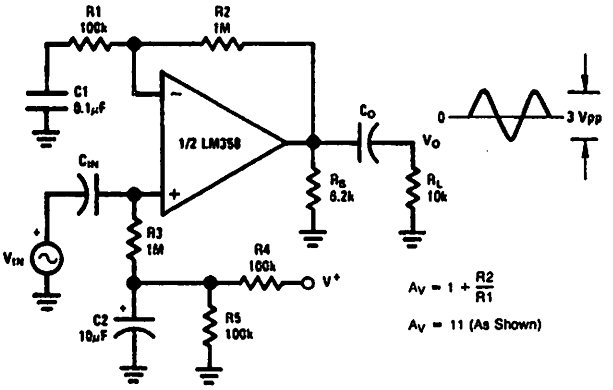


$V_O = V_R$

TL/H/7787–25

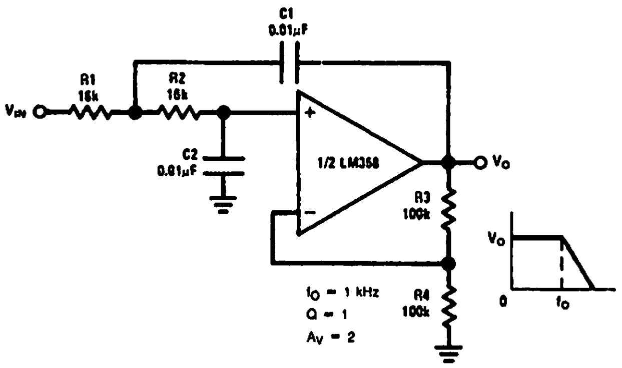
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier



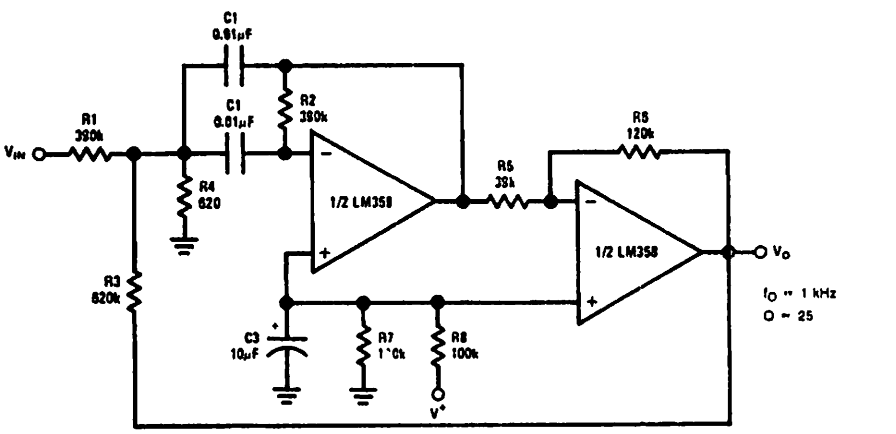
TL/H/7787-26

DC Coupled Low-Pass RC Active Filter



TL/H/7787-27

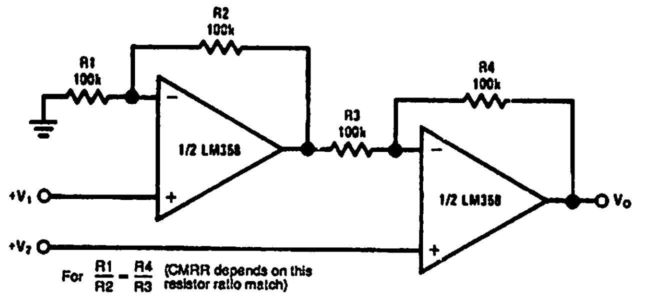
Bandpass Active Filter



TL/H/7787-28

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z, DC Differential Amplifier



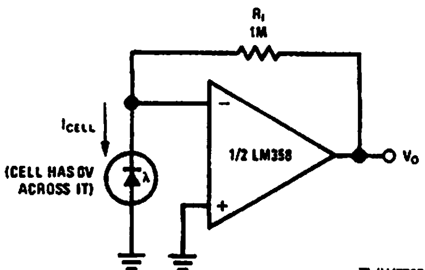
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

TL/H/7787-29

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

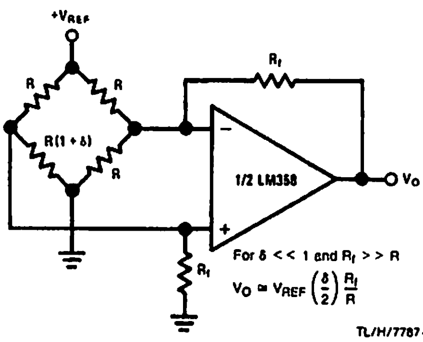
As Shown: $V_O = 2\,(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/7787-30

Bridge Current Amplifier

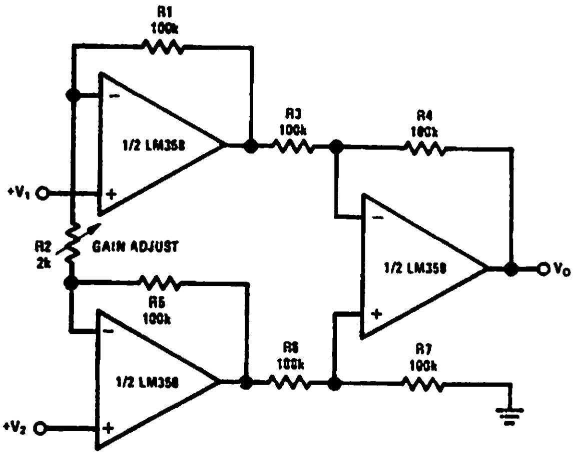


For $\delta << 1$ and $R_f >> R$

$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$

TL/H/7787-33

High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787-31

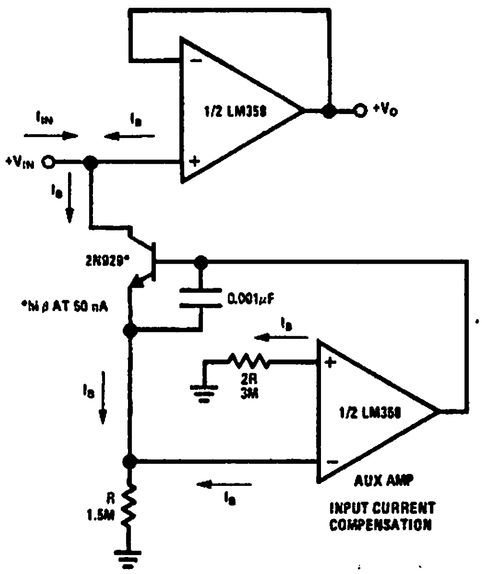
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101\,(V_2 - V_1)$

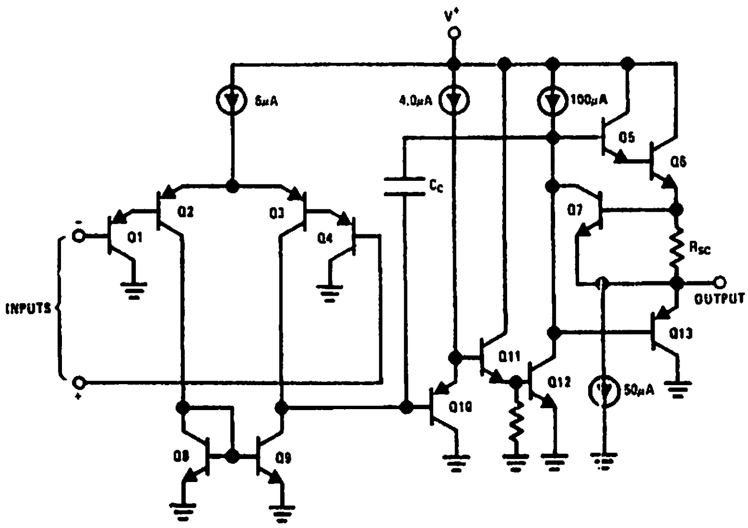
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/7787-32

Schematic Diagram (Each Amplifier)



TL/H/7787-3

FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised April 2002

CD4069UBC
Inverter Circuits

General Description

The CD4069UB consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

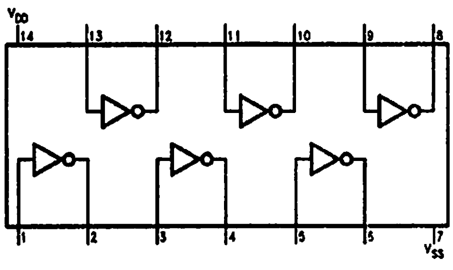
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} typ.
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MM74C04

Ordering Code:

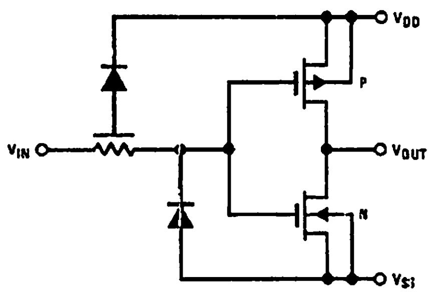
Order Number	Package Number	Package Description
CD4069UBCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4069UBCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4069UBCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

Connection Diagram



Schematic Diagram



Absolute Maximum Ratings (Note 1)
(Note 2)

DC Supply Voltage (V_{DD})	−0.5V to +18 V_{DC}
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and Electrical Characteristics table provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25			0.25		7.5	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5			0.5		15	
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	
V_{OL}	LOW Level Output Voltage	$\|I_O\| < 1$ µA								V
		V_{DD} = 5V		0.05		0	0.05		0.05	
		V_{DD} = 10V		0.05		0	0.05		0.05	
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	$\|I_O\| < 1$ µA								V
		V_{DD} = 5V	4.95		4.95	5		4.95		
		V_{DD} = 10V	9.95		9.95	10		9.95		
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	$\|I_O\| < 1$ µA								V
		V_{DD} = 5V, V_O = 4.5V		1.0			1.0		1.0	
		V_{DD} = 10V, V_O = 9V		2.0			2.0		2.0	
		V_{DD} = 15V, V_O = 13.5V		3.0			3.0		3.0	
V_{IH}	HIGH Level Input Voltage	$\|I_O\| < 1$ µA								V
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0			4.0		
		V_{DD} = 10V, V_O = 1V	8.0		8.0			8.0		
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0			12.0		
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 3: V_{SS} = 0V unless otherwise specified.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

CD4069UBC

AC Electrical Characteristics (Note 5)

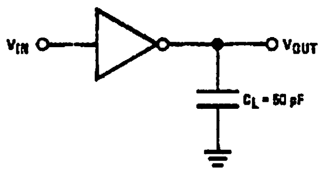
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, t_r and $t_f \leq 20$ ns, unless otherwise specified

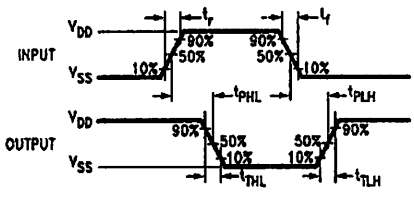
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	$V_{DD} = 5V$		50	90	ns
		$V_{DD} = 10V$		30	60	
		$V_{DD} = 15V$		25	50	
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		80	150	ns
		$V_{DD} = 10V$		50	100	
		$V_{DD} = 15V$		40	80	
C_{IN}	Average Input Capacitance	Any Gate		6	15	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 6)		12		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note—AN-90.

AC Test Circuits and Switching Time Waveforms

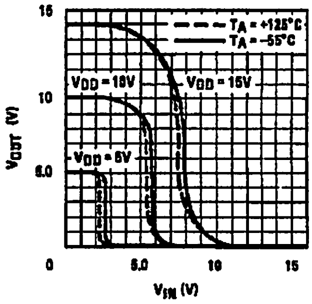




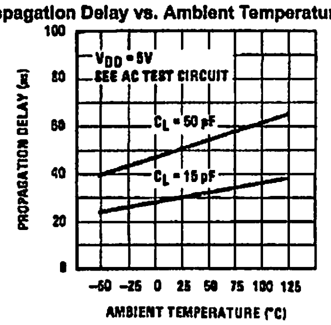
$t_r = t_f = 20$ ns

Typical Performance Characteristics

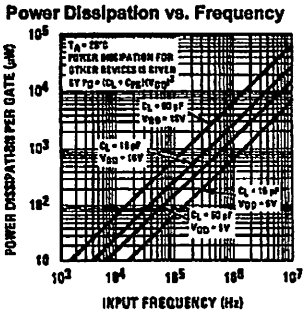
Gate Transfer Characteristics



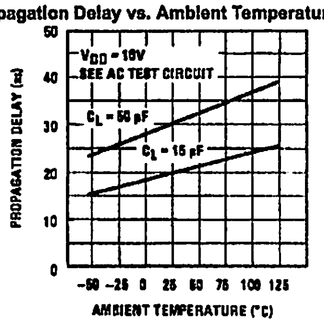
Propagation Delay vs. Ambient Temperature



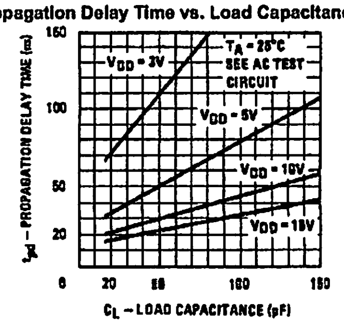
Power Dissipation vs. Frequency



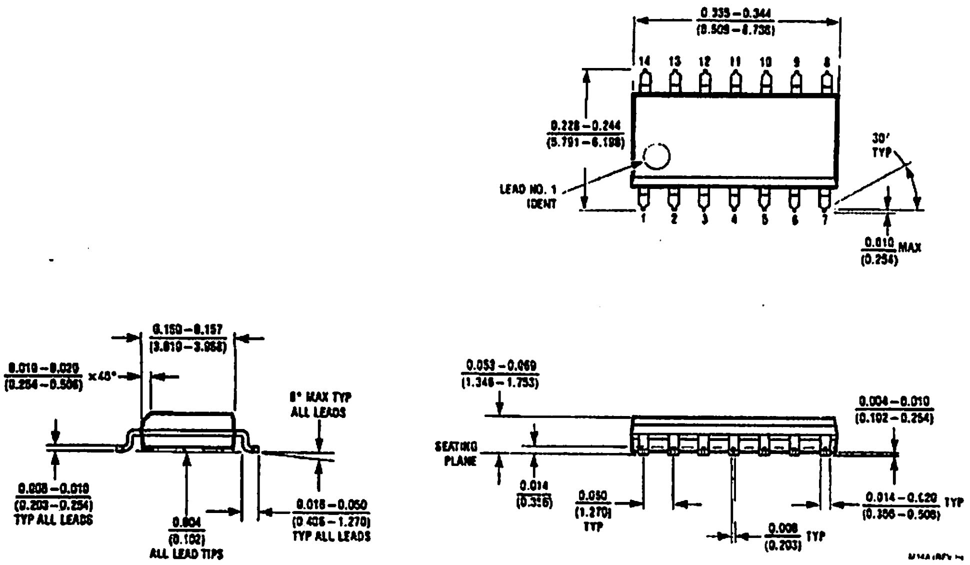
Propagation Delay vs. Ambient Temperature



Propagation Delay Time vs. Load Capacitance



Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

ɘatures

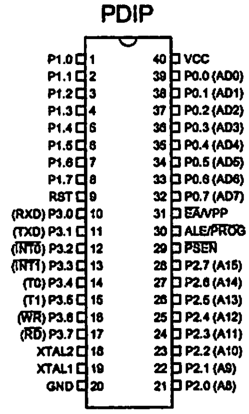
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

escription

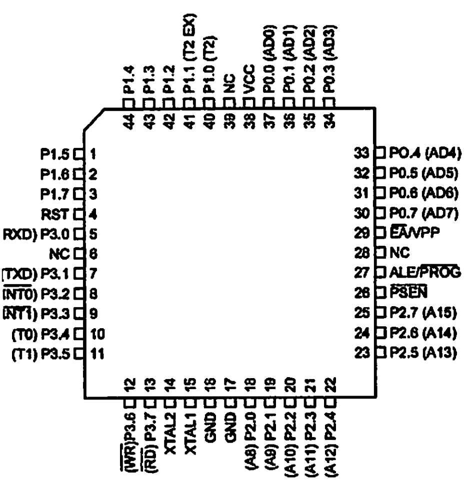
ıe AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K tes of Flash programmable and erasable read only memory (PEROM). The device manufactured using Atmel's high-density nonvolatile memory technology and is mpatible with the industry-standard MCS-51 instruction set and pinout. The on-chip ash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash ı a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ıighly-flexible and cost-effective solution to many embedded control applications.

in Configurations

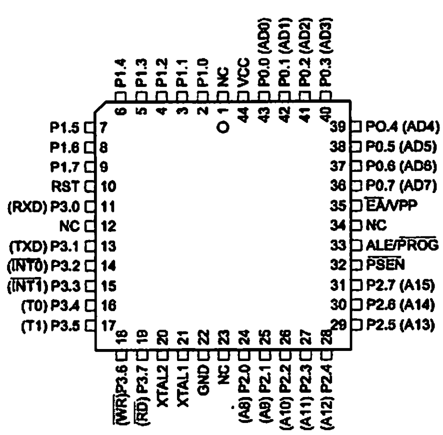
PDIP



PQFP/TQFP



PLCC



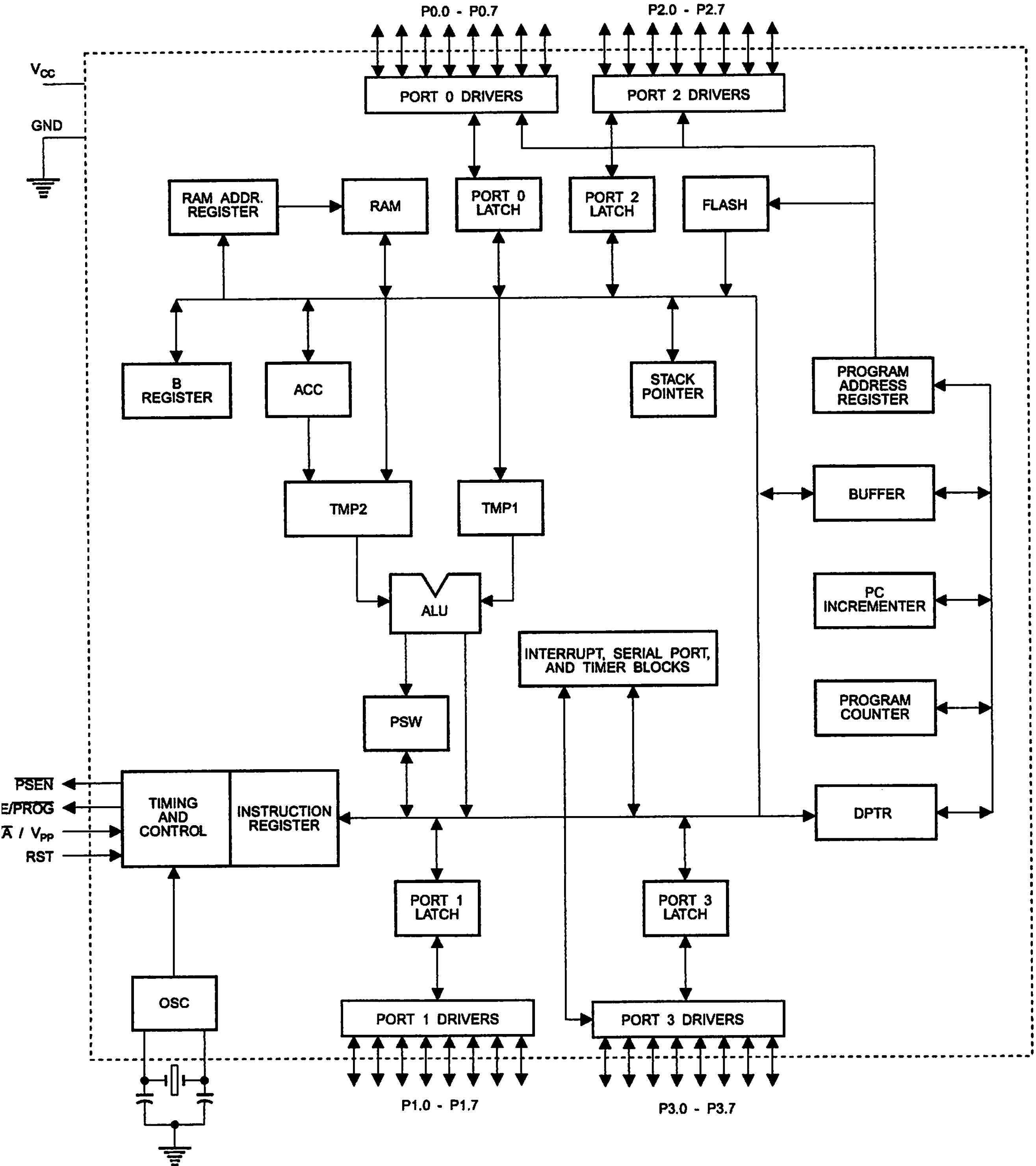
8-bit Microcontroller with 4K Bytes Flash

AT89C51

Not Recommended for New Designs. Use AT89S51.

Rev. 0265G–02/00

lock Diagram



ılse is skipped during each access to external Data əmory.

ɉesired, ALE operation can be disabled by setting bit 0 of ᖴR location 8EH. With the bit set, ALE is active only durȷ a MOVX or MOVC instruction. Otherwise, the pin is əakly pulled high. Setting the ALE-disable bit has no fect if the microcontroller is in external execution mode.

$\overline{\text{SEN}}$

ogram Store Enable is the read strobe to external proam memory.

hen the AT89C51 is executing code from external proam memory, $\overline{\text{PSEN}}$ is activated twice each machine cle, except that two $\overline{\text{PSEN}}$ activations are skipped during ıch access to external data memory.

$\overline{\text{A}}$/VPP

cternal Access Enable. $\overline{\text{EA}}$ must be strapped to GND in der to enable the device to fetch code from external proam memory locations starting at 0000H up to FFFFH. ote, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be ternally latched on reset.

$\overline{\text{A}}$ should be strapped to V_{CC} for internal program cecutions.

ıis pin also receives the 12-volt programming enable voltȷe (V_{PP}) during Flash programming, for parts that require 2-volt V_{PP}.

TAL1

ıput to the inverting oscillator amplifier and input to the ternal clock operating circuit.

TAL2

utput from the inverting oscillator amplifier.

›scillator Characteristics

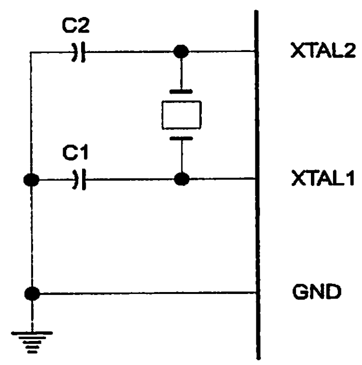
TAL1 and XTAL2 are the input and output, respectively, f an inverting amplifier which can be configured for use as n on-chip oscillator, as shown in Figure 1. Either a quartz ystal or ceramic resonator may be used. To drive the əvice from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

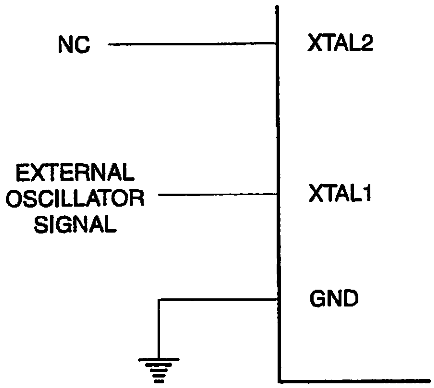


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

›tatus of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

gure 2. External Clock Drive Configuration



ower-down Mode

the power-down mode, the oscillator is stopped, and the struction that invokes power-down is the last instruction ecuted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ock Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

rogramming the Flash

ıe AT89C51 is normally shipped with the on-chip Flash əmory array in the erased state (that is, contents = FFH) ıd ready to be programmed. The programming interface :cepts either a high-voltage (12-volt) or a low-voltage $_{CC}$) program enable signal. The low-voltage programing mode provides a convenient way to program the Γ89C51 inside the user's system, while the high-voltage ogramming mode is compatible with conventional thirdırty Flash or EPROM programmers.

ıe AT89C51 is shipped with either the high-voltage or w-voltage programming mode enabled. The respective p-side marking and device signature codes are listed in e following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

ıe AT89C51 code memory array is programmed byte-byıte in either programming mode. *To program any nonank byte in the on-chip Flash Memory, the entire memory ust be erased using the Chip Erase Mode.*

rogramming Algorithm: Before programming the Γ89C51, the address, data and control signals should be ıt up according to the Flash programming mode table and gure 3 and Figure 4. To program the AT89C51, take the llowing steps.

Input the desired memory location on the address lines.

Input the appropriate data byte on the data lines.

Activate the correct combination of control signals.

Raise $\overline{EA}$/V_{PP} to 12V for the high-voltage programming mode.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89C51 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

lash Programming Modes

lode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7
Vrite Code Data		H	L		H/12V	L	H	H	H
₹ead Code Data		H	L	H	H	L	L	H	H
Vrite Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
;hip Erase		H	L	(1)	H/12V	H	L	L	L
₹ead Signature Byte		H	L	H	H	L	L	L	L

ɔte: 1. Chip Erase requires a 10 ms $\overline{PROG}$ pulse.

gure 3. Programming the Flash

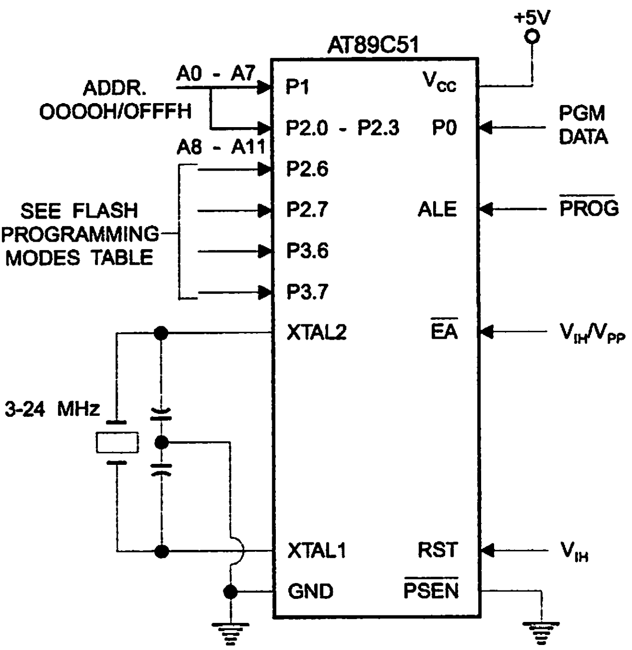
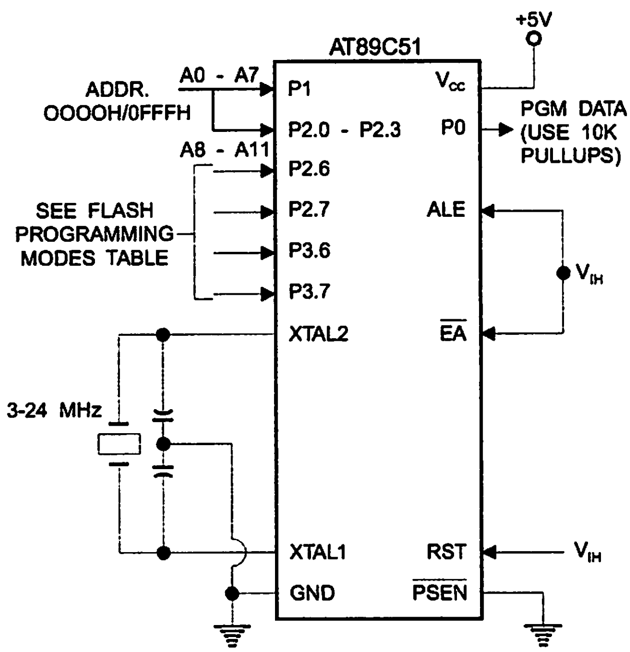
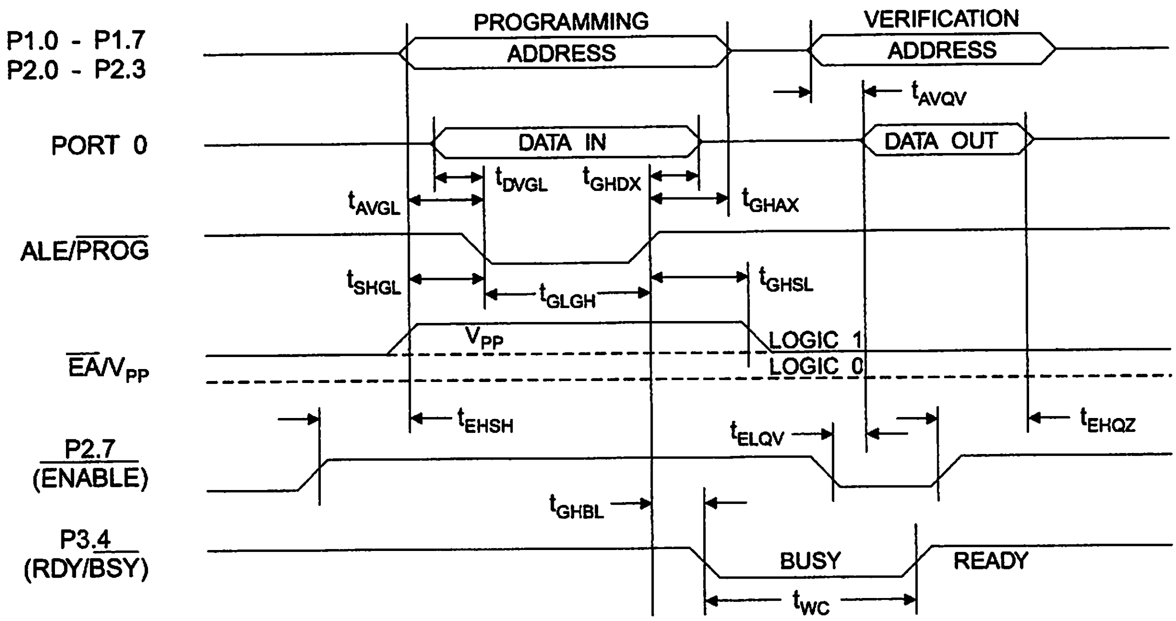


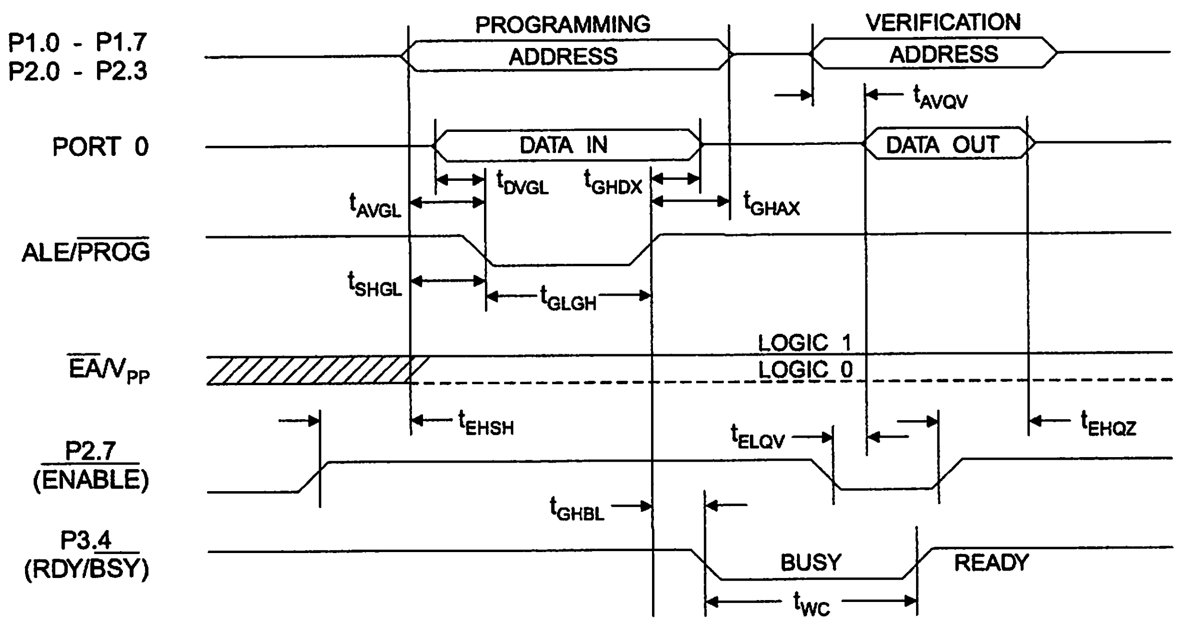
Figure 4. Verifying the Flash



lash Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



lash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



lash Programming and Verification Characteristics

, = 0°C to 70°C, V_{CC} = 5.0 ±10%

;ymbol	Parameter	Min	Max	Units
$/_{PP}$[1]	Programming Enable Voltage	11.5	12.5	V
$_{PP}$[1]	Programming Enable Current		1.0	mA
I/t_{CLCL}	Oscillator Frequency	3	24	MHz
$_{AVGL}$	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
$_{GHAX}$	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
$_{DVGL}$	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
$_{GHDX}$	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
$_{EHSH}$	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
$_{SHGL}$	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
$_{GHSL}$[1]	V_{PP} Hold after $\overline{PROG}$	10		μs
$_{GLGH}$	$\overline{PROG}$ Width	1	110	μs
$_{AVQV}$	Address to Data Valid		$48t_{CLCL}$	
$_{ELQV}$	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
$_{EHQZ}$	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
$_{GHBL}$	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	μs
$_{WC}$	Byte Write Cycle Time		2.0	ms

ote: 1. Only used in 12-volt programming mode.

bsolute Maximum Ratings*

)perating Temperature	-55°C to +125°C
3torage Temperature	-65°C to +150°C
/oltage on Any Pin vith Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
)C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

$_A$ = -40°C to 85°C, V_{CC} = 5.0V ±20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

otes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

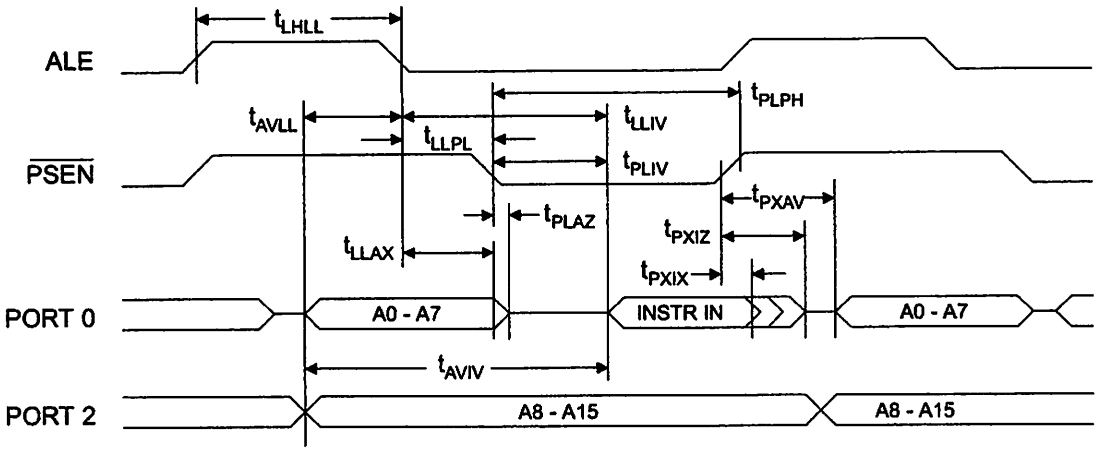
C Characteristics

ıder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ıtputs = 80 pF.

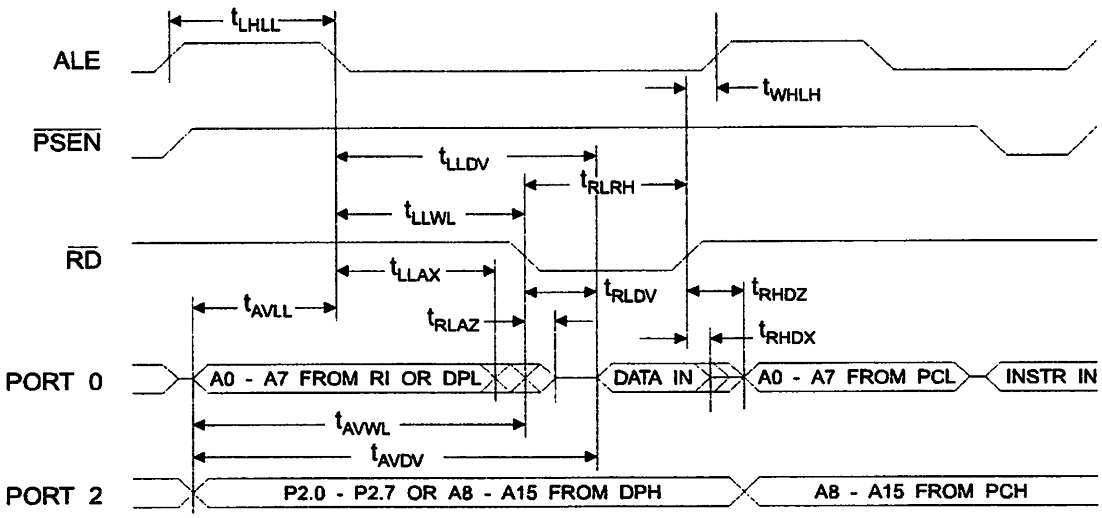
xternal Program and Data Memory Characteristics

;ymbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
l/t_{CLCL}	Oscillator Frequency			0	24	MHz
LHLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
AVLL	Address Valid to ALE Low	43		t_{CLCL}-13		ns
LLAX	Address Hold after ALE Low	48		t_{CLCL}-20		ns
LLIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LLPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
PLPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
PLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
PXIX	Input Instruction Hold after $\overline{PSEN}$	0		0		ns
PXIZ	Input Instruction Float after $\overline{PSEN}$		59		t_{CLCL}-10	ns
PXAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
AVIV	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
PLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
RLRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WLWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
RLDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
RHDX	Data Hold after $\overline{RD}$	0		0		ns
RHDZ	Data Float after $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LLDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
AVDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
AVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
QVWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
WHQX	Data Hold after $\overline{WR}$	33		t_{CLCL}-20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

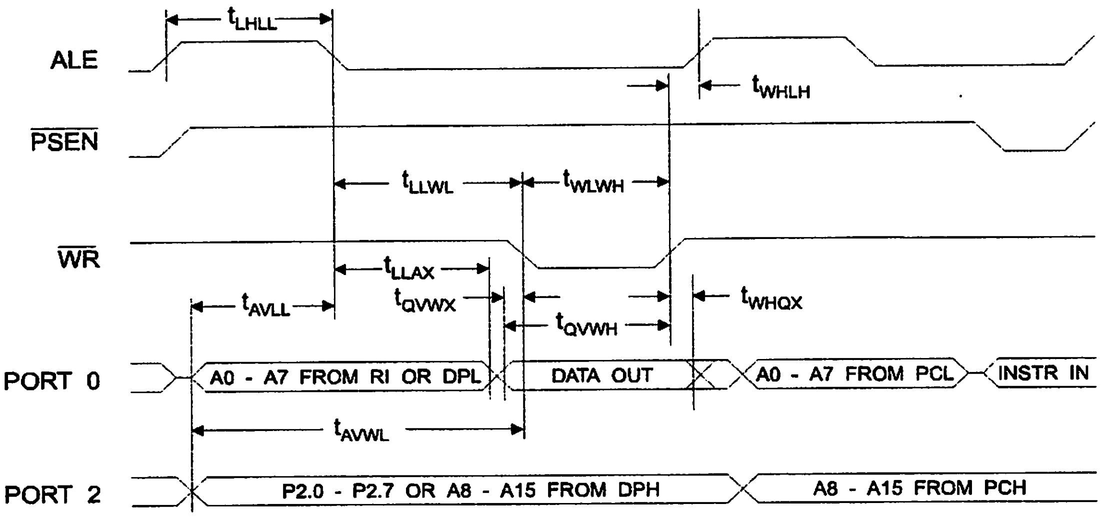
xternal Program Memory Read Cycle



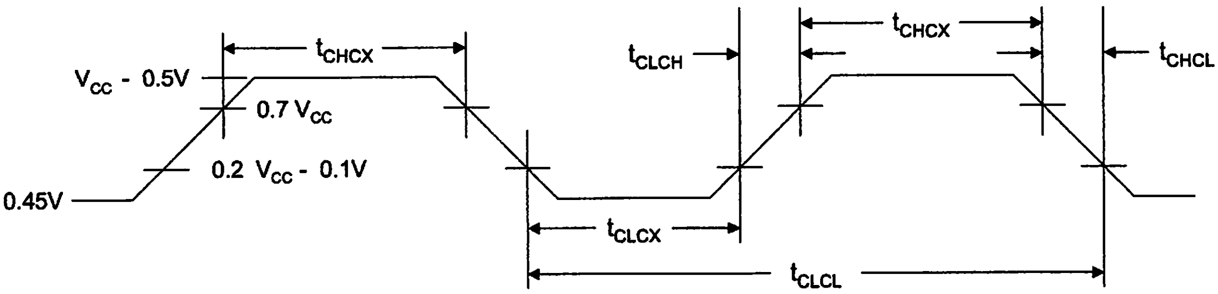
xternal Data Memory Read Cycle



xternal Data Memory Write Cycle



xternal Clock Drive Waveforms



xternal Clock Drive

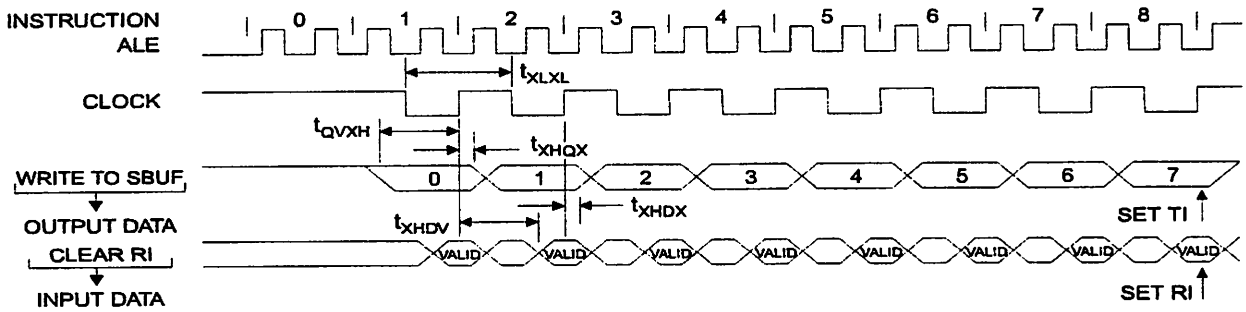
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

erial Port Timing: Shift Register Mode Test Conditions

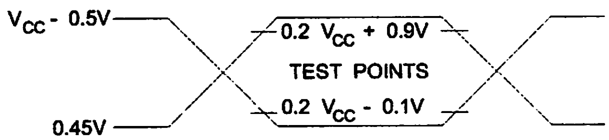
$_{CC}$ = 5.0 V ±20%; Load Capacitance = 80 pF)

ymbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
LXL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
VXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
HQX	Output Data Hold after Clock Rising Edge	50		$2t_{CLCL}$-117		ns
HDX	Input Data Hold after Clock Rising Edge	0		0		ns
HDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

hift Register Mode Timing Waveforms

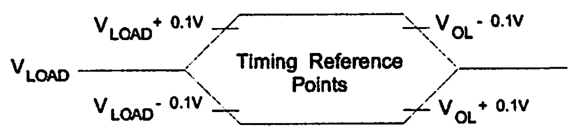


C Testing Input/Output Waveforms[(1)]



ote: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[(1)]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

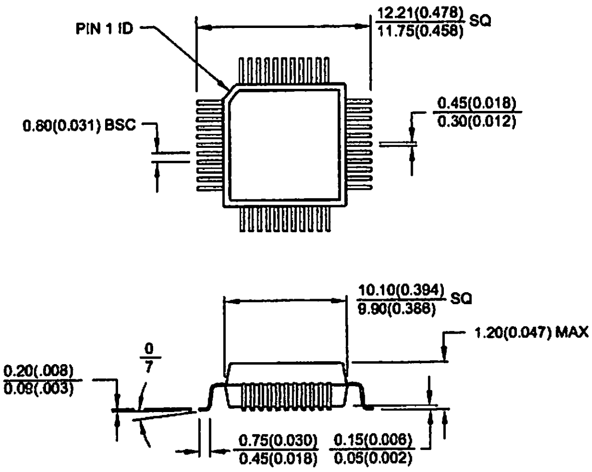
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ±20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0° C to 70° C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40° C to 85° C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ±20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0° C to 70° C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40° C to 85° C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ±20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0° C to 70° C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40° C to 85° C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ±20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0° C to 70° C)
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40° C to 85° C)
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

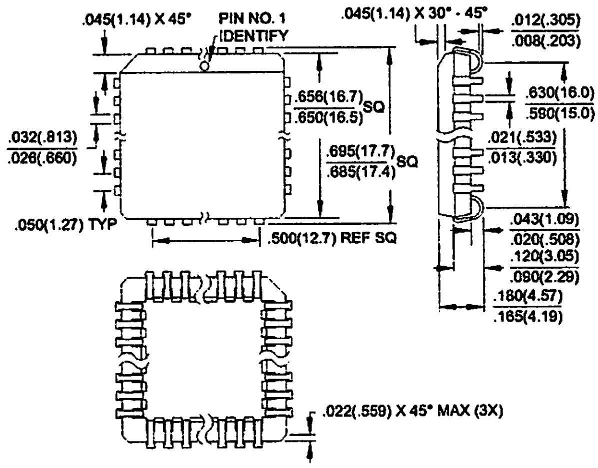
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

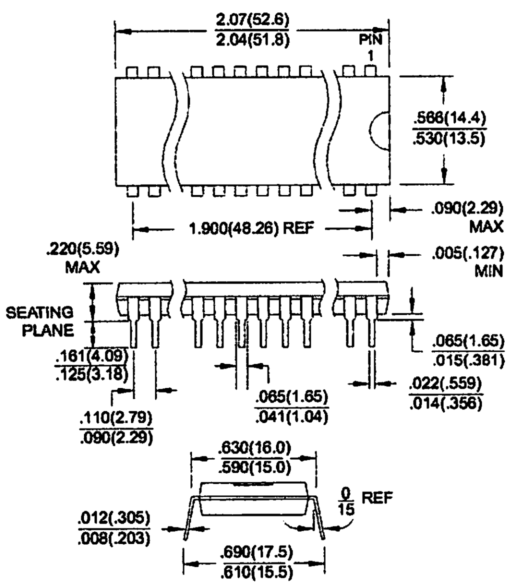


Controlling dimension: millimeters

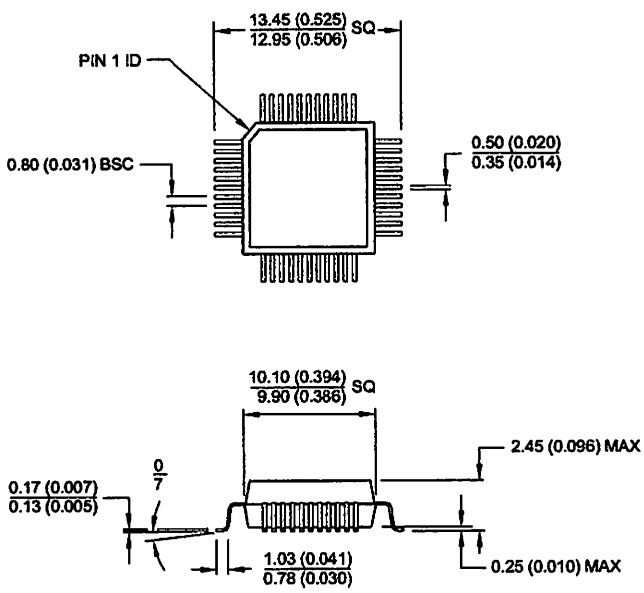
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters