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***Abstract*— We present a Cartesian I/Q modulator based on dual 10-bit RF-DACs. Non-overlapping LO signals and a segmented RF-DAC architecture with scaled bit currents contribute to good linearity and allow low-complexity DPD. Unit-cell flip-flops with a balanced clock distribution enable a high sample rate. Drive slope control for data switches reduce out-of-band emissions. Implemented in 22 nm FDSOI CMOS, the modulator operates up to 26 GHz with a maximum sample rate of 11 GS/s. The modulator is used to demonstrate transmission of a 64QAM signal at 13.2 Gb/s, a 256QAM signal at 7.33 Gb/s, and an OFDM signal comprising four aggregated 400-MHz 64QAM channels at an EVM of 6.43 %. The results demonstrate the potential of the proposed modulator architecture for realization of ultra wideband transmitters for high performance mm-wave systems.**

***Keywords*— IQ modulator, RF-DAC, CMOS**

I. Introduction

The data traffic of global mobile networks reached 78 EB per month in the 3rd quarter of 2021 [1]. For the last decade, the data traffic has a compound annual growth (CAGR) of 50 % without any sign of slowing down. To sustain such a growth, wireless networks increasingly make use of the millimeter wave (mmW) frequencies, where broad and contiguous spectrum is available. For example, most 5G mmW frequency bands defined today are around 3 GHz wide [2]. Such bandwidths impose unprecedented, yet inevitable, challenges to radio transmitters, especially at the base-station side. Unlike a handset or consumer-premises equipment, which uses only a portion of the spectrum some of the time, the radio base-stations operate over the entire spectrum all the time. Therefore, critical transmitter components, such as the digital-to-analog converters (DACs), with sufficient dynamic ranges and bandwidths for modern communication signals are keenly in need. In particular, CMOS implementation brings tight integration and low cost in such applications [3].

Complex modulation formats such as high-order QAM can provide high data rates per channel bandwidth, but require low Error Vector Magnitude (EVM) for low Bit-Error Rate (BER) [4]. These accuracy requirements, in turn, require high-resolution D-to-A conversion. Additionally, practical use of a modulator in a wireless system necessitates high Adjacent Channel Power Ratio (ACPR) values, enabled by oversampling to push out image signals far enough to be suppressed with a linear filter; but oversampling increases the sample rate far beyond Nyquist. Even with oversampling, modulator non-linearities will cause the ACPR to deteriorate; digital pre-distortion (DPD) may be used to linearize the conversion, at the cost of computations or table lookups performed at very high sample rate. Although DPD can be used to compensate transmitter nonlinearities, a linear and well-behaved RF-DAC transfer characteristic is desirable as it may allow DPD complexity to be reduced. A segmented non-linearly scaled RF-DAC with increasing transistor widths for higher output codes has been shown as a way to self-linearise RF-DAC output [5]. To design a high-resolution, high-sample-rate modulator with non-linearities that are easy to compensate for is nevertheless a considerable challenge.

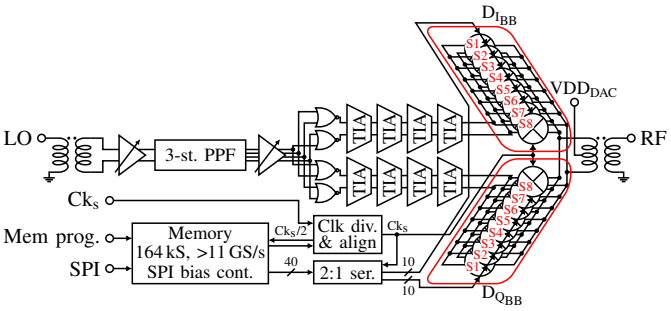


Fig. 1. RF-IQ modulator block diagram showing the full RF path and the on-chip supporting circuitry. The segmented RF-DACs are encircled in red.

In this paper, we present a Cartesian RF-DAC modulator designed with these issues in mind. The modulator is realized in 22 nm CMOS and operates within the 20–26 GHz frequency range. With a 2×10 b resolution and 25 %-duty-cycle LO signals, it supports data bandwidths of 13.2 Gb/s for a 64QAM signal at 11 GS/s, or 7.33 Gb/s for a 256QAM signal. This performance is reached using only a 1D DPD based on a memoryless third-order polynomial function.

II. Design

A block diagram of the complete 2×10 b RF-IQ modulator is shown in Fig. 1, including the 25 %-duty-cycle quadrature LO generation, the two 10 bit RF-DACs, and the on-chip memory used for storing the baseband I/Q waveforms.

A. Quadrature LO generation

Accurate quadrature LO signals are essential in order for precise generation of high-order QAM signals. Generating

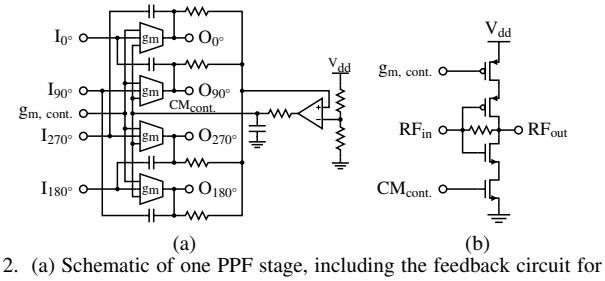


Fig. 2. (a) Schematic of one PPF stage, including the feedback circuit for the common-mode control. (b) Schematic of the g_m cell used in the PPF stages.

these LO signals with the target of driving RF-DACs further adds to the challenge due to the large capacitive load presented by the RF-DACs. In addition to the large total transistor width, the distributed layout, with LO distribution to all unit cells, further increases the load seen by the LO drivers.

The quadrature phases are generated with a 3-stage active poly-phase filter (PPF) using a g_mC topology [6]. A schematic of one PPF stage is shown in Figure 2a together with the g_m cell in Fig. 2b. For a unit amplitude imbalance, the inputs to the first stage are connected using the Type-II configuration presented in [7]. The g_m cell is based on an inverter topology, featuring an additional top-placed PMOS transistor for transconductance control. In addition, a bottom-placed NMOS transistor combined with a feedback network keep the common-mode voltage constant, thus eliminating the need for DC-block capacitors between the filter stages. VGAs are located before and after the PPF to allow a constant signal swing independently of the filter bias settings. In a multiple-input-multiple-output (MIMO) transceiver, the active PPF can be shared among multiple transmitters by dividing the output signal into multiple paths, thereby reducing the cost, both in terms of power and area, per transmitter.

Non-overlapping LO signals [8] are used to reduce the cross-modulation distortion resulting when the I- and Q-branches are directly summed at the output of the RF-IQ modulator, see Fig. 1. CML-NOR gates form the non-overlapping signals from the quadrature sine-wave signals provided by the PPF. Two signals with 90° offset are fed to the parallel NMOS transistors while a single PMOS transistor is used for bias and gain control. The signals are then buffered through two 4-stage TIA buffers that drive the RF-DACs. With non-overlapping LO signals, the DC-level is no longer at half the peak-to-peak voltage as for sine-wave signals. Rather, the level is dependent on the signal duty cycle, varying from stage to stage as a result of the TIAs inverting characteristic. A large output voltage swing is enabled by asymmetrically sized TIAs that shifts the switch-voltage towards the DC-level.

B. Segmented RF-DAC

A high DAC linearity is essential to support high-order QAM modulation without using high-complexity DPDs. A segmented non-linear scaling combined with bias tuning has been demonstrated as a method for achieving a highly linear RF-DAC [5]. With non-overlapping LO signals, we can apply the same linearisation concept also to a Cartesian RF-IQ modulator, using two segmented RF-DACs, each having 8

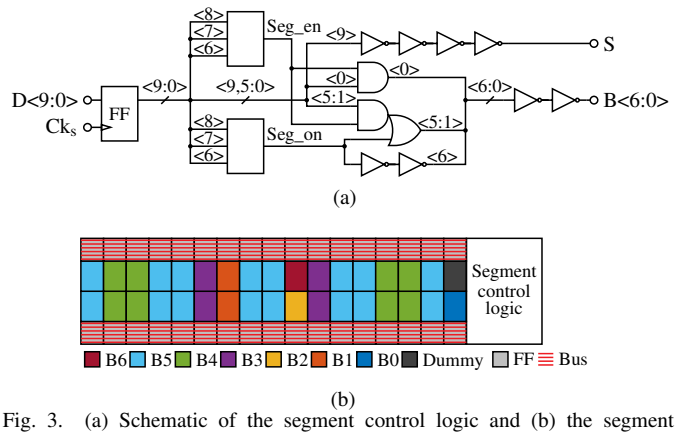


Fig. 3. (a) Schematic of the segment control logic and (b) the segment floorplan showing the placement of the binary grouped unit cells.

segments. Each DAC uses a ratio of 1.4 between the unit cell sizes in the lowest and highest segments. Although the scaling is realized in hardware, the non-linear characteristic can be tuned through the LO magnitude and/or VDD_{DAC}.

For effective operation at a high sample rate, a fast and regular segment control logic is essential. We use binary scaling within each segment, allowing for a minimalistic segment decoding logic, shown in Fig. 3a. Here, the signals *Seg_en* and *Seg_on* are realized using three-input gates unique to each segment; the former signal enables the segment in binary mode, while the latter activates all the unit cells in the segment. The segment floorplan is shown in Fig. 3b, highlighting the unit cell placement. Each segment contains 32 unit cells and one half-size LSB cell.

The segment unit cells are based on the topology presented in [3]. The in-cell flip-flops relax the alignment constrains for the control signals and simplify the layout, as only a single signal (the sample clock) requires careful alignment throughout the RF-DAC core. This clock is distributed using a single H-tree per core. A drive slope control for the RF-DAC data switches allows for increased rise/fall times at lower sample rates, which reduces out-of-band emissions while only slightly affecting the in-band performance [9].

C. Input and output RF matching

The input and output matching networks were implemented using interleaved baluns located in the topmost metal layers. The baluns provide the single-ended/differential conversion, while their inductance resonate out circuit capacitance at the center frequency. Shunt MOM capacitors were used to tune the matching to the desired band. In the output matching network, these capacitors are switchable to allow for band adjustments.

D. Test circuitry

In order to evaluate the RF-IQ modulator, a variety of digital baseband I/Q waveforms must be provided at a high sample rate. A 164 kS, >11 GS/s SRAM memory generates these signals on-chip. The memory is programmed through a low-speed serial interface. Digitally programmable on-chip bias sources are used to reduce the pad-count.

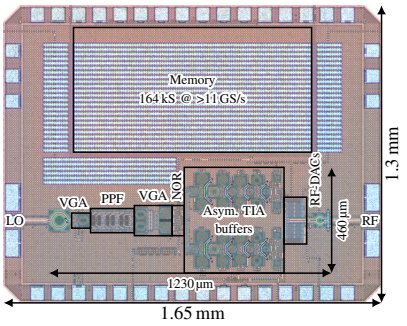


Fig. 4. Chip photo of the 20–26 GHz RF-IQ modulator. Core area is dominated by the LO generation. The chip area is limited by the waveform memory.

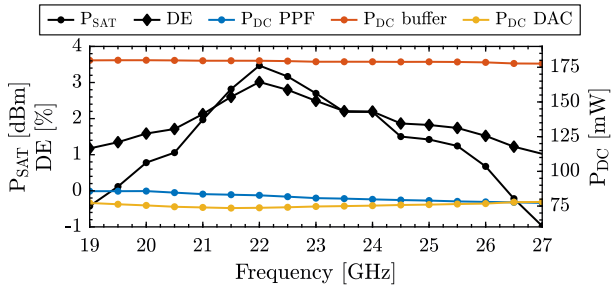


Fig. 5. Saturated RF output power, drain efficiency, and transmitter power consumption for the poly-phase filter, TIA buffers, and the RF-DACs versus carrier frequency. The power consumption for the RF-DACs does not include the digital parts.

III. Experimental Results

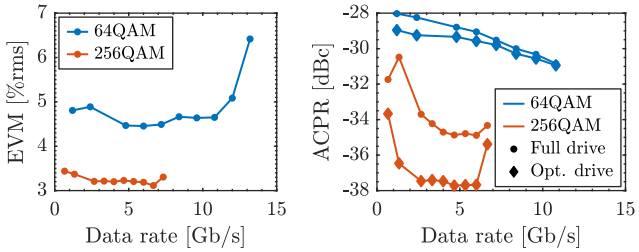
The RF-IQ modulator, shown in Fig. 4, has been implemented using GlobalFoundries 22 nm FDSOI CMOS process. The entire design, including the LO generation circuitry, measures 1230 µm × 460 µm. The RF-DACs alone measure 80 µm × 200 µm. The full chip including pads measures 1.65 mm × 1.3 mm; the area is dominated by the waveform memory.

The design has been evaluated up to a sample rate of 11 GS/s using the coplanar LO and RF pads as the calibrated reference planes.

A. Continuous-wave measurements

The static properties of the RF-IQ modulator were evaluated using a Keysight PNA-X vector network analyser. The saturated output power, drain efficiency (DE), and DC power consumption for the poly-phase filter, TIA buffers and the RF-DACs (not including their digital circuits) are shown at different carrier frequencies in Fig. 5. All static performance was evaluated with all unit cells active in both RF-DACs. The measured 3 dB bandwidth is between 20–26 GHz, with a peak output power of 3.47 dBm at 22 GHz.

An image-rejection ratio (IRR) >35 dB has been measured across the range 19–25 GHz. The amplitude- and phase-imbalance have been measured to be <0.2 dB and <2°, respectively, in this range. The IRR has been measured at the output of the RF-IQ modulator; thus, the quadrature LO generation on its own is expected to achieve a higher IRR.



(a) (b)

Fig. 6. (a) EVM and (b) ACPR versus data rate for different modulation formats and full/optimum drive slope setting, all with a BER $<10^{-3}$. Instrument limitations prevent ACPR measurements for the widest-band 64QAM signals.

B. Wideband modulated measurements

The dynamic performance has been evaluated at 23 GHz using 64- and 256QAM single-carrier (SC) signals at up to 11 GS/s, and also 64QAM OFDM signals at up to 9 GS/s. The SC signals were oversampled 5× and 12× respectively, using a digital RRC pulse shaping filter with 0.1 rolloff factor. The OFDM signals were zero-padded to fill all tones provided by the higher sample rate. In addition to the segmented scaling, a static memoryless 1D third-order polynomial DPD was used in all wideband modulated measurements to compensate for a small amount of residual compression.

Measurements of the wideband modulated RF signals were performed using the vector network analyser in spectrum-analyser mode. The measured EVM and ACPR are presented versus data rate in Fig. 6. In Fig. 6b, a large ACPR improvement is visible when optimizing the drive slope setting (the EVM is substantially unchanged). The ACPR improvement seen for higher data rates is caused by the output matching network, which brings an increased suppression of the noise-floor far-out from the channel. Constellation diagrams and output spectra are shown in Figs. 7a to 7d for the 64- and 256QAM SC signals. The combined constellation for a 4×400 MHz 64QAM OFDM signal is shown in Fig. 7e together with the OFDM spectrum in Fig. 7f. With modulated signals, the RF-DACs consume 18.1 mW for the RF output, and 9.7 mW/(GS/s) for the digital circuits including clock distribution in the RF-DAC cores.

The 2×10 b RF-IQ modulator is compared with the state-of-the-art implementations in Table 1. For 64QAM SC, an EVM <6.42 % and an ACPR <-28.9 dBc is achieved up to a peak data rate of 13.2 Gb/s at 11 GS/s. With 256QAM SC, an EVM <3.31 % and an ACPR <-33.7 dBc is achieved up to a peak data rate of 7.33 Gb/s at 11 GS/s. The RF-IQ modulator is also capable of up to 4 aggregated 400 MHz 64QAM OFDM channels with an EVM <6.43 % and an ACPR <-28.4 dBc, giving a peak data rate of 8.52 Gb/s, at a sample rate of 9 GS/s.

IV. Conclusion

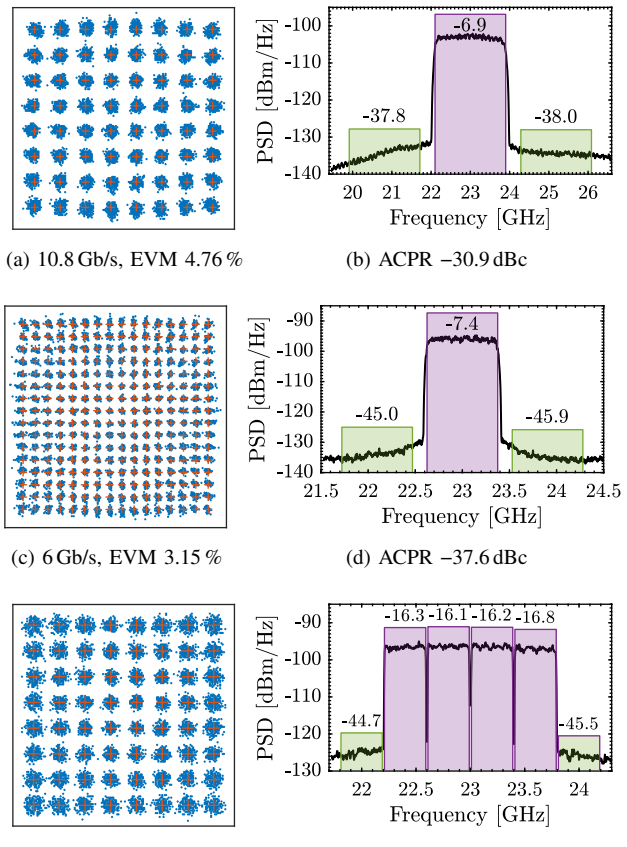
We have presented a 2×10 b, 11 GS/s, 20–26 GHz Cartesian RF-IQ modulator implemented in a 22 nm FDSOI technology. The high sample rate enabled by the 22-nm CMOS technology together with the high resolution, segmented non-linear scaling, and a simple 1D polynomial DPD enable high-order

Table 1. Performance comparison with published CMOS RF modulators at 23 GHz and up, supporting at least 64QAM.

	This work			[10]	[11]		[12]	[13]	[9]
Technology	22 nm SOI			45 nm SOI	28 nm		22 nm SOI	28 nm	28 nm
Topology	Cartesian			Cartesian	Cartesian		Cartesian	Polar	Polar
Resolution [b]	2×10			2×6	2×10		2×6	2×7 (p) 7 (m)	10 (p) 6 (m)
Frequency [GHz]	20–26			18–32	20–32		28	60–67[1]	59–71
Supply voltage [V]	0.85			4.5–6	1		0.9/1.8	0.9	0.9
Peak P_{sat} [dBm]	3.47			19.9	19.02		21.23	12.6	11.5
Drain efficiency [%]	3			15.6	34.4		36.7	25.9	42
Modulation format	64QAM SC	256QAM SC	64QAM OFDM	64QAM SC	64QAM SC	256QAM SC	64QAM SC	64QAM SC	64QAM SC
Sample rate [GS/s]	11	11	9	2[2]	2		2.4	5.28[3]	3.52[2]
OSR	5	12	-	1	4	16	-	3[3]	1
EVM [%rms]	6.42	3.31	6.43	4	3.59	2.75	3.31	4.07	5.82
ACPR [dBc]	−28.9	−33.7	−28.4	-	−33.6	−32.4	−30.8	-	-
Data rate [Gb/s]	13.2	7.33	8.52[4]	12	3	1	2.4	10.56	42.2[5]
Area [mm^2]	<0.47			2.41[6]	0.2		2.2[6]	<0.115	3.24[6]

[1] Graphically estimated. [2] Highest sample rate achieving at least 64QAM. [3] 2× interpolation in DAC. [4] 4 aggregated 400 MHz channels.
[5] Two transmitters using different polarizations. [6] Including pads.

QAM formats with multi-GHz bandwidths. To the best of our knowledge, this is the first time that a CMOS RF-IQ modulator has been demonstrated to support up to 4 aggregated 400 MHz 64QAM OFDM channels simultaneously.



(a) 10.8 Gb/s, EVM 4.76 % (b) ACPR −30.9 dBc

(c) 6 Gb/s, EVM 3.15 % (d) ACPR −37.6 dBc

(e) 8.5 Gb/s, EVM 6.43 % (f) ACPR −28.4 dBc

Fig. 7. Constellation diagrams and output spectrum for SC-64QAM (a) and (b), SC-256QAM (c) and (d), and 4×400 MHz OFDM-64QAM (e) and (f), all achieving a BER <10^{-3}. A sample rate of 9 GS/s is used in all three cases. Band power is presented in dBm.

ACKNOWLEDGMENT

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