Model of Switched-Capacitor Programmable Voltage Reference: Optimization for Ultra Low-Power Applications

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***Abstract*—This paper proposes an analytical model for the optimized design of a switched-capacitor programmable voltage reference (SC-PVREF). This PVREF topology guarantees a straightforward design, easy portability across different technology nodes, and does not require any special technology option. The developed model allows the study of the trade-offs and the a priori evaluation of the system performance. Circuit optimization is carried out with MATLAB and permits SC-PVREF to achieve current consumptions of tens of nanoampere, suitable for ultra low-power applications.**

***Index Terms*—Programmable voltage reference, switched-capacitor, modelling, bandgap, circuit optimization, ultra-low power applications.**

I. Introduction

Systems-on-chips for IoT applications require accurate and low-power voltage references. Recent technology and circuit design advancements have allowed quiescent currents at nanoampere levels both in supply circuits and in the generation of the voltage references [1]. Moreover, in power-constrained applications large benefits can be obtained by the programmability of the voltage references. Indeed, programmable voltage references PVREFs can be exploited to limit the energy consumption in digital with dynamic voltage scaling. Additionally, in analog domain, they allow to precisely control the operating range of start-up circuits, and to reduce the power consumption in voltage regulators [2]. By using unity gain feedback, the current consumption I_{DD} due to the feedback resistors can be avoided [3]. Fig. 1 shows four approaches in literature for generation of a programmable voltage reference. The continuous time (CT)-PVREF in Fig. 1(a) aims to overcome the trade-offs among power consumption, area, and range of programmability. The voltage reference V_{REF} is derived from a leakage-based bandgap circuit without calibration [2]. The reference programmability is obtained by the selection with a multiplexer of the tapping point in the bandgap load. This approach achieves remarkable figures of merit, but it is severely penalized by the large process variations of the bandgap topology [4]. The floating gate-based (FG)-PVREF approach is shown in Fig. 1(b). Here, after the write phase, a defined amount of charge is stored to set V_{FG}. The voltage is then buffered to provide driving capability. Floating gate devices guarantee very long retention, and no additional circuits for V_{REF} verification are required. This PVREF benefits of a simple and straightforward design, at the cost of the integration of a non-standard technology

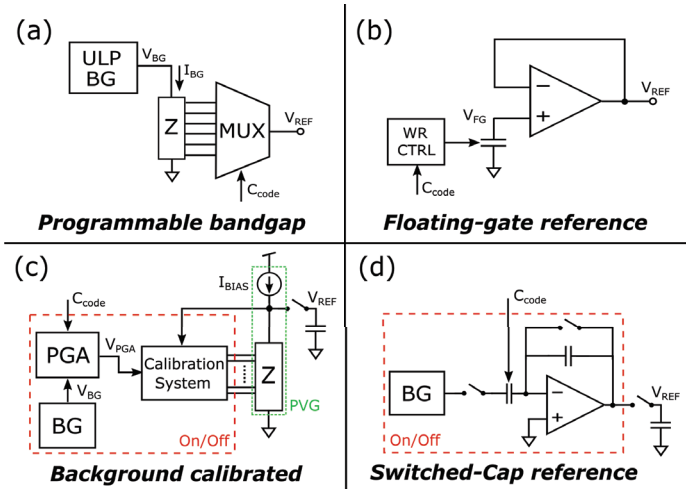

Fig. 1: *Approaches for PVREF implementations in literature: (a),(b) continuous time; (c),(d) duty cycle-based.*

option [5], [6]. For PVREF generation also duty cycle-based topologies, like those in Fig. 1(c) and 1(d), have been proposed in literature. The background-calibrated (BC)-PVREFs in [1] periodically calibrates an ultra low-power voltage reference generator (PVG), by means of the bandgap output V_{BG}, amplified with a programmable gain amplifier (PGA). After the calibration, all the power-hungry circuits are turned off. A re-calibration system is turned on periodically to compensate V_{REF} variations due to the low temperature coefficient of PVG. Big energy saving is obtained with large duty-cycles of re-calibration. Despite the remarkable metrics, BC-PVREF requires a complex mixed-signal architecture. A continuous time switched capacitor (SC) PVREF implementation is proposed in [7]. This topology provides a large and accurate programmability, at the cost of an I_{DD} of tens of microampere. The voltage V_{BG} is provided to an SC amplifier, where a controllable capacitance ratio sets the desired amplification. A duty cycled-based SC-PVREF can be exploited to reduce the average I_{DD}, periodically turn on the power-hungry circuits, and refresh the voltage reference, Fig. 1(d). In this scheme, the temperature coefficient of V_{REF} is dictated directly by V_{BG}. Hence, this SC-PVREF does not need any complex background calibration. Moreover, compared with CT and FG PVREFs, it does not require any special technology option, and it can be easily ported in different nodes.

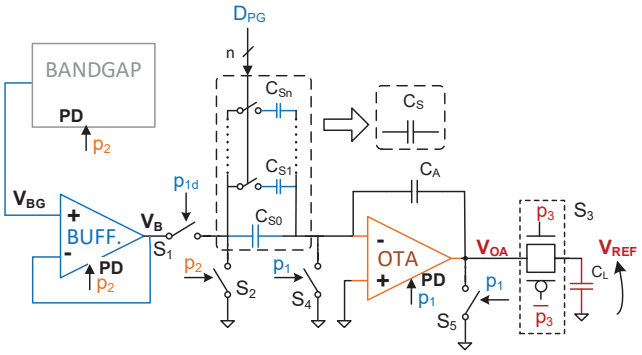

Fig. 2: *Schematic view of the SC-PVREF.*

This paper proposes an analytical model for the optimized design of a duty cycle-based SC-PVREF. The model, developed in MATLAB, allows the evaluation of the trade offs of this topology, and to obtain current consumption suitable for ultra low-power applications.

II. SC-PVREF

The schematic of an SC-PVREF is shown in Fig. 2. In this design, the voltage stable on temperature V_{BG} is generated by a low-power bandgap circuit, and provided to the SC amplifier for the desired amplification. Ultra low-power bandgap circuits suffer for limited driving capability. Therefore, a unity-gain buffer must be used to drive the sampling capacitor of the PGA C_S, controlled by the switches S1, S2, and S4. In Fig. 2, the gain variation is obtained by changing the sampling capacitor with an array of binary scaled capacitor, i.e. from C_{S0} to $C_{S1} \cdot (2^n - 1) + C_{S0}$, controlled by the code D_{PG}. This scheme allows an amplifier output voltage range V_{OA} from $V_{REF,min}$ to $V_{REF,max}$:

$$V_{REF,min} = \frac{C_{S0}}{C_A} \cdot V_{BG} \quad (1)$$

$$V_{REF,max} = \frac{C_{S1} \cdot (2^n - 1) + C_{S0}}{C_A} \cdot V_{BG} \quad (2)$$

Finally, V_{OA} is sampled by means of the switch S3, and stored on the capacitor C_L. Fig. 3 shows the timing diagram used for the control of the SC-PVREF. Here, the bandgap and the buffer are enabled only in the sampling phase, with p_1 high and p_2 and p_3 low, to limit the power consumption. While C_S samples the output buffer voltage V_B, the amplifier is in power-down. The OTA output is shorted to ground by the switch S_5, and disconnected from the output node, with S_3 open. In the next phase, with p_2 high, the amplifier is turned on for the amplification of V_{BG}, and V_{OA} settles to $G \cdot V_B$, with G=C_S/C_A, set by D_{PG}. The signal p_{1d} is slightly delayed with respect to p_1 to avoid the charge injection from the input switch [8]. In the refresh phase with p_3 high, the OTA output is connected to the capacitor C_L through the transmission gate S_3. This phase is mandatory to compensate the accumulated error of V_{REF} in the previous phase, due to the leakage current through the transmission gate S_3. Finally, in the sleep phase, all the circuits are kept off-state to save energy. The system periodically wakes up to refresh or reprogram the output voltage V_{REF} on the capacitor C_L.

A. SC-PVREF Model

This section describes with equations the analytical model of the SC-PVREF in Fig. 2. The model computes the system current consumption I_{DD}, starting from a target maximum reference output noise v_{REFn}. The value of the sampling capacitance C_S of the PGA is obtained from the root mean square value of v_{REFn}, with a gain G_x=C_{Sx}/C_A:

$$G_x^2 \cdot \left(\frac{k\,T}{C_{Sx}} + \frac{2kT\gamma}{C_{Sx}} + \frac{2kT\gamma}{G_x C_L} + \frac{kT}{G_x^2\, C_L} \right) \leq \alpha_n^2\, v_{REFn}^2 \quad (3)$$

where α_n^2 is the noise budget contribution relative to the SC-PVREF, excluding the bandgap, to the overall PVREF noise power v_{REFn}^2, k is the Boltzmann constant, T the absolute temperature, γ the noise gamma factor of the input devices in the buffer and the OTA [9]. The first and last terms in the brackets in (3) are the kT-over-C noise contributions of C_S and C_L, respectively, while the second and the third terms refer to the buffer and the OTA, respectively. This approximation holds assuming first-order transfer function, and the input devices of OTA and buffer as the main noise contributors. The value of α_n is an optimization parameter and depends on the power consumption and noise of the bandgap reference. As matter of example, the designs in [10] and [11] report with V_{BG} = 1.2 V output noise contributions of 200 μV, with a current consumption I_{DD} = 13 nA, and 80 μV, with I_{DD} = 420 nA, respectively.

The settling error of V_B in the sampling phase affects the output reference V_{REF}. Such error contribution, evaluated at the maximum gain G_{max}, is constrained below a maximum value, e_{sOUT}

$$e_{sB} \equiv V_B^{\infty} - V_B\,(t_S) \leq \frac{e_{sOUT}}{G_{max}} \quad (4)$$

where V_B^{∞} is the asymptotic value of $V_B(t)$ after the rising edge of p_1. Since the transistors are biased in weak inversion, the $V_B(t)$ transient from t_0 to t_1 is affected by the slew rate limit SR_B, which is calculated from the current consumption of the buffer I_B:

$$SR_B = \frac{I_B}{\beta_B\, C_S} \quad (5)$$

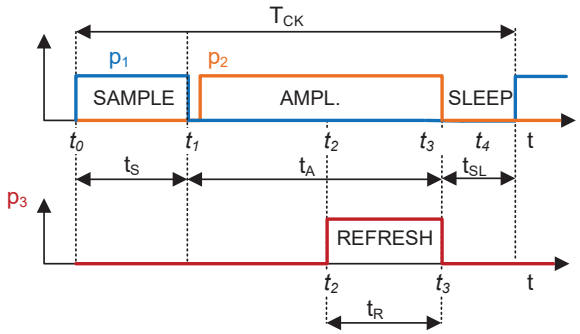

Fig. 3: *Timing diagram of the SC-PVREF.*

In our model, the coefficient β_B depends on the amplifier topology, and it represents the ratio between the buffer current consumption I_B and the bias current of the input pair. For a single-stage operational amplifier β_B=1 and for a folded-cascode amplifier β_B=2. Thus, V_B in the sampling phase is approximated with the following piecewise function:

$$\begin{aligned} V_B(t) &= SR_B \cdot t \;\forall\, t \le t_{xB} \\ V_B(t) &= V_{BG} + a_B \cdot exp\left(-\frac{t}{\tau_S}\right) \;\forall\, t > t_{xB} \end{aligned} \tag{6}$$

where the time shift $t_0 \rightarrow 0$ has been implemented. The values of b_B and t_{xB} are found by ensuring the continuity and the derivability of $V_{REF}(t)$ at the switch time t_x between the slew-rate limited and the exponential settling transient phases. The time constant τ_S is equal to $R_{OB}\,C_S$, where R_{OB} is the closed-loop output resistance of the buffer. The model assumes a first-order open-loop transfer function for both buffer and OTA. In the amplification phase of Fig. 3, the OTA is switched on and the output voltage V_{OA} must settle within the target error, i.e. e_{sOUT}, at t_2. As for the buffer output in (6), the signal $V_{OA}(t)$ from t_1 to t_2 is approximated by a piecewise function, modeling the slew-rate regime and the exponential settling:

$$\begin{aligned} e_{sO} &= (G_{max} \cdot V_{BG}) - SR_O \cdot t'_A \;\; \forall\, t'_A \le t_{xO} \\ e_{sO} &= -a_O \cdot exp\left(\frac{t'_A}{\tau_{OTA}}\right) \;\; \forall\, t'_A > t_{xO} \end{aligned} \tag{7}$$

where $t'_A = t_A - t_{suO} - t_R$, being t_{suO} the OTA start-up time, SR_O the OTA slew-rate, and the time constant τ_{OTA} related to C_S and the OTA transconductance G_M, i.e. $\tau_{OTA} \approx C_S/G_M$. In the previous sleep and sampling phases, and in the interval of the amplification phase from t_1 to t_2, the output capacitor is disconnected from the OTA and discharged through the off-state resistance of the switch S_3, i.e. R_{OFF}. The SC-PVREF is sized to limit the drop of the output voltage V_{REF}, with S_3 open, below ΔV, i.e. $G \cdot V_{BG} - V_{REF}(t_2) \le \Delta V$.

$$G \cdot V_{BG} \cdot \left[1 - exp\left(\frac{T_{CK} - t_R}{R_{OFF}\,C_L}\right)\right] \le \Delta V \tag{8}$$

In the refresh phase with p_3 high, the correct output voltage is restored and V_{REF} exponentially settles to the programmed reference value starting from $G{\cdot}V_{BG}{-}\Delta V$. It is worth noticing that with ΔV lower than tens of millivolt, no slew-rate limiting occurs at the OTA output. Also in this case the settling error is constrained to be lower than e_{sOUT}:

$$\Delta V \cdot exp\left(\frac{-t_3}{R_{ON}C_L}\right) \le e_{sOUT} \tag{9}$$

where R_{ON} is the on-resistance of S_3. The static current consumptions of the buffer and the OTA are estimated from their output resistance R_{OB} and transconductance G_M, respectively:

$$I_B \;\approx\; \beta_B \frac{2\,n\,v_{th}}{R_{OB}} \tag{10}$$

$$I_{OTA} \;\approx\; 2\,\beta_{OTA}\,n\,v_{th}\,G_M \tag{11}$$

where the devices in the buffer and the OTA are assumed in weak inversion, the coefficient β_{OTA} depends on the OTA topology as for β_B, n is the slope factor, and v_{th} the thermal voltage. The overall power consumption of the SC-PVREF is estimated starting from (10) and (11) with:

$$\begin{aligned} I_{DD} = I_{osci} &+ \frac{t_S}{T_{CK}} \cdot (I_{BG} + I_B) + \\ &+ \frac{t_A}{T_{CK}}\, I_{OTA} + \frac{C_S\, V_{BG}^2}{T_{CK}\, V_{DD}} + \\ &+ \frac{C_L}{2T_{CK}\, V_{DD}} \left[V_{REF}^2 - (V_{REF} - \Delta V)^2\right] \end{aligned} \tag{12}$$

where V_{DD} is the supply voltage. In (12), the fourth and the last terms are the average dynamic current, supplied by the buffer and the OTA to charge C_S and C_L, respectively. A consumption approximation of 1 pA/Hz is common in literature for the joint contribution of the oscillator and clock driver, i.e. I_{osci}. In the model, I_{osci} is doubled to include the generation with delay lines of the other control phases, from the clock signal T_{CK}. The current consumption of the bandgap I_{BG} can be estimated from the state-of-the art designs reported in literature. A value in a range from tens to hundreds of nanoampere is a solid assumption, considering bandgap topologies featuring high accuracy and stability over process corners [4]. The value of C_S is calculated from the noise budget as in (3). All the contributions of the settling error at the output are constrained one order of magnitude below the programmability step, i.e $\frac{C_{S1}}{C_A} \cdot \frac{V_{BG}}{10}$. The aspect ratio of the MOS devices in S_3, $(W/L)_3$ is linked to the R_{ON} and R_{OFF} values computed at $(W/L)_3$ = 1, for the selected technology node. The design optimization of the SC-PVREF of Fig. 2 targets the minimum current consumption I_{DD}, starting from the maximum acceptable drop affecting V_{REF} in (8), the value of C_L, constrained by a pre-defined silicon area, and the output noise, through α_N. The free parameters in the design are: C_S, t_S, t_R, T_{CK}, $(W/L)_3$, I_{BG}, and I_{OTA}.

III. Simulation Results

A MATLAB script has been developed to extract from the proposed model, with a gradient-based function, the set of optimum parameters for the design of the SC-PVREF. The optimization targets the minimum system current consumption I_{DD}, with noise and area as possible design constraints. Indeed, from the output noise specification the bandgap noise and the value of α_n are obtained. Whereas, the value of C_L is determined by the area constraint and by the capacitance density, in the chosen technology node.

Fig. 4(a) and Fig. 4(b) show the results of two optimizations in a 55-nm technology, sweeping C_L, with $\alpha_n = 0.05$ and $\alpha_n = 0.25$, respectively. The design settings are v_{REFn} = 400 μV and ΔV $\le$500 μV. In both graphs, the maximum I_{DD} corresponds to the minimum C_L, and in the low-noise scenario of Fig. 4(a) emerges clearly the trade-off between I_{DD} and the occupied area. In the scenario of Fig. 4(b), a minimum I_{DD} value, below 10 nA, is found for a range of C_L from

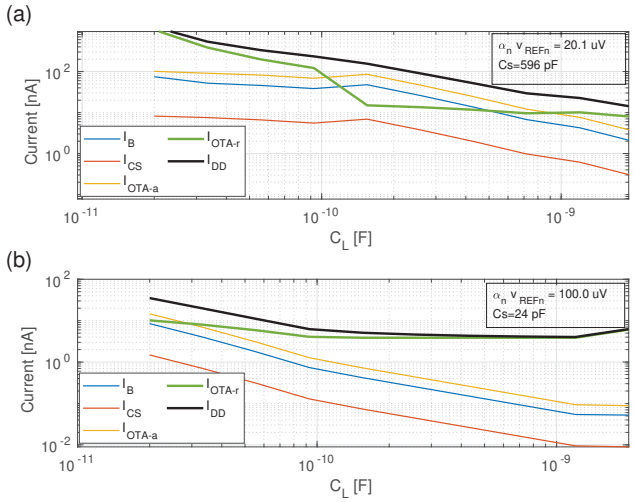

Fig. 4: *Estimated I_{DD} of the SC-PVREF vs. C_L with α_n=0.05 (a) and α_n=0.25 (b).*

400 pF to 1n F, approximately. Therefore, the proposed model allows the concurrent optimization of current consumption and silicon area in the higher-noise case. The current consumption of the OTA in the whole amplification phase, i.e. I_{OTA-a}+I_{OTA-r}, overrides the contributions of the buffer I_B, and of the sampling capacitor I_{CS}, for every value of C_L. Since the contribution of the bandgap I_{BG} is negligible, its current consumption requirement can be relaxed, targeting better accuracy and temperature coefficient. The bar chart in Fig. 5 reports the detailed average current consumptions of the SC-PVREF blocks for the low-noise scenario in Fig. 4(a), with C_L= 1 nF. The current consumptions of the timing circuit I_{osci} and due to the C_L capacitor I_{CL} are also reported. Fig. 6 shows in contour plot the results of the I_{DD} optimization, while sweeping C_L and the output noise. The graph confirms that the low-noise scenario is penalized by the trade-off I_{DD}-C_L. On the other hand, in scenarios with more relaxed noise specifications, SC-PVREF can achieve low I_{DD} with small C_L, and hence small area. Finally, we point out that, through the proposed model, current consumptions in the range of

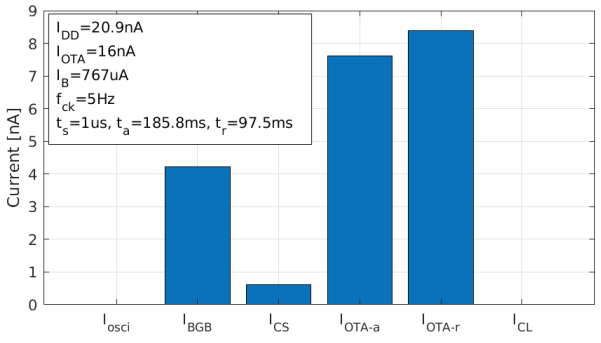

Fig. 5: *Average current consumption of the SC-PVREF blocks, low-noise case (α_n=0.05) with C_L=1 nF. $I_{BGB} \equiv I_B + I_{BG}$.*

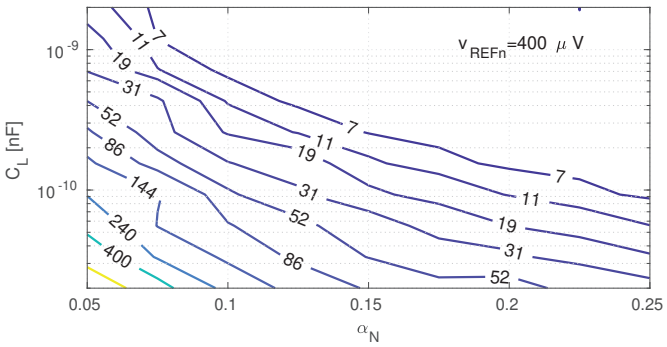

Fig. 6: *Contour plot of simulated I_{DD} vs C_L and noise (buffer and SC-PGA). Labels of isolines: I_{DD} in nanoampere.*

few tens of nanoampere can be obtained for the SC-PVREF with reasonable values of integrated C_L and output noise. The obtained results make the SC-PVREF suitable for ultra low-power applications.

IV. Conclusions

The paper has proposed an analytical model for the SC-PVREF. The model allows to carry on in MATLAB the design optimization and the a priori evaluation of the system performance, starting from the specifications of output noise and silicon area. The reported simulation results show that, by means of the proposed optimization process, the SC-PVREF architecture can achieve current consumptions in the order of tens of nanoampere, retaining the accuracy and temperature coefficient of the bandgap reference. This feature makes the topology suitable for ultra low-power applications.

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