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# OCVD measurement of ambipolar and minority carrier lifetime in 4H-SiC devices: relevance of the measurement set-up

Giovanna Sozzi, *Member, IEEE*, Sergio Sapienza, Roberta Nipoti, *Member, IEEE*, and Giovanni Chiorboli

Abstract—The Open Circuit Voltage Decay (OCVD) method is a well-known technique for performing electrical measurements of carrier lifetime: the main advantages lie in the simple setup and the possibility of performing measurements in commercial devices without the need of removing the package, as for optical methods. Despite several researchers have reported carrier lifetimes measured by the OCVD method in different devices, there has been little discussion about the potential effect of experimental setup on the obtained results. By comparing the outputs of experimental measurements with those of numerical simulations, this study investigates the overlooked effect of the OCVD measurement set-up on the former. Due to the growing importance of SiC-based devices, the analysis is applied to a 4H-SiC PiN diode. Two main points are addressed: i) the effect of circuit set-up on the ambipolar lifetime is discussed and a method, originally developed for improving the estimate of low-level carrier lifetime in OCVD measurements, is used to correct the measured lifetime for this influence; ii) the origin of the local minimum eventually appearing in the lifetime versus time curves is also investigated. It is found that the minimum can also be related to the time constant of the experimental set-up, arising doubts about the usual interpretation of this minimum as the minority carrier lifetime. A method is thus proposed to help discriminate between the two interpretations.

Index Terms— Carrier lifetime, OCVD, PiN diodes, 4H-SiC.

## I. INTRODUCTION

Silicon Carbide power device have been gaining an increasingly important role in a variety of power systems, such as photovoltaic converters, power supplies, motor control, electric/hybrid vehicles or telecommunications, that can benefit from the excellent physical properties of SiC [1].

Among the different SiC polytypes, presently, 4H-SiC has the larger wafer diameter and the better electronic quality. Commercial SiC power devices are made of the 4H-SiC polytype.

Depending on the specific device and application, the major features of SiC power devices include low on-resistance and fast switching performance typical of MOSFETs, SBD or JBD, but also potential drawbacks as in the case of the switching loss associated with the MOSFETs' body diode.

Bipolar devices are limited in their switching-speed by the stored minority carrier that also determines the large reverse recovery during turn-off, that however is lower than in their Silicon counterparts.

As known, the carrier lifetime is the key parameter for a reliable prevision of device features like the on-resistance and the switching frequency, that control the forward voltage drop and the reverse recovery time, respectively.

Due to the growing importance of SiC-based electronic devices, an accurate estimate of carrier lifetime and its dependence on temperature is thus a fundamental step towards the development of models to be used at the early design stage of a device or to evaluate the performance of a power converter, or, for example, the behavior of a MOSFET's body diode.

Although several reports on the SiC physical properties are available, the accuracy and investigated temperature range need further investigations: for that reason, we performed OCVD measurements on an unpackaged 4H-SiC PiN diode that was internally manufactured. The fact that the structure, doping, and processing data of such diode are known allows us to verify the experimental findings through numerical analysis of the diode behavior.

As known, the carrier lifetime can be measured either by optical (such as the time-resolved photoluminescence, TRPL, the photo-conductance decay, PCD, or the time-resolved free carrier absorption method, FCA)[2] and electrical methods (such as the current recovery time (CRT)[3] and the opencircuit voltage decay (OCVD) [4]). In general, optical measurements can be affected by surface recombination, while the electrical ones are mainly influenced by the experimental method used [5].

Regarding the electrical methods, the CRT technique investigates the drift region next to the pn junction, where damage induced by ion-implantation may be present and strongly reduces the minority carrier lifetime, in the case of ionimplanted emitter [6]. On the other hand, the OCVD technique results in a mean carrier lifetime averaged over the drift region.

Moreover, the carrier lifetime measured by electrical methods often deals with the difficulty of a reliable quotation of the lifetime that may depend on the current-injection and the device geometry, as shown in [7].

The purpose of this paper is to investigate the influence of the experimental set-up on OCVD measurement of both ambipolar (or high-level) and minority carrier lifetime of PiN

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G. Sozzi, S. Sapienza, and G. Chiorboli are with the Department

of Engineering and Architecture, Università di Parma, I-43124 Parma,

Italy (e-mail: giovanna.sozzi@unipr.it).

R. Nipoti is with the CNR-IMM of Bologna, I-40129 Bologna, Italy.

diodes that must be carefully analyzed, as we will show.

The relevance of R-C effects, attributable to both measurement set-up and device junction capacitance and leakage, has recently attracted scientific attention for the solar cells [8–10], while was not sufficiently considered for SiC diodes in high-injection conditions.

We also discuss the origin of the local minimum appearing in the measured lifetime versus time curve after biasing the diode in high-injection regime, commonly interpreted as the minority carrier lifetime, that we show may be related to the circuit time constant.

Results can be also useful during the characterization of the body diode of a MOSFET as we recently showed [11], or the drift region of IGBT or BJT.

#### II. DEVICE AND METHODS

# A. Measured Device

The measured PiN diode belongs to a family of vertical diodes fabricated by ion implantation on commercial n-type 8° off-axis <0001> 4H-SiC homo-epitaxial wafer. The bulk wafer thickness is 372 µm and its resistivity is 0.021  $\Omega$ ·cm. The epilayer is 25 µm thick and has a net donor concentration of 3×10<sup>15</sup> cm<sup>-3</sup>. The p<sup>+</sup> emitters are circular of 150-1000 µm diameters obtained by selected area Al<sup>+</sup> ion hot implantation with 2·10<sup>20</sup> cm<sup>-3</sup> dopant concentration over a depth of about 200 nm from the wafer surface. Annealing temperature and time are 1950°C and 5 min, respectively. No surface passivation is performed.

Anode and cathode ohmic contacts are e-gun evaporated Ti/Al (80 nm/350 nm) and Ni (150 nm), respectively. After alloying, anode contacts are made thicker by sputtered 350 nm Al (2% Si). Anode contacts are circular and centered on the anode region but with a 50  $\mu$ m-smaller diameter. More details on diode fabrication are in [12]. Diodes of 150  $\mu$ m diameter have been used for this study.

The diode ambipolar carrier lifetime is measured in air at room temperature (RT) with the OCVD method [4]. In this technique the diode is driven in the forward conduction region by a bias current which is suddenly terminated: the consequent voltage decay,  $V_{out}(t)$ , which is sustained by the carriers injected into the base of the diode, is recorded.

The carrier lifetime is extracted from the slope value  $dV_{out}/dt$  of the linear trait appearing after the voltage drop (this latter ideally due only to the diode series resistance [13] by (1)):

$$\tau = -n \, \frac{kT}{q} \cdot \left(\frac{dV_{out}}{dt}\right)^{-1} \tag{1}$$

with k, T, and q, Boltzmann constant, absolute temperature, and elementary electron charge, respectively, and where the factor *n* is 1 or 2 depending on whether the injection level is low or high [14]. For n = 2 (1), the high-level (low-level) lifetime  $\tau_{HL}$  ( $\tau_{LL}$ ) is obtained.

# B. Experimental set-up

The block diagram of the experimental set-up used for implementing the OCVD measurements is shown in Fig.1. The SMU (Source-Monitor Unit) Keithley 2400 provides a bias forward current density,  $J_B$ , of 210 A/cm<sup>2</sup>. A mercury wetted relay from Pickering with a maximum operating current of 3 A and an open circuit resistance >  $10^{12} \Omega$ , is used to separate the diode polarization unit from the device to avoid the bounce effects during switching, as suggested in [15]. The relay opening is controlled by a Philips PM5781 programmable pulse generator. The relay turn-on time is of the order of 10 ns.  $V_{out}(t)$  is acquired with Tektronix P6139A passive probes connected to the eight-bit Tektronix DPO7254 Digital oscilloscope with a sampling rate up to 20 GSa/s (additional details on the experimental set-up can be found in [7]).



Fig. 1. Experimental set-up used for OCVD measurements: block diagram of the test bench - the central square block is the PCB. The Source-Monitor Unit (SMU) provides the forward current to bias the diode.

### C. OCVD measurements

In the initial trait of the  $V_{out}$  transient after the voltage drop, the charge stored in the drift region is large, and the dominant capacitance contribution is the diffusive one. This charge returns to the equilibrium value through recombination processes and the  $V_{out}$  vs time curve approaches a linear decay [16], as qualitatively illustrated in Fig. 2 ("ideal decay" curve), with the slope equal to  $dV_{out}/dt=-nkT/q\cdot 1/\tau$ .

As the decay proceeds, the diffusion charge exponentially reduces with time and the junction capacitance, Cj, increases. When the junction capacitance is appreciable, the voltage decay starts deviating from the ideal-case and slows-down ("junction capacitance" curve in Fig. 2); also external capacitances, as the one due to the measurements set-up, can add to the Cj enhancing the effect.

Similarly, in the presence of a resistance in parallel to the diode, the voltage decay can deviate from the ideal-case since carriers may leave the diode neutral regions through the resistive parallel path; in this case the decay accelerates in comparison to the ideal case and the measured lifetime is underestimated ("shunt resistance" curve in Fig. 2).

As suggested by Green [17], by observing the differential of the voltage decay it is possible to cancel out the effect of both junction capacitance and shunt resistance that determine the departure from the ideal linear relationship of lifetime on voltage (as described by (1)) by connecting extra resistance or capacitance in parallel with the diode: the compensated voltage



Fig. 2 Typical trends of open circuit voltage decays showing the ideal decay curve and the effect of junction capacitance, and shunt resistance.

decay will result in a constant  $dV_{out}/dt$ , as in the ideal case, over a larger time interval, facilitating the extraction of the carrier lifetime from the measured curve.

The measured diode has shown a capacitance-dominated behavior, so that an extra-resistance,  $R_{EXT}$ , has been connected in parallel to the diode, as explained in the following.

#### D. Diode model and numerical simulation

A three-dimensional numerical model of the measured diode has been realized with the Sentaurus-tcad suite.

The cylindrical symmetry of the diode, allows to simulate half of the cross-section on a symmetry plane, i.e., the section inside the black frame in Fig. 3a, while the 3D current is calculated in a post-simulation step. In particular, the anode region is circular with a diameter of 150  $\mu$ m; the metal contact is centered on it but with a 50  $\mu$ m-smaller diameter.

The diode behavior is described by the Poisson, electron and hole continuity, and drift-diffusion equations. Specific models for 4H-SiC account for band-gap narrowing [18] and incomplete ionization of dopants [19]. The carrier lifetime is



Fig. 3. a) Schematic drawing of the diode model; b) mixed-mode circuit used in the numerical simulation of diode OCVD. The diode model and circuit parameters are described in the text.

assumed to be controlled only by traps related to the carbon vacancies [20, 21] systematically found in 4H-SiC n-doped epilayers [12, 22]. Recombination processes are described by the Shockley-Read-Hall statistic.

The fundamental parameters of 4H-SiC and additional details about the diode simulation can be found in our previous works [23].

The OCVD measurement is simulated by introducing the 3D diode model into the mixed-mode circuit of Fig. 3b, where the remaining components, due to the experimental set-up, are described by spice-like compact models. In particular,  $R_{scope} = 10 \text{ M}\Omega$  and  $C_{scope} = 8 \text{ pF}$  are the scope resistance capacitances, respectively,  $R_{EXT}$  is the variable external resistor used in measurements, and  $C_{TOT}$  is the parallel of circuit parasitic  $\approx 1 \text{ pF}$  plus the relay and scope capacitance (5 + 8 pF).

In the OCVD simulations of the diode, the device is firstly biased in forward condition by the same current density,  $J_{BIAS}$ , of measurements, afterward the switch is opened and the open circuit voltage decay evaluated; the simulations are repeated for the same  $R_{EXT}$  values used in measurements and for additional values of 10 and 100 k $\Omega$ .

# **III. RESULTS AND DISCUSSIONS**

# A. Measured OCVD curves and ambipolar carrier lifetime

The measured open-circuit voltage decay curves of a 150  $\mu$ m-diameter diode are shown in Fig. 4 for R<sub>EXT</sub> values varying from 270 k $\Omega$  to 10 M $\Omega$ ; the forward bias current density, J<sub>BIAS</sub>, of about 210 A/cm<sup>2</sup> is switched off at time 0  $\mu$ s.

The voltage step appearing at the relay opening is due to the diode internal series resistance, as explained in [13]. After the current is suddenly terminated, a potential remains across the junctions due to the presence of excess carriers in the drift region: this potential decays in time as the excess carriers return to equilibrium.

The OCVD curves of Fig.4 are initially filtered according to [24] to remove noise, then the carrier lifetime is calculated from the slope value  $dV_{out}/dt$  of the linear trait after the voltage drop [14], as explained in section IIA (Fig.5).

The behavior of lifetime appearing in Fig.5a for 250 ns after the voltage drop is not significant as it is the result of the numerical filtering algorithm.



Fig. 4. Measured open circuit voltage decays for a bias current density  $J_{BIAS} = 210 \text{A/cm}^2$  and variable external resistance,  $R_{EXT}$ .

The parasitic inductance of the device and measuring circuit can affect the voltage decay immediately after the relay opening and might add some ringing to the voltage decay, making more complicated the estimation of the reciprocal slope.

In the presence of ringing, since the OCVD technique requires a sudden open circuit condition [5], a reasonable approach could be to decrease the bias current, which however must remain high enough to ensure the high-injection condition required in the case of  $\tau_{HL}$  estimation.

The ambipolar carrier lifetime,  $\tau_{HL}$ , calculate for each  $V_{out}(t)$  curve in Fig. 4 is reported in Table I for different  $R_{EXT}$ .

TABLE I

 $\begin{array}{l} \text{Extracted } \tau_{MIN} (\text{calculated } @ \ V_{\text{out}} = 2.2 \ V) \ \text{and} \ \tau_{HL} \ \text{for each value} \\ \text{of shunt resistance, } R_{\text{ext}}, \ \text{and} \ Circuit \ \text{equivalent resistance, } R_{\|\cdot\|}. \end{array}$ 

$R_{EXT}\left(M\Omega\right)$	$\tau_{HL}\left(ns\right)$	$R_{\parallel}\left(M\Omega\right)$	$\tau_{MIN}\left(ns\right)$
0.27	175	0.263	116
0.56	296	0.53	221
0.82	360	0.758	307
1	380	0.91	372
2.2	$\approx 510$	1.8	-
10	$\approx 630$	5	-
$\infty \ (\text{no} \ R_{\text{EXT}})$	pprox 680	10	-

The extracted  $\tau_{HL}$  shows a strong dependence on the  $R_{EXT}$  values, spanning from 175 ns to  $\approx 680$  ns as  $R_{EXT}$  increases from 270 k $\Omega$  to infinity (in this last case only the resistor  $R_{scope} = 10 \ M\Omega$  is connected in parallel to the diode).

How to identify the reliable  $\tau_{HL}$  among the values of Table I is shown hereinafter.

Fig. 5a plots the computed  $\tau = -(2kT/q) \cdot (dV_{out}/dt)^{-1}$  versus time for each curve of Fig. 4. Two regions can be identified: region I where curves show a local maximum or an inflection point, and region II where the curves show a local minimum.

 $τ_{HL}$  should thus be estimated from the local maximum visible in region I for R<sub>EXT</sub> in the interval 270 kΩ (yellow curve) to 2.2 MΩ (green curve), while for larger R<sub>EXT</sub> the capacitive effect is dominant and the local maximum is replaced by an inflection point, as in the cases of R<sub>EXT</sub> = 10 MΩ (red curve) and R<sub>EXT</sub> = ∞ (i.e., no R<sub>EXT</sub>, black curve) shown in Fig. 5a.

However, this notable point varies with  $R_{EXT}$  as reported in Table I. As a consequence, the choice of the  $\tau$  value that should be assigned to  $\tau_{HL}$  becomes questionable; that is, depending on the equivalent resistance and capacitance of the measurement circuit, the lifetime values extracted with the OCVD technique can be quite different.

One possible implication of the observed behavior is that a single measurement of the diode voltage decay cannot rule out the influence of the experimental set-up on the measurement, being it a simple scope or a complex electronic circuit as in [15].

Fig. 5b plots the differential of the voltage decay  $|dV_{out}/dt|$  versus decay time as suggested in [17] for each curve of Fig. 5a. For  $R_{EXT} < 1 \ M\Omega$ , the curves of Fig. 5b show the typical shape of a shunt resistance-dominated decay, while for  $R_{EXT} > 10 \ M\Omega$ , they appear to be controlled by the diode junction capacitance, Cj, in parallel with  $C_{TOT}$ .

The  $|dV_{out}/dt|$  curve discriminating between the shunt resistance- and the capacitance-dominated regime is



Fig. 5. a) Measured lifetime calculated as  $\tau = (2kT/q) (dV_{out}/dt)^{-1}$  versus time. The vertical dotted-dashed marks the regions of local maxima and inflection points (reg. I) and minima (reg. II); b) Differential of the open circuit voltage decay versus time for a bias current density  $J_{BIAS} = 210 \text{ A/cm}^2$  and different shunt resistance,  $R_{EXT}$ .

qualitatively indicated by the dotted-dashed line sketched in Fig. 5b, which represents the ideal diode decay. The corresponding experimental curve superimposes the dotted-dashed line for an optimal shunt resistance of 1 M $\Omega$ , as shown by the blue curve in Fig. 5b: it corresponds to a lifetime of 380 ns (see the blue curve in Fig. 5a).

A reliable determination of the carrier lifetime thus requires readjusting the  $R_{EXT}$  value to move  $|dV_{out}/dt|$  towards the ideal voltage decay, i.e. the compensated curve.

#### B. Minority carrier lifetime

Previous studies [15, 24] have reported that the OCVD waveform of a diode initially biased in high-level injection regime exhibits two distinct linear traits, corresponding to a local maximum and a local minimum in the lifetime calculated by (1), respectively related to the ambipolar and minority carrier lifetimes.

In our measurements, we also see a local minimum, but it varies with  $R_{EXT}$  (see Fig. 5a, curves from blue to yellow, and also data reported in Table I), raising some doubts about its interpretation as the minority carrier lifetime.

To investigate further the origin of this minimum and the observed dependence on  $R_{EXT}$ , we developed the numerical model of the measured diode described in section II, and simulated the open circuit voltage decays.

# 1) Simulated OCVD curves: minority carrier lifetime estimate

The diode open circuit voltage decay has been simulated both

in the ideal case, i.e., with neither external resistor nor capacitor connected in parallel to the modeled device, and with the same  $C_{TOT}$ ,  $R_{scope}$ , and  $R_{EXT}$  used in measurements ( $R_{EXT} = 10, 100 \text{ k}\Omega$  are also simulated); in both cases, the diode has been biased with the same  $J_{BIAS}$  used in measurements. The diode model and the schematic of the simulated mixed-mode circuit is sketched in Fig. 3b.

Two different combinations of electron,  $\tau_e$ , and hole,  $\tau_h$ , lifetimes have been considered in the simulations: i)  $\tau_e = 280$  ns and  $\tau_h = 100$  ns and ii)  $\tau_e = \tau_h = 190$  ns, both corresponding to the measured high-level lifetime  $\tau_{HL} = \tau_e + \tau_h = 380$  ns.

i) The simulated OCVDs for  $\tau_e = 280$  ns and  $\tau_h = 100$  ns are shown in Fig. 6 for R<sub>EXT</sub> ranging from 10 k $\Omega$  to  $\infty$  (no R<sub>EXT</sub>).

In this case, the lifetime extracted from the simulated OCVD curves with (1) show a local maximum corresponding to the high-level lifetime,  $\tau_{HL}$ , and a local minimum,  $\tau_{MIN}$  (Fig. 7a that should be related with the minority carrier lifetime, as in [15, 24]. In particular, since the low level lifetime is obtained by (1) with n = 1,  $\tau_{MIN}$  should correspond to two-times the low-level lifetime,  $\tau_{LL} \approx \tau_h$ .

The ideal voltage decay of the diode, i.e. no external resistor or capacitor due to the experimental set-up connected in parallel to the modeled device, is reported as comparison (the black dotted-dashed curve in Fig. 7a): a value of  $\tau_{HL} = 296$  ns and  $\tau_{MIN} = 212$  ns can be obtained from the compensated curve, the fuchsia one. These values have to be compared with  $\tau_e + \tau_h = 380$  and  $2 \cdot \tau_h = 200$  ns defined in the simulations.

 $\tau_{HL}$  is lower than  $\tau_e + \tau_h$  because of the carrier flow from the epi-layer to the heavily doped regions of the device [16], while the slight overestimation of the minority carrier lifetime (106 ns instead of 100 ns) could be further reduced by adjusting the  $R_{EXT}$  value (in fact, the same  $R_{EXT}$  of measurements are used in simulations).

When the capacitor and resistor of the external circuit with  $C_{TOT}=14 \text{ pF}$  and a  $R_{EXT}=10 \text{ M}\Omega$  (red curve in Fig. 7a) are connected in parallel to the diode model, the simulated local minimum slightly increases in value compared to the ideal decay curve due to the effect of the external capacitance, (compare the red and black dotted-dashed lines in Fig. 7a). Moreover,  $\tau_{MIN}$  is observed to depend on  $R_{EXT}$ .



Fig. 6. Simulated open circuit voltage decays for a bias current density  $J_B = 210 \text{ A/cm}^2$  and variable shunt resistances,  $R_{EXT}$ . The black dotted-dashed line corresponds to the ideal diode open-circuit voltage decay.

With R<sub>EXT</sub> in the range 560 k $\Omega$  -10 M $\Omega$  (i.e. from fuchsia to red curves in Fig.7a),  $\tau_{MIN}$  varies between -7% and +6% around the ideal case value,  $\tau_{MIN} = 225$  ns.

For  $R_{EXT} < 560 \ k\Omega$ , instead, a marked dependence of  $\tau_{MIN}$  on  $R_{EXT}$  appears, with  $\tau_{MIN}$  suddenly dropping to values that are uncorrelated with the carrier minority lifetime (yellow, dark-green and brown curves).

ii) In the case of equal electron and holes lifetimes  $\tau_{HL} = \tau_e + \tau_h$  and  $\tau_{MIN} = 2\tau_h$  have the same value so that the local minimum is not visible in the  $\tau_{HL}$  curves for  $R_{EXT} \ge 1 \text{ M}\Omega$  (blue line in Fig. 7b).

However, as in the previous case, a local minimum appears as  $R_{EXT}$  reduces, largely varying with  $R_{EXT}$ , and whose value is uncorrelated with the minority carrier lifetime. The observed strong dependence of  $\tau_{MIN}$  on  $R_{EXT}$ , suggests an influence of the external circuit set-up on the OCVD waveform.

Supposing an exponential decay due to circuit set-up, the slope of the plot of  $\tau_{MIN}$  versus  $R_{\parallel}$  is proportional to the total circuit capacitance  $C_{TOT}+Cj$ . In fact, if  $|dV_{out}/dt| = V_{out}/(R_{\parallel}\cdot(C_{TOT}+Cj))$ , equation (1) with n = 2 modifies to (2):

$$\frac{\tau}{2}\frac{v_{out}}{v_{th}} = R_{||} \cdot (C_{TOT} + C_j) \tag{2}$$

where  $v_{th}$  is the thermal voltage and  $R_{\parallel}$  the circuit equivalent resistance.

The plot of (2) versus  $R_{\parallel}$ , calculated from the simulated  $\tau_{MIN}$ in Fig. 7a for 10 k $\Omega \leq R_{EXT} \leq 270 \text{ K}\Omega$  (black squares) and



Fig. 7. Lifetime, calculated from the simulated OCVD decays as  $\tau = (2kT/q)$  $(dV_{out}/dt)^{-1}$ , versus time; electron,  $\tau_e$ , and hole,  $\tau_h$ , carrier lifetimes are: a)  $\tau_e = 380$  ns,  $\tau_h = 100$  ns; b)  $\tau_e = \tau_h = 190$  ns.



Fig. 8.  $(\tau_{MIN}$ ·Vout)/(2·v<sub>th</sub>) versus the circuit equivalent resistance  $R_{\parallel}$  calculated from the simulated curves of Figs. 7. The dashed lines are the regression lines and  $R^2$  the corresponding correlation coefficient.

Fig. 7b 10 k $\Omega \leq R_{EXT} \leq 820$  k $\Omega$  (black squares) in the case of an unbalanced and balanced lifetime, respectively, have a slope of about 17 pF as shown in Fig. 8, which is consistent with the sum of 14 pF due to the measurement set-up and about 3 pF of the internal diode capacitance: the interpretation of this quantity as the time constant of the RC circuit is thus demonstrated.

# 2) Measured OCVD curves: minority carrier lifetime estimate

As anticipated, the measured lifetime curves versus time in region (II) of Fig. 5a, exhibit local minima varying with  $R_{EXT}$ : the  $\tau_{MIN}$  extracted for each  $R_{EXT}$  are reported in Table I, and roughly correspond to a  $V_{out}$  of about 2.2 V.

These minima have been analyzed in light of the simulation results.

At first, the equivalent resistance of the circuit  $R_{\parallel}$  has been calculated as the parallel of  $R_{EXT}$ ,  $R_{scope}$ , and  $R_d$  (this latter, extracted from the diode I-V curves at  $V_{out} = 2.2$  V, is larger than 70 M $\Omega$ ); the resulting  $R_{\parallel}$  are reported in Table I.

Secondly, the junction capacitance has been evaluated by C-V measurements made at high frequency ( $f_0 = 1$  MHz) to make the contribution of diffusion capacitance negligible, as explained in [25]: a value of Cj  $\approx$  2.7 pF is measured for V<sub>out</sub> = 2.2 V, as depicted in Fig. 9.

Finally, the measured  $(\tau_{MIN} \cdot V_{out})/(2 \cdot v_{th})$  has been drawn versus  $R_{\parallel}$ : as shown in Fig. 10, the measured data (symbols) are



Fig.9. Diode capacitance versus voltage measured at 1 MHz.



Fig. 10. Measured  $(\tau_{MIN}$ ·Vout)/(2·v<sub>th</sub>) (full squares) calculated at  $V_{out}$ =2.2 V versus the circuit equivalent resistance  $R_{\parallel}$ . The red dash line is the regression line and  $R^2$  the corresponding correlation coefficient.

well interpolated by a straight line whose slope is  $\approx$  16 pF, to be compared to the sum of Cj  $\approx$  2.7 pF and C<sub>TOT</sub>  $\approx$  14 pF.

This supports the interpretation of  $\tau_{MIN}$  as determined by the RC constant of the circuit as an alternative to the minority carrier lifetime.

In conclusion, the evidence from this study suggests that the ambipolar and minority carrier lifetimes can be affected by the capacitive (or resistive) behavior of the DUT plus the circuit set-up, causing the departure of the OCVD curve from linearity, so that corrective actions need to be implemented.

The compensation of the capacitive (resistive) behavior of OCVD curves by connecting a resistor (capacitor) in parallel with the DUT, as originally proposed by Green for the minority lifetime measurement, can be used to estimate the ambipolar lifetime cleaned up from the set-up influence.

On the basis of the findings above, we can draw the following indication for a reliable estimate of the ambipolar and minority carrier lifetimes.

a) A first measure of the DUT in the circuit set-up allows discriminating, between an open circuit voltage decay dominated by the capacitance or the shunt resistance.

b) An external resistor,  $R_{EXT}$  (as in the present work) or capacitor, has to be connected in parallel to the device to compensate for it, and measurements have to be repeated for different values of  $R_{EXT}$  ( $C_{EXT}$ ).

c) The differential of the OCVD curves for various  $R_{EXT}$  ( $C_{EXT}$ ) allows to identify the optimal  $R_{EXT}$  ( $C_{EXT}$ ), i.e. the one giving a flat curve, from which the ambipolar lifetime can be calculated.

d) In the case, a second linear trait, potentially related to the minority carrier lifetime, appears in measurements, a plot of  $\frac{\tau Vout}{2 v_{th}}$  versus the circuit equivalent total resistance,  $R_{\parallel}$ , can help discriminate between the minority carrier lifetime or the circuit RC time constant.

e) If the experimental points of  $\frac{\tau Vout}{2}$  versus  $R_{\parallel}$  lie on a straight line, the slope gives the equivalent circuit capacitance, that can be also separately estimated; in this case the local minimum,  $\tau_{MIN}$ , calculated by (1) is uncorrelated with the minority carrier lifetime.

f) In case point e) does not occur, the minority carrier lifetime can be calculated from the  $\tau_{MIN}$  of the compensated curve, i.e., the one with the optimal  $R_{EXT}$  (or  $C_{EXT}$ ).

# IV. CONCLUSIONS

The carrier lifetime measurements by OCVD technique of a 4H-SiC PiN diode has been proven to be heavily affected by the set-up parasitic and scope resistances and capacitances that may cause the departure of the OCVD curve from linearity so that corrective actions and careful analysis of experimental voltage decay curves need to be performed to obtain a reliable estimate of the carrier lifetime.

The method previously proposed by Green to improve the OCVD measurement of minority carrier lifetime, has been shown to be a viable approach to follow for the estimate of the ambipolar carrier lifetime, too.

Moreover, the still considerable ambiguity about the interpretation of the local minimum eventually appearing in the lifetime waveform extracted from the OCVD measurements of a diode initially biased in high-injection regime has been also addressed with the help of numerical simulations. As a result, a method has been proposed to help to clarify the origin of this minimum, commonly attributed to the minority carrier lifetime, that can be also related to the RC constant of the circuit, as demonstrated in the present study.

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