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Power Hardware-in-the-Loop Test Bench for Permanent Magnet Synchronous Machines based on a Parallel Hybrid Converter

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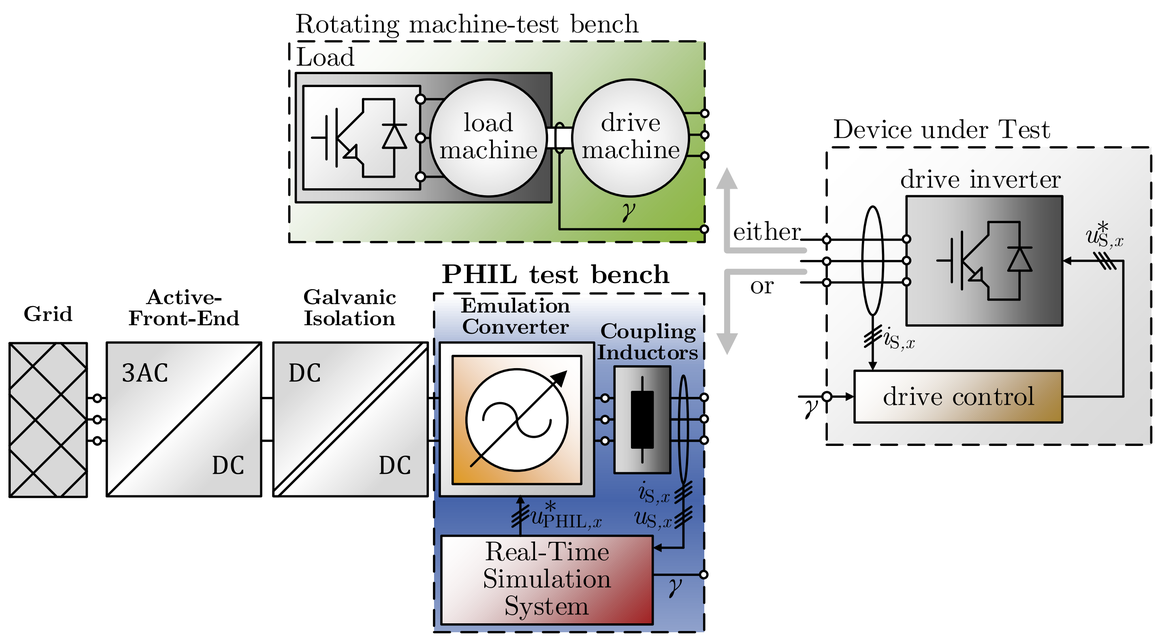
Abstract: This poster presents a Power Hardware-in-the-Loop (PHIL) emulation test bench for emulating highly utilized permanent magnet synchronous machines (PMSM). The emulation converter of the PHIL test bench is a Cascaded H-bridge based Parallel Hybrid Converter (PHC) with a 17-level output voltage and a modulation frequency of 1 MHz. The nonlinear machine is emulated with a sampling frequency of 5 MHz and is implemented on the FPGA of a Real-Time Simulation System (RTSS)

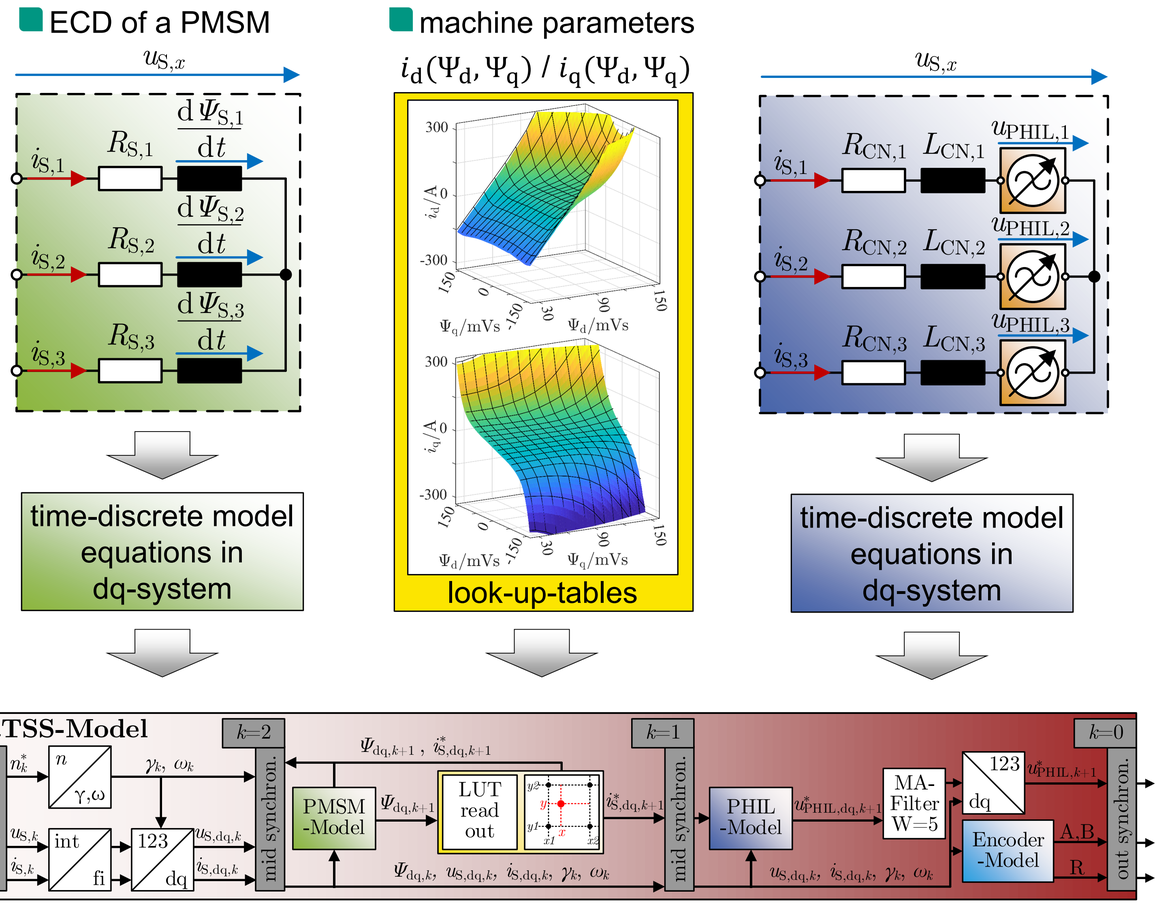
Power-Hardware-in-the-Loop (PHIL) test bench concept



- Replacing expensive and space-consuming rotating machine test benches with modern Power-Hardware-in-the-Loop (PHIL) emulation test benches
- Emulation of a non-linear machine based on the model inside the Real-Time Simulation system
- Current flow between DUT and PHIL corresponds perfectly to the real machine currents, even current ripples are emulated perfectly

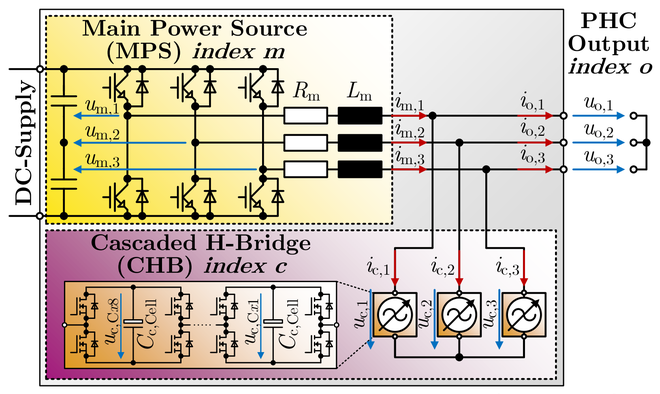
PMSM and PHIL modeling:

- ECD of a PMSM
- machine parameters $i_d(\Psi_d, \Psi_q)$ / $i_q(\Psi_d, \Psi_q)$
- ECD of the PHIL test bench



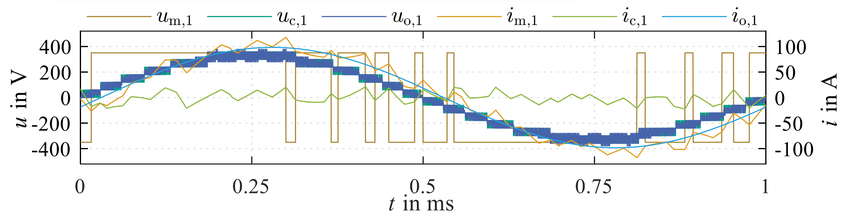
- The RTSS model is implemented on the Kintex-7 FPGA of an in-house developed modular signal processing system based on the ZYNQ7030 system-on-chip (SoC) from Xilinx
- Model sampling frequency is 5 MHz and model output is down sampled by a moving-average filter to the 1 MHz modulation frequency of the PHIL emulation converter

Cascaded H-Bridge based Parallel Hybrid Converter as Power Hardware-in-the-Loop Emulation Converter



Basic Concept

- Voltage only defined by the low-power multilevel converter (CHB)
  $\rightarrow u_o = u_c$
- Active power current only delivered by the high power two level converter (MPS)
  $\rightarrow i_{o,123} = i_{m,123} - i_{c,123} \approx i_{m,123}$
  with $\frac{i_{c,rms}}{i_{m,rms}} \approx 11\%$

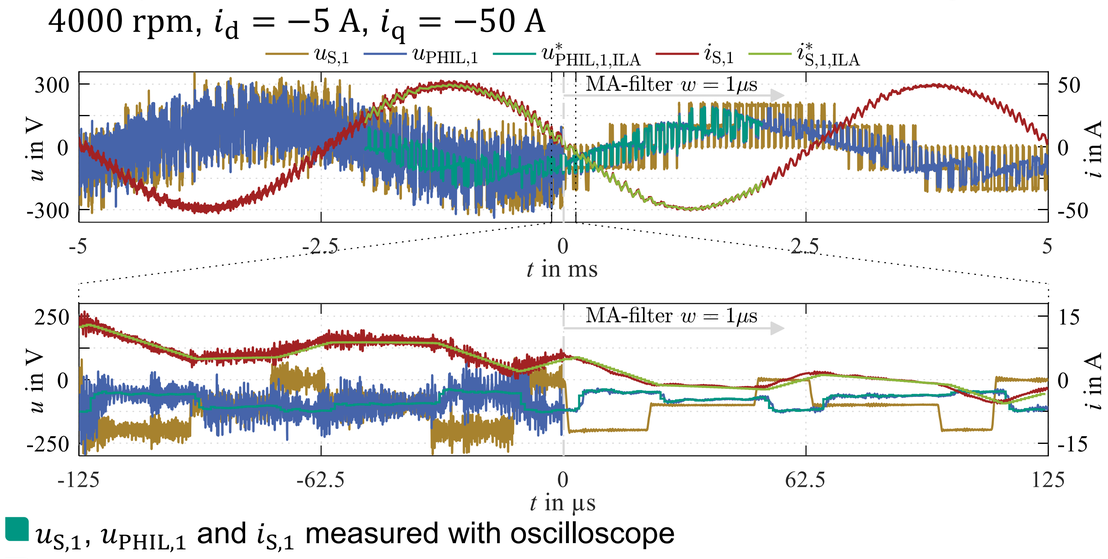


$\hat{u}^*_{o,1}$=325 V	f^*_o=1000 Hz
$i_{m,1,rms}$=71 A	$\tilde{f}_{m,SW}$=11.5 kHz
$i_{c,1,rms}$=7.8 A	$f_{c,SW}$=1 MHz
$i_{o,1,rms}$=69.4 A	R_{Load}=3.25Ω L_{Load}=100µH

Simulation results of the PHCs first phase with a passive ohmic-inductive-load

Measurement Results

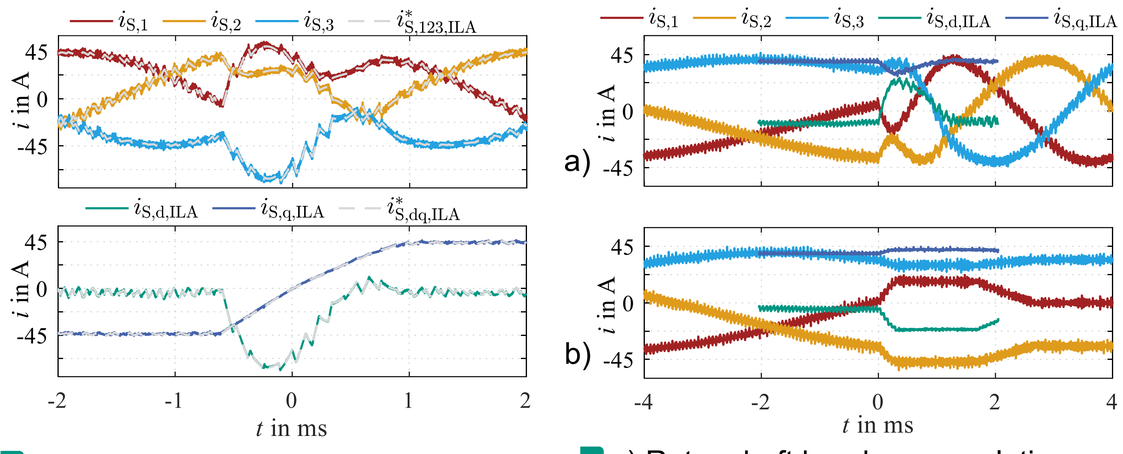
- Steady-state operation with zoom to $-125\mu s < t < 125\mu s$ @ $n = 4000$ rpm, $i_d = -5$ A, $i_q = -50$ A



- $u_{S,1}$, $u_{PHIL,1}$ and $i_{S,1}$ measured with oscilloscope
- $u^*_{PHIL,1}$ and $i^*_{S,1}$ loged inside the RTSS FPGA with 1 Msps

➤ Real current $i_{S,1}$ between PHIL and DUT corresponds perfectly to reference value $i^*_{S,1}$ calculated by the PMSM model

- Dynamic current and speed step operation



- Current reversal step at 4000 rpm with $i_d = -5$ A from $i_q = -45$ A to $i_q = 45$ A
- PMSM model reference vales in gray
- a) Rotor shaft breakage emulation
  → speed step from 1000 to 4000 rpm
- b) abruptly locked rotor emulation
  → speed drop from 1000 to 0 rpm

➤ Correct emulation of the current ripple, saturation effects and cross coupling effects during dynamic current and rotor speed step changes