NELSON MANDELA UNIVERSITY

PROFESSORIAL INAUGURAL LECTURE

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Topic:

THE INVISIBLE ENEMY OF SATELLITE ELECTRONICS

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The invisible enemy of satellite electronics

Abstract: Spacecraft electronics are susceptible to the adverse effects of space radiation. Our jobs as engineers and scientists is to find ways to characterize these effects and find ways to mitigate it in order to ensure seamless operation of the satellite mission

Summary of lecture:

The reconfigurable nature of Field Programmable Gate Arrays (FPGAs), together with their relatively low cost and ease of implementation, provided the space industry with an attractive solution for high level computer systems applications. Unfortunately, FPGAs are susceptible to Single Event Effects (SEEs) such as Single Event Transients (SETs), Single Event Upsets (SEUs) and Total ionizing dose effects.

SETs are caused by charged particles depositing charge on circuit elements through ionization. These deposited charges cause elevated local voltage levels in the circuit elements, which leads to incorrect logic values [1].

In a combinational logic element, the charge will leak away (over several hundreds of picoseconds) and the element, and consequently the system, will return to a consistent state. However, when synchronous logic is disturbed by a SET on a clock edge, the temporary incorrect logic value is latched into the register. This incorrect value can then propagate through the rest of the system compromising its functional integrity. SETs that are erroneously latched by a register are called SEUs. High energetic particle strikes to a memory element such as the configuration memory of an FPGA, causing a bit flip, are also called SEUs.

The response of a particular family of FPGAs to SEUs, is a function of its configuration memory [2]. For example, SRAM FPGAs are a family of FPGAs which have configuration memory that consists of SRAM cells. It has been shown that the configuration memory of SRAM based FPGAs is sensitive to SEUs, which causes a bit flip, when struck by an energetically charged particle [2]-[3]. This could cause a change in functionality.

Flash based FPGAs, on the other hand, have configuration memory that consists of Flash memory cells, which have been shown to be resistant to SEUs [4]-[5]. However, previous tests have shown that Flash FPGAs are sensitive to soft errors, or SETs, in the combinational user logic, and to SEUs in the sequential logic elements [6].

In this lecture, we concentrate on the SET mitigation schemes used in FPGAs as well as testing methods to characterize the processors for space applications. In order to use FPGAs in a radiation environment, the mitigation must be applied to the user logic, as well as the memory elements.

A well-known and common mitigation scheme for correcting the SEU errors in FPGAs is Triple Modular Redundancy (TMR) [7]. The main disadvantage of TMR is the excessive area overhead. The hardened design has at least three times more area and power consumption than the original circuit, excluding TMR overhead. When the TMR hardened designs are implemented with a hardware description language or via the manufacturer's software tools, it instantiates redundant triplicate circuits in the user design as well as voting circuits [8]. This method of implementing TMR results in four [9] to seven times [10] resource increase, which limits its usage to reliability-critical applications.

Another common mitigation method, however, to mitigate SETs in the user combinational logic of FPGAs, is to use a SET filter at the inputs of each sequential element [6], [11]-[12]. If SEU hardened latches are used in the circuit's sequential logic, SETs in combinational logic can become the primary source of observable errors, if captured by a memory cell [6], [11]-[12]. To avoid SET capture by any memory element, the SET filter technique could be used [6], [13].

The generally accepted advantage of using the filter technique in FPGAs is to provide a gate count and power savings advantage with respect to TMR. Since SET filters are placed at the inputs of the sequential elements only, there is no need to provide triple redundancy in the user logic, and it is therefore, assumed that there will be a resource savings with respect to TMR.

The lecture attempts to illustrate the concepts with easy-to-understand general concepts by means of animations.

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Full Text of Lecture

Thank you, professors, for that introduction.

I think I will go straight to the presentation, and I hope you enjoy it. Thank you.

The focus of today's lecture will be the invisible enemy of satellite electronics. However, before I go into that topic, I would like to discuss a typical low Earth orbit Satellite.

I will show this via two animations. The first one that you see in this animation is bearing the university's name. Of course, we don't have our own satellite, but who knows, perhaps if we partner with the correct institution in future, it might become a reality. However, what I can say with certainty is that we are involved in some aspects of satellite technology, and we are actively contributing to the field.

The current animation that is playing is shown from the viewpoint of an observer some distance from the Earth, such that the satellite orbit and Earth rotation can be seen underneath.

The second one is from the satellite's point of view. That is, a camera is mounted on the satellite and moving with it.

By looking at the first animation, we can see that due to the Earth's rotation, it is possible to combine the advantages of low altitude orbits with global coverage using these near polar orbiting satellites, which have orbital planes that crosses the poles. These satellites, for obvious reasons, are termed polar orbiting satellites and are launched into orbit at high inclinations to the Earth rotation, such that they cross high latitudes near the Poles.

Most of these orbits are circular to slightly elliptical at distances ranging from about 700 to 1700 kilometers from the geoid. The geoid is the geometry that the ocean surface would have under the influence of gravity if other influences such as winds and tides were absent.

The satellites at different altitudes travel at different speeds. What high inclination means is that the sub-satellite point moves North or South along surface the projection of the earth's axis, as seen in this animation.

If the orbit is designed correctly, the sub-satellite point can be largely in the day or the night side of the planet during the satellite orbit. Such a satellite orbit is called sun synchronous. In order for this to happen, the orbital speed of the satellite would have to phase with the rotation of the earth. The result is that the phase of the satellite maximizes its coverage of the day side of the planet.

The ground track of the satellite is displaced to the west after each orbital period due to the gravitational effects and also the rotation of the earth, and can be seen in this animation. The displacement of longitude is a function of orbital period, which is often less than two hours for low altitude orbits.

What the next animation shows is that of the rotation of the satellite around the earth from the satellite's point of view. This might appear strange to you since we are used to seeing the earth from some distance as shown in previous animation. However, this animation shows more or less the coverage that the satellite would see as it rotates the earth.

Although it appears as though the Earth is rotating South to North, this is not the case. It only appears so if the satellite is kept constant, that is, the view is relative to your position in space. However, this view is advantageous to some degree to appreciate my explanation of the polar earth orbit.

Satellite orbits are not the focus of what I want to discuss. I want to tell you about the invisible enemy that satellites face on a continuous basis and we as design engineers must ensure that satellites perform according to their specifications at all times, and that is no easy task. The invisible enemy that I am referring to is called space radiation. Most people are familiar with radiation on the human body and that it can cause serious illness and in high doses even death. However, very few realize that the study of radiation on electronics is a very active and important area of research to ensure any adverse effects to satellite operations are mitigated as much as possible.

Even though they are over hundreds, even thousands of kilometers above us, satellites play a very important part in our everyday lives, whether we realize it or not.

As mentioned earlier, satellites are constantly exposed to space radiation. However, before we look at the ways of mitigating the effects of the radiation, which is the focus of my research and the main focus of this lecture, I first want to explain where the radiation originates.

Cosmic rays are high energy protons and atomic nuclei that moves through space at nearly the speed of light. They originated from the sun and outside of the solar system in our own galaxy, and also from distant galaxies.

Upon impact with the Earth atmosphere, cosmic rays produce showers of secondary particles, some of which reach the surface and can be easily detected by devices such as, for example, Geiger counters, although the bulk is intercepted by the magnetosphere or the heliosphere.

I will discuss this effect later as it is important to consider when designing a satellite for particular missions. Cosmic rays are an even present low flux component of the terrestrial radiation environment and is the main component in interplanetary space. They consist of galactic cosmic rays, solar cosmic rays, and terrestrial cosmic rays. The composition of these rays are approximately 85% protons, 14% alpha particles and 1% heavy nuclei. All of which come from outside the solar system.

It is important to remember that for high energy particles from galactic cosmic rays, both geomagnetic shielding and spacecraft shielding are relatively ineffective. Cosmic rays in general contribute more to single event effects than total ionizing dose effects, both of which I will discuss later, however, next I want to focus on the radiation from our sun and its effects as it pertains to satellite electronics.

A solar flare is a sudden flash increase in brightness of the son, usually observed on its surface and in close proximity to a sunspot. Powerful flares are often accompanied by what's called a coronal mass ejection. Even the most powerful flares are barely detectable in the solar irradiance. The problem for us is that flares are closely associated with ejection of plasmas and particles through the sun's corona into interplanetary space. If the ejection is in the direction of the earth, particles associated with this disturbance can penetrate into the upper atmosphere and cause bright auroras, and may even cause disruption to long range communications, and of course to satellite electronics.

Solar cosmic rays have a slightly different composition compared to their galactic counterparts. What you can see in the animation at the moment is my representation of this coronal mass ejection which can engulf the Earth many times over.

Moving towards the earth, the magnetic field of the earth traps electrons, protons, and some heavy ions that originate from the solar wind. These particles spiral about closed loops of the magnetic dipole of the earth and move back and forth between the regions of maximum magnetic field strength, which is located at the poles.

The electrons drift west to east, while the protons drift east to west. The motion of these particles around the earth forms domains which are referred to as radiation belts or Van Allen belts, as illustrated in the animation. This is not an accurate version of the radiation belts but merely to give you a sense of what it looks like.

The trapped electrons occupy two zones, the inner and the outer zones. The inner zone extends to an altitude of about 2.4 Earth radii from the equator, while the outer zone extends from an altitude of 2.8 to about 12 earth radii. The region between the two zones is referred to as the slot. Electron density in the slot is usually low. However, it may increase a few orders of magnitude during magnetic storms. Like electrons, protons cannot be assigned to inner and outer zones since they have energies that decreases monotonically with increase in altitude, up to a trapping boundary of about 3.8 earth radii. Trapped protons may have energies as high as 5 MeV, with peak fluxes for the most energetic particles occurring at relatively low altitudes.

The South Atlantic Anomaly is also worth mentioning and is very important. It is a result of the offset of the earth's magnetic dipole to the axis of rotation by approximately 11 degrees with a displacement towards the western pacific. This causes a dip in the magnetic field, which causes the radiation belts to reach the lower altitudes over the coast of Brazil. This anomaly is responsible for most of the radiation absorbed by spacecraft in low earth orbits.

Cyclic variations and solar activity also have an effect on the flux of particles within the radiation belts. There are mathematical models that have been created to provide estimates for the fluxes of each particle in different orbits. Exposure to protons and heavy ions on spacecrafts is of grave concern since they are the main cause of single event effects, which I'll discuss later. Both protons and electrons should, however, be considered when it comes to total dose absorbed by spacecrafts in orbit.

What you can see in this animation is the satellite in orbit surrounded by a sea of particles. However, not every particle that interacts with the satellite will cause an upset. This can easily be explained by a concept called cross section.

Imagine two balls rolling towards one another. The likelihood of a collision depends on easy to grasp concepts. How big they are or how precisely they are aimed at each other. When you start talking about the likelihood of particles colliding, things get a bit trickier. That is why physicists use the term cross section.

Unlike solid objects, elementary particles behave as tiny waves of probability. In physics, a cross section describes the likelihood of two particles interacting under certain conditions. Those conditions include, for example, the number of particles in the beam, the angle at which they hit the target, and what the target is made of.

Cross sections are among the most important measurable quantities in nuclear, atomic and particle physics. We also used the concept to characterize the operation of electronics in the presence of high energy radiation.

What I will show in the next few short animations is an illustration of these concepts without relying on mathematical detail as to the calculation of the cross section. However, I am sure you will get a good understanding of what it means physically. This is important to understand how electronics are characterized for single event effects.

What you will see in the following number animations is a collection of 194 balls or targets arranged in a grid formation separated by 10 centimeters. Above it is a plane that releases 1000 smaller projectiles, also called particles, under the influence of gravity, and my aim is to see under what conditions the targets are dislodged from their positions and fall to the ground below. By counting the number of balls that fall to the ground and knowing the cross-sectional area of the target grid, we can get an estimate of the cross section. I also change the mass of the targets, the distance between them, as well as the horizontal target plane angle to see if the probability of interaction is function of these parameters.

It is important to note that the cross-sectional area of the projectile plane is larger than that of the target grid plane. If we assume that the projectiles are evenly distributed in the projectile plane, it is an easy calculation to get the actual number of particles that cross the target grid and use that in our calculations to get the cross section.

Note on the righthand side of the screen that the parameters of the experiment are shown. Also shown is a count to indicate the number of targets that fell to the ground. Next, we will show the same clips in slow motion and give a brief explanation to show all the interactions of the projectiles or the targets as a function of mass or energy and distance, among other considerations. In the first experiment, it can be seen that most of the projectiles simply fall between the gaps of the target grid with only some touching the targets. In this instance, both the projectile and target mass is 0.2 kilograms and the number of targets that fell is around 43.

In the second video, the angle of the target plane was changed to 45 degrees while everything else stayed the same. The number of targets that fell remains at around about 43.

In the third video, the target plane is rotated to 90 degrees. The experiment is repeated with everything remaining the same, and as expected, the number of targets that fell is close to 40.

In experiment four, the target plane is rotated by 135 degrees, which is equivalent to 45 degrees, and we expect the number of targets that fall to be within the same error of margin as 45 degrees, which is around 40.

Experiment five is interesting in a different way to the previous ones, because we changed the target mass from 0.2 kilograms to one kilogram to see if the result is similar or slightly differently. The results show that the total number of particles that fall is 27, which is significantly less than the 43 we had previously, meaning that mass, or energy, has an effect on the outcome.

Experiment six is even more dramatic than the previous one because we increased the target mass to 10 kilograms, leaving the projectile mass at 0.2 kilograms. The results show that only one of the targets fell, meaning that the projectile mass of 0.2 kilogram is not enough to cause much interaction. This is also

important when we do radiation experiments. We have to get the projectile energy correct to cause an effect in our electronics.

In the next animation the projectile as well as target mass is the same at 0.2 kilograms, however, we bring the targets closer to each other in the Y direction by 5 centimeters. We expect when you bring the targets closer together, it will be easier to dislodge, and indeed that is the case. This seems like common sense, and the results seem to support that assumption. The number of particles that interacted and dislodge the targets end up around about 60.

In the next experiment it can be observed that the target and projectile planes are not aligned. In other words, the entire 1000 projectiles do not flow through the target grid plane. In this case, our result is not valid, and we cannot do a proper calculation. Thus, it is important that we align the target and the projectile plane correctly with each other to be able to get sensible results. This is similar to what we do at iThemba labs as well. We must align the target properly with the beam.

Now for the interesting part of my talk. What you can see in the next animation is a very simple implementation of a satellite on board circuit that could represent an on-board computer. In the middle of the board, a microprocessor is located that counts from 0 to 7, making it a 3-bit counter. This simple circuit will illustrate the point of how errors can occur within satellite electronics.

This animation shows a microprocessor that has been decapsulated, showing the silicon die. Take note that the size of the silicon die is much smaller than the actual size of the microprocessor cover. The reason why we sometimes decapsulate it is because it is needed in the calculation of the cross section. We need to know the actual cross section of the silicon die to be able to perform our calculations.

Now that we discussed the circuit board, I would like to go a little bit deeper and show you the details of the implementation of a 3-bit counter. What can be observed is 3 flip-flops combined with combinational logic. Flip-flops are also called memory elements. These memory elements store what is called a finite state machine and implements its operation. Next, we convert the digital signals with a binary to 7 segment display so that the counter can be seen. This particular counter counts from 0 to 7, and then repeats itself.

The current animation is identical to the previous one, except that it is in a radiation environment. Although particles can be seen, the circuit performs exactly as intended. However, in the next example, an error occurs in one of these flip-flops that results in an error in the output.

In this video we focus on the middle flip-flop. The count sequence is the same as before. However, at some stage the middle flip flop will be affected by a particle strike and the internal signals no longer change as it should from black to blue and blue to black, as expected. At some stage the counter on the right does not count from zero to 7 in the correct sequence, which means an error has occurred.

Our job as engineers is to find ways to quantify the errors that occur. We have to find the cross section of this particular IC with no protection and find methods to mitigate these errors from occurring.

In the next circuit, we tripled the internal components. This is called triple modular redundancy. An error in one part of the circuit can be detected and mitigated by what is called a majority voter, to vote out an error signal. The error will still occur within the middle flip flop, however, the majority voter will only agree with the two on the sides and still give the correct output.

The problem with triple modular redundancy is that we are wasting space within the microprocessor because we can only use one third of its full capacity. However, if we want to have a circuit without any errors, this is the tradeoffs that we must make. There are others that will be introduced as we proceed. In the current circuit we only have one combinational logic or one copy thereof. This mean that an error there can still result in an error in the rest of the circuit.

In the following circuit, which is also an implementation of this 3-bit counter, we have, in addition to triple modular redundancy of the memory elements, also triple modular redundancy for the combinational logic. This is called full triple modular redundancy and is one of the most secure ways of making sure that no errors occur. However, this uses the most resources and is the most power-hungry implementation in an FPGA or microprocessor. The idea with this implementation is that we do not want any errors in the critical systems of the circuit. It is not the most efficient way of implementing a circuit within a microprocessor because in a satellite application you want to implement as much logic as possible. There are other ways, and we have developed some ways at the university to reduce the resources internally to a microprocessor.

What is shown in this next animation is the same 3-bit counter. However, instead of making use of full triple modular redundancy, we inserted a filter after the combinational logic. This filter, developed at Nelson Mandela University, can filter out glitches in circuits or single event transients. Instead of tripling the combinational logic, we can insert it after each output. This filter will detect a glitch occurring and will filter it out to give the correct signal at the output. The circuit saves space within the microprocessor compared to full triple modular redundancy.

In a real test implementation, we implement more complicated circuits with industry benchmark circuits that is put in beams. Single Event Effect (SEE) testing was carried out at the Neutron Therapy Vault of the NRF iThemba Labs in Cape Town, South Africa. The separated sector cyclotron at the facility is capable of accelerating proton beams to a maximum kinetic energy of 200MeV. However, our testing was carried out in open air at a single beam energy of 66 MeV in the Neutron Vault.

The board was mounted on an XY Table (not as shown in the animation). This XY Table, operated remotely, allows for vertical and horizontal positioning of the DUT with respect to the proton beam.

A control board was used to detect and flag any upsets that occurred in the Device Under Test (DUT) during testing while a National Instruments Compact DAQ card was used for remote data capture and monitoring via an ethernet cable. A wall of lead blocks was used to give some protection for the monitoring equipment against the radiation.

Test circuit 1, which implemented a shift register string with no protection, displayed the highest cross section per bit among all test circuits. This is indeed as expected, with test circuit 1 having 10 times the cross section per bit, at a proton energy of 66 MeV, than its nearest rival.

It was expected that test circuit 2 would have lower cross section per bit than the unmitigated design, since all latches were protected with local TMR. In spite of this, SETs were indeed expected to propagate to the memory elements, since the user logic was not protected. Compared to test circuit one, the results show that most SEE effects are due to particle strikes directly to the latches.

Test circuit 3 consisted of DMR protection of the user logic and one SET filter inserted before each TMR memory element. Although the user logic was protected against SETs, this circuit was still vulnerable to

SETs affecting the filter. However, the introduction of DMR and the SET filter did indeed decrease the cross section per bit, compared to the unmitigated design.

Similar to test circuit 3, test circuit 4 provided DMR protection of the user logic. However, in addition to this, it also provided TMR protection of the SET filters, which were inserted before each TMR latch, in addition to providing 2 majority voters for the next stage of the DMR user logic. This design would normally be expected to provide full SET and SEU protection, however, the global clock and clear signals were not protected, and an SET could still affect the latches and register as a SEU since it is the only source of errors together with the user IOs, which were located on the same FPGA bank. In spite of this, test circuit 4 indeed provided a lower cross section per bit than circuit 3.

Test circuits 5, 6,7 and is discussed in the next graph.

Test circuit 5, which were identical to test circuit 4, had the global clock and clear signals tripled to test whether errors on the global signals had a significant effect on the cross section. Indeed, test circuit 5 showed a 7 times lower cross section at 66 MeV, compared to test circuit 4, and the second lowest overall cross section per bit, with only Full global TMR having a lower cross section.

Test circuit 6, which implemented full triple modular redundancy, displayed the lowest cross section per bit than any of the designs. Since full global TMR is the most robust mitigation scheme, this result was expected. However, the full global TMR designs generally occupies the most device resources, for identical circuits. As with the other test circuits, no protected was provided for the user IOs, which is the only source of potential errors.

Test circuit 7 provided DMR SET protection of the user logic with 2 SET filters inserted before each latch, which was not protected against SEU's. Although the cross section per bit is lower than test circuit 4, it does not provided better SEU protection than implementation 5, where the global signals are tripled.

Test circuit 8 was the only implementation that provided SET mitigation of the user logic by making use of the delay element SET filter, and local TMR for the latches.

Compared to the unmitigated design, it provided 18 times better cross section per bit, with the only source of potential errors coming from the unmitigated IO ports. The worst case corresponds to the highest design's cross section running at the maximum allowed frequency, and in our case an infinite frequency due to the latch operation. This is indeed the unmitigated design, with the different implementations of the SET filter providing various levels of protection.

Although no protection of the IO logic was implemented, it is expected that an implementation of the user logic protection, with either test circuit 5 and 8, would provide maximum SEU protection, using minimal device resources.

The aim of the work was to demonstrate effectiveness of the AND-OR SET filter technique in the presence of proton bean irradiation, and this was demonstrated at a single proton energy, however, additional testing will be required to demonstrate the accuracy of the Bendel 1 parameter curves.

Results for 8 implementations with various SET propagation scenarios was presented. The experimental results shed light on the trade-off between area and reliability of the circuit. While the full TMR implementation shows the lowest SEU, it is also the costliest in terms of area. Therefore, a combination of redundancy and SET filter can be used for an optimal SEU mitigation.

All implementation circuits use latches which are either transparent or blocking. Edge triggered flip-flops with a small timing window will change the results as it would be hard for a SET in a combinational circuit to be latched into a flip-flop as compared to a latch.

Various implementations and evaluation in-beam show the efficiency of the AND-OR SET mitigation circuit in eliminating SETs and single event upsets (SEU) compared to unmitigated designs. Since the AND-OR filter techniques was previously shown to be more beneficial in terms of device resource overhead compared to full global TMR, it is a viable option for use in sequential circuits operating in a radiation environment.

The following results is that for a Xilinx Artix 7 FPGA. The difference in these results is that variation of the testing setup was carried out by manually degrading the beam energy level using Perspex placed in the line beam right ahead of the DUT. Three Perspex plates were used, each with different thick-ness (8mm, 16mm and 24mm) placed to allow a different number of particles through, while allowing minimum scattering. According to the Stopping and Range of Ions in Matter (SRIM) simulation at iThemba LABS, no Perspex translated to maximum energy available (i.e. 66MeV). The 8mm thick plate degraded the beam energy to 45.9MeV; 16mm thick plate degraded the energy to 31.969MeV while the 24mm plate degraded the energy to 7.79MeV. SRIM data was provided by our collaborator Dr Arno Barnard from Stellenbosch University.

The setup for the total ionizing dose testing is shown in the aerial view animation.

A new board undergoing testing is mounted on a fixed trolley that was placed beyond the turntable. This trolley is adjustable, as it allowed for the distance between the board and the Cobalt 60 source to be varied, effectively allowing for the dose rate to be chosen.

It was desired that the device under receive a total dose of 100 kRads, as many satellite missions are required to survive this dose. At the back of the trolley was a protective barrier formed by a series of interlocking lead blocks that served the same purpose as in the single event effects setup. It protected the monitoring electronics from getting damaged by the radiation. The support electronics was also set up in a similar manner as the set up at iThemba Labs, with the DAQ card that was directly connected to a Windows laptop that was located outside the radiation chamber.

The Ethernet cable was connected to the DAQ card and to the Windows laptop outside the radiation chamber through a cable duct that ran through a 1-meter-thick concrete wall of the chamber. Lead blocks with small cutouts for cables were inserted on either side of these cable ducts to minimize the amount of radiation and ionized air that could travel to the operator outside. During the TID test, the device was set up to run industry benchmark circuits while we monitored the supply current of the FPGA boards, as well as the IO currents of the FPGA chip.

Results shown in the next animation, will also be discussed later. However, I must add that my 13-year-old son and daughter insisted that I make night-time scene while walking through the irradiation facility. This animation was created purely for dramatic purposes. However, the layout is identical to the real building. It does give you a sense of what it feels like to walk through this building, especially if you are claustrophobic. So please bear with me and enjoy……

The results shown in this graph confirmed a new design technique for TID mitigation in Field Programmable Gate Arrays. The method consists of applying Switched Modular Redundancy to

configuration memory in the FPGA. For devices which are subject to gate bias cycling, the maximum acceptable dose is higher than if the irradiation bias were applied continuously. By adding redundancy and applying a resting policy, one can significantly prolong the useful life of MOS components in space.

It was shown experimentally that by applying FPGA system redundancy on a power cycling bases, the system lifetime is increased significantly. By resetting the configuration memory, the functional lifetime of the FPGA resembles that of power cycling. By applying redundancy in the configuration memory, the lifetime of the SRAM FPGA was increased in the presence of ionizing radiation. It was also shown that the IO ports do not contribute to the increase in power supply current and that the main cause of the increase current was due to the FPGA core.

What we show in the next two diagrams is the results of a signal that was sent to the input of the FPGA while we monitored the time delay to reach the output, before your irradiation. After radiation the same test was done. We found that there is an increase in the time delay, which tells us that total ionizing dose influence the timing parameters of the FPGA. This test was done for the Polar-Fire FPGA which showed a degradation of 7% in the delay.

The result of the next graph is that of the Intel Atom microprocessor. It failed at about 21 kRad, which means that it is not the best choice for a satellite that is going to be in low earth orbit.

To conclude, together with our collaborators at Stellenbosch University, the physicists at iThemba Labs and the Fruitfly Radiation Facility, Nelson Mandela University can perform Single Event Upset testing in order to determine device cross-section under various conditions, some of which was shown. We also developed a Single Event Upset Mitigation Technique to mitigate the adverse effects of high energy radiation, while saving device resources compared to Full Triple Modular Redundancy. The technique is fully patented in the US.

We are also able to qualify electronic devices for total ionizing dose, in order to determine under what conditions it will breakdown, and developed a technique to prolong its lifetime by means of Switched Modular Redundance. Together with space weather models, we can estimate the lifetime of a satellite in orbit. Based on the results of the Switched Modular Redundancy, we recommend that all critical parts of a satellite be switched off or put in standby mode when crossing the South Atlantic Anomaly.

The university is also doing Total Ionizing Dose testing on behalf of SCS Space, for the electronics of an export Satellite.

For more detailed technical information regarding my work, please visit my google scholar profile.