CREATION AND CHARACTERIZATION OF SILICON NANOWIRE ELECTRON RATCHETS FOR USE AS GEOMETRIC DIODES AT ROOM TEMPERATURE

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A dissertation submitted to the faculty at the University of North Carolina at Chapel Hill in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Chemistry.

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ABSTRACT

James Powell Custer Jr: Creation and Characterization of Room-Temperature Silicon Electron Ratchets for Use as Geometric Diodes
(Under the direction of James F. Cahoon)

Ratcheting effects, like that of a socket wrench, convert a fluctuating, unbiased force into unidirectional motion. If these effects could be applied to electrons, it may unlock advances in high speed signal processing and energy harvesting. However, to create an electron ratchet, control over the geometry must be achieved on the order of the mean-free-path of the electron. This level of precision was achieved using vapor-liquid-solid (VLS) growth of nanowires (NW) followed by wet chemical dopant-selective etching. Modulation of the nanowire diameter created a cylindrical sawtooth geometry with broken inversion symmetry on a nanometer length scale.

In a two-terminal device, the NW structures responded as a geometric diode that funnels electrons preferentially in one direction through specular reflection of quasi-ballistic electrons at the NW surface. This ratcheting effect manifests itself in an asymmetry in current when comparing forward and reverse bias currents. Generally it was shown that wires with deeper etching, leading to steeper funnel shapes, yielded higher asymmetries. With properly tuned surfaces, maximum asymmetries of $>10^3$ were achieved. To fully demonstrate the electron ratcheting mechanism the devices were measured with alternating current and showed charge rectification up to an instrument limited frequency of 40 GHz. Because the devices have ultra-low capacitance, their frequency response is believed to be ~1 THz and limited not by resistance-capacitance time, but by the electron flight time through the geometry. To gain insight through

simulation, a finite-element model was created to measure the electrostatics of the device, but its neglect for ballistic transport of charges, means that it did not predict the experimental current asymmetry. An analytical model was created to measure the transmission probability of a particle through a diode shape and a Monte Carlo model was made to consider charge carrier scattering and semiconductor physics as particles transport through the geometry. Both models agree with experiment, providing further evidence for the ballistic nature of the electrons in the geometry. The findings presented in this work demonstrate the creation of the structurally-tunable NW geometric diodes that have applications in THz sensing, data processing, and energy harvesting.

For everyone, together we can save the world. I can only hope this work made it a better place.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF EQUATIONS

LIST OF SYBMOLS AND ABBREVIATIONS

1D	One-Dimensional
2D	Two-Dimensional
2DEG	Two-Dimensional Electron Gas
3D	Three-Dimensional
A	Amps
AC	Alternating Current
ALD	Atomic Layer Deposition
AM	Amplitude Modification
BHF	Buffered Hydrofluoric Acid
BNC	Bayonet Neill–Concelman
C	Capacitance
^{o}C	Degrees Celsius
CVD	Chemical Vapor Deposition
cm	Centimeter
D	Outer Wire Diameter
d	Constriction Diameter
dbm	Decibel Milliwatt
DC	Direct Current
***D*e**	Diffusion Constant
DRIE	Deep Reactive Ion Etching
E	Electric Field
e	Fundamental Charge
EBL	Electron-Beam Lithography

EDS	Energy Dispersive X-Ray Spectroscopy
E_f	Fermilevel
E_{gap}	Bandgap Energy
ENGRAVE	Encoded Nanowire GRowth and Appearance through VLS and Etching
Eq.	Equation
eV	Electron Volts
F	Farads
f	Focal Length
fc	Cutoff Frequency
FIB	Focused Ion Beam
FE	Finite Element
fs	Femtosecond
g	Gram
GHz	Gigahertz
GSG	Ground Source Ground
Hz	Hertz
I	Current
IPA	Isopropyl Alcohol
IR	Infrared
I-V	Current-Voltage
k	Fermi Wavevector
K	Kelvin
k_b	Boltzmann's Constant
l	Constriction Length

L	Ratchet Length
LB	Landauer-Büttiker
L_T	Thermal Length
m^*	Effective Mass
mA	Milliamps
MFP, λ	Mean Free Path
mH	Millihenry
mL	Milliliter
MIBK	Methyl Isobutyl Ketone
MIM	Metal-Insulator-Metal
MMA	Methyl Methacrylate
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
mW	Milliwatt
mV	Millivolt
n	Electron concentration
N	*f*-Number
N_D	Donor Dopant Density
NP	Nanoparticle
NPGS	Nanometer Pattern Generation System
nm	Nanometer
NW	Nanowire
p	Hole concentration
PCB	Printed Circuit Board
PMMA	Poly(methyl methacrylate)

R	Resistance
RF	Radio Frequency
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealer
s	Seconds
S_{21}	Transmitted Power
sccm	Standard Cubic Centimeters Per Minute
SEM	Scanning Electron Microscope
SMA	SubMiniature version A
SMU	Source Measure Unit
STEM	Scanning Transmission Electron Microscope
T	Temperature
τ_m	Mean Free Time
TEM	Transmission Electron Microscope
THz	Terahertz
TP	Transmission Probability
UV	Ultraviolet
v	Velocity
V	Voltage
V_{app}	Voltage Applied
V_{DC}	Rectified DC Output Voltage
VLS	Vapor-Liquid-Solid
VNA	Vector Network Analyzer
XPS	X-ray Photoelectron Spectroscopy

^{o}	Degree
ε	Dielectric Constant
ε_0	Permittivity of Free Space
ε_R	Dielectric Constant of the Semiconductor
μ_e	Electrical Mobility
μm	Micron
Ω	Ohms
ψ	Potential
θ	Ratchet Angle
φ	Constriction Angle
ρ	Space Charge Density
δ	Ratio of Transmission Probability

CHAPTER 1: INTRODUCTION[1]

1.1 Semiconductors

Semiconductors are the backbone of all modern technology. Silicon (Si), the most widely used semiconductor, is the main component in typical solar panels as well as the material used to make the chips in our computers and phones. A semiconductor is as its name implies something with conductivity somewhere between a metal and an insulator. There are many types of semiconductors: group 14 elements, combinations of group 13 and 15 elements, and even organic compounds, but for the purpose of this dissertation I will be focusing on Si because of the high level of synthetic and compositional control that is possible with this material in a nanowire geometry..

At room temperature, Si typically has an intrinsic carrier concentration of ~$1x10^{10}$ cm^{-3}. To increase the carrier concentration and conductivity, Si can be doped with other elements that either add electrons to create *n*-type Si or add holes to create *p*-type Si. Compared to Si, group 15 elements have an extra electron, so when added to Si that electron becomes a free negative charge carrier. On the contrary, group 13 elements have one less electron than Si, so when they are added they form a hole which becomes a free positive charge carrier. For this work, Phosphorous (P) is used to create *n*-type Si, and Boron (B) is used to create *p*-type Si.

[1] Portions of this chapter are reprinted with permission from Custer, J. P.; Low, J. D.; Hill, D. J.; Teitsworth, T. S.; Christesen, J. D.; McKinney, C. J.; McBride, J. R.; Brooke, M. A.; Warren, S. C.; Cahoon, J. F. Ratcheting quasi-ballistic electrons in silicon geometric diodes at room temperature. *Science* **2020,** *368*, 177-180.

The addition of dopants can increase the room-temperature carrier concentration close to ~$1x10^{20}$ cm^{-3}. However, at doping levels above ~$1x10^{18}$ cm^{-3} the doping level is so high that the semiconductor can be considered degenerately doped. Degenerate doping is when the Fermi level of the semiconductor approaches $3k_BT$ of the conduction or valence band, where k_B is the Boltzmann constant and T is temperature. In this situation the Fermi level is close enough to the bands that the semiconductor acts like a metal with high conductivity and more of a sea of free charge carriers.

The ability for semiconductors to have different doping levels leads to many of their interesting and useful properties because their important parameters for electrical conduction can be tuned through doping. Doping level affects the amount of scattering in the system, the speed of the charge carriers, and many other things, so let's explore some of these parameters that are critical for working with and understanding semiconductors.

1.1.1 Mean Free Path

The MFP (λ) will have a dependence on the electron scattering rates within the semiconductor, which depend on temperature and defect density (related to the doping level). The value of MFP is important because in the limit where the MFP of the charge carrier is longer than a given distance of interest, the charge carriers can be treated like ballistic particles that do not scatter and travel like billiard balls bouncing through a geometry.[1] This gives rise to a lot of interesting properties that will be discussed later in the dissertation.

To determine the MFP all that is necessary is to know the speed of the electrons and the rate that they are scattering. Therefore, $\lambda = v\tau_m$ where v is the velocity of an electron and τ_m is the mean free time, or the momentum relaxation time. However, there are several different methods to calculate these values, so for brevity I will only go through a few.

1.1.1.1 Mobility

In order to get at the MFP of a charge carrier in the semiconductor, we must first think about the mobility of the charge carriers. Mobility describes how quickly a charge carrier can move through a semiconductor. Mobility can be simulated and modeled, or calculated from empirical fits for electrons and holes. For the purposes of this dissertation, I will discuss the empirically derived relationship between electrical mobility (μ_e) and donor dopant density (N_D) of *n*-type Si at room temperature (T = 300 K). The change in electrical mobility with N_D at 300 K has been empirically determined to follow the relationship[2]:

$$\mu_e(N_D) = \left\{92 + \left(\frac{1360 - 92}{1+(N_D/1.3e17)^{0.91}}\right)\right\} \text{cm}^2\text{V}^{-1}\text{s}^{-1} \ . \tag{1.1}$$

This relationship shows that mobility is ~1400 $cm^2s^{-1}V^{-1}$ up until a doping level of ~10^{16} cm^{-3}. Then it steadily decreases to ~100 $cm^2s^{-1}V^{-1}$ at ~10^{19} cm^{-3} and plateaus there for any higher doping levels.

1.1.1.2 Mean Free Time & Diffusion Constant

Once mobility is determined, it can be used to find the mean free time, or the momentum relaxation time (τ_m). Within the Drude model and parabolic band dispersion approximation, mean free time can be calculated using the following equation:

$$\tau_m = \frac{m^* \mu_e}{e}, \tag{1.2}$$

where m^* is the effective mass of the electron and e is the fundamental charge of an electron. Fundamental charge is a constant, 1.6x10^{-19} C, but the effective mass must be calculated for an electron in Si. To calculate m^* we must consider the electron rest mass (m_e, 9.1x10^{-31} kg) as well as both the longitudinal ($m_l^* = 0.98m_e$) and transverse ($m_t^* = 0.19m_e$) effective masses of the Si conduction band. For an electron moving in three-dimensions (3D) there are two longitudinal

modes and four transverse modes to consider. Therefore, we must take the weighted average of the longitudinal and transverse modes as such:

$$m^* = \frac{3}{\frac{1}{m_l^*} + \frac{2}{m_t^*}}. \quad (1.3)$$

This yields an m^* of $0.26m_e$, which can be plugged into eq. 1.2 to find τ_m. Note that if the charge carrier is moving in two-dimensions (2D) or one-dimension (1D) a different weighted average of the modes must be taken. Or, if the charge carrier is a hole and not an electron a different effective mass must be calculated. Before discussing electron velocity to get at the MFP, there is another value that is related to the scattering time that can be used with velocity to get the MFP.

The diffusion constant, D_e, characterizes the ability for charges to diffuse through a system. D_e can be related to μ_e using the Einstein relation, where:

$$D_e = \frac{k_B T}{e} * \mu_e. \quad (1.4)$$

With mean free time and diffusion constant, we can now find velocity to get the charge carrier MFP.

1.1.1.3 Charge Carrier Velocity

There are several different ways to think about the velocity of charge carriers in a semiconductor. First there is the thermal velocity (v_{th}) of the charges that is the velocity of the charges purely based on the temperature of the system. The value v_{th} can be calculated using:

$$v_{th} = \sqrt{\frac{3k_B T}{m^*}}. \quad (1.5)$$

At room temperature (T=300 K) with $m^* = 0.260m_e$, we get $v_{th} = 2.29 \times 10^7$ cm/s. This value can be multiplied by τ_m to find the MFP.

Alternatively, for ballistic regions within a semiconductor we can think of the velocity of a charge carrier as the velocity at which a charge is emitted from a source such as a metal or a degenerately doped section into a ballistic area. The velocity at which the electron is emitted through thermionic emission is called the Richardson velocity (v_R) and can be calculated as:[3]

$$v_{\mathrm{R}} = \sqrt{\frac{k_{\mathrm{B}} T}{2\pi m^*}}. \tag{1.6}$$

To get MFP using the Richardson velocity we must employ D_e instead of the mean free time. The MFP can then be calculated as follows:

$$\lambda = \frac{D_{\mathrm{e}}}{v_{\mathrm{R}}} \sqrt{\frac{3}{2\pi}}, \tag{1.7}$$

Despite these two methods appearing different and using different motivation, they actually give mathematically the same values for MFP when using the same doping level and temperature.

An alternate method to deduce λ is to use the 0 K Fermi velocity, v_{F}, to estimate λ as $\lambda = v_{\mathrm{F}}\tau_{\mathrm{m}}$. The value of v_{F} for the 3D Si conduction band assuming parabolic band dispersion and T = 0 K can be expressed for the longitudinal and transverse effective masses as $v_{\mathrm{F},l} = \hbar\, k_{\mathrm{F},l}/m_l^*$ and $v_{\mathrm{F},t} = \hbar\, k_{\mathrm{F},t}/m_t^*$, respectively, where:

$$k_{\mathrm{F},l} = \left(\frac{3\pi^2 n}{g}\frac{m_l}{m_t}\right)^{\frac{1}{3}}, \; k_{\mathrm{F},t} = \left(\frac{3\pi^2 n}{g}\sqrt{\frac{m_t}{m_l}}\right)^{\frac{1}{3}}, \tag{1.8}$$

$k_{\mathrm{F},l}$ and $k_{\mathrm{F},t}$ are the Fermi wavevectors for the longitudinal and transverse effective masses, $\hbar$ is Planck's constant divided by 2π, n is the 3D carrier density, and g the 3D degeneracy of the bands (g = 6 for 3D Si). Again, the weighted average of the transverse and longitudinal electrons

must be used to arrive at the correct velocity. Once the velocity is found it can be multiplied by τ_m from before to arrive at the MFP. Note that the Fermi velocity can be calculated for the case of 1D and 2D charge carriers, but the appropriate values of $k_{F,l}$ and $k_{F,t}$ must be used. I do stress though that these calculations are for carriers at 0 K, and because of this the carriers have no thermal energy distribution. Therefore, these may not be relevant for systems that are at room-temperature.

I also acknowledge that the calculated velocities are slightly greater than the saturation drift velocity (v_d). Saturation drift velocity occurs when there is a strong field that is moving carriers along a conductor. The carriers are speed up in the drift direction by the field, but they are slowed down by scattering events and impurities that limit the maximum velocity. The value of v_d has been empirically determined to follow the relationship[2]:

$$v_d = \frac{1.53e9T^{-0.87}E/1.01T^{1.55}}{\left[1+\left(E/1.01T^{1.55}\right)^{2.57e-2T^{0.66}}\right]^{1/2.57e-2T^{0.66}}}, \tag{1.9}$$

where E is the electric field. Using T = 300 K and a high field value of $E = 10^5$ V/cm we find v_d = 1.02 x 10^7 cm/s, which is ~2 times smaller than v_F. It should be expected that the high velocities would lead to a reduction in τ_m; however, the reduction of τ_m does not occur immediately but rather over the time scale for energy relaxation, which can be on the order of several hundred femtoseconds (fs).[3,4] Indeed, the phenomenon of velocity overshoot occurs because of this effect. Velocity overshoot is when a charge carrier can briefly achieve velocities significantly higher than the drift velocity. This occurs over small length scales, for example in ballistic regions, where a charge carrier is not scattering from impurities or phonons. Because a charge is temporarily between scattering events, it can achieve higher velocities and thus "overshoot" the saturation velocity.

1.2 Ratchets

Ratchets are part of our daily lives and for the most part go unnoticed, or at least aren't typically deeply thought about. A general definition for a ratchet is a system that only allows motion in one direction despite force being applied in more than one direction.[5] The prototypical example of a ratchet would be a socket wrench, which converts oscillating rotation into unidirectional mechanical action. However, ratchets can be found just about anywhere from seatbelts that lock using a ratchet mechanism when a sudden force is applied to biological motor proteins that convert thermal fluctuations into transport.[6] At its basic roots, being able to direct motion in the presence of a non-directional force has applications in almost every field from, chemistry,[7] to biology,[6] to physics,[8] so gaining a better understanding of ratcheting mechanisms can lead to deeper understanding in all of these fields.

1.2.1 Particle Ratchets

A tilting ratchet (Fig. 1), for instance, has a spatially periodic but asymmetric geometry or potential that converts an oscillating force into directed motion.[9] In the example in Fig. 1 the grey circles are particles that undergo directed motion when the asymmetric ratchet geometry is tilted back and forth.

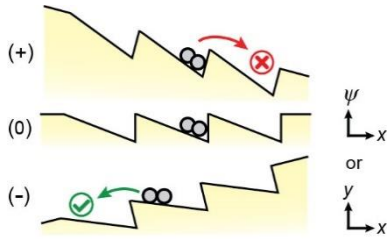

Figure 1.1: Tilting ratchet. Schematic illustration of the tilting ratchet under positive, zero, and negative applied forces. Axes denote asymmetry in potential (ψ) or geometry (y) as a function of spatial position (x).

Tilting ratchets have been realized for microscopic particle-based systems such as microfluidic beads.[10] In order to create a tilting ratchet, the particle that is being directed and the

geometry in which it is interacting with need to be on the same order of magnitude so that the particle can adequately experience the asymmetry in the geometry. Additionally the force being applied needs to be slow enough to match the speed of the particle. If the force being applied is fast (or too slow) the particle will not move in the desired direction. These requirements are not exceptionally difficult to achieve on a macroscopic scale where the particles can be seen optically and the geometry can be fabricated with standard methods; however, ratcheting systems become far more complicated when the particles that are being ratcheted are much smaller, say, the size of electrons.

1.2.2 Electron Ratchets

Electron ratcheting effects have remained a relatively illusive phenomena to experimentally measure, as only a few different materials systems have been reported[9,11-13] because of the requirements needed to ratchet electrons. Thinking back to the requirements for a particle ratchet, it follows that for an electron ratchet one needs a geometry with asymmetry on length scales of electron motion, or the MFP of an electron. MFP can be calculated as outlined in section 1.1.1. However, for reference typical MFPs at room-temperature in metals are single digit nanometers (nms) or less, and in semiconductors they range from 10s of nms to 100s of nms depending on the quality and type of semiconductor. Longer MFPs, upwards of 10s to 100s of μms can be achieved in select well-regulated systems, or at ultra-low temperatures near absolute zero.[14-16] This means that either you need to have a well-designed, complex system at low-temperature that has a very high MFP, or you need to have nanofabrication methods that grant precise control of geometries on the length scales of typical materials. An added complication for electron ratchets is that the surface of the ratchet must at least to some degree provide a specular reflection so that electrons can be properly directed. Specular reflection means

that when the particle bounces off of the surface its reflection has same angle out as the angle that it came in it. If this can be achieved, the electrons around the asymmetry can be treated like ballistic particles moving through a structure bouncing off of walls like billiard balls without scattering.[1] This changes how we think of standard current conduction because now current can be determined by the ratio of charges that make it through a ballistic region vs those that get back reflected.[1,17,18] This concept will be examined more deeply in chapter 6 of the dissertation. For now, let's take a look at previous work that has been able to create electron ratchets.

This exploration of prior literature is not intended to be a thorough review of past work but only a brief explanation of some of the key systems used to create electron ratchets. More specifically, I will only discuss tilting electron ratchets whose operation is dominated by ballistic or quasi-ballistic carriers inside systems containing fabricated asymmetric structures. This will exclude the robust field of "flashing ratchets",[19] where the operation of the ratchet is dominated by "flashing" an asymmetric potential to guide charge carriers in a given direction. This will also exclude the tangential field of "self-switching diodes", which rely on asymmetric potentials.[20]

With these restrictions on literature in mind, the electron ratchet field discussed here is limited down quite considerably, leaving only a few experimental systems. However, these systems still provide a rich background. Really only two prior materials systems have been able to show ballistic tilting electron ratcheting because of the prior discussion on requirements for creating electron ratchets.

The first materials system used to create these geometric electron ratchets were two-dimensional electron gasses (2DEG). A 2DEG can form in metal-oxide-semiconductor field-effect transistors (MOSFET);[21] however, the ones used for electron ratchet studies are formed from complicated systems built from layers of precisely tuned semiconductors as shown in Fig.

1.2. When the layers are tuned properly, a quantum well forms that allows a thin layer of electrons to move freely in 2 dimensions, but confines it in the 3rd. Like the name implies, these electrons behave like a gas in 2D in that they have extremely high mobilities and low scattering rates, especially at temperatures around 4 K. These high mobilities, and in turn long MFPs are a good system for studying electron ratchets because it means the fabrication methods only need to be precise within 100's of nms (or even up to μms at low temperature).

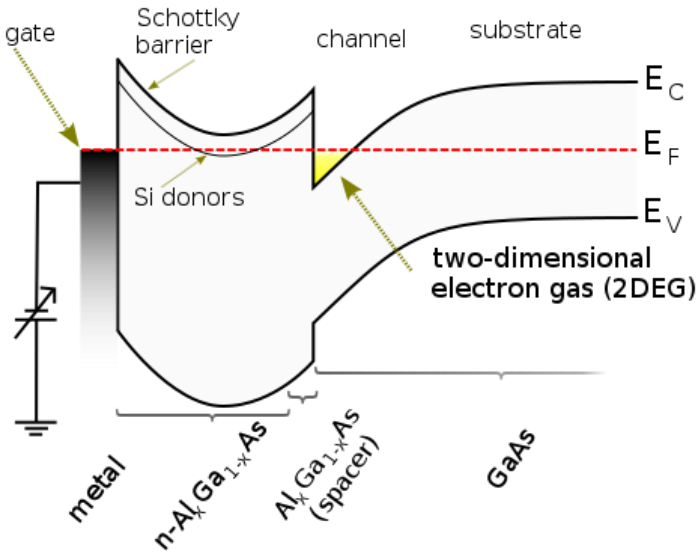

Figure 1.2: 2DEG band schematic. The band structure for a common method to make a 2DEG. The 2DEG forms in the highlighted yellow region of the band structure. Reused under the creative commons attribution-share alike 3.0 unported license.

There were essentially simultaneous demonstrations of the experimental geometric ratcheting effect first shown in 1998 by Song et. al.[22] and Linke et. al.[23] Song etched an asymmetric triangular antidot (aka a hole) in a 2DEG at 4 K.[22] The dot was in the center and there were 2DEG leads from either side and the top and bottom. When electrons were sent in from either side of the dot, they were forced down by the bouncing off of the dot and collected at the bottom. If ballistic effects were not in play, it would be equally likely for the electrons to go to the top or bottom. Linke etched away everything except for the shape of the triangular diode symbol and showed asymmetric electron transport at temperatures below 4 K. Linke's work was

followed up shortly after by putting the arrows in series,[9] but not much has come of it since. Song's work was quickly followed up by creating an array of smaller antidots that was able to function at room temperature and rectify signals up to 50 GHz.[11,13,24] This work has been followed up by others, but has not made many large strides since it's conception besides being experimentally shown to respond to frequencies into the 100s of GHz.[25,26]

The second material system that has been used to experimentally demonstrate geometric electron ratchets has been graphene. Graphene is a single sheet of atomically thin carbon that has received a lot of attention in the past two decades leading to the scientists that discovered it to win the Nobel Prize.[27] It can be made by peeling graphite with tape (called mechanical exfoliation) or by growing it using chemical vapor deposition (CVD). Similarly to a 2DEG, graphene has excellent transport of electrons in 2 dimensions with room-temperature mobilities in excess of 15,000 $cm^2\ V^{-1}\ s^{-1}$.[28] These mobilities lead to MFPs in the 100s of nms, which means that is the length scale the fabrication of the graphene must be on.

Graphene was simulated to work as a ballistic geometric electron ratchet,[29] and then was experimentally realized by Dragoman et. al.[30] and Zhu et. al.[31] at basically the same time. The graphene is shaped like an arrow that allows charges to be funneled through in one direction, but mostly blocked in a reverse direction. Both of these works report room-temperature electron ratcheting in the form of diodes that direct charges simply based on their shape. The work by Zhu et. al. from Bolder shows their device ratcheting a THz signal, but admittedly the signal is very weak (in the nV), and they do not report ratcheting at any other frequencies. This work was followed up a year later.[12] A few years later, Aimin Song revisited the designs of the antidots used in the 2DEGs, but this time used Graphene as the high-mobility material and showed excellent ratcheting behavior.[32] This work was followed up by demonstrating that the electron

ratchets could be used to sense and image in the THz spectrum.[33] This work has sparked a few follow-up papers that have studied modifying the geometry of the electron ratchets.[34,35] Thus far all tilting electron ratchets based on the geometry of the system have been fabricated in 2D materials. This brings us to today and my work.

In order to make an electron ratchet at room temperature in Si, there needs to be control of the geometry – and encoded asymmetry – on the order of the MFP of electrons in Si. Using the equations in section 1.1.1 we can find that the MFP is in the 10s of nms, but it is highly dependent on the doping level, where the lower the doping level the higher the MFP.

Nanowires (NW) offer a nice template to control the morphology of Si on the length scales of 10s of nms. NWs are one-dimensional (1D) structures that have a high aspect ratio where the length in one direction is many times larger than the other two directions. A typical method to make nanowires is the vapor-liquid-solid mechanism (VLS) using a chemical vapor deposition (CVD) system. To grow Si NWs by VLS gold (Au) nanoparticles (NPs) are deposited on a surface and heated above the Si/Au eutectic temperature. Then silane gas is introduced to the CVD and supersaturates the Au with Si. As more Si incorporates into the Au/Si alloy, a cylinder of single crystal Si crystallizes out beneath the Au with the diameter of the NP. Furthermore, dopant gasses can be introduced to dope the Si *n*- or *p*-type. This general method has been around since 1964,[36] and there have been many refinements and improvements to understanding it, but there have been very few techniques that have allowed encoding of highly controllable dopant asymmetry.

An improvement for VLS grown NWs came in the early days of the Cahoon lab. Early work in the group demonstrated a CVD system that had computer controlled mass flow controllers that were able to precisely control the gasses introduced into the reactor. This became especially

useful when doping the NWs because it allowed for axial control of the dopants within the NW with sub 10 nm resolution.[37] With precise control of the dopants within a NW came a new found control of the NW morphology when a dopant selective etch was employed. The etching method etched lower doped regions more quickly than regions that were higher doped. Essentially, anything that can be made with a lathe, could now be made on a nanowire with single-digit nm precision. Follow-up work refined the process further.[38-41] With precise control over both geometry and doping (and in turn MFP) down to single digit nms, the stage is set for Si NWs to be used as a model system for creating geometric electron ratchets.

1.3 Typical Diodes

The kind of electron ratchets discussed thus far manifest themselves as diodes, namely: geometric didoes, or morphological diodes. For the purposes of this dissertation, I will use geometric diode. To explore why geometric diode electron ratchets are interesting, let's first investigate how typical diodes are made, what they do, and what their limits are.

Diodes are pervasive in technology. There are millions in our phones, computers, and any other piece of technology. A diode allows electrical current to flow easily in one direction, but blocks it in the other direction. In all kinds of diodes, aside from geometric diodes, the current asymmetry is caused by an asymmetry in a potential barrier. In the presence of a time-averaged zero volt alternating current (AC) signal (Fig. 1.3A) one half of the wave can go through the diode, but the reverse direction of the wave is blocked. That chops the signal in half and makes the average no longer zero volts (Fig. 1.3B), which is called rectification. An AC signal can be rectified into a direct current (DC) output that can be used for data processing, sensing, or energy (Fig. 1.3). This ability allows diodes to take signals and turn them into the 1's and 0's that our devices read as data. There is a limit to the speed of the wave that can be rectified, which is

called the frequency response of the diode. Essentially, the faster an AC signal is, the more difficult it is to rectify for two major reason.

The first reason is that any intrinsic capacitance (C) within the diode acts to shunt the signal through the diode without rectifying it. In addition, any intrinsic resistance (R) serves to dampen the signal. Therefore, the combination of R and C called the RC time serve to limit the frequency that a diode can rectify according to the following equations:

$$f_c = \frac{1}{2\pi RC}. \tag{1.10}$$

Where f_c is the frequency at which the rectified DC output voltage has dropped to half of its maximum value (also called the -3db point). The second major reason that effects some diodes is the minority carrier diffusion time. For diodes that rely on both electrons and holes, their frequency response is limited additionally by the speed of the minority carriers (whichever carrier is less, holes or electrons) diffusing in and out of a region. Minimization of RC time and removal of minority charge carriers would allow faster signals to be rectified.

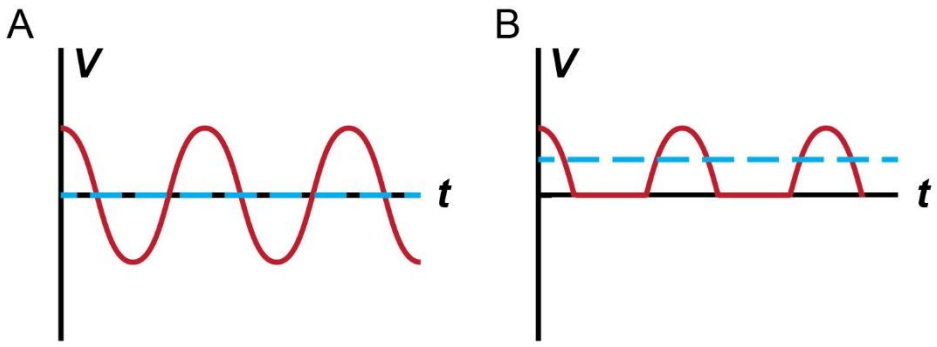

Figure 1.3: Signal rectification. (**A**) A time-averaged zero voltage signal in red. The dashed blue line is showing the zero voltage average vs time. The axes are voltage on the y-axis and time on the x-axis. (**B**) The same signal from A that has been sent through a diode (red) showing one half of the wave being chopped off to yield a time average that is no longer zero (blue dashed).

1.3.1 P-N Junction Diodes

Perhaps the most widely used diode is the p-n junction diode. This diode, like its name suggests is the junction between *p*-type Si and *n*-type Si. *N*-type Si's group 15 dopants donate their extra electron to create fixed positive charges and free, mobile negative charges. Conversely, *p*-type Si's group 13 dopants donate their holes (or absence of electron) to create fixed negative charges and free, mobile positive charges. When these two sides are brought together initially the mobile charges combine and cancel out to leave a region that has just fixed charges (Fig. 1.4). As the region of fixed charges grows it builds up an electric field that prevents more mobile charges from combining. An equilibrium is struck between drift and diffusion of mobile charges that fixes the size of the depletion region in the absence of an applied field. However, when a positive voltage is applied to the left side of figure 1.4 and electrons flow from right to left (current flows left to right) the depletion region shrinks. This is called forward bias because it is easier for charges to flow and thus is more conductive in this direction. When the voltage is flipped the depletion region grows and it is harder for current to flow. This is called reverse bias. It's this asymmetry in current created by the depletion region (potential barrier) that allows a p-n junction to function as a diode.

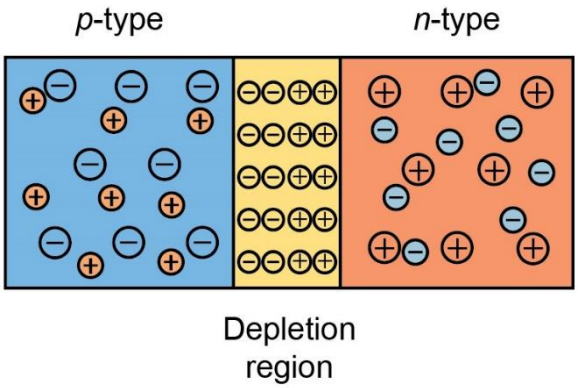

Figure 1.4: P-N junction schematic. Schematic diagram of the charges in a Si p-n junction. The blue side is *p*-type Si with fixed negative charges (blue) and mobile positive charges (orange). The orange side is *n*-type Si with fixed positive charges (orange) and mobile negative charges (blue). The yellow center is the depletion region where all the mobile charges have cancelled out.

P-N junctions are pervasive in technology because of their ease of fabrication and ability to come in many macroscopic shapes and sizes. They are also able to handle high voltages and currents depending on their fabrication. Unfortunately, they fall short when they are used to rectify high-speed signals. Their depletion region acts as a large potential barrier that further functions as a large capacitor in the middle of the diode. This capacitor shunts high-speed signals and prevents rectification. In addition, they are limited by the time associated with minority carriers diffusing in and out of the depletion region. Therefore, standard p-n junction frequency responses go out to the MHz, and under well-tuned systems can reach the low GHz. Lastly, to "turn-on" a p-n junction diode there needs to be constant DC voltage supplied to overcome the potential barrier and put the diode in a useful state. For Si, that voltage is ~0.7 V, which can be a considerable amount of power depending on the application.

1.3.2 Schottky Barrier Diodes

Schottky barrier diodes are the go to diode when it comes to high-frequency signals. A Schottky barrier is created at the interface of a semiconductor and a metal as shown in Fig. 1.5.[21] When the semiconductor comes in contact with the metal, the Fermi level equilibrates with the work function of the metal causing the bands of the semiconductor to bend (in the case of Fig. 1.5 the conduction band is bending up). In the situation in Fig. 1.5 electrons traveling from the semiconductor to the metal can overcome the potential barrier through thermionic emission or by tunneling. In the forward bias state the conduction band is shifted up allowing for easier transport. However, in reverse bias, the conduction band lowers creating a large potential barrier that is difficult to overcome. Note that this occurs so long as the semiconductor is not degenerately doped, in the case of degenerate doping, the depletion region becomes small enough for charges to easily tunnel through it in both directions and an Ohmic contact can be

formed. The diode behavior from a Schottky barrier is generated from an asymmetric potential barrier, but unlike p-n junctions, the potential barrier is thinner leading to less capacitance and there are no minority carriers to wait around for. Because of this, well-designed Schottky barrier diodes can operate into the 100's of GHz. However, because Schottky barriers are still potential barriers, a turn-on voltage must be supplied to put the diode in a useful state. This voltage is lower than a p-n junction, but still significant at ~0.2 V.

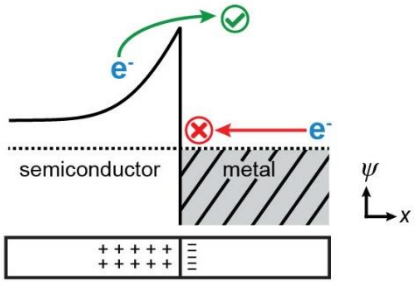

Figure 1.5: Schottky barrier. Band diagram of a Schottky-barrier diode (upper), showing metal on the right and the conduction band for an *n*-type semiconductor on the left. Dashed line represents the Fermi level. Lower schematic represents the depletion region, showing regions of positive and negative charge density at the semiconductor-metal interface.

1.3.3 Metal Insulator Metal Diodes

Metal-insulator-metal (MIM) diodes have been around since the 60's,[42] but they have gained more attention recently due to their potential ability to rectify frequencies into the THz. This type of diode is comprised of a thin (<20 nm) layer of insulator (or two) sandwiched between two different metals with different work functions.[43] When a voltage is applied, the Fermi levels of the metals and the insulator bands shift asymmetrically and allow tunneling or thermionic emission in one direction, but block it in the other. MIM diodes can rectify frequencies in to the THz (and potentially into optical frequencies[44]) and also have low, near zero turn on voltage. Unfortunately, they suffer from reliability and fabrication issues when trying to make devices that respond to the highest frequencies because the insulator needed is so thin (<5 nm), that there are frequently pinholes and other defects that short the device.

1.4 Geometric Diodes

Geometric diodes are fundamentally different from all other diodes because they do not use a potential barrier to create asymmetry in current. Instead, the asymmetry in current is created by the asymmetry in the shape of the system. When asymmetry is introduced along the direction of charge transport at the right scale it allows charges to flow more easily in one direction then the other (Fig. 1.6). Geometric diodes are based on the electron ratcheting mechanism, so all of the requirements discussed in section 1.2.2 apply here as well as the literature discussed in section

Geometric diodes are formed from one continuous material and are majority carrier devices that do not need a potential barrier. Because there is no potential barrier, theoretically geometric diodes can achieve truly zero-bias turn-on voltage, where there is no DC voltage that is needed to be supplied to put the diode into a useful state. In theory then, the same signal that is being sent to a device, can then be rectified into useful power because there is no power lost from supplying a constant DC voltage to turn the diode on. Additionally, they have exceptionally high theoretical frequency response. Their frequency response is not dictated by RC time because their capacitance is so low, it is instead limited by the flight time of the charge carriers through the system. They can theoretically achieve frequency responses into the THz.

The THz region of the spectrum is relatively uncharted territory. From ~0.1 to ~10 THz is commonly referred to as the THz gap where there are distinct lack of practical devices.[45] This region of the spectrum has waves that are very hard to sense because they are typically too fast to be rectified by traditional diodes, but the waves do not have enough energy to generate an electron-hole pair for photocurrent generation in devices. The combination of THz sensing, and zero-bias turn-on voltage unlocks many potential applications such as: high-speed data transfer,

astronomical exploration, materials defect characterization, security, and long wavelength energy harvesting.[46]

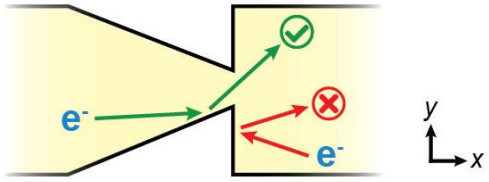

Figure 1.6: Geometric diode schematic. Schematic illustration of a geometric diode in a sawtooth geometry showing specular reflection of electrons coming from the left and right.

CHAPTER 2: METHODS[2]

2.1 Nanowire Growth

2.1.1 Instrumentation and Gasses

Nanowires (NWs) were grown via the vapor-liquid-solid (VLS) mechanism in a home-built, computer controlled chemical vapor deposition (CVD) system. The system is constructed primarily of 304L stainless steel tubing joined by ConFlat fittings (Kurt J. Lesker) or welds. The oven is a single-zone 1 inch tube furnace (Lindberg BlueM) that heats a 1 inch fused-quartz tube (Chemglass Life Sciences) mounted via Ultra-Torr fittings (Swagelock). Individual gas flows are controlled by fast mass flow-controllers (MKS P4B). The vacuum pumping system uses a Kashiyama SDE120TX dry screw pump to obtain a base pressure of ~3.5 x 10^3 torr. A custom built Labview program controls all gas flows, pressures, and heating. Gases used include hydrogen (H_2; Matheson TriGas; 5 N semiconductor grade), silane (SiH_4; Voltaix), phosphine (PH_3; 1000 ppm PH_3 in H_2, Voltaix), diborane (B_2H_6; 1000 ppm PH_3 in H_2, Voltaix), and hydrochloric acid (HCl; Matheson TriGas, 5N). Prior to any reactions, the quartz tube is heated to 600 °C, and each dopant gas was pulsed for 30 seconds to remove excess pressure from the line before then being heated to 950 °C for 1 hour with 20 sccm of Ar flowing to remove contaminants. If any tube will be exposed to HCl an "HCl bakeout" is used to clean the tube initially and from time to time as dopant gases deposit on the surface. For the HCl bakeout the

[2] Portions of this chapter are reprinted with permission from Custer, J. P.; Low, J. D.; Hill, D. J.; Teitsworth, T. S.; Christesen, J. D.; McKinney, C. J.; McBride, J. R.; Brooke, M. A.; Warren, S. C.; Cahoon, J. F. Ratcheting quasi-ballistic electrons in silicon geometric diodes at room temperature. *Science* **2020,** *368*, 177-180.

quartz tube is heated to 950 °C and HCl (2 sccm) and Ar (18 sccm) are flown for 10 minutes. Then the HCl is turned off and 20 sccm Ar is flown for 50 minutes.

2.1.2 Substrate Preparation

The growth substrate began as a 380 μm thick Si wafer with 600 nm of wet thermal oxide (University Wafer). The wafer was cut into sections ~ 2 cm x 1 cm because that fits nicely into the tube furnace. These sections were sonicated in acetone, then rinsed with acetone and isopropyl alcohol (IPA) and dried with nitrogen. This cleaning process removes dirt and dust from the surface. The substrate was then inserted into a UV-Ozone cleaner (Samco UV-1) for 300 s at 150 °C for further cleaning. The substrate was then covered in poly-L-lysine (0.1% w/v in water) for ~ 4 minutes to make it hydrophilic. The substrate was rinsed with nanopure water (Barnstead Nanopure; 18 MΩ*cm) and dried with nitrogen. Gold nanoparticles (NPs) (BBI International; citrate stabilized) of diameters 100-200 nms are diluted in nanopure water at a ratio of 1:4 and dispersed onto the substrate for ~ 4 minutes. This ratio and time gives a good density for wire transfer to device substrates. The substrate was then washed with nanopure water and dried with nitrogen, and placed in the UV-Ozone cleaner for 300 s at 150 °C. The substrate is then inserted into the fused quartz tube which is attached to the CVD. The tube is evacuated to ~ 3.5×10^{-3} Torr and the temperature is stabilized to the temperature at which the nanowire growth will begin.

2.1.3 420 °C Growths

NWs were nucleated at 440-450 °C with 200 standard cubic centimeter per minute (sccm) H_2 and 2.00 sccm SiH_4 at 40 torr total reactor pressure for 15 minutes. Following nucleation, a degenerately doped *n*-type section was grown by adding a flow of 20 sccm PH_3 while simultaneously ramping the temperature to 420 °C over 15 minutes. To encode a sawtooth

portion into the wires, the PH_3 flow was controllably ramped from 20 to 0 sccm in steps with a duration of 3 seconds or more each, and then abruptly returned to 20 sccm to encode a second degenerately doped section. Different durations can be used to form different geometries. For all *n*-type geometric diode single-NW devices, the dopant precursor flow rate was set to 0 sccm (i.e. completely off) for 15 seconds at the end of the ratchet geometry and before the second degenerately-doped segment, correlating to ~50 nm of the typically ~400 nm total ratchet length. The importance of this will be discussed in chapter 3 and chapter 6. Attempts to grow *p*-type wires using B_2H_6 as the dopant gas were unsuccessful at this temperature.

2.1.4 510 °C Growths

NWs were nucleated at 510 °C with 200 sccm H_2 and 2.00 sccm SiH_4 at 40 torr total reactor pressure for 15 minutes. Following nucleation, a degenerately doped *p*- or *n*-type section was grown by adding a flow of 15 (17) sccm B_2H_6 (PH_3). To encode a sawtooth portion into the wires, the B_2H_6 or PH_3 flow was controllably ramped from 20 to 0.35 or 0 sccm in steps with a duration of ~3 seconds or more each, and then abruptly returned to 20 sccm to encode a second degenerately doped section. For all *n*-type geometric diode single-NW devices, the dopant precursor flow rate was set to 0 sccm (i.e. completely off) for 3 seconds at the end of the ratchet geometry to achieve a low doping level. Note that for *p*-type wires a dopant precursor flow went down to 0.35 or 0 sccms, but the doping level in the *p*-type wires is much lower than the *n*-type wires, so a similar or lower doping level compared to the *n*-type can be achieved without turning off the dopant precursor flow.[40] However, ideally, the *p*-type wire growth should go to zero to achieve the highest MFP.

2.2 Nanowire Etching

After growth, NWs were mechanically dry transferred to device substrates (discussed in section 2.5). A standard wet chemical etch consists of the following steps. Etching in buffered hydrofluoric acid (BHF; ~5% by volume) for ~10 s to remove the surface oxide. Rinse by dipping in two separate nanopure water cups for ~10 s to remove the BHF. Rinse by dipping in semiconductor grade IPA for ~10-30 seconds to remove the water. (It seems that the IPA helps the wires stick to the surface.) Dipping in a room-temperature aqueous KOH solution (20% by weight) for a precise time (typically 30-200 s) to achieve the desired morphology. (KOH is used because it is able to etch the NWs based on how doped they are. The more doped the wire, the less it etches.) Rinse by dipping in an aqueous solution of acetic acid (~2 % by volume) for ~15 s to quench the KOH and stop etching. Rinse by dipping in nanopure water for ~10 s. Rinse by dipping in IPA for ~10 s. (Ending with IPA helps the wires stick to the surface. Water more easily picks up and removes wires because of the interplay of surface tension and adhesion.) Blow drying with nitrogen. The KOH solution selectively etches the sections that have a lower doping level faster than the sections that have a higher doping level. The degenerate sections nominally do not etch. For wires that are grown at 510 °C, there is typically gold on the surface that prevents the etching. To get rid of the gold, a gold etch is used. A gold etch consists of the following steps. ~10 s in BHF to remove oxide that can form over the gold, ~10 s in nanopure water rinse, ~10 s in IPA rinse, ~30-60 s in aqueous KI solution (KI:I_2:water, 1:1:4 by weight) to dissolve the gold, ~10 s in water x2 rinse, ~10 s in IPA rinse, blow dry with nitrogen. Following the gold etch, the standard etch conditions can be used. For *n*-type wires grown at 510 °C, if the maximum dopant precursor flow (20 sccm) is used, then the doping level is high enough to achieve BHF etching on the degenerate sections. Therefore, a slightly lower flow of 17 sccm is

used to prevent BHF etching while still maintaining a good degenerate etch stop in the KOH solution.

2.3 Surface Modification

For wires that do not have a specific surface modification conducted on them, a native silicon oxide of ~1-2 nm will grow on the wires over the course of weeks.[47] The majority of the oxide will form in the first day, but it can take up to 2 months to fully reach it's temperature limited form.[47] For devices where a specific surface modification is not noted, the devices were attempted to be measured as quickly as possible (and in a vacuum chamber) after device fabrication to minimize the formation of oxide (discussed further in electrical measurements section).

2.3.1 Alumina Coating

Alumina deposition was performed on device wafers prior to device fabrication using a Veeco/Cambridge Nanotech Savannah S200 atomic layer deposition (ALD) system. Immediately preceding alumina deposition, NWs were etched with BHF to remove surface oxide. The ALD deposition parameters included 200 °C chamber temperature, 20 sccm nitrogen carrier gas flow, 0.015 s pulse times for water and trimethyl aluminum, and wait times of 8 s. 100 cycles were performed to produce an alumina thickness of ~10 nm. This recipe was chosen because it has been shown to be reliable, but other methods could be used. Device fabrication followed the same procedure as for NWs without alumina treatment (discussed in section 2.5) except that the BHF etch prior to metal deposition was extended to 75 s.

2.3.2 Thermal Oxidation and Hydrogen Anneal

Oxidation and annealing processes were conducted in a MILA-5000 rapid thermal annealer (RTA). NWs were thermally oxidized and annealed on device substrates directly

following aqueous KOH etching but prior to device fabrication. Thermal oxidations were performed in pure oxygen (AirGas, Ultra-high purity) by ramping to 900 °C over 30 seconds, holding at temperature for an additional 30 seconds, cooling from 900 to 300 °C in ~20 seconds, and then cooling from 300 °C to room temperature in ~3 minutes, yielding an oxide thickness of ~6 nm.[48] We were hesitant to hold the high temperature for any longer than 30 s, because longer exposure to high temperatures could lead to dopant diffusion.

Hydrogen anneals were performed in forming gas (5% H_2 in 95% N_2; AirGas 5% hydrogen balance nitrogen standard). The samples were ramped to 600 °C over 30 seconds, held at 600 °C for 15 minutes, ramped from 600 °C down to 300 °C over 1 hour, held for 15 minutes at 300 °C, and ramped to room temperature over an hour. These forming gas anneal conditions have previously been determined to yield low surface recombination velocities in Si NW photovoltaic devices[49] meaning that they passivate surface defects.

2.4 Imaging

To image the wires optically, a Zeiss HAL 100 halogen lamp on a Zeiss AxioImager A2M upright microscope was used. A 10x objective with a numerical aperture of 0.2 and a working distance of 14.3 mm (Zeiss EC Epiplan 10x/0.2 HD WD=14.3 M27) was used for low magnification images and spectra. A 50x objective with a numerical aperture of 0.7 and a working distance of 1.1 mm (Zeiss EC Epiplan 50x/0.7 HD WD=1.1 M27). The majority of imaging was done in darkfield mode because in darkfield, the light scattered off of the nanowires is highly diameter dependent and can give a rough idea of the diameters of the samples.

For scanning electron microscopy (SEM), a FEI Helios 600 Nanolab Dual Beam system was used. Typical acceleration voltage was 5 kV with an imaging current of 86 pA. This voltage and current tends to not damage the samples and still gives good image quality. Transmission

electron microscopy (TEM), scanning transmission electron microscopy (STEM), and energy dispersive x-ray spectroscopy (EDS) was performed using an FEI Tecnai G2 Osiris S/TEM with Super-X EDS system. NWs were mechanically contact-transferred directly onto lacey-carbon TEM grids (Ted-Pella #01895). STEM imaging was performed at 200 kV with a sub-nanometer probe with a current of ~2 nA (spot size 3, 4k extraction voltage). Drift-corrected STEM-EDS maps were obtained using the Bruker Esprit software.

2.5 Device Fabrication

2.5.1 Marker Pattern Creation

First, a device substrate is chosen based on if the device will be used for high-frequency measurements, or just DC measurements. Device substrates consisted of either Si wafers with 100 nm of thermal oxide and 200 nm Si_3N_4 for DC measurements (referred to as DC substrate) or 0.5 mm quartz wafers with 400 nm of LPCVD (low-pressure CVD) Si_3N_4 on both sides for AC measurements (referred to as AC substrate). Both substrates are capped with Si_3N_4 to prevent etching of the surface in BHF and KOH. For DC substrates, the conductive silicon allows for ease of imaging in the SEM. For AC substrates the quartz prevents parasitic capacitance that affects AC measurements. Substrates were prepared by etching marker patterns into their surfaces using deep reactive ion etching (DRIE; Alcatel AMS 100). The substrate is coated in 3 layers of methyl methacrylate (MMA; MicroChem (8.5) EL9), and 1 layer of poly-(methyl methacrylate) (PMMA; MicroChem 950PMMA.A7) to generate a total thickness of ~1.5 μm. This thickness creates a thick enough mask that the DRIE will not etch fully through. Each layer was deposited and then spun for 5 s at 500 rpm, and then 30 s at 4000 rpm using a spin coater (Laurell Technologies Model WS-650-23B). After spinning, each layer was baked at 180 °C for 60 s.

The marker pattern is then defined with electron-beam (e-beam) lithography (EBL) using an FEI Helios 600 Nanolab Dual Beam System and Nanometer Pattern Generation System (NPGS). An accelerating voltage of 30 kV was used with a beam current of 340 pA and 11 nA for the smaller and larger sections respectively, with a dosage of ~300-400 μC/cm^2 for both. These settings allow for a high enough voltage and current to turn the PMMA in MMA where the beam hits it. The smaller, inner pattern is written at 100x, and the larger outer pattern is written at 65x. 100x allows for the writing of precise small features, and 65x is the farthest the SEM zooms out to achieve the largest field of view. The pattern is developed in methyl isobutyl ketone (MicroChem MIBK/IPA 1:3 Developer) for 60 s before being rinsed with IPA. The MIBK only dissolves regions where the SEM beam hit the polymer because the MIBK only dissolves MMA, not PMMA. If longer than 60 s is used to develop, the MIBK will undercut and dissolve the MMA that is under the PMMA that is still there.

For DC substrates, the DRIE recipe used was 2 minutes of 25 sccm C_4F_8 and 125 sccm Ar with 1000 W source power and 100 W substrate bias and 10 mbar He pressure to etch through the nitride and oxide. Then 45 s of 100 sccm Ar and 100 sccm of SF_6 with 500 W source power and 50 W substrate bias and 10 mbar He pressure to etch through the Si. The SF_6 chemically etches the Si while the initial step just physically ablates the surface. This yielded an overall etch depth of ~1 μm. For quartz wafers, the DRIE recipe used was 16 sccm of C_4F_8 and 24 sccm Ar with 600 W source power and 100 W substrate bias and 5 mbar He pressure. The process was run for 2 min and then transferred to the interlock to cool for ~5 minutes. That was repeated twice for a total of three times to yield a total etch depth of ~900 nm and a substrate:polymer selectivity of ~1:1. Excess polymer left after the DRIE was cleaned off with acetone, IPA, and UV-Ozone. More details are discussed in chapter 5.

Prior to marker patterns being made by DRIE, the pattern was made with a metal stack (Cr, 3nm; Au, 50 nm) evaporated with e-beam evaporation. These metal marker patterns are not typically used anymore because the metal negatively affects the etching of the NWs and can be easily rubbed off when transferring wires to a marker pattern. The DRIE etched patterns are more difficult to see in the SEM for NPGS, but when using a low scan speed it is okay. The DRIE patterns are more robust and offer more consistent NW etching in addition to minimizing stray capacitance in AC measurements.

2.5.2 Contact Creation

2.5.2.1 DC Devices

For wires that do not need to be measured at high-frequency, NWs are dry transferred onto a marker pattern on a DC substrate and etched to the desired structure. Then the device is coated with 2 layers of MMA and 1 layer of PMMA (MicroChem 950PMMA.A2). This thickness allows for the polymer to be significantly taller than the wires. A pattern for the metal contacts was defined using EBL with NPGS, same conditions as the marker patterns, except that a dosage of ~330 μC/cm^2 is used. This dosage turns the PMMA to MMA, but does not over expose the sample and distort the pattern. The contacts go from larger outer pads, to smaller pads, and then to ~1 μm contacts that connect to each wire (Fig. 2.1A and C). The MMA/PMMA was developed according to the same conditions as the marker patterns. The device was etched in BHF (~50 % in water) for 10 seconds (to remove silicon oxide on the wires where the metal contacts will contact the wire), and electron-beam evaporation (Kurt Lesker PRO Line PVD 75) was used to deposit 3 nm of Ti and 150-300 nm of Pd to form the contacts depending on the diameter of the wires. The 3 nm of Ti makes the metal stick to the surface, but Ti has a mismatch in work function compared to Si. Therefore, Pd is needed to match the work function of silicon

to form ohmic contacts. The electrons from Pd can tunnel through the Ti to match the work function. Typically the amount of metal deposited was the NW diameter + 50 nm.

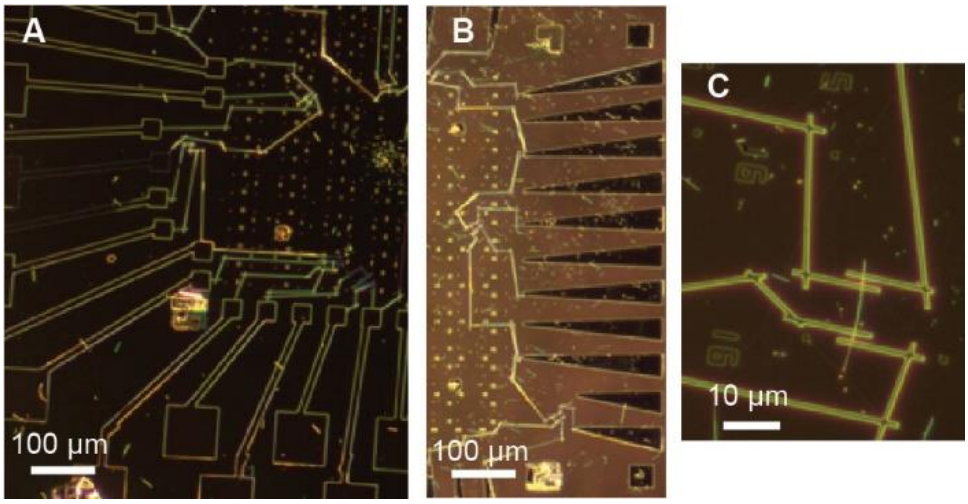

Figure 2.1: Metal contacts. Examples of (**A**) DC contacts where no high-frequency is needed, (**B**) Strip-line high frequency contacts, (**C**) a zoomed in view of the metal contacts connecting to a wire.

2.5.2.2 AC Devices

For wires that will be used in high-frequency measurements, a quartz AC substrate marker pattern is used. For this fabrication, the steps are all the same as the DC substrate devices, except for the following. 3 nm of AuPd alloy was sputtered on the PMMA before writing contacts using NPGS to reduce charging during e-beam lithography (EBL). Then after writing the contacts, but before developing the contacts, a gold etch (as outlined in the etching section) is done for 30 s to remove the sputtered metal. Previously, PEDOT-PSS was used to mitigate the charging in the EBL, but it left residue that made the marker patterns unusable.

There is a significant difference in the design of the contacts between the DC and AC (high-frequency) devices. For AC measurements, the metal was designed to smoothly taper down to the size of the contacts to the wire in order to minimize reflected power from abrupt

geometry changes (Fig. 2.1B).

2.5.2.3 THz Devices

Devices used to measure 600 GHz signals were fabricated with the same process as the AC devices with the exception of instead of creating a pattern of various contacts for each marker pattern, only one, relatively large meta-material antenna was patterned for a single wire across the marker pattern (Fig. 2.3).

2.5.2.4 CO_2 Devices

Devices used to measure 28 THz signals from a CO_2 laser were fabricated with the same process as the DC devices with the exception of metal antennas (the metal same as the contacts) that were one, one half, and one fourth wavelength of the signal were fabricated on each wire. In retrospect however, the fabrication method of the AC devices would have been better suited for these devices to reduce parasitics, and the antennas should have been simulated on top of the substrate to ensure they were resonant at the proper wavelength.

2.6 Electrical Measurements

All electrical measurements, except where noted, were performed using a probe station (Lakeshore TTPX Cryogenic Probe Station) under vacuum (<5 mTorr) to prevent oxide formation and also prevent water and other impurities from being on the NW surface. Something like a small film of water can serve to gate the NWs when they are as small as they are. Typically, less than 1 hour elapsed between etching of the NW in BHF and KOH solutions and coating the NW in polymer (ideally it should be done as quickly as possible to minimize oxide formation). Less than 48 hours elapsed between etching and insertion in the probe station (this time includes time in the evaporator at ultra-high vacuum). Ideally this time should be minimized to prevent oxide formation. If another surface modification method is being used one should be

careful to not have oxide under the coating by preventing air exposure or BHF etching the wires just before surface modification. Each wire had at least 2 metal contacts on either side of the diode to ensure that the contacts were Ohmic.

2.6.1 DC Measurements

DC measurements were conducted using a source measure unit (SMU, Keithley 2636B) with triax cable connections (Belden 9222 50 Ω) and ZN50R-25-W lakeshore probe tips. For low temperature measurements, a Cryofab liquid nitrogen dewer was used to provide liquid nitrogen to the probe station and a Lakeshore Model 350 Cryogenic Temperature Controller was used to control the temperature of the stage between 77 K and 350 K. Between changes in temperature, tips were lifted (changing temp will make the tips move from metal expansion) and the sample was given several minutes to equilibrate in temperature before being measured. For DC measurements, the DC substrate and contact pattern, showed in Fig. 2.1A was used to maximize the number of devices that could be fabricated on a single chip.

2.6.2 AC Measurements

Many different AC measurements were attempted. This methods section will only go through what worked, but chapter 5 will go into more detail on the measurements that were tried and didn't work.

AC measurements were conducted according to the schematic in Fig. 2.2 with a Keithley 2636B SMU serving as the voltmeter and an Antrisu 37369C vector network analyzer (VNA) serving as the signal source. The inductor was 7.8 mH and was used to remove parasitic series capacitance. The resistor was 30 MΩ and was chosen to approximately match the voltage drop across the diode while staying mismatched from the 10 GΩ input impedance of the SMU. The capacitor was 6.8 nF and was chosen to minimize background noise from parasitic elements and

to integrate the signal. The AC signal was delivered from the VNA to the probe station through a 30 inch SMA cable (CentricRF 40 GHz 2.92 mm SMA C549-086-30). From the probe station, the signal traveled through a 7 inch internal SMA cable (Lakeshore HMWC-07-00K 40GHz) to a 50 μm GSG probe tip (GGB Picoprobe 40A-GSG-50). For AC measurements, the AC substrate and stripline contact pattern, shown in Fig. 2.1B was used reduce back reflections of the AC signal that arise in abrupt changes in geometry. Additionally, a ~1/2 inch Teflon block was used instead of the standard stage in the probe station to further reduce stray capacitance.

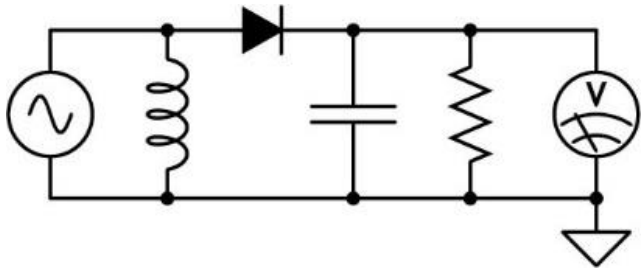

Figure 2.2: AC measurement schematic. Circuit diagram of the AC measurement setup.

2.6.2.1 AC Power Sweeps

To measure if the AC signal was being rectified at all, the signal was sent to the diode and the amplitude of the signal was slowly increased from essentially off to values around -1 decibel milliwatts (dbm). Powers greater than this could be supplied to the diode, but at times they ran the risk of destroying the NWs, and after destroying too many nice wires, I decided to play it safe. Additionally, any time anything was turned on or off on the VNA I lifted the tips to avoid an accidental shock to the NW. As the VNA was set to sweep in power, the SMU was holding the open circuit condition and measuring voltage. This measured the output from the NW, which is the rectified DC voltage from the AC signal.

2.6.2.2 Frequency Response

For the frequency response measurements the same power sweep measurement was done just at different frequencies. Frequency could not be swept because in our measurement setup

there is not a clear way to correlate the output from the VNA to the measured signal in the SMU. Additionally the measurement speed of the SMU is slow. This is a disadvantage of the current measurement setup that could be improved with different instrumentation.

Returning to the measurement, the difference between the maximum rectified DC output voltage and the noise floor was taken to get a value for DC output. Measurements were done in groups of 5 with frequencies that were close to each other to determine if a signal was coming from a specific resonance in the measurement or if it was a cleaner signal. To normalize out some parasitics that were causing less power to get to the diodes to be rectified (and artificially lowering the DC output), the DC output voltage was divided by the S_{21} measurement of power transmitted through the measurement setup. The S_{21} measurement was done on stripline metal contacts on the same substrate as the devices. One GSG probe was put on one side of three contact lines and another probe was put on the other end of the three lines. To get the transmitted power, the same kind of cables and probes were used for the input and output. This is not ideal, because it is in theory double the parasitics, but it gets us a rough estimate of how the power is transmitting through a blank measurement setup with no diode in it. Also note that in name our two GSG probes are the same, but they appear slightly visually different under microscope.

2.6.2.3 AC Psuedo-Solar Cell Measurements

To mimic the operation of a solar cell, measurements were conducted to extract the power output from the diodes from an incident AC signal. The VNA was held at a constant power and frequency and the SMU swept an applied voltage and measured the current.

2.6.2.4 AC Signal Processing Measurements

To demonstrate signal processing abilities an amplitude modification (AM) signal (programmed using the Tektronix ArbExpress 3.4 software) was encoded using a Tektronix

AFG3102C arbitrary function generator. The signal was applied to a constant power AC signal from an HP 83623a signal generator to modulate the signal. The SMU was set to the open circuit condition and measured voltage. The voltage measurement was the limiting factor for the speed of the measurement because the SMU cannot measure voltage very quickly.

2.6.2.5 600 GHz Measurements

These measurements were conducted in collaboration with the Padilla group at Duke University. To demonstrate rectification into the Terahertz (THz) regime, NWs were connected to meta-material antennas (designed by the Padilla group) on the AC substrates. The antennas (Fig. 2.3) were tuned to be resonant at ~600 GHz according to finite-element simulations.

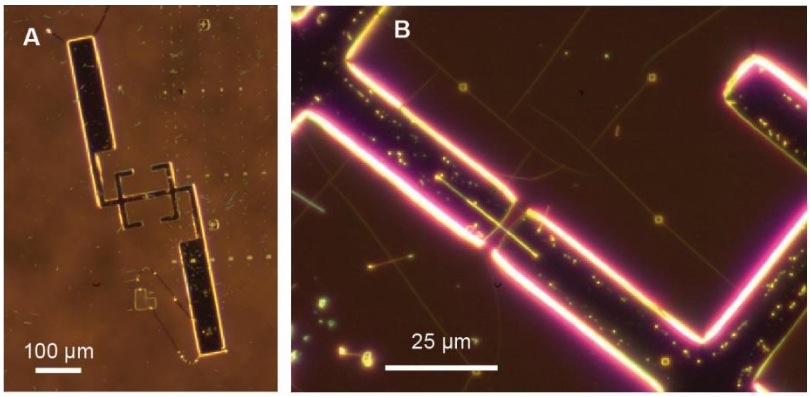

Figure 2.3: 600 GHz antenna. (**A**) Optical image of a THz metal meta-material antenna on quartz marker pattern. (**B**) Zoomed in optical image of the center of the antenna on the wire.

A Virginia diodes 580 GHz to 620 GHz Amplifier Multiplier Chain was used to supply the THz signal. The signal was directed using mirror optics to the sample as shown in the red dotted line in Fig. 2.4A. The signal was aligned with a HeNe laser on the sample (Fig. 2.4B). The sample was wire bonded using a West Bond model 7476D-79 with 1% Si/Al wire to a custom printed circuit board (PCB). The PCB connected to pin connectors that led to coaxial cable leading to a Bayonet Neill–Concelman (BNC) to triax converter that led to the SMU. This setup was used over probe tips due to geometric constraints in the measurement setup. The THz signal

and the HeNe laser were aligned using an infrared (IR) camera and a meta-material absorber array (Fig. 2.4C). The array absorbed the THz and generated heat that could be measured by the camera, then the HeNe laser was aligned to be on top of the THz beam. The polarization of the sample was aligned by eye as the antennas are quite large and can be seen by eye.

To conduct the measurement the THz beam was aligned to the sample and the SMU was set to the open-circuit condition to measure voltage from the DC output rectified voltage.

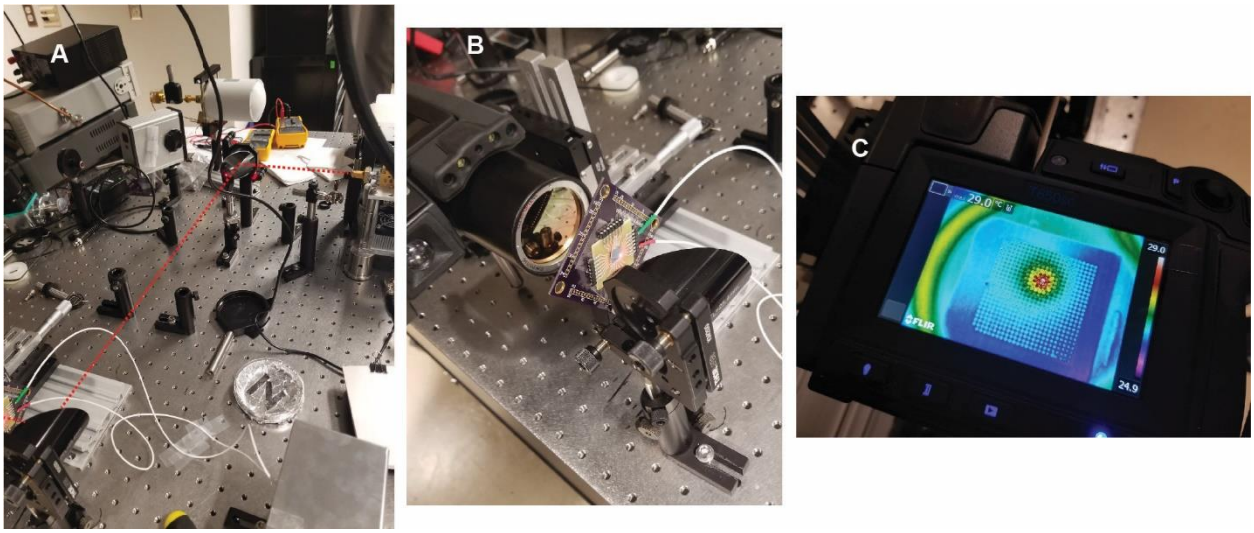

Figure 2.4: 600 GHz setup. (**A**) Measurement setup showing the THz beam path with a dotted red line. (**B**) Image of the sample which has been wire bonded to a PCB that is connected to external pin outputs that lead to the SMU. The alignment laser (red dot) can be seen on the sample. An IR camera can be seen behind the sample. (**C**) Display from an IR camera showing a meta-material array that selectively heats up when the THz beam is incident on it. The red dot is where the beam is most intense. Note these images were taken in the Padilla lab at Duke University.

2.6.2.6 CO_2 laser Measurements

These measurements were done in collaboration with Atkin group at UNC Chapel Hill. In an attempt to demonstrate rectification at 28 THz, an Access Lasers L3 CO_2 laser was used as a THz source. The signal ranged from 26 to 29 THz and had various modes where the peak power was around 200-250 mW with a spot size diameter of ~0.5 cm. The beam was aligned to a HeNe

laser and directed to the sample. The sample had antennas that may have been resonant to the signal (Fig. 2.5). Signatone micropositioners (S-725) and probe tips (SE-TL) were used to measure the signal contact to the device. The contacts went from Triax cables to the SMU which was in the open circuit condition to measure DC output voltage. Additionally, a chopper was used to chop the signal with a Zurich Instruments HF2LI lock-in amplifier to try to find small signals. Also it was attempted to measure current. None of the attempts resulted in any signal. However, upon further calculation it seems unlikely the diode would respond at such a high frequency. Additionally, if it were to respond, it would likely require the AC quartz substrate and to ensure that the antennas are actually resonant to the signal. Therefore, it could be worthwhile to repeat this measurement, but these needs to be significant optimization.

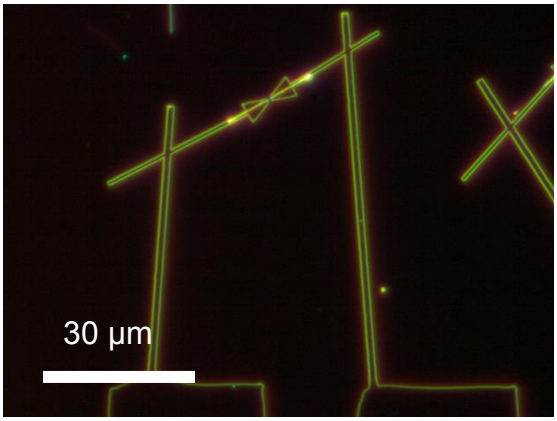

Figure 2.5: CO_2 measurement antennas. Optical image of one of the antennas used in the CO_2 measurement setup

2.7 Simulations

2.7.1 Finite Element Modeling (COMSOL)

COMSOL Multiphysics was used for finite-element modeling of the geometric diodes by representing the NW as a 2D simulation domain with cylindrical symmetry. The model includes drift, diffusion, depletion, accumulation, and recombination effects as described previously.[37]

The simulated geometry consisted of a NW 100 nm in diameter with two uniformly-doped *n*-type sections (5 x 10^{19} cm^{-3} donor density) each 380 nm in length adjacent to a geometric diode section 220 nm in length with a dopant profile described by a single exponential decay down to 1 x 10^{17} cm^{-3} donor density in accord with the experimentally measured EDS map. The geometric parameters of the diode section were D = 100 nm, d = 30 nm, L = 200 nm, $\theta = 10.1°$, and $\varphi = 53.2°$. The region around the constriction includes a fillet with radius of 5 nm to more accurately reflect the NW geometry.

2.7.2 Analytical Geometry Modeling

For qualitative comparison to experiment, an analytical model that calculates the theoretical DC current asymmetry of a geometric diode was developed. It considers all possible trajectories that a ballistic charge carrier may take such that it travels an axial distance equal to or less than the mean free path and passes through the NW constriction, undergoing zero, one, or multiple specular reflections at the NW surface depending on the trajectory. The model is built in python 3+. This model is discussed in depth in the simulation chapter.

2.7.3 Monte Carlo Modeling

For additional comparison to experiment, a Monte Carlo model was developed to simulate charge carrier flight through a Si NW. The model is built in python 3+, and partially follows a prescription from Lundstrom's *Fundamentals of Charge Transport*.[3] This model is discussed in depth in the simulation chapter.

CHAPTER 3: DESIGNING, GROWING, AND ETCHING SILICON NANOWIRE ELECTRON RATCHETS FOR USE AS GEOMETRIC DIODES[3]

3.1 Introduction

Semiconductor nanowires have been grown since the 1960s;[36] however, as discussed in chapter 1, controlling the shape of the nanowire beyond just the diameter of the NP and growth length has been sought after, but difficult to achieve. There have been examples,[50-56] (this is merely a sample of a few) but none have demonstrated unilateral control over the entire geometry of the NW with high precision. Prior work in the Cahoon lab created a process to chemically etch nanowires to achieve control over their geometry named "Encoded Nanowire Growth and Appearance through VLS and Etching" (ENGRAVE).[37,38] The ENGRAVE method finely controls the doping level of Si NWs using computer controlled pneumatics and mass flow controllers. With precisely controlled doping levels encoded, the wires are then etched in a dopant-selective etch to reveal a structure based on the encoded dopants. This process is perfectly suited for the creation of geometric diodes because it offers control over doping and the geometry down to sub 10 nm length scales.[57]

For geometric diodes it's necessary to have control of the geometry of a system to about the MFP of charge carriers in the system. The ideal geometric diode would have a long MFP with control over geometry down to the smallest resolution while maintaining high conductivity. Unfortunately, for doped semiconductor geometric diodes there is a tradeoff between doping

[3] Portions of this chapter are reprinted with permission from Custer, J. P.; Low, J. D.; Hill, D. J.; Teitsworth, T. S.; Christesen, J. D.; McKinney, C. J.; McBride, J. R.; Brooke, M. A.; Warren, S. C.; Cahoon, J. F. Ratcheting quasi-ballistic electrons in silicon geometric diodes at room temperature. *Science* **2020,** *368*, 177-180.

level, conductivity, and MFP. The higher the doping level the higher conductivity, but also higher doping levels lower the MFP, which then requires finer control of the geometry to match that decrease in MFP. Fortunately, the ENGRAVE process offers control over both the doping and geometry. The Si NWs can be degenerately doped for the majority of the structure so that Ohmic contacts can be created, but then the doping level can be dropped to both create the desired geometry and also lengthen the MFP.

3.2 Results and discussion

Within the constraints of a NW geometry, a geometric diode takes the form of a two terminal structure with an asymmetric funnel or 'sawtooth' structure as shown in Fig. 3.1A. In an ideal geometric diode, there is control over all of the geometric parameters shown in Fig. 3.1A: the outer wire diameter (*D*), constriction diameter (*d*), ratchet length (*L*), ratchet angle (θ), constriction length (*l*) and constriction angle (φ). To achieve this control a VLS growth mechanism coupled with ENGRAVE was used (see Methods section 2.1 and 2.2). In order to form the desired shape of the nanowires as shown in the SEM images in Fig. 3.1B, a dopant flow profile was determined (Fig. 3.1C).

3.2.1 N-type Nanowires

N-type wires were grown at 420 °C yielding a typical growth speed of ~200 nm/min depending on the doping level. A long (~>15 μm) degenerately doped section is grown with the PH_3 flow at 20 sccm, then an asymmetric doping profile like that of Fig. 3.1CII, then another degenerate section. Referring to Fig. 3.2 B-D, the doping level can be calculated. The measured chemical doping levels from the EDS spectra in Fig. 3.2 B-D are within a factor of 2-3 of the expected doping level encoded during VLS growth based on the gas-phase ratio of PH_3 to SiH_4. The absence of a P signal in Fig. 3.2D (with zero PH_3 flow) indicates that the P chemical doping

level is at least below ~10^{19} cm^{-3}, the approximate limit of detection for STEM EDS analysis. Moreover, considering that the active carrier concentration (*i.e.* the effective doping level) is ~4 times smaller than the chemical doping level (discussed in chapter 4), the active carrier concentration should be below ~2.5 x 10^{18} cm^{-3}. This result is consistent with prior studies by scattering scanning near-field optical microscopy on NWs grown under the same conditions, which suggest a doping level below ~10^{18} cm^{-3} for nominally intrinsic segments grown directly after degenerately doped *n*-type segments[58]. We emphasize that these are upper limits, and the actual doping level in the nominally intrinsic segments are likely to be below (potentially by orders of magnitude) these estimates.

Outside of the gradient doped section, the degenerate sections allow for Ohmic contact to the NW because the doping level is so high that the metal contacting the wire forms a depletion region that is so thin that the charges can just tunnel through it. To modulate diameter, the dopant precursor flow rate was rapidly varied during VLS growth to vary dopant concentration along the NW axis to yield abrupt and radially uniform profiles[38] as shown by scanning transmission electron microscopy elemental analysis for *n*-type NWs doped with phosphorus (Fig. 3.2). Wet-chemical etching of the NWs yielded a diameter profile that is dependent on the encoded dopant profile.[37,39] For example, Fig. 3.1B displays SEM images of two *n*-type NW segments that were etched under the same conditions but yielded different values of θ and *d* with the same *D* and *L*. The dopant and diameter profiles for the two segments (Fig. 3.1C) demonstrate that larger θ and lower *d* were synthetically encoded by using lower doping levels within the tapered region. The growth conditions are easily reproducible, but the current method for the wet etching process introduces a lot of variability in the NW geometric diode fabrication as shown in Fig. 3.3 where all the wires shown are from the same device, and are therefore from the same growth, on the

same substrate, and etched at the same time. Despite all of this, there is a high degree of variability in the final geometries. This issue may be fixed with more thorough Au etching and a flow system that would more uniformly replenish the etchant. This flow system would replace dipping the devices by hand in etching solutions with a flow pump system that could be controlled to refine more precise etch times with cleaner etch solutions.

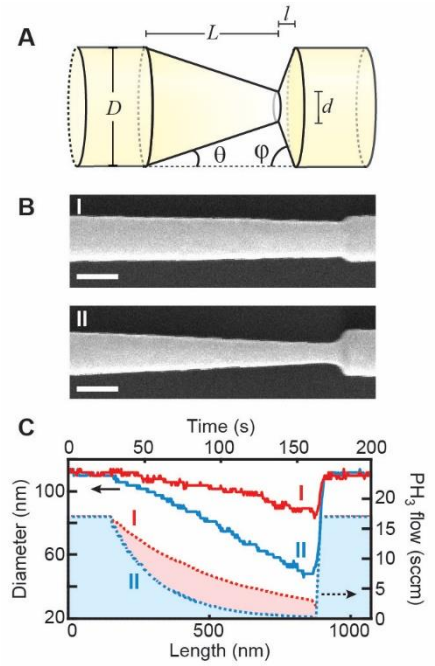

Figure 3.1: Designing Si NW ratchets. (**A**) Design and geometric parameters for a two-terminal NW geometric diode with 3D morphology. (**B**) SEM images of two NW geometric diodes; scale bars, 100 nm. (**C**) Diameter profiles (solid lines) and phosphine (PH_3) dopant precursor flow profiles (dashed lines) for the two geometric diodes, I (red) and II (blue), shown in panel C.

The outer diameter of the wire, *D*, is reasonably reliably controlled through the diameters of the Au NPs used for growth, however, there is some disparity in the sizes leading to a distribution of diameters within ~20 % of the stated diameter of the NPs with our current method. For our purposes we did not need perfectly uniform *D*'s, so no efforts were made to try to achieve that; however, it would be possible to do, for example, by fixing Au NPs in predefined

oxide wells. Additionally, the etching process can nominally etch the whole wire slightly (a few nms), even the degenerate sections, especially if there is a fully formed oxide which serves to reduce the diameter of the entire wire slightly, not just in the low doped regions.

Ratchet Length, *L*, is reliably controlled by the length of time over which the dopants were decreased in the growth. However, there are a few unreliable aspects of *L*. Sometimes the geometry appears to have an initial *L* with a certain θ, and then after a given length, the diameter would rapidly decrease giving a second θ (shown in Fig. 3.3A and E). Additionally, sometimes it appears that one side of the sawtooth will etch faster than the other (shown in Fig. 3.3C). The origin of these effects is still unknown, but it is likely due to different growth directions within a wire growth leading to faceted etching[59] or an effect from Au or other impurities on the surface of the wire or the substrate.

Typical values for *d* to start showing any diode behavior were ~50 nm, but to act as a good diodes, values closer to ~30 nm were necessary. Constriction diameter, *d*, had the most variability in the current etching process, but no serious effort has been made to try to generate more uniform etching. Wires that were from the same growth chip, on the same device wafer, and etched for the same time would yield drastically different *d*'s (Fig. 3.3). I think the likely culprit to the dramatic differences in etch depth, and in turn *d*, are from specific surface chemistries. There could be impurities in different concentrations on the wire surface or the device chip surface or even in the etchants that effect the mass transport of the etching process. It is well known that gold and other impurities affect chemical etching of Si.[47,60] In order to have finer control of the etching process, I recommend exploring the flow cell etching process mentioned earlier. This flow cell would reduce impurities by constantly supplying fresh etch solution flowing over the wires. A moonshot suggestion would be to try to find a dopant-

selective gas phase etchant. Although there are currently no specific examples to point to, that does not mean a dopant-selective gas phase etchant does not exist. The process could resemble something akin to a reactive ion etching (RIE) system, with etchants similar to XF_2 or HBr Plasma.[61-65]

For angles, the ratchet angle, θ, is limited to the same issues that are present in *d* and *L*. The only additional note about θ is that the region near the neck where the angle is defined is slightly filleted, so thinking about a straight edge angle is not quite the reality of the experimental system. The constriction angle φ is, however, limited from a more ideal value of 90° likely by the limited mass transfer ability in the wet-etch process, yielding typical values of 30° to 60°. Thus, through control of catalyst diameter, etch conditions, and doping level, the fabrication process yielded direct structural tunability over the geometric parameters.

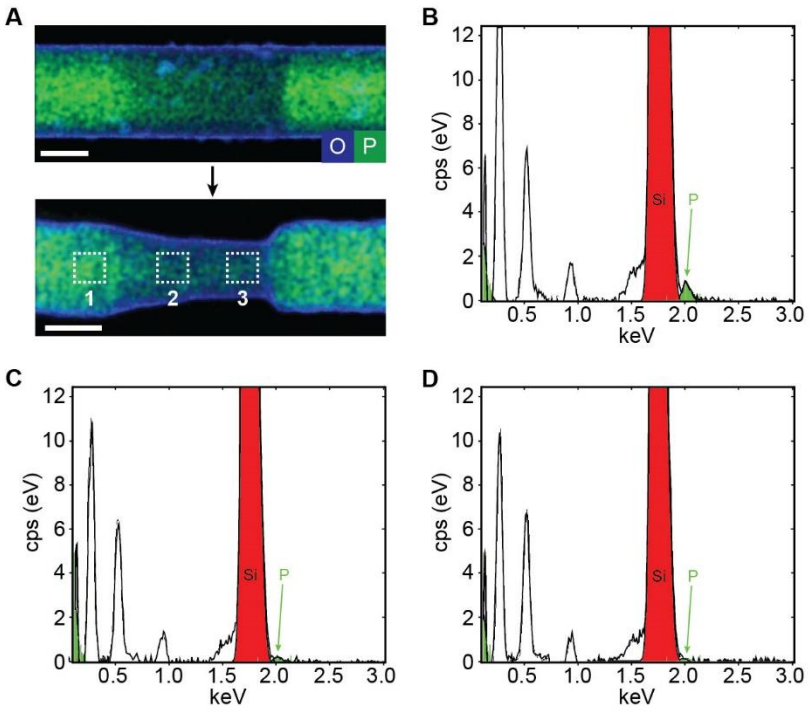

Figure 3.2: High-resolution scanning transmission electron microscopy (STEM) elemental analysis by energy dispersive x-ray spectroscopy (EDS). (**A**) STEM-EDS elemental maps of P (green) and O (blue) for Si NWs encoded with the dopant profiles for an encoded NW ratchet

before etching (upper) and after etching (lower); scale bars, 50 nm. Boxes in the lower panel denote regions, labeled 1-3, for EDS spectral analysis. Note that the NW imaged here contains a substantially shorter ratchet length than typically used in geometric diode devices to facilitate high resolution STEM imaging of the entire ratchet region. (**B**-**D**) EDS spectra of region 1 (panel B), region 2 (panel C), and region 3 (panel D), as denoted by the dashed boxes in the lower panel of panel A. Fits to the Si peaks are shown in red, and fits to the P peaks are shown in green. Quantification of the Si and P signals yields an apparent chemical doping level of ~1.6 x 10^{20} cm^{-3} in region 1, ~6.5 x 10^{19} cm^{-3} in region 2, and no discernable doping in region 3, as apparent from the lack of a peak associated with P in the spectrum in panel D.

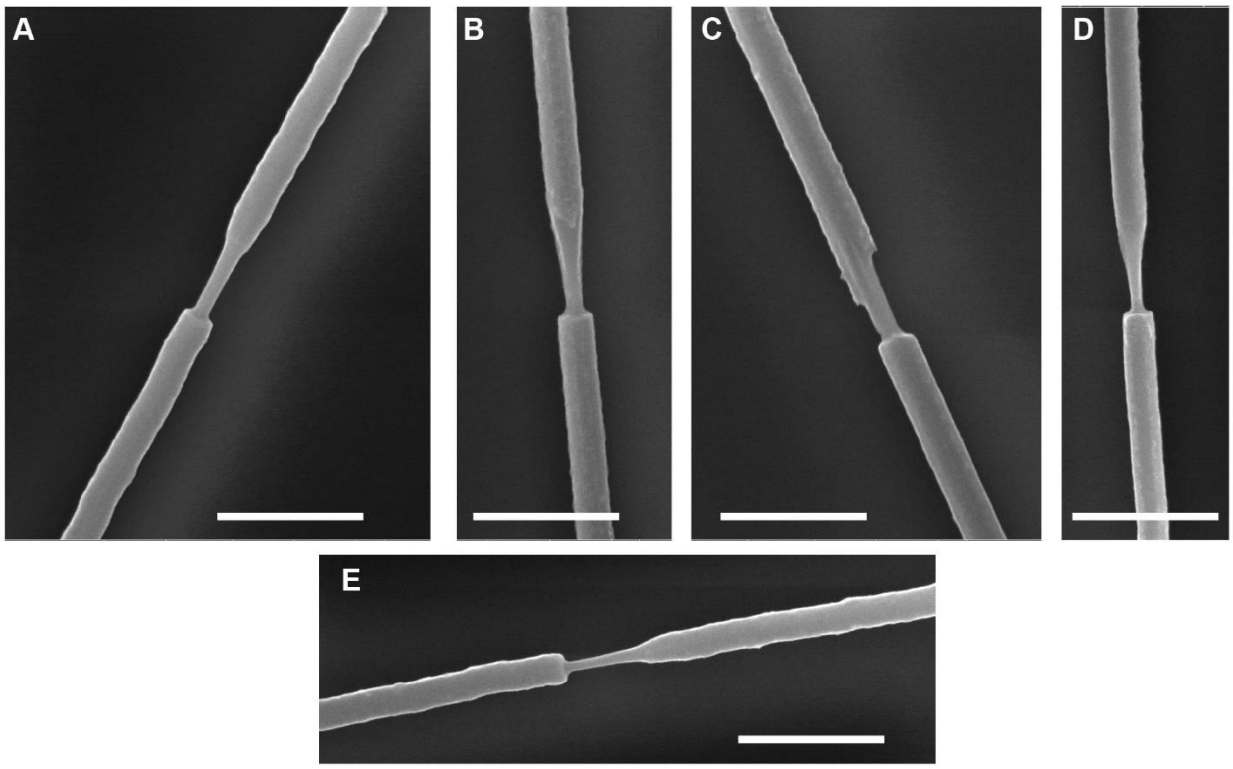

Figure 3.3: SEM images of wires from one device. (**A**-**E**) SEM images of wires all from the same device that used the same growth, device substrate, and were etched at the same time. All scale bars are 500 nm.

N-type wires were also grown at 510 °C, and despite looking physically like good geometric diode candidates (Fig. 3.4), they did not show any significant diode behavior. The major differences in the 510 °C growths were that the sawtooth sections were longer due to the faster growth rate (~300 nm/min), the PH_3 flow only went to zero for 3 seconds as opposed to 15

seconds, and the overall doping level is higher due to the higher temperature. Further investigation needs to be done into why the 510 °C growths did not show diode behavior because only 3 device substrates (~8 wires / substrate) were ever made, but it is likely the case that the doping level was too high at the constriction which caused the MFP to be too low to see ballistic effects.

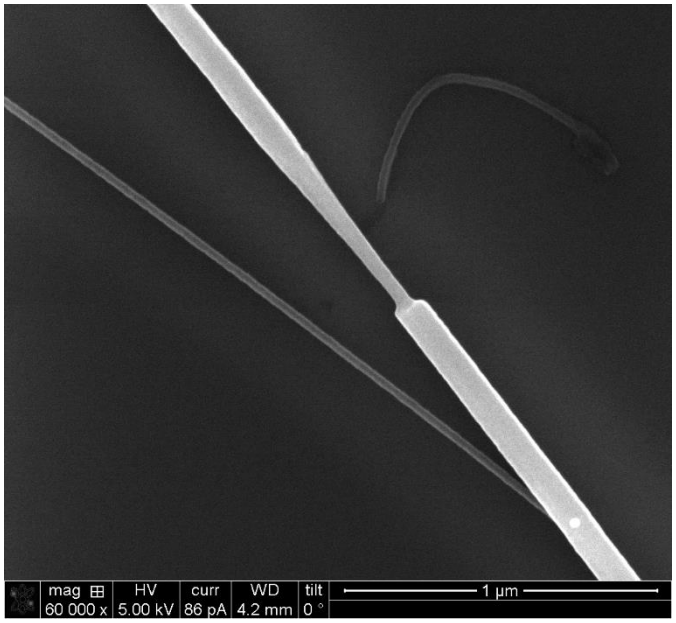

Figure 3.4: SEM image *n*-type wire grown at 510 °C. SEM image of an *n*-type wire grown at 510 °C after being etched on a device substrate.

The geometry and dopant profile created by the ENGRAVE process is beneficial because it creates a unique situation that likely facilitates the creation of a ballistic / quasi-ballistic region. When looking at the dopant profile shown in the EDS maps in Fig. 3.2, the profile shows a continuum of dopants that decreases from degenerate doping to nominally low doping as the sawtooth narrows. At some point there is a transition from degenerate doping to non-degenerate doping and at this location it's reasonable to approximate the degenerate sections as metallic segments contacting a quasi-ballisitic semiconducting region. These degenerate, metallic-like sections (with low MFP, but high Fermi energy) can inject carriers into the quasi-ballistic, lower doped (higher MFP) region from either side. This will be discussed in more detail in chapter 6.

All ratchet geometries described herein that showed diode behavior used dopant profiles that produced nominally intrinsic Si at the constriction and had features on a scale comparable to the electron MFP in Si at room temperature, which we estimate to be ~10 to ~30 nm or more. Here we show the calculation of MFP.

3.2.2 Mean Free Path

The mean free path, λ, will have a dependence on the electron scattering rates within the semiconductor, which depend on temperature and defect density. Here, we use the empirically derived relationship between electrical mobility, μ_e, and donor dopant density, N_D, of *n*-type Si at room temperature (T = 300 K) to determine the effect of dopant concentration on λ within the ratchet portion of the *n*-type NWs. The following calculations will rely heavily on section 1.1.1 (MFP).

Conservatively estimating N_D to range from 10^{17} to 10^{18} cm^{-3} (see Fig. 3.2), the effective N_D reflective of the active carrier concentration within the smallest diameter segments of the ratchet, we can use eq. 1.1 to estimate an electrical mobility μ_e of 801 to 263 $cm^2V^{-1}s^{-1}$, respectively, which, using eq 1.2 and $0.26m_e$, corresponds to a momentum relaxation time τ_m of 118 to 39 fs, respectively, and, using eq. 1.4, a diffusion constant D_e of 20.7 to 6.8 cm^2/s, respectively. The value of v_{th} is calculated using eq. 1.5 for T = 300 K and $m^* = 0.260m_e$, we get $v_{th} = 2.29 \times 10^7$ cm/s and a corresponding λ = 8.9-27.1 nm using τ_m = 39-118 fs.

Equivalently, the mean free path can be calculated using eq. 1.7 where v_R is the Richardson velocity, or the unidirectional thermal velocity with which charge carriers would approach the ratchet geometry from the degenerately doped *n*-type segment.[3] The value of v_R can be calculated using eq 1.6 giving a value of $v_R = 5.28 \times 10^6$ cm/s using T = 300 K and $m^* = 0.260m_e$. From eq. 1.7, we get λ = 8.9-27.1 nm using τ_m = 39-118 fs, the same as determined

from the thermal velocity, as expected.

As discussed in section 1.1.1, an alternate method to deduce λ is to use the 0 K Fermi velocity, v_F, to estimate λ as $\lambda = v_F\tau_m$. In the quasi-ballistic NW geometric diode, the degenerately doped *n*-type segments with a carrier density $n = 4 \times 10^{19}$ cm^{-3} (see Fig. 3.2 and Chapter 4) serve as the electron reservoir that injects electrons into the quasi-ballistic region of the nanostructure at a velocity determined by eqs. 1.8. Using the weighted average of the transverse and longitudinal electrons, we get $v_F = 2.20 \times 10^7$ cm/s. Using τ_m = 39-118 fs, we then estimate the mean free path as λ = 8.5-26 nm, which is in good agreement with the values calculated by the thermal velocities. We also note that the Fermi velocity can be estimated in the case of a one-dimensional (1D) material. However, even if the ratchet geometry were to show evidence of 1D behavior, we believe the more accurate velocity would be the Fermi velocity of the 3D (100 nm diameter or larger) degenerate *n*-type segments that serve as the electron reservoirs for injection of electrons into the quasi-ballistic ratchet geometry. We also acknowledge that the calculated v_F is slightly greater than the saturation drift velocity, v_d, as discussed in section 1.1.1. However, considering the degenerate doping levels of the *n*-type segments, abrupt change in dopant profile, short length scales, and large potential drop over the ratchet segment, the NW geometric diode is very likely to exhibit velocity overshoot, allowing electrons to travel at velocities up to several times the saturation drift velocity.[21]

Given the above considerations on the mean free path λ at room temperature (T = 300 K), we cite an expected value of ~10-30 nm by taking the approximate lower and upper estimates of the values. We emphasize that this is a conservative estimate and that doping levels below 10^{17} cm^{-3} would result in even large values of the mean free path. For example, a doping level of 10^{16} cm^{-3} would result in a τ_m of 184 fs and a λ of ~40 nm. Moreover, the exact value of mean free

path is a distribution and not a hard cut-off for the observation of ballistic effects; indeed, quasi-ballistic behavior can occur on length scales longer than the formal mean free path.[66,67]

3.2.3 P-type Wires

P-type Si NWs were also grown and shaped into geometric diodes. P-type is only grown at 510 °C because the higher temperature is needed for the Boron dopant incorporation.[40,49] A big difference for the p-type wires is that the doping level is much lower than the n-type wires.[40,58] The lowest encoded gas phase doping level is ~1.5 x 10^{19} cm^{-3}; however, it has been shown that the active doping level is roughly two orders of magnitude lower than the encoded doping for *p*-type NWs. The p-type wires used to create a device had a flow of 0.35 sccm B_2H_6 which correlated to a doping level at the constriction of ~1 x 10^{17} cm^{-3}.[40] However, device performance should improve if the doping level is dropped down to 0 sccm. The MFP for holes can be calculated in the same method as in section 1.1.1, but hole mobility must be used and hole effective mass must be used. Typical hole mobilities are ~3x smaller than electron mobilities, and MFP would follow closely with that approximation.[21]

P-type NWs have not been as extensively studied, and therefore there is not much data on various geometries. However, it seems that all of the same discussion of the geometric parameters and their reproducibility also affect the *p*-type NWs.

3.2.4 Encoding Diodes in Series

In addition, the bottom-up process allowed multiple geometric diodes to be encoded in series within a single NW. The sawtooth sections can be encoded right next to each other as shown in Fig. 3.5, or a space of degenerate section can be placed between them. The difference between the two placements will be discussed in chapter 4.

Figure 3.5: Sawtooth sections in series. SEM image of a NW with three geometric diodes encoded in series; scale bar, 200 nm.

3.3 Conclusion

In conclusion, bottom-up VLS NW growth coupled with the ENGRAVE process is an excellent platform to control both the doping level and geometry of a structure with sub 10 nm resolution. This control can be used to create highly-tunable sawtooth shapes on the order of the MFP of charge carriers that will be tested as geometric diodes. The growth process is reasonably reliable as long as the growth substrate is clean; however, the wet chemical etch process in its current state introduces a lot of variability in the tuning of the geometry. Therefore, my recommendation is to explore using a flow-cell architecture for etching. In this set-up the etchant would flow over the NWs, continuously providing fresh solution, which should reduce impurities and increase reproducibility. A moonshot suggestion would be to attempt to find an in-situ, gas phase, dopant selective etching process in the CVD.[61-65] The benefits of either a flow-cell or potentially a gas-phase etchant would be increased reproducibility and precision.

I also recommend exploring bringing the dopant flow profile all the way to 0 for the *p*-type wires. This should serve to increase the MFP of the charges and increase the geometric diode performance (discussed in the next chapter).

CHAPTER 4: MEASURING NANOWIRE GEOMETRIC DIODES WITH DIRECT CURRENT[4]

4.1 Introduction

Chapter 3 demonstrated how the ENGRAVE process can create tunable NW geometries that could be ideal for geometric diodes. To test the performance of the geometric diodes as diodes, they need to be measured under DC and compared to typical diodes. Conventional electrical diodes—which include two-terminal semiconductor *p*-*n* junctions and metal-semiconductor Schottky barriers—control the flow of electrons. However, they operate through a fundamentally different set of mechanisms, relying on capacitive depletion regions, band bending, and band offsets for their function. In a Schottky diode (Fig. 1B), electrical current flows in the forward direction through thermionic emission of electrons over a voltage-dependent potential barrier, and current is blocked in the reverse direction by the Schottky barrier.[21] Typical diodes can achieve DC asymmetries, calculated as the magnitude of the ratio of forward-bias current, $I(+|V_{app}|)$, to reverse-bias current, $I(-|V_{app}|)$, at a given applied voltage (V_{app}), $> 10^6$ at 1 V. Geometric diodes are an alternative paradigm that take advantage of non-centrosymmetric structures to induce current flow preferentially in one direction.[11,68,69] A geometric diode (Fig. 1.6) can be created by using a sawtooth geometry in which electrons undergo quasi-specular reflection at the boundaries of the structure, directing electrons through a constriction in the forward direction. In the reverse direction, electrons are reflected backward, blocking current. To

[4] Portions of this chapter are reprinted with permission from Custer, J. P.; Low, J. D.; Hill, D. J.; Teitsworth, T. S.; Christesen, J. D.; McKinney, C. J.; McBride, J. R.; Brooke, M. A.; Warren, S. C.; Cahoon, J. F. Ratcheting quasi-ballistic electrons in silicon geometric diodes at room temperature. *Science* **2020,** *368*, 177-180.

function, the physical dimensions of a geometric diode must be comparable to the mean free path (MFP) of the majority carrier, allowing the devices to operate in the ballistic or quasi-ballistic regime, in which surface reflections dominate over other charge-carrier scattering mechanisms.[69]

Four-terminal ballistic rectifiers operating at cryogenic temperatures[22] and room temperature[24] and quantum ratchets operating at cryogenic temperatures[9] have been reported with two-dimensional electron gases. Rectifying devices have also been fabricated with graphene,[12,32] but two-terminal geometric diodes with large DC asymmetry (>5) at room-temperature have yet to be realized. Now let's examine the performance of the NW geometric diodes compared to typical diodes and compared to previous geometric diodes.

4.2 Results and Discussion

To probe the geometric diode behavior, *n*-type single-NW devices were fabricated (see Methods section 2.5) as shown by the representative SEM images in Fig. 4.1. The NWs had two degenerately doped sections with the sawtooth geometry between (see methods section 2.1.3 and Fig. 4.1). Four electrical contacts were defined per NW to ensure Ohmic contacts (Fig. 4.2). A voltage was applied across the degenerate sections to ensure there was no diode behavior (Fig. 4.2C and D). Except where noted, measurements were performed under vacuum directly after fabrication (see Methods section 2.6). DC current-voltage (*I*-*V*) curves were collected using the polarity indicated in Fig. 4.1.

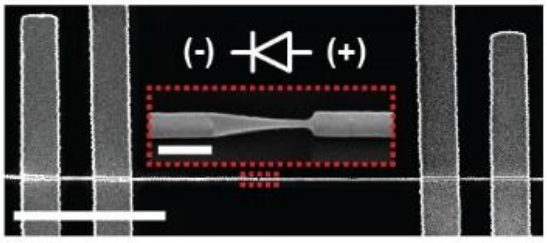

Figure 4.1: SEM image of NW device. SEM image of a single-NW device with two Ti/Pd electrical contacts on either side of the geometric diode; scale bar, 5 μm. Inset: higher

magnification SEM image of the red boxed region and circuit-diagram representation of the geometric diode, showing the anode (+) and cathode (-); scale bar, 250 nm.

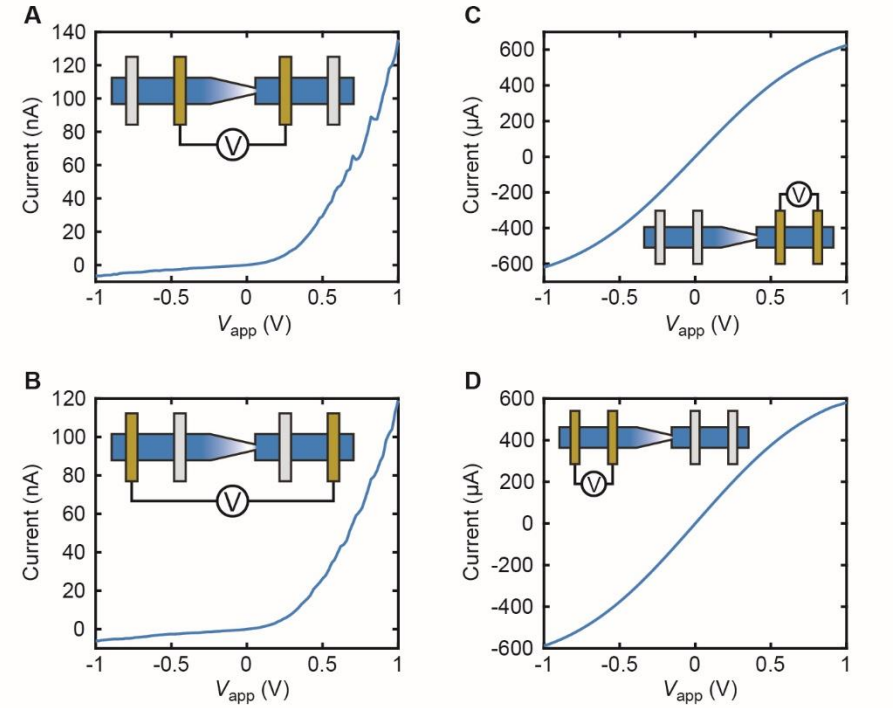

Figure 4.2: Single-NW electrical measurements. (**A**, **B**) *I*-*V* curves for a NW geometric diode with four electrical contacts as measured through the two inner contacts (panel A) and two outer contacts (panel B). The curves show the same diode behavior, indicating that the electrical contacts do not influence the observed characteristics. This check was performed for all NW geometric diode device data reported. Insets: schematic diagram of the NW, electrical contacts, and measurement geometry. (**C**, **D**) *I*-*V* curves for the degenerately doped *n*-type sections measured through the right two (panel C) and left two (panel D) electrical contacts. The data confirms that the contacts are Ohmic with linear *I*-*V* behavior for current magnitudes less than ~200 μA. Note that the curvature at higher currents results from current saturation effects due to the small size of the NW and is not an indication of Schottky diode behavior. Linear fits of the linear regions combined with measurement of the exact NW diameter and channel lengths by SEM yield a resistivity of ~1.8 x 10^{-3} Ω·cm, which correlates to an active doping level of ~4 x 10^{19} cm^{-3} using the known resistivity of bulk P-doped Si.[70] The active doping level is within a factor of 4 of the chemical doping level measured by EDS (see Fig. 3.2) and agrees with previous measurements.[38] Insets: schematic diagram of the NW, electrical contacts, and measurement geometry.

4.2.1 Geometric Parameters

When voltage was applied across the etched geometric diode region, the current measured showed distinct diode behavior dependent on the geometry of the NW etch. To frame

the comparisons of asymmetry to geometry, we'll start with a simplified and condensed version of all of the data. Room-temperature results for four NWs with θ (defined in chapter 3) ranging from 0 to 13° are shown in Fig. 4.3. The NW with θ = 0°, corresponding to an unetched wire, showed a linear *I*-*V* response despite the asymmetry in the doping profile that creates the funnel shape when etched. NWs with θ > 0° show increasingly nonlinear and diode-like *I*-*V* responses. The DC asymmetry of the devices progressively increases from unity to > 10 for $|V_{app}| = 1$ V (inset of Fig. 4.1). Results for > 100 measured devices showed that the DC asymmetry exhibited the polarity indicated in the diode schematic in Fig. 4.1 with 100% yield.

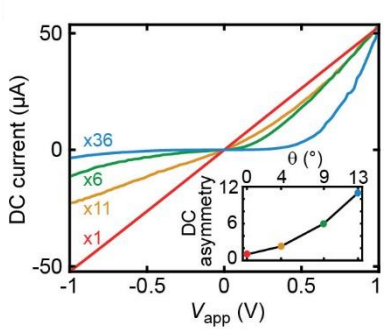

Figure 4.3: Diode behavior vs angle. (**A**) *I*-*V* curves measured from four separate single-NW devices with θ of 0° (red), 4° (orange), 9° (green), and 13° (blue). Current values for each device are scaled by the factors indicated. Inset: DC asymmetry at $|V_{app}| = 1$ V as a function of θ.

Diving deeper into each geometric parameter individually, we can look at Fig. 4.4. In all of the plots the y-axis is DC asymmetry and the x-axes are the various geometric parameters defined in Fig. 3.1A. As *d* goes down, generally higher asymmetries can be achieved, but a small *d* does not necessarily mean that asymmetry will be high. There seems to be no clear trend in *L*. The dependence on θ is about the same correlation as *d*, where generally the larger the θ the higher the asymmetry, but a high θ does not guarantee a high asymmetry. Perhaps the strongest trend is seen in φ, where it appears that having a shallow φ strongly prohibits the ability to have a large asymmetry. *D* is similar to *L* in that there is no clear trend. To fully appreciate the effects of

geometry on asymmetry and diode performance we have to consider multiple geometric parameters at once because they all relate to and affect each other.

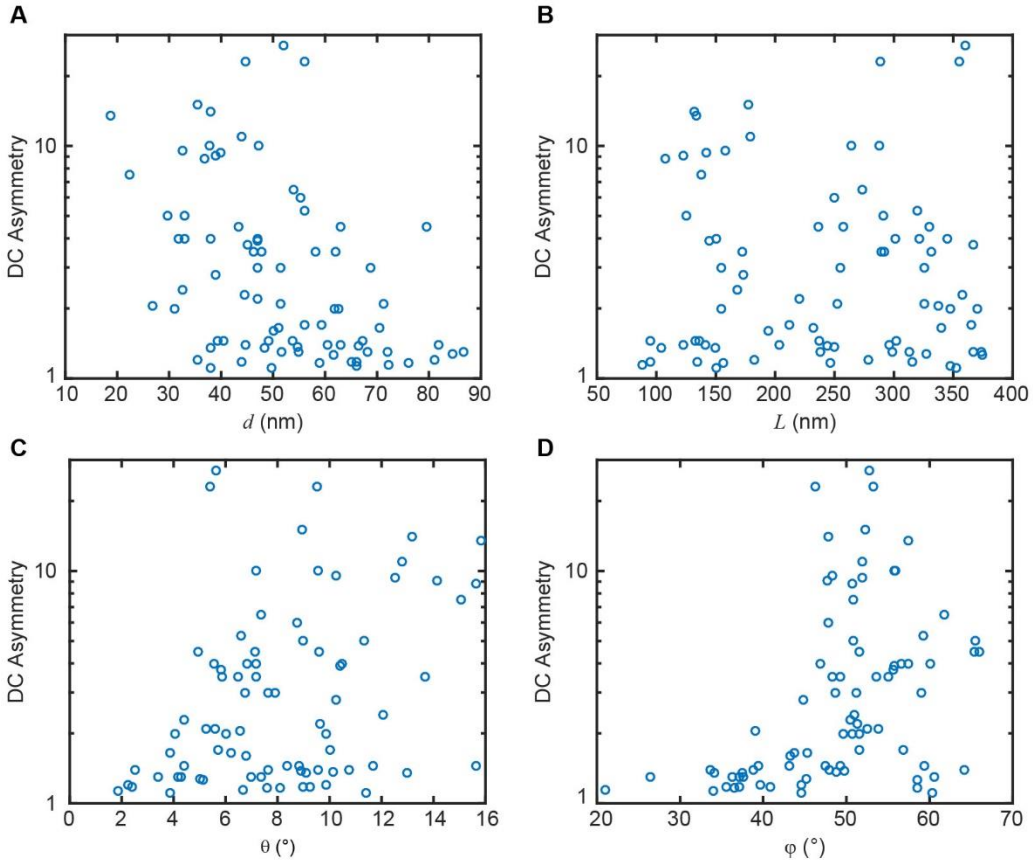

Figure 4.4: DC asymmetry vs geometric parameters. (**A**) DC asymmetry vs neck diameter, *d*. (**B**) DC asymmetry vs ratchet length, *L*. (**C**) DC asymmetry vs ratchet angle, θ. (**D**) DC asymmetry vs constriction angle, φ.

Figure 4.5 displays experimental results correlating measured geometric structures with the *I-V* behavior. Champion devices for each value of *f*-number (*N*) - with $N = f/D$, where *f* is the effective focal length of the ratchet (Fig. 4.5A) and $N = (2\tan(\theta))^{-1}$ - exhibited a trend of increasing DC asymmetry with decreasing *N*. As expected, there was no correlation between *N* and φ; however, lower values of φ precluded a high DC asymmetry. Images of three select devices (labeled 1 to 3), each with a DC asymmetry > 10 (inset of Fig. 4.5B) show the various geometries that produced high asymmetry values.

Experimentally there seems to be a variety of geometries that product high asymmetries.

This is likely because of the relatively low sample size of the data (compared to a simulation that could simulate millions of geometries) and because the surface plays a significant role in producing quality diodes. All of the data discussed thus far have been wires with nominally no surface coating, but certainly slightly different amounts of oxide are present from air exposure despite the efforts to measure the wires directly after fabrication and in a vacuum chamber. Additionally, and probably most likely the cause of the large discrepancies, is surface charge defects and mobile impurities. The etch process is known to cause defects and likely leaves impurity charges, such as potassium, that induce different surface charge effects that affect the diode performance.[21,47,49,71] This effect needs to be studied more deeply, but I will discuss some preliminary data.

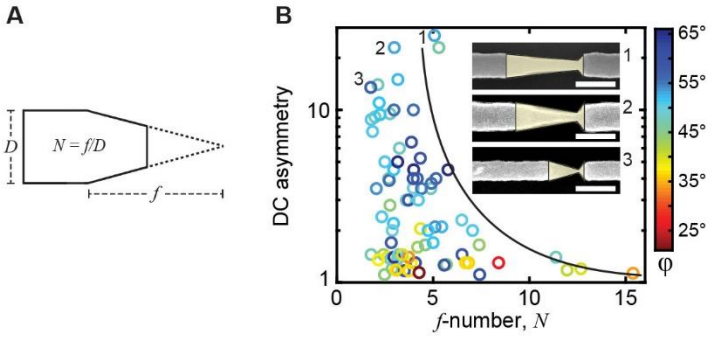

Figure 4.5: DC asymmetry vs *f*-number. (**A**) The geometric parameters *f* and *D* that define *N* are shown. (**B**) Experimental values of DC asymmetry at $|V_{app}|$ = 1 V collected from 81 single-NW devices plotted as a function of *N*. Data points are color-coded according to the constriction angle φ. The black line is a guide to the eye. Inset: SEM images of three high asymmetry devices, labeled 1-3, overlaid with a diagram of their geometry; scale bars, 200 nm.

4.2.2 Surface Coatings

Devices with prolonged air exposure, for which native oxide has formed on the surface (Fig. 4.6), show significantly higher asymmetries than devices with no surface oxide. Fig. 4.6A shows *I*-*V* curves over time for a diode that was left out in air (in the dark). The longer the diode is exposed to air, the higher the asymmetry. Note that both the reverse and forward bias currents go down with time, but the reverse bias current goes down much more than the forward, leading

to the higher asymmetry (Fig. 4.6B). This indicates that the probability for a carrier to transmit in the forward is lowered by oxide formation, but not nearly as much as the probability is lowered for carriers in the reverse direction. Given the right conditions and wire, asymmetry can reach values > 10^3, as shown by the *I-V* curve and DC asymmetry data in Fig. 4.6C. The champion room-temperature DC asymmetry (Fig. 4.6C), achieved with a stable surface oxide on *n*-type NWs after extended exposure to ambient conditions, yielded a value of ~1600 at $|V_{app}| = 1$ V with $\varphi = 46°$ and $N = 5.4$. The higher asymmetry with surface oxide can be attributed to a smaller effective constriction and band bending that screened surface defects and improved specular reflection. Note there is voltage dependence to the asymmetry as shown in the inset of Fig. 4.6C. This voltage dependence is likely caused by charge carrier drift becoming more aligned down the axis of the wire. The saturation shown in the forward bias of Fig 4.6C is then likely caused by carriers reaching some form of saturation drift velocity as discussed in chapter 1.

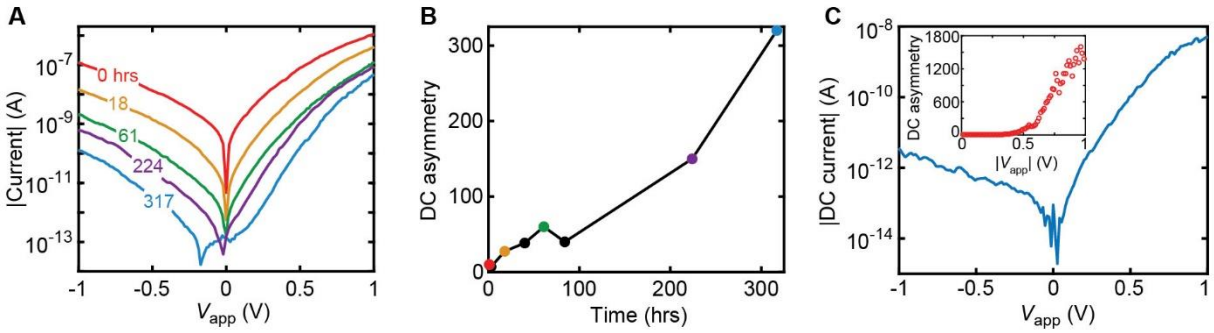

Figure 4.6: Geometric diodes with surface oxide. (**A**) Semi-log *I-V* curves for a single-NW device measured as a function of time after device fabrication, including 0 hours (red), 18 hours (orange), 61 hours (green), 224 hours (purple), and 317 hours (blue). The time-dependent behavior is attributed to the growth of native oxide on the NW surface. We attribute the changes to a reduction in the effective constriction diameter and to passivation of the NW surface, improving the specular reflection of quasi-ballistic electrons. (**B**) DC asymmetry as a function of time at $|V_{app}| = 1$ V as derived from the data in panel A. (**C**) Semi-logarithmic *I-V* curve for a device with stable native oxide. Inset: DC asymmetry as a function of $|V_{app}|$.

In addition to native oxide formation on the wire surface, alumina was coated onto the wires using ALD (see Methods section 2.3.1) and a thermal oxide was formed on the surface followed by a hydrogen anneal using an RTA (see Methods section 2.3.2). Generally, the alternate surface coatings produced similar results to that of the fully formed native oxide. Based on ~10 single-NW devices, both the hydrogen anneal and oxide treatment, which has shown to decrease surface recombination and defects[49] (Fig. 4.7A), and alumina coating (Fig. 4.7B) showed similar results. The main difference between the oxide and the alumina is that the alumina is additive to the surface, and the oxide eats into the Si. It seems that all surface coatings decreased the magnitude of the current to some extent (anywhere from almost none, to several orders of magnitude). However, oxide does seem to lower it more than alumina (likely due to the additive vs subtractive nature of the coating). This is difficult to measure directly however, because the wires are not measured pre- and post-surface modification. The lower current is likely due to the charge double layer pinching off the neck a bit. With the oxide, if too much oxide is grown, the wire will pinch completely off and no current will flow. Surface modification does definitely serve to increase the asymmetry of the wires. The higher asymmetry with surface modification, as discussed before, can be attributed to a smaller effective constriction and band bending that screened surface defects and improved specular reflection.

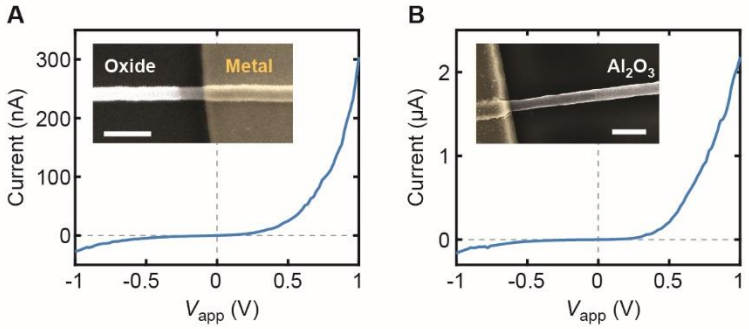

Figure 4.7: NW geometric diode devices with hydrogen-annealed thermal oxide and alumina surface treatments. (**A**) *I-V* curve for a NW geometric diode treated with a thermal oxidation at 900 °C and hydrogen anneal (see materials and methods for conditions). Inset: SEM image of an oxidized NW on the left and a metal contact on the right. The contrast on the NW results from

the removal of the oxide with BHF in the vicinity of the metal contact (false colored yellow) prior to metal deposition, revealing the bare NW surface (grey) and thermally-oxidized surface (white). (**B**) *I-V* curve for a NW geometric diode treated with an alumina Al_2O_3 coating of 10 nm deposited by atomic layer deposition directly following NW etching to define the geometric diode. Inset: SEM image of an alumina-coated NW on the right and the metal contact on the left. The contrast on the NW results from the removal of the alumina with BHF in the vicinity of the metal contact (false colored yellow) prior to metal deposition, revealing the bare NW surface (dark grey) and alumina-coated surface (light grey). Neither the thermal oxide treatment nor the alumina treatment show demonstrably different results compared to NWs with a fully formed native oxide. This result indicates that surface passivation is important but also that the diode performance is not strongly dictated by the exact nature of the passivation treatment.

It is curious that both the alumina and silicon oxide have similar effects on wire performance because they have opposite charge densities. Silicon oxide has a positive charge, inducing a negative charge density in the Si and alumina has a negative charge, inducing a positive charge density in the Si. This could indicate that the more important aspect of surface modification is passivating and screening surface defects rather than providing a certain charge density.[21,47,72] Initial results do suggest that alumina does decrease current, but typically less than one of magnitude total. More high current, high asymmetry devices have been created by coating with alumina. However, the surface treatments could also be trapping impurities at the surface that would have a huge impact on device performance. This is evidenced by the fact that wire performance still changes over time despite surface coatings. For the case of the alumina, this could also be oxide formation under the alumina surface by oxygen penetrating through the thin alumina. Lastly, wires that have a surface coating can show open behavior at low voltages (<1 V), but when taken to higher voltages (>2 V) show extremely high asymmetries. Values greater than 10^4 have been measured, but this effect is not well understood. It could be that the charge double layer is preventing charges from flowing at all, but then at high voltages it can be overcome and then propel charges through. More work certainly needs to be done to fully understand the impact of the surface and its modification to wire performance.

4.2.3 Temperature Modification

Because MFP substantially increases at lower temperatures,[21,73] we measured temperature-dependent *I-V* characteristics between 350 and 77 K (Fig. 4.8). As temperature decreased, the DC asymmetry increased from 3.5 at 350 K to ~500 at 77 K, which is consistent with an increase in MFP. Figure 4.8A shows *I-V* curves for the same wire measured at various temperatures. Note that similarly to the oxide formation, both the reverse bias and the forward bias current go down, but the reverse bias current goes down significantly more than the forward bias current. This leads to an exponential increase in asymmetry (Fig. 4.8B). This means that as temperature is lowered and MFP is increased, the transmission probability of carriers going through the funnel backwards is more negatively affected than the transmission probability of the carriers going in the forward direction. This effect will be revisited by simulations in chapter 6.

As shown in the data at 77 K, the diode current can go below the noise level of the SMU at low voltages and temperatures. This is even more pronounced in other temperature data that is not shown. The effect of the diode current going so low in both directions is not fully understood.

MFP can be calculated for the charge carriers around the neck in many different ways, and also using different doping levels depending on where exactly the doping level lies (see Chapter 3). Four different methods are shown in Fig. 4.8C and D. The trends in MFP (especially in Fig. 4.8D) nominally match the trends in asymmetry shown in Fig. 4.8B. This provides qualitative evidence that the MFP has a strong effect on diode performance; however, we are not sure what the exact relationship between asymmetry and MFP should be, but this will be discussed in simulations in Chapter 6.

Lastly, note that wires that had the encoded doping levels used to create the geometric diodes, but that were unetched, were also measured at 77 K. Unetched wires showed no diode performance at low temperature that might have arisen just from the doping profile (Fig. 4.8E).

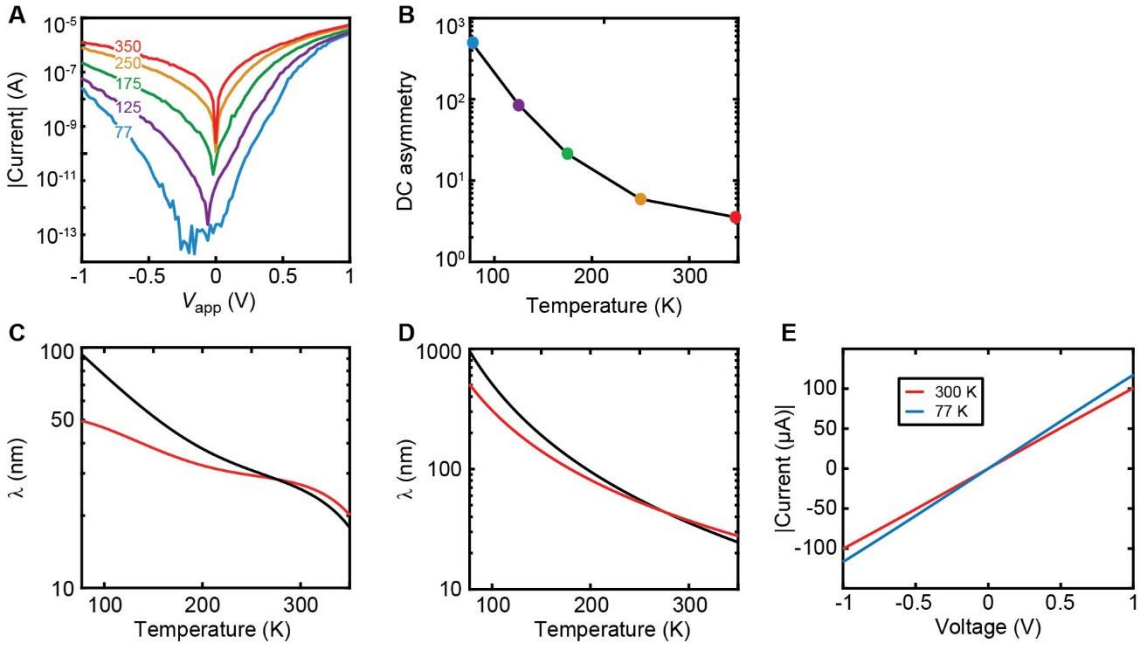

Figure 4.8: Temperature dependent geometric diode behavior. (**A**) Semi-log *I-V* curves of a single-NW device measured at temperatures of 77 K (blue), 125 K (purple), 175 K (green), 250 K (orange), and 350 K (red). Note that the wire has a stable native oxide. Decreasing the temperature increases the mean free path (λ) of the electrons and thus increases the impact of the asymmetric geometry on the *I-V* behavior. (**B**) DC asymmetry as a function of temperature at $|V_{app}| = 0.5$ V. The colored data points correspond to the *I-V* curves in panel A. Note that a lower V_{app} was used to preclude local Ohmic heating of the NW that could cause deviation of the local temperature from the measured temperature. (**C**) Semi-log plot of mean free path, λ, as a function of temperature for a doping level of ~10^{17} cm^{-3}. The red curve was created by using the empirically-derived electrical mobility from fitting sample 139 (*n*-type Si at dopant concentration of 1.3 x 10^{17} cm^{-3}) from reference [74]. The mobility was converted to τ_m (eq 1.2), which was multiplied by thermal velocity, v_{th} (eq 1.5), to arrive at λ. The black curve was created using the same method except that instead of v_{th}, the Fermi velocity, v_F, was used. (**D**) Semi-log plot of mean free path, λ, as a function of temperature for a doping level of ~10^{16} cm^{-3}. The red curve was created by using an electrical mobility determined from eq. 1.1 at an *n*-type doping level of 10^{16} cm^{-3}, and then multiplying it by 1.43 x 10^9 x $T^{-2.42}$ to account for the temperature dependence,[2] which trends as $T^{-2.4}$.[2,74] The 1.43 x 10^9 value is a fitting parameter from table 2 in reference [2]. The mobility was converted to τ_m, which was multiplied by v_{th} to arrive at a λ. The black curve was created using the same method except that instead of v_{th}, v_F was used. The trend in experimentally measured DC asymmetry with temperature in panel B follows the same trend as λ with temperature as seen in panels C and D, suggesting that λ is a key parameter in determining the performance of the geometric diodes. (**E**) *I-V* measurement of an unetched wire measured at 300K and 77K.

4.2.4 P-type Wires

P-type NW devices were fabricated and exhibited a reversal of diode polarity, as expected because the majority carriers changed from electrons to holes (Fig. 4.9). Figure 4.9A shows the direction of the applied voltage for the measurements in Fig. 4.9B and C. With that direction of applied voltage in mind, for n-type devices the electrons flow left to right when a positive voltage is applied (Fig. 4.9B). This means it's easier for current to flow (despite being backwards from electron flow). When a negative voltage is applied, the electrons are blocked, and it is harder for current to flow.

Now for *p*-type devices everything is flipped, and rightfully so because now the majority carrier is holes, not electrons. When a positive voltage is applied, the holes try to move right to left, and they are mostly blocked leading to lower overall current (Fig. 4.9C). When a negative voltage is applied, the holes move from left to right and higher current is achieved. This offers a fair amount of confirmation in the proposed mechanism of geometric diode quasi-ballistic transport because it shows that the majority carrier dictates the direction of the transport.

There is limited data (~8 single NW devices) on *p*-type devices, but curiously they seemed to have better initial asymmetry than the *n*-type devices. At first this doesn't make a lot of sense because the effective mass of a hole is higher than that of an electron, which would lead to a lower MFP at a given doping level. However, overall the *p*-type wires have been shown to have a lower doping level which could lead to better performance. Perhaps the most curious thing about the p-type wires is that when looking at their geometry (Fig. 4.10), we would not expect to them to have high asymmetry because their neck diameter is still quite large. However, the wire in Fig. 4.10 gave an initial asymmetry of 450. The wires with the best performance had d = ~65 nm, D = ~95 nm, L = ~450 nm. Their saving grace is that they did seem to have a very

abrupt constriction side wall with an l = ~16 nm. This could be more evidence that the constriction angle is very important for achieving high asymmetry. Certainly more data needs to be collected generally on p-type devices and on how their surface affects performance. Systematic data on oxide formation was not collected, so I do not want to make any unfounded conclusions in this dissertation about surface.

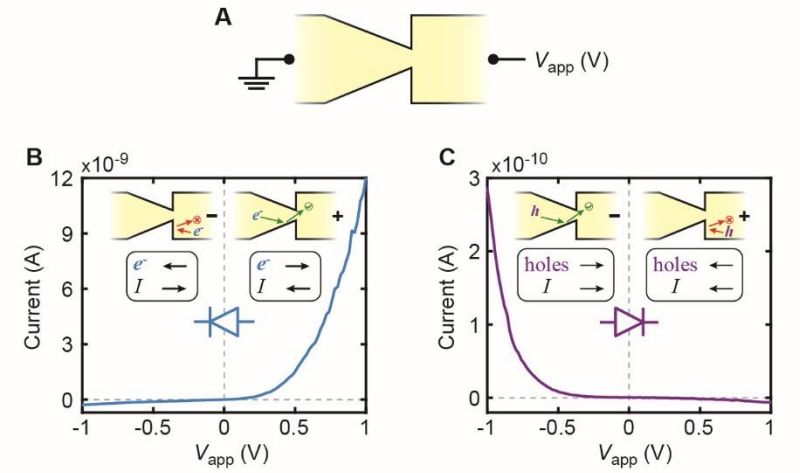

Figure 4.9: Comparison of *n*-type and *p*-type geometric diodes. (**A**) Diagram of the electrical measurement configuration for all single-NW geometric diode devices, where voltage (V_{app}) is applied to the side of the NW with the constriction while the ratchet side of the NW is held at ground. Note that this definition of the sign of the applied bias causes forward bias condition to be reached at a negative applied bias in the case of *p*-type devices. (**B**) *I*-*V* curve for an *n*-type NW geometric diode created using phosphorus (P) dopants with electrons as the majority carrier. The vertical dashed line separates reverse bias (left) from forward bias (right). Insets (upper): schematic diagram of electron trajectories and net electron and current flow in the structure under reverse bias (left) and forward bias (right). Inset (lower): electrical circuit diagram showing the standard diode symbol with the direction of the applied voltage indicated. (**C**) *I*-*V* curve for a *p*-type NW geometric diode created using boron dopants with holes as the majority carrier. The vertical dashed line separates reverse bias (right) from forward bias (left). The lowest encoded gas phase doping level is ~1.5 x 10^{19} cm^{-3}; however, it has been shown that the active doping level is roughly two orders of magnitude lower than the encoded doping for *p*-type NWs, causing the doping level at the constriction to be ~1 x 10^{17} cm^{-3}.[40] Insets (upper): schematic diagram of hole trajectories and net hole and current flow in the structure under reverse bias (right) and forward bias (left). Inset (lower): electrical circuit diagram showing the standard diode symbol with the direction of the applied voltage indicated. Note that the direction of the diode for the *p*-type device has reversed compared to the *n*-type device because of the change from electron majority carrier to hole majority carrier.

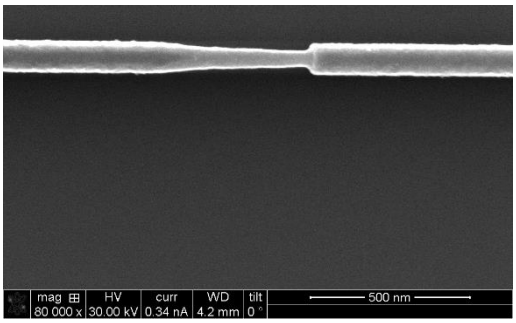

Figure 4.10: SEM of *p*-type wire. SEM image of a p-type wire used in a device. Scale bas is 500 nm.

4.2.5 Diodes in Series and Parallel

The bottom-up fabrication process also facilitated the series connection of multiple subunits within a single NW, as illustrated by the SEM image of geometric diodes in series in Fig. 3.5. It is difficult to extrapolate conclusions from diodes that are gown back to back in series like shown in the Fig. 3.5. Wires that had that had sawtooth sections that were back to back that were measured generally had lower overall current and low overall asymmetry. This makes sense because the voltage drop that propels the charges through the wire is now spread out over multiple subunits. Therefore, if there were two identical geometric diodes in series, it should take twice as much voltage to achieve the same asymmetry as one of those diodes.

To test this idea, two geometric diodes encoded in a single NW, but spaced out so that there is a degenerately doped n-type between them, were measured separately and in series. The *I-V* curves from these measurements are shown in Fig. 4.11A. When measured in series, the device exhibited the expected combined response from the two individual diodes because the non-ballistic, degenerate *n*-type segments between the diodes acted as an Ohmic connection between the two. Analogously, separate NWs can be externally wired in parallel and also exhibit the expected current summation (Fig. 4.11B). Together the results indicate that a combination of geometric control, surface treatments, and series or parallel connections can be used to create

customizable *I-V* characteristics.

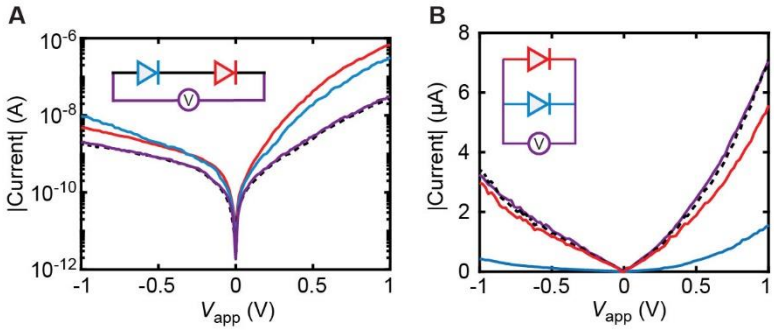

Figure 4.11: Series and parallel measurements. (**A**) Semi-logarithmic *I-V* curves for two diodes encoded in series within a single NW, showing the *I-V* response across both diodes (purple) and response of the individual diodes (red and blue). Dashed line represents the predicted response of the series-connected diodes based on the responses of individual diodes. (**B**) *I-V* curves for two devices connected in parallel, showing the *I-V* response across both diodes (purple) and response of the individual diodes (red and blue). The dashed line represents the predicted response of the parallel-connected diodes based on the responses of individual diodes and matches experimental data.

4.3 Conclusion

VLS grown Si NWs shaped using the ENGRAVE process show tunable diode behavior. The diode behavior is characterized using DC asymmetry. Prior to surface modification of the wires, DC asymmetry values at 1 V are measured between 1 (for unetched wires) up to 10's (for well etched wires. The asymmetry is tunable using the geometry, and generally the more deeply etched a wire is (producing a larger θ), the higher asymmetry it can achieve. However, all of the geometric parameters affect each other, and most notably a wire must also have a high φ in order to have a high asymmetry. Generally geometry is a good predictor of asymmetry and diode behavior, but the fabrication process prevents it from being ideal. Things like surface defects and mobile impurities could be distorting the trends in geometry.

The nature of the surface has a large impact on diode behavior. A native oxide serves to increase asymmetry and decrease overall current in *n*-type wires. A hydrogen anneal and thermal oxide (which should serve to decrease surface defects) has roughly the same effect as a native oxide. Curiously, alumina (which has the opposite charge to oxide) also serves to improve

asymmetry and seemingly does not decrease the magnitude of current as much. This perhaps means that passivating defects is more important that the nature of the surface coating, but more works needs to be done to confirm this. Specifically work that is able to measure wires pre- and post-surface modification.

Bringing diodes to low temperature increases the MFP of the charges, which increases the asymmetry, but at the sacrifice of ~1 order of magnitude of overall current. This serves to confirm the quasi-ballistic transport mechanism. Also *p*-type wires were measured and they showed reversal of asymmetry due to the switching from electrons to holes as the majority carrier.

Wires can be hooked up in series and parallel and exhibit the expected Ohmic combination of the two when measured separately and then together. Therefore, through control of geometry, surface, and series and parallel connections, fully customizable *I*-*V* characteristics can be achieved. This level tunability is unparalleled in any other diode system and is a key advantage geometric diodes have over other diode systems whose properties are locked in by the material chosen. In other systems to get different electronic properties, a separate material must be used, but for geometric diodes simply a different shape can be created. Additionally geometric diodes could be used to lead to more straightforward creations of complex electronic systems. For example, a full wave rectifier could in theory be created all on one NW simply by putting two diodes facing one direction and two facing the other direction with degenerate sections between them all. Indeed this is a natural next step to demonstrate the power of geometric diodes.

CHAPTER 5: MEASURING NANOWIRE GEOMETRIC DIODES WITH ALTERNATING CURRENT[5]

5.1 Introduction

Typical diodes can achieve high DC asymmetries (> 10^6) at a given V_{app}. However, because their operation relies on a potential barrier, they possess a large capacitance. Thus, their ability to rectify AC at high frequencies is fundamentally limited by a *RC* time constant.[75] Geometric diodes have such low capacitance that they are theoretically limited not by *RC* time constants but rather by the inherent ballistic motion and flight time of charge carriers. The quasi-ballistic operation of the geometric diodes enables electron ratcheting at high AC frequencies, which manifests as rectification of an AC signal to produce a DC voltage (V_{DC}). The flight time of charge carriers through the quasi-ballistic region of the structure dictates the inherent response time, and for electrons at the Fermi velocity moving through the Si geometric diode, it is expected to exceed ~1 THz.

To elaborate more deeply on the frequency response, the characteristic length scale over which an electron would need to move within one AC cycle inside a NW geometric diode is ~100 nm. Considering electrons moving at v_{th} or at v_F (section 1.1.1.3), we use room temperature for v_{th} and $n = 4\text{x}10^{19}$ cm^{-3} for v_F and deduce a flight time of ~440 fs or ~455 fs, respectively. These time scales correspond to frequencies exceeding 1 THz. Moreover, we note that the "THz regime," which denotes a frequency range with a notable absence of functional devices, is

[5] Portions of this chapter are reprinted with permission from Custer, J. P.; Low, J. D.; Hill, D. J.; Teitsworth, T. S.; Christesen, J. D.; McKinney, C. J.; McBride, J. R.; Brooke, M. A.; Warren, S. C.; Cahoon, J. F. Ratcheting quasi-ballistic electrons in silicon geometric diodes at room temperature. *Science* **2020,** *368*, 177-180.

generally considered to span ~0.1-3 THz. The combination of zero-bias turn-on voltage and AC operation into the terahertz (THz) regime,[46,75] may unlock applications that include high-speed signal processing or data transfer [26,76] and long-wavelength energy harvesting.[77,78]

5.2 Results and Discussion

Before testing wires at high-frequency, the substrate and contacts had to be optimized to reduce parasitic elements that would dampen the signal before it gets to the device. It was determined that the device substrate and layout for the DC devices (see Methods section 2.5.2.2 and 2.6.2) will not work for the AC devices. The DC substrates are conductive Si with a thin dielectric on top. This means that the AC signal can be shunted through the top of the substrate, thereby reducing the signal that goes to the device dramatically. This can be experimentally shown by applying an AC signal directly to a substrate and then measuring it using an oscilloscope at a different place on the substrate. The solution to this was to use a quartz substrate. However, just quartz could not be used because during the etch process, the wires would come off of the surface. Instead, a Si_3N_4 coated quartz wafer was used (see Methods section 2.5). This substrate reduced substrate conductivity and capacitance dramatically.

To get this substrate to work for marker patterns was not trivial. Metal could be deposited to form the marker pattern, but that would increase capacitance and hindered etching, so we turned to the DRIE. The DRIE had a tough time getting through the quartz and nitride without destroying the PMMA:MMA polymer resist and/or turning it into an impenetrable barrier. Nothing that was tried could remove this polymer (not UV/ozone, sonication, piranha) so it likely formed a Teflon like material. Eventually the recipe listed in the methods section was tried. It worked exceptionally well, but it did heat the substrate up to at least 90 °C. Initially, I thought that the temperature would destroy the selectivity, but it only improved it. It certainly

wasn't supposed to get that hot, as the temperature was originally set to 10 °C, so it was probably an issue with our specific DRIE because it is very old. However, that mistake led to a discovery and got the marker patterns to work. Once the substrates were made into marker patterns, the charging had to be dissipated. Originally PEDOT:PSS was tried, but they could not resolve large structures (it actually worked well for small (>10 μm) patterns). The solution turned out to be much simpler and just involved sputtering like any other sample (see Methods section 2.5). Additionally, a ~1/2 inch Teflon block was put on top of the metal stage in the probe station to further reduce parasitics (this may have been overkill though).

The layout of a DC device is such that there are abrupt changes in geometry in the metal contacts going from a large to small width (see Fig. 2.1A). These abrupt changes in geometry cause AC signals to be back-reflected (thus reducing the amount of signal that can get to the device). The solution to this was to switch to a "strip-line" geometry that had only smooth transitions between geometries (Fig. 2.1B). This reduced back-reflected AC signal.

5.2.1 Initial AC Measurement Setup

To test the frequency response of the diodes up to the instrumental limit of 40 GHz, the circuit shown diagrammatically in the inset of Fig. 5.1A was used to measure V_{DC} (see Methods section 2.6.2). Figure 5.1A shows the expected proportional increase of V_{DC} with power and verifies high-frequency electron ratcheting at 40 GHz. The y-axis is in V_{DC} and is the rectified output voltage across the load resistor in the schematic. The lower x-axis is the power output of the AC signal as dialed in on the VNA. Note that dBm is a measure of power, and the actual current or voltage supplied is a function of the resistance of the system. This does not usually matter when everything is at 50 Ω, but our wires are not 50 Ω, instead they are closer to 1 MΩ. For this reason, the voltage amplitude of the AC signal as if it were going through a 50 Ω resistor

is listed on the top x-axis. This voltage is a best-case scenario, if parasitics were minimized. Even so, due to the impedance (AC resistance) mismatch of the VNA output (which is expecting 50 Ω) and the NW (which is ~1 MΩ) there is a significant amount of back-reflected signal. This means that even if the signal makes it to the diode perfectly, the diode itself will reject a lot of the signal, and even the signal that does make it through will be dampened.

To conduct the measurement at all, parasitic elements in the measurement setup had to be minimized and the correct instrumentation had to be acquired. The first thing was getting the right substrate and device layout as discussed previously. The other major thing was understanding and accounting for parasitic elements in the measurement setup. Standard probe tips are only good to ~1 GHz, and to go higher GSG tips are needed. The GSG tip brings grounds right to the edge of the tip to increase shielding and reduce power loss in transmission. We also had to switch out all of the cabling in the probe station to put in high frequency cabling. This was straightforward and could be just bought from Lakeshore. We had to do this for external cabling as well (see Methods section 2.6.2).

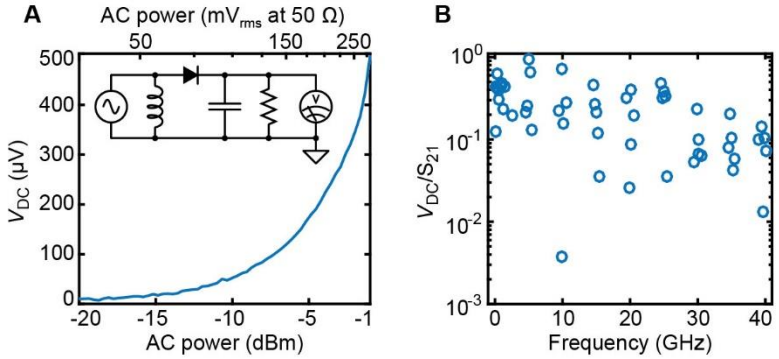

Figure 5.1: High-frequency electron ratcheting. (**A**) V_{DC} as a function of applied AC power at 40 GHz, with power displayed in units of dBm (lower axis) or voltage across a 50 Ω load (upper axis). Inset: circuit diagram of the measurement setup. (**B**) V_{DC} normalized to S_{21} as a function of frequency for a single NW device.

Then we had to get the proper instrumentation to supply the signal to the device. We tried different VNAs and signal sources that all had different frequency ranges and powers. We have

not landed on the ideal instrument for the measurement we were doing, so that is a potential place for improvement. See Methods section 2.6 for the instruments used, but ideally we would have just a signal source that was cable of frequencies up to 40 GHz. Going beyond 40 GHz requires new probe tips and new cabling as when you start to get around 100 GHz and up, all of the electronics are optimized for only a specific band of the spectrum.

Perhaps most importantly we had to understand and account for parasitics by adding an inductor, capacitor, and resistor to our measurement setup as shown in Fig. 5.1A inset. With the proper setup (as described in the Methods section 2.6.2), the raw measurement looks like Fig. 5.2A. The power is swept repeatedly at a fixed frequency and the V_{DC} is the difference between the peak and the trough. The voltage can go negative or positive depending on the voltage of the diode. However, before optimization there was parasitic capacitance. The inductor in the inset in 5.1A was 7.8 mH and was used to remove parasitic series capacitance. Before the introduction of the inductor there was a considerable series capacitance before the signal reached the device that caused initial large spikes in voltage when the tips were set down (Fig. 5.2B)

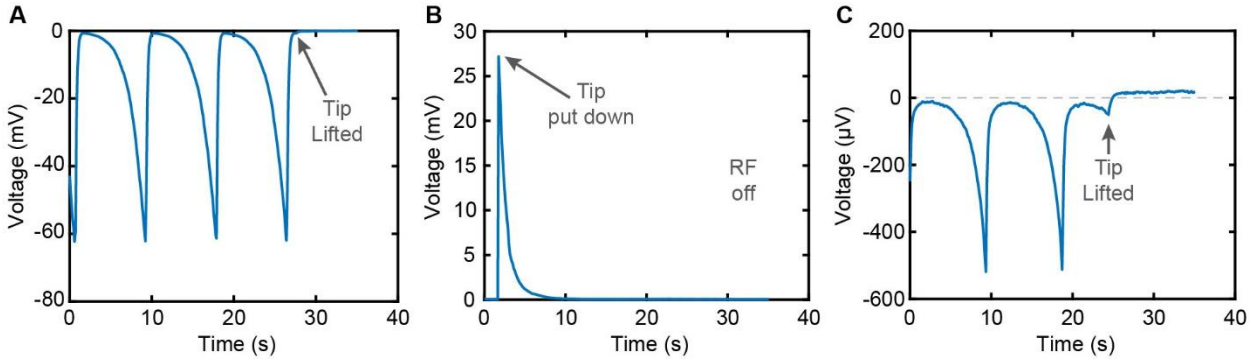

Figure 5.2: AC measurement issue demonstrations. (**A**) Ideal frequency measurement as discussed in the methods. Repeating power sweep from -27 to -1 dbm at 5.2 GHz with the SMU holding the open circuit condition and measuring voltage. Arrow indicates when GSG tip was lifted off the contacts. (**B**) Demonstration of series capacitance. The spike is from the tip being put down on the sample with no RF on. No inductor is present. (**C**) Demonstration of minor offset at low voltages. Ideal frequency measurement as discussed in the methods. Repeating power sweep from -27 to -1 dbm at 40 GHz with the SMU holding the open circuit condition and measuring voltage. Arrow indicates when GSG tip was lifted off the contacts.

To get rid of this, an inductor was placed in parallel before the diode to shunt the built up charge on the parasitic series capacitance to ground. A large enough inductor was chosen as to not affect the AC signal, but really any large inductor should do the same thing. The resistor was 30 MΩ and was chosen to approximately match the voltage drop across the diode while staying mismatched from the 10 GΩ input impedance of the SMU. The particular wire measured had a forward bias resistance of ~2 MΩ, so a resistor that was slightly larger than that (30 MΩ) produced the highest DC output signal. Resistors that were higher or lower both gave lower DC output voltages. When the resistor is lower resistance than the diode's forward bias resistance, then the voltage drops across the diode, but not over the resistor (and the signal that is measured is the voltage drop over the resistor, not actually the voltage drop over the diode). When the resistor is more resistive than the diode more of the voltage drops across the resistor leading to more signal, but if the resistor is too high, then none of the voltage drops over the diode and so no DC output is produced in the first place. Therefore, the "goldilocks" resistor (which reflects the optimization of both diode rectification and magnitude of the measured voltage signal) must be found for each wire. The capacitor was 6.8 nF and was chosen to minimize background noise from parasitic elements and to integrate the signal. The diode outputs a half wave after it has rectified a signal, and a capacitor serves to integrate that signal to a DC signal that can be measured across the resistor (load). For this measurement, the capacitor seemed to be minimizing a parasitic element that was causing an offset in the SMU voltage noise floor. Without the capacitor, the SMU noise floor was in the 10^{-4} V range, but with the correct capacitor it was taken down to low 10^{-5} V range (Fig. 5.2C). The noise floor is shown in Fig. 5.2C at the end of the measurement at ~25 s the GSG tip supplying the RF is lifted up and the tip leading to the SMU is still down, but just measuring noise. I am unsure the source of this

parasitic element that caused this offset. It could have been something internal to the SMU, but a 6.8 nF capacitor removed it. Once this measurement was optimized, all other high frequency measurements just built off of this and used essentially the same setup.

5.2.2 AC Frequency Sweeps

Figure 5.1B shows V_{DC} as a function of frequency normalized by the separately measured transmitted power (S_{21}) through a transmission line on the device chip. This normalization partially accounts for frequency-dependent parasitic elements within the measurement system that alter the AC power applied to the device at each frequency (Fig. 5.3). Parasitic elements can be minimized using the methods discussed in section 5.2.1, but they cannot be removed entirely. On top of that, because parasitics come in the form of impedance, their values change with frequency, thus the amount of power that the diode receives changes with frequency. This is most obviously demonstrated in figure 5.3A, which shows the S_{21} through a metal stripline. To measure S_{21}, the VNA is setup to transmit a signal out of the output, through the same measurement setup as the standard setup, but instead of going to a NW, the signal goes to a metal strip. On the other side of the strip is a mirror image of the setup that sent the signal in (same cables, but the GSG tip is slightly different looking in appearance despite being the same model number). Then those cables lead to the input of the VNA and the amount of signal that made it through the setup and was collected at the output is compared to the amount that was sent out from the input. The power can be held and then the frequency can be swept. As shown in Fig. 5.3A, the S_{21} collected is very noisy with dramatically different values when only moving in small increments of frequency. This noise is due to the frequency dependence of the parasitic elements causing different resonances in the signal where sometimes the signal is strong and other times it is cancelled out. Note that frequencies below ~3 GHz are reasonably flat and

strong, and then higher frequencies see a significant overall drop off with considerable resonances. This drop off is parameterized by the equation in Fig. 5.3A:

$$y = 0.1033e^{-0.061x}. \quad (5.1)$$

For the actual NWs I did not just put down the tips and sweep the frequency at a certain power because I destroyed too many wires when doing that. Instead the VNA was set to sweep power at a fixed frequency and then the tip was put down and the SMU was set to measure voltage (hold the open circuit condition). This way seemed to not introduce voltage spikes associated with turning on devices or initiating sweeps that could destroy a device. Therefore, to get each V_{DC} at each frequency, the measurements had to be done individually. Every point in Fig. 5.3B is a separate measurement. The frequencies measured were in groups of n-0.5, n-0.2, n, n+0.2, n+0.5 GHz where n is the frequencies listed on the x-axis of Fig. 5.3B, as well as 0.9, 0.6, 0.4, 0.3, 0.1, and 0.05 GHz. The V_{DC} was determined by subtracting the minimum output voltage (when the signal was virtually 0 (left side of Fig. 5.1A)) from the maximum output voltage (when the signal supplied was its strongest (right side of Fig. 5.1A)). This difference is the reported V_{DC} in Fig. 5.1B and 5.3B. The raw V_{DC} shown in 5.3B demonstrates a trend where frequency is falling off quite considerably with frequency. This drop originates not from a loss of diode response, but rather from parasitic elements considering that the devices should respond into the THz regime.

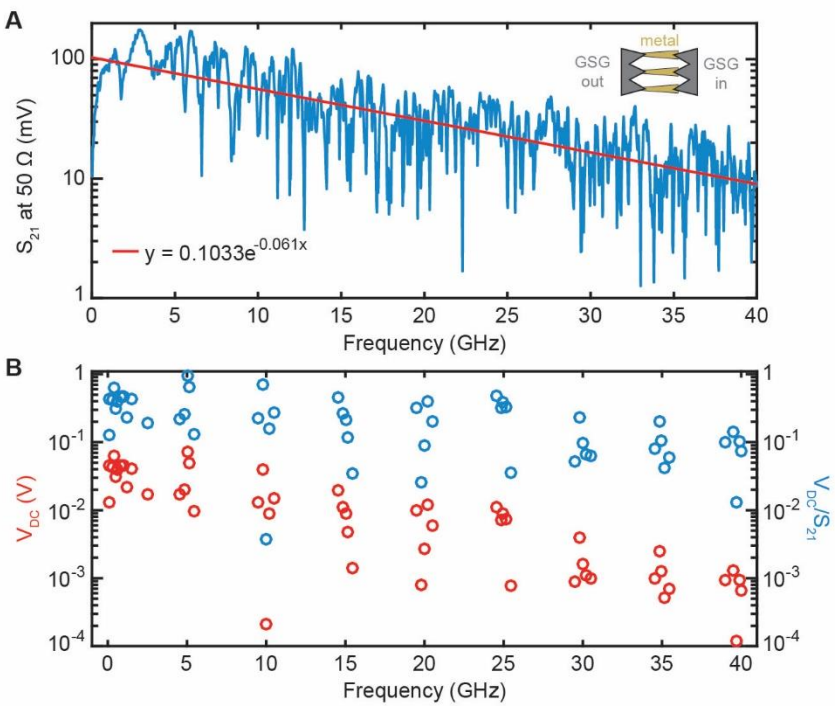

Figure 5.3: High-frequency rectification normalization. (**A**) S_{21} as a function of frequency measured across a transmission line on a NW device chip. S_{21} is plotted as voltage across a 50 Ω load. Resonances from parasitic elements in the measurement set-up can be seen throughout the frequency range measured. The data is fit to an exponential decay (red line) to produce a smoothly varying frequency-dependent function for signal normalization. Inset: Schematic diagram of the S_{21} measurement. (**B**) Unnormalized V_{DC} values from the measurement of a single NW geometric diode (red, left-hand axis) and normalized values (blue, right-hand axis) of V_{DC}/S_{21} for the same diode using the exponential fit to S_{21}. Normalization produces a more frequency-independent response from the geometric diode by accounting for the reduction in power applied to the diode as frequency increases due to the parasitic elements in the measurement setup. However, not all parasitic elements can be accounted for due to the impedance mismatch of the NW and the signal generator.

However, equation 5.1 can be used to normalized the rectified signal, V_{DC}, from the diode. This normalized signal accounts for a significant portion of the parasitics, and as seen in the blue dots of Fig. 5.3B, when the V_{DC} is normalized, the trend of the V_{DC} falling off with frequency is more or less removed. However, the normalization does not unilaterally account for all the resonances that can be seen in the S_{21} measurement that are also present (but in different locations and magnitudes) in the measurement of the diode. An example of this would be the points at 10 or 25 GHz that are dramatically lower than the rest of the grouping. These points are

the whole reason that measurements were taken in groups of frequencies, because any given point could be on a resonance frequency that is lowering the value of V_{DC}. However, moving the frequency slightly gets the measurement off of that resonance and should return it to a higher value. All this being said, the quantity V_{DC}/S_{21} shows a relatively flat response from 100 MHz out to the instrument limited 40 GHz, highlighting the broadband electron ratcheting effect in these diodes. More work should be done on characterizing more diodes at high frequency as well as trying to push the frequencies measured beyond 40 GHz.

5.2.3 Energy Harvesting Example

Because of their high-frequency response and their low turn-on voltage, the geometric diodes could be used for energy harvesting and signal processing applications. Figure 5.4 shows *I-V* curves of a geometric diode rectifying Wi-Fi signals (5.2 GHz) at varying powers (see Methods section 2.6.2.3). Admittedly, the diode "curves" look nothing like a typical diode because there is no curve to them, but this is because of the low voltage range shown, and the diode used only had an asymmetry of ~30. The *I-V* "curves" progressively shifted into quadrant II, as opposed to quadrant IV because the diode behavior is actually the inverse of a typical diode. As the curves progressively shift more into quadrant II AC power increased, corresponding to increasing power conversion and demonstrating the ability for the diodes to serve as long-wavelength energy harvesters in analogy to the operation of a solar cell.[8] The geometric diodes could serve as the rectifying component of rectennas,[77-79] harvesting background radiation for low-power consumption devices.[80]

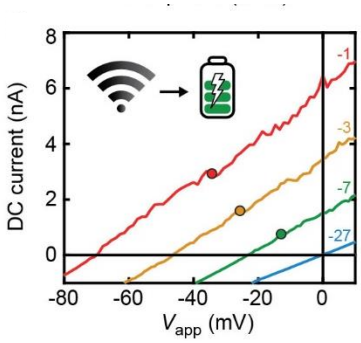

Figure 5.4: Energy Harvesting. *I-V* response of a geometric diode with 5.2 GHz AC applied at powers of -27 (blue), -7 (green), -3 (orange), and -1 dBm (red). Circles denote the maximum power points for each diode. Inset: schematic illustration of energy harvesting at WiFi frequencies.

5.2.4 Signal Processing Example

Similarly, Fig. 5.5 shows the response of a geometric diode to a 20 GHz AC signal that was amplitude modulated between -27 and -5 dBm to convey musical notes, producing clear V_{DC} levels for each signal amplitude (see Methods section 2.6.2.4). For this measurement the GSG tip was able to be put down and held down while the signal was modulated without destroying the wire. A different signal source was used because it allowed its signal to be externally modulated by an arbitrary function generator (see methods section 2.6.2.4). The signal was amplitude modulated to varying levels to match the levels of a musical scale. From this data, in the form of notes on a solfège scale can be encoded (Fig. 5.5).

Regardless, this example highlights the signal demodulation and processing capabilities of the geometric diodes. Together, Fig. 5.4 and 5.5, demonstrate that a single input signal could simultaneously provide data and be rectified into useable power.[81] These demonstrations, combined with the ability to create parallel and series-connected custom diodes, highlight the potentially diverse application space for high-frequency electron ratchets operating at room-temperature.

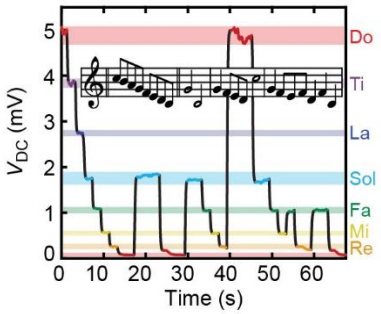

Figure 5.5: Signal Processing. Demodulation of a 20 GHz square-wave amplitude modulated signal, corresponding to musical notes, by the geometric diode. The V_{DC} response time is limited not by the diode but by the measurement unit and integrating capacitor. Color-coding corresponds to the solfège shown on the right-hand axis. Inset: sheet music corresponding to the input signal.

5.2.5 CO_2 Laser Measurement

To test the diode's response well into the THz regime (but below the bandgap of Si) we attempted to measure the response of the wires at 28 THz using a CO_2 laser (see Methods section 2.6.2.6) with the help of Prof. Joanna Atkin's group, particularly Clayton Casper. The measurement idea was to direct a THz signal to the diode with an antenna on it and measure if the diode produced a DC offset. However, execution was a little more complicated. The device fabrication was the same for these wires as typical devices except that instead of 4 contacts, 2 bowtie antennas were contacted to the wires (see Methods section 2.6.2.6). The antenna sizes used were ¼, ½, and 1 wavelength of 28 THz. The THz signal was directed to the NW using THz optics and then directed downwards onto the sample. Then probe tips were used to come in from the sides to contact to the metal contact pads. The SMU was set to either measure current or voltage. The signal was also chopped and a lock-in amplifier was used (see Methods section 2.6.2.6). None of this resulted in a signal from the THz though. In retrospect, the wires most likely do not respond to such a high frequency because the limit of their flight time. Curiously, a strong signal was seen using the lock-in amplifier from the above bandgap, green HeNe laser, but that is expected from the band structure and metal contacts. If the measurement were to be

retried there are two things that definitely need to be improved. The first is that the quartz AC substrate should be used, and second is that the antennas should be simulated to make sure they are resonant at the proper wavelengths. I personally learned a lot from the CO_2 measurement setup that I then took into later free-space THz measurements (discussed next), but it was certainly a quick and dirty first shot that has a lot of room for optimization. All that being said, I would not try it again until the frequency response is confirmed at a lower frequency… like 600 GHz.

5.2.6 600 GHz Measurements

Building off of the knowledge learned in the 28 THz free-space measurement, a 600 GHz free-space measurement was attempted with the help of Dr. Padilla and his group at Duke. The general idea of the measurement is quite simple and mimics the CO_2 laser measurement: direct a 600 GHz free-space signal to a diode and measure to see if it produces a DC offset. This measurement is a little more complicated than the CO_2 laser measurement though because unlike the 28 THz beam that can be tracked with a heat sensitive film, the 600 GHz beam is very difficult to detect. In order to detect the THz beam, a metamaterial array (built by the Padilla group) is put in front of an IR camera (see Fig. 2.4C). The beam was aligned using a HeNe laser and the metamaterial array, then the sample was brought into the same spot as the HeNe laser.

The meta-material antenna that was connected to the wires was designed by the Padilla group and was tuned to be resonant for the desired frequency and also considered the specific substrate that we were using (see Methods section 2.6.2.5). Only one antenna and wire could fit on each marker pattern because they were so big. The antenna were big enough to be directly contacted by the probe tips, and at first a set-up was tried where the sample was lying flat and the beam would come down onto it from a 45 °. Then probe tips would come in from the sides and

touch to the antennas ends. However, the metal does not stick as well to the quartz substrates, so touching down the probe tips more or less destroyed the samples. It was also difficult to see with the camera we were using.

Then we switched to a setup where the sample was stood up perpendicular to the laser table. This method was also much better for the Padilla group because they did not have to change around any of their optics. However, for this method the sample needed to be wire bonded (see Methods section 2.6.2.5). The sample could be wire bonded directly on the large pads of the metamaterial antenna, and I was told that this does not affect the resonance of the antenna or the ability for the signal to couple in, but I cannot find literature about that. The wire bonds lead to custom PCBs that led to pin connectors. Each side of the antenna was connected to the SMU and either voltage or current was measured when the signal impinged onto the sample. This did not produce any noticeable signal. Additionally a chopper and lock-in were used, but that also did not produce a signal. Initially we thought it was working because I was chopping the signal with my hand, but it turned out that bringing my hand close the sample produced a sizable signal due to poor shielding. Note that only a few wires made it to the setup, but none were ideal and all were eventually destroyed by a static shock after the wire bonding process.

When this measurement is repeated I would make sure that the wires used have good asymmetry (>3), but perhaps more importantly have reasonably low resistance. For example, if a diode had an asymmetry of 10 with current of 10^{-6} at 1 V, I would choose that wire over one that had an asymmetry of 100 with current of 10^{-10} at 1 V. Also be very careful when handling the wires after wire bonding because they are very sensitive to shock. The wire bonds could perhaps be put off to the side. For example, make a small contact that went from the metamaterial antenna to a larger pad that could have the wire bond. This would have to be vetted with the

collaborators though. Additionally, 94 GHz free-space measurement could be tried, but the antennas would have to be considerably larger. Also a non-metamaterial antenna could be tried. A simple bowtie (which has been shown to work for THz sensing[33,82,83]) could work and uncomplicate the device fab. I would also be less dubious that a wire bond to a large bowtie would interrupt the signal very much. The 600 GHz measurement is promising, but there needs to be optimization in the sample to fully vet if the wires are responding to those signals or not.

5.3 Conclusion

Si NWs have been demonstrated as a functional experimental system to create tunable geometric diodes. These diodes have been measured at DC to confirm their diode behavior. In order to confirm their ability to operate as electron ratchets, their ability to rectify an AC signal was measured. The amplitude of a 40 GHz AC signal was swept across a NW diode and the rectified DC output voltage (V_{DC}) was shown to have an exponential increase as expected, confirming the diode's rectification ability out to 40 GHz. In order to conduct this measurement, great lengths had to be taken to mitigate parasitic elements in the setup. This same measurement was conducted at various frequencies from 50 MHz to 40 GHz to measure the broadband response of the diode. Initially the raw V_{DC} values look like they fall off with frequency, however, when V_{DC} is normalized with S_{21} to account for parasitics, the frequency response is quite flat out to 40 GHz. The measurement with V_{DC} was attempted by wirelessly transmitting the signal, but this did not work in a very quick and dirty attempt. There is a lot of room for improvement in this measurement. Additionally V_{DC} from the wires (coupled to antennas) was attempted to be measured using a free-space measurement at 28 THz and 600 GHz. Neither of these measurements showed any signal, but the results should not be taken as conclusive given the large number of uncertainties and improvements needed in the experimental design. The

response of the wires should however be confirmed at 600 GHz before retrying at 28 THz because upon further calculation (see section 5.1) 600 GHz should be just on the edge of the frequency response of the diodes and 28 THz is likely beyond it. That being said just because a frequency is beyond the –3 dbm point it does not mean that there will be no signal, it just means that the signal will be much weaker.

The diodes were experimentally confirmed to operate up to an instrument limited 40 GHz. It is likely that the diodes have response out to ~1 THz based on calculations of charge carrier flight time. Therefore, a natural next step will be to confirm the diode response past 40 GHz. The issues are that as frequency gets above 40 GHz, special equipment is needed in bands of ~20 GHz to properly guide the signal to the target and this equipment is expensive. Free-space measurements are likely the easier alternative, but they come with their own set of complications, namely ensuring the signal is getting to the device by alignment of optics and optimization of antenna.

CHAPTER 6: SIMULATING AND UNDERSTANDING NANOWIRE GEOMETRIC DIODES[6]

6.1 Introduction

In order to more fully understand the physics of what is happening inside the geometric didoes, the NW structures were simulated using several different methods. It's critical to understand the transport mechanisms involved around the structural and dopant asymmetry to fully determine what is giving rise to the diode behavior. Finite-element (FE) modeling using a home-built simulation in Comsol Multiphysics has been shown to do a good job of capturing the band bending, doping, and electrostatics of semiconductor systems.[84] Initially the NWs were simulated using Comsol; however, Comsol neglects the potential for the quasi-ballistic / ballistic nature of the charge carriers.

To more fully simulate the charge transport in the NWs, an analytical model was built in python. The analytical model takes a given shape and creates an array of starting points within one MFP of the diode neck. Then all paths from each starting point are determined. Then the ratio of all paths that will make it through on direction versus the other is determined. This ratio leads to a ratio transmission probabilities that can be correlated to DC current asymmetry. This model also employs motivation from an adapted Landauer-Büttiker (LB) formalism.[1,17,18,85-88]

The analytical model works nicely for looking at purely ballistic charge carriers, but it ignores much of the semiconductor device physics because it purely looks at geometry. For this

[6] Portions of this chapter are reprinted with permission from Custer, J. P.; Low, J. D.; Hill, D. J.; Teitsworth, T. S.; Christesen, J. D.; McKinney, C. J.; McBride, J. R.; Brooke, M. A.; Warren, S. C.; Cahoon, J. F. Ratcheting quasi-ballistic electrons in silicon geometric diodes at room temperature. *Science* **2020,** *368*, 177-180.

reason a Monte Carlo model was built to consider more device physics. Monte Carlo method is widely used to model many physical systems, including semiconductor device physics.[3,89-91] A Monte Carlo simulation can be considered as a computational experiment with a number of variables which may not be feasibly obtained through physical experimentation. A typical algorithm randomly generates an input for each variable from its respective probability distribution over a predefined domain and outputs the result of a deterministic computation. Each variable repeatedly samples from its respective distribution until thousands of possible initial conditions have been simulated, which results in the probability of occurrence for different events. For the model created in this work, charge carriers are allowed to flow through a given geometry that matches the NW diodes. The charge transport is dictated by the initial momentum and direction of that charges, as well as a distribution functions that determine the scattering within the semiconductor. This model allows the consideration of ballistic charge carriers and takes into account doping levels and other semiconductor device properties that are characterized by distribution functions. Modeling geometric diodes with this combination of simulation techniques, coupled to experimental data, allows for a much more complete understanding of the charge transport phenomena within the NWs.

6.2 Results and Discussion

6.2.1 Finite-Element Modeling

We modeled the diodes to understand the geometric dependence of the behavior. FE electrostatic simulations (Fig. 6.1), which have been shown to accurately describe NW *p-n* junctions,[84] were created. The donor dopant distribution can be seen in Fig. 6.1 and matches to our best approximation of what the doping level is expected to be based on EDS maps and gas phase ratios. This exponential drop in doping level leads to a very small area in which the

potential drops (Fig. 6.1B and C Top). This rapid drop in potential leads to very high field strengths at and around the neck (Fig. 6.1B and C upper middle). Interestingly, the direction of the field flips within the funnel structure. The field flip comes from the abrupt change in doping as shown in the space charge density (Fig. 6.1B and C lower middle). When -1 V is applied to the right side the field flip is close to the constriction, but when +1 V is applied to the right side the field flip is farther up the funnel and at a much weaker location in the field. This difference is likely the cause of the asymmetry in the current as shown in Fig. 6.1D. Notably, the direction of this asymmetry is in the opposite direction of the experimentally measured current asymmetry. The FE simulations did not reproduce the diode response of the devices because they did not account for the quasi-ballistic nature of electrons.

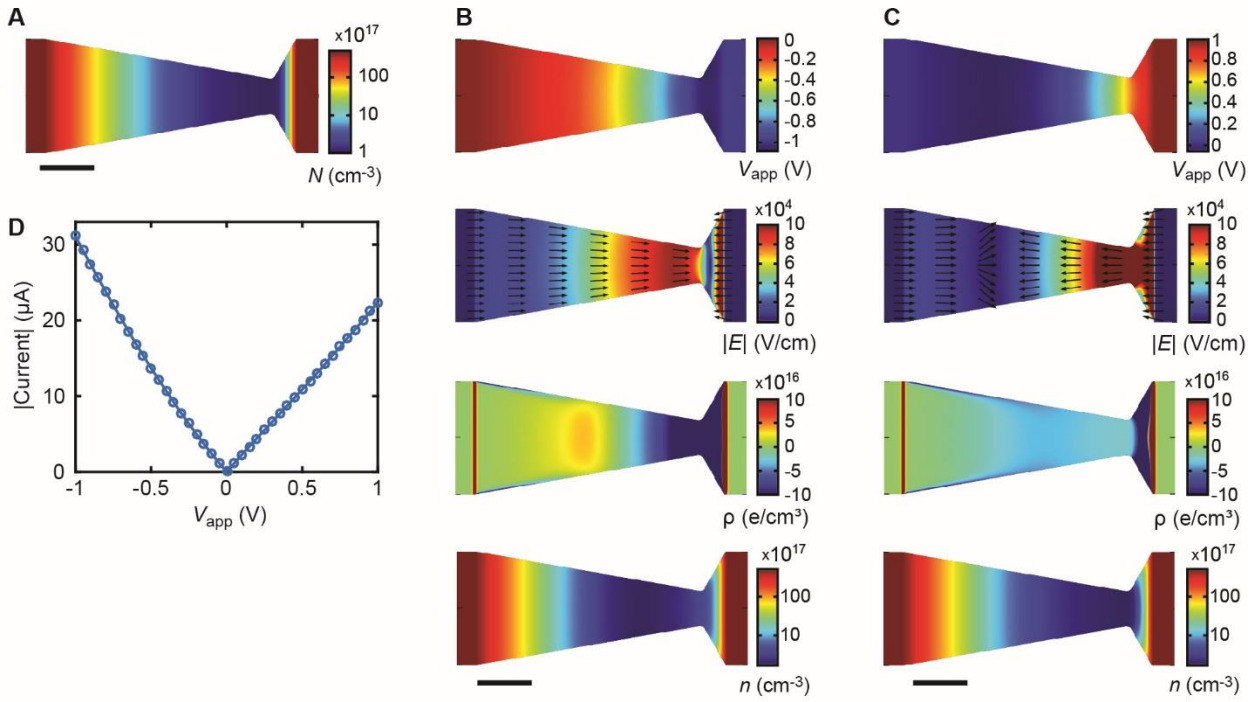

Figure 6.1: Finite-element simulations of a NW ratchet geometry. (**A**) Donor dopant distribution (N_D) used in the simulation and based on the measured dopant distribution as determined by the gas phase ratio of Si:P and EDS mapping with STEM (Fig. 3.2); scale bar, 50 nm. (**B**, **C**) Finite-element simulation results at V_{app} = -1 V (panel B) and V_{app} = 1 V (panel C), showing the electric potential ψ (top), electric field $|E|$ with normalized field lines (upper middle), space charge density ρ (lower middle), and electron concentration n (bottom); scale bars, 50 nm. Note: V_{app}

almost entirely drops across the ratchet, causing the electric field strength to reach values of 10^5 V/cm, allowing electrons to approach the saturation drift velocity of Si and ensuring directed transport of electrons through the ratchet. (**D**) Simulated *I*-*V* curve from the finite-element model showing a DC asymmetry of 0.72 at $|V_{app}| = 1$ V. Note that the simulated DC asymmetry is in the opposite direction of the experimentally measured DC asymmetry and results from depletion effects within the structure. The disagreement of the finite-element results and experimental results highlights the importance of quasi-ballistic charge carrier motion within the structure, which is not captured by the finite-elemental modeling.

The FE simulations did however, demonstrate that the degenerately-doped *n*-type segments adjacent to the sawtooth geometry caused all potentials to drop across the sawtooth region and therefore could serve as electron reservoirs that could inject electrons into the sawtooth region. This is good evidence that the LB formalism could be an important part of the transport mechanism for carriers around the constriction. Thus we built an analytical model that took motivation from the LB formalism.

6.2.2 Analytical Model

Note that the analytical model was largely built by Jeremy Low. We developed a simple analytical model[92] to qualitatively capture ballistic effects by describing the trajectories of single electrons within the sawtooth region (Fig. 6.2) assuming ballistic, specular trajectories without phase coherence effects.[69] Briefly, the model integrates over trajectories that originate with a narrow angular distribution (accounting for the field-driven transport) within one MFP of the constriction, considering both direct transmission through the constriction and multiple specular reflections from the NW surface. It permits the calculation of transmission coefficients for passage through the constriction,[22,69] and we use the ratio (δ) of transmission coefficients in forward and reverse bias for qualitative comparison to the DC asymmetry measured by experiment. The geometry of the model can be swept through any of the given geometric parameter discussed earlier to compare the geometric dependence of δ to the geometric dependence of DC asymmetry in experiment.

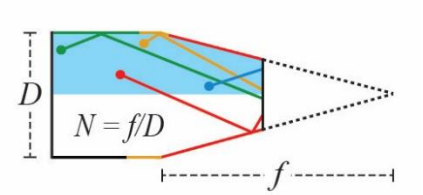

Figure 6.2: Analytical model introduction. Schematic illustration of the analytical model showing example trajectories of electrons originating within a set MFP of the constriction that successfully pass through the constriction. Colored trajectories denote qualitatively different pathways that involve either direct transmission (blue) or specular reflection (green, orange, and red) from the corresponding color-coded segments of the NW surface. The geometric parameters *f* and *D* that define *N* are also shown.

6.2.2.1 Some Quantum Physics and LB Formalism

Before discussing the analytical model in full, we first must dive into some quantum physics to understand the motivation behind the model. This may seem out of place at the moment, but it will all tie into each other as the chapter progresses.

Assuming parabolic band dispersion, the Fermi wavelength, λ_F, of a material can be expressed as $\lambda_F = 2\pi/k_F$. For a 1D material, the Fermi wavevector (k_F^{1D}) can be expressed as:

$$k_F^{1D} = \left(\frac{\pi n_{1D}}{g_{1D}}\right), \tag{6.1}$$

where n_{1D} is the carrier density in 1D and g_{1D} is the band degeneracy for 1D Si. Using n_{1D} = 1.26-0.126 x 10^7 cm^{-1} (calculated assuming a 10 nm diameter cylinder of Si) for 1D Si assuming g_{1D} = 2, we get λ_F^{1D} = 3.18-31.8 nm. Similarly, using n = 10^{18}-10^{17} cm^{-3} (the conservative doping levels for the constriction as discussed in chapter 3) for 3D Si and taking the weighted average of values determined from the longitudinal and transverse Fermi wavevectors (using eqs. 1.8), we get λ_F = 39.5-85.0 nm. Considering that the values of λ_F are comparable to the size of the constriction in the NW geometric diodes, it is possible that effects from sub-band formation could be present in the NW geometric diodes. Nevertheless, when the analysis of the geometric diode device performance is analyzed using the DC asymmetry, the effect of sub-band formation

is eliminated, as indicated in the following section by the result for δ in eq. 6.10. Thus, it is likely that sub-band formation plays a role in the absolute value of the current measured from geometric diode devices; however, the demonstration of the geometric diode effect and influence of geometry on the performance should be unaffected by sub-band formation when analyzed in the context of the DC asymmetry. We note that the relatively high temperatures utilized in chapters 4 and 5 preclude the unambiguous, direct observation of the effect of sub-band formation (*e.g.* quantized conductance) on the device properties, so future studies utilizing measurement temperatures below 10 K will be needed to thoroughly understand the role of sub-band formation in this class of device.

In addition to sub-band formation, we can consider the potential influence of phase coherence effects in the NW geometric diodes. The thermal phase coherence length, L_T, for electrons at room temperature (T = 300 K) can be estimated as:[66,67]

$$L_T = \sqrt{\frac{\hbar D}{k_B T}}, \tag{6.2}$$

which yields L_T = 4.2-7.3 nm using D = 6.8-20.7 cm^2/s. In a ballistic regime, L_T can alternately be calculated as distance over which wavevectors separated by thermal energy $k_B T$ go out of phase by one radian (assuming $E_F >> k_B T$), giving:

$$L_T = \frac{\hbar v_F}{k_B T}. \tag{6.3}$$

Using v_F = 2.20 x 10^7 cm/s, we get L_T = 5.6 nm. In either case, the results for L_T are less than 10 nm, with an average value of 5.7 nm, and indicate that phase coherence effects are unlikely to play an important role at room temperature within the NW geometric diode devices.

This brings us to the LB formalism. The LB formalism was developed to describe charge

flow through a 1D ballistic point contact where there are 2 reservoirs of charges connected by a 1D channel.[87] It was then generalized to include more than one channel.[17,88] Typical descriptions of current and resistance do not work in 1D channels, so this formalism aimed to provide a description.

Let's take a conceptual look at the LB formalism, and then the math around it will be addressed within the deeper description of the analytical model. Figure 6.3A shows a fabricated 2DEG system where a 2DEG has holes cut into it. The holes create a channel where the channel width is smaller than the Fermi wavelength of the charges, thus confining the charges down from 2D to 1D. The charges then pass through in a completely ballistic manner, only experiencing scattering at the walls. If we follow a charge we can see that it begins in a reservoir, reservoir 1. The reservoirs are a source of orders of magnitude more charges when compared to the amount that pass through the point contacts. To go through the channel, the charge enters lead 1 and can do one of two things. It can either go through the lead, fly through the ballistic region and make it to lead 2 and reservoir 2 (Fig. 6.3A lower, a1). Or, it can be backscattered and end back up in reservoir 1 again (b1). The same thing can happen from reservoir 2 to 1. When a voltage is applied across the contact, the applied field will cause charges to flow in the direction of the field as it becomes more favorable to go from reservoir 1 to 2 or vice versa. Current can then be calculated by comparing all the values for a1, a2, b1, and b2 to get an overall transmission probability for charges going in either direction. Note that true LB formalism requires 1D transport and phase coherent charges. As discussed in the prior section, that is likely not the case for our system, so we only take motivation in using the LB formalism to describe our system, but do not take it to give rigorous quantitative values, merely qualitative comparisons.

That being said, if we look at Fig. 6.3B, our NW geometric diode system closely mimics

the ideal situation for the implementation of the LB formalism. Instead of a 1D contact, our neck is only nearly 1D (as discussed earlier), and our region near the neck is likely quasi-ballistic, and not perfectly ballistic (as discussed earlier in the discussion on MFP). Because our system is very close, we take motivation from the LB formalism to get qualitative comparisons for values of transmission probability for charges moving through our NW neck. In our situation, it is quite interesting to consider the difference in shape of the ballistic region in Fig. 6.3A and the shape of the quasi-ballistic region in 6.3B. Depending on exactly where the "ballistic region" is defined to start in 6.3B (which is going to be gradient, so it's really tough to say it starts anywhere exactly) the backscattered charges will have a much larger effect on amount of charges that make it from one side to the other.

When charges are flowing from left to right, they are injected into a region that has a shallow funnel to guide them to reservoir 2. However, when charges are moving from right to left, they mostly encounter a wall in which they will largely be backscattered. Indeed, it is the presence of these backscattered charges that we think leads to the asymmetry in our diodes.

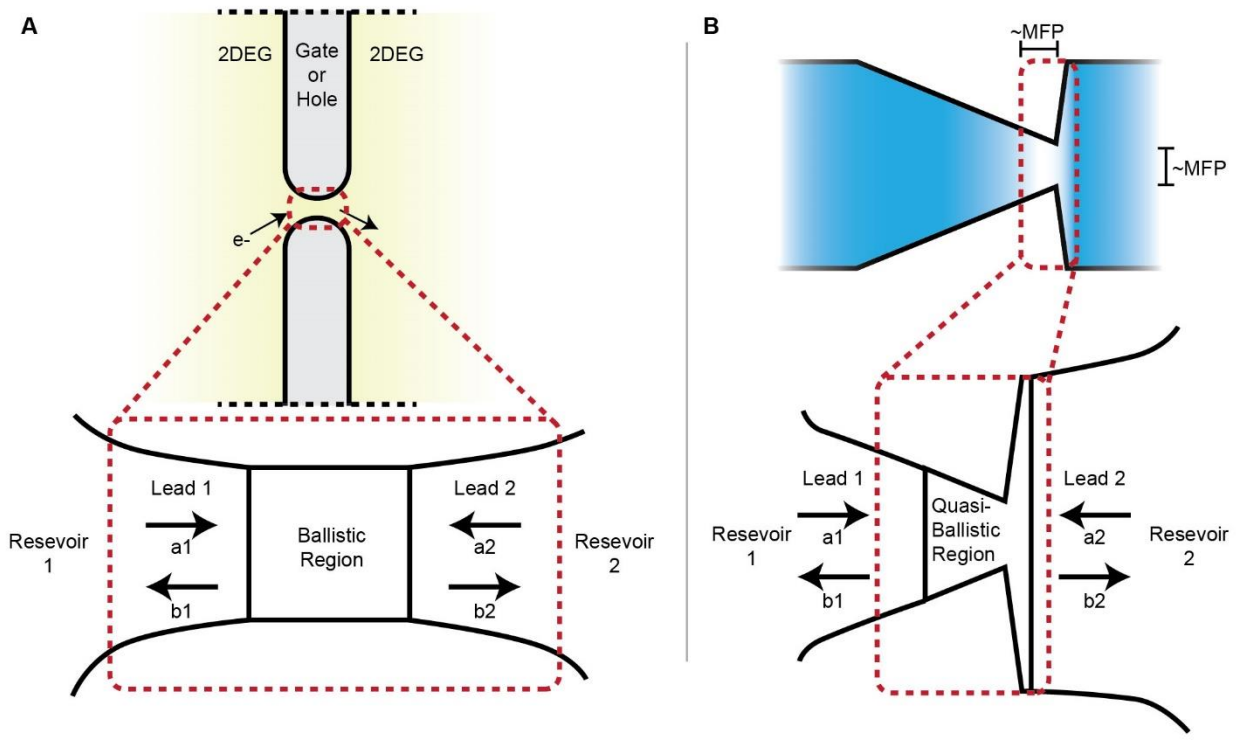

Figure 6.3: Landauer-Büttiker explaination. (**A**) (Upper) 2DEG (yellow) where a hole or gate has been placed (grey) to form a quantum point contact. The electrons are confined in two dimensions by the nature of the 2DEG, and then are confined to only 1D in the region within the red dashed-line rectangle because the hole creates a confinement that is less than the Fermi wavelength of the charges. (Lower) Zoom in on the rectangle in the upper figure. Current can flow from resovoir 1 through lead 1 to lead 2 and into resovoir 2 (a1) or vice versa (a2). Alternatively, they can be leave from lead 1 and be back-scattered and return to lead 1 (b1) and same for lead 2 (b2). To get through they must travel through the 1D ballistic region. (**B**) (Upper) NW geometric diode (blue and white) where the relative doping level is shown going from high doping (blue) to low doping (white). Similar to the 2DEG, electrons become more confined as they reach the red dashed-line rectangle because the geometry shrinks and the MFP increases. (Lower) Zoom in on the rectangle in the upper figure. Current can flow from resovoir 1 through lead 1 to lead 2 and into resovoir 2 (a1) or vice versa (a2). Alternatively, they can be leave from lead 1 and be back-scattered and return to lead 1 (b1) and same for lead 2 (b2). To get through they must travel through the 1D ballistic region.

6.2.2.2 Deep Description of the Analytical Model

Here is a more thorough description of the model. For qualitative comparison to experiment, the analytical model calculates the theoretical DC current asymmetry of a geometric diode by considering all possible trajectories that a ballistic charge carrier may take such that it

travels an axial distance equal to or less than the mean free path and passes through the NW constriction, undergoing zero, one, or multiple specular reflections at the NW surface depending on the trajectory. Fig. 6.4 shows examples of possible trajectories that undergo one (Fig. 6.4A) or two (Fig. 6.4B) surface reflections; however, arbitrary number of reflections are considered by the model. All possible trajectories are integrated, using an angular probability distribution function, $G(\alpha)$, to account for the effect of an electric field (see eq. S11 below), to find the fraction of trajectories that pass through the constriction. This quantity is represented as a probability, $P_{ij}^{m}(D,d,\theta,\varphi,\lambda,\sigma)$, for transmission ($i \rightarrow j$) of a charge carrier from the ratchet side (i = 1) to the constriction side (j = 2), or vice versa, under either forward bias (m = +) or reverse bias (m = –). The value of P_{ij}^{m} (see eq. 6.4) depends on the mean free path (λ), the NW geometry (D, d, θ, and φ), all of which are parameterized in the domain for each region of integration (D_s), and the angular probability distribution function as described by the parameter σ (see eq. 6.5). P_{ij}^{m} is calculated as:

$$P_{ij}^{m} = \frac{1}{M_{\mathrm{o}}} \sum_{s} \left(\iint_{D_{\mathrm{s}}} dz dr \left[2\pi r \int_{\alpha_{si}}^{\alpha_{sf}} G(\alpha) d\alpha \right] \right), \tag{6.4}$$

where M_{o} is the total number of trajectories, s is the index running over all integration regions of various types, D_{s} is the domain for each region of integration, α is the angle of the trajectory with respect to z, α_{si} and α_{sf} are the initial and final angles that successfully pass through the constriction for each integration region, $G(\alpha)$ is the angular distribution function, z is the spatial coordinate along the NW axis, r is the spatial coordinate along the NW radius (see Fig. 6.4C). The factor $2\pi r$ (with r internal to the NW geometry by reflection, as needed) accounts for the cylindrical symmetry of the NW, as illustrated in Fig. 6.4C.

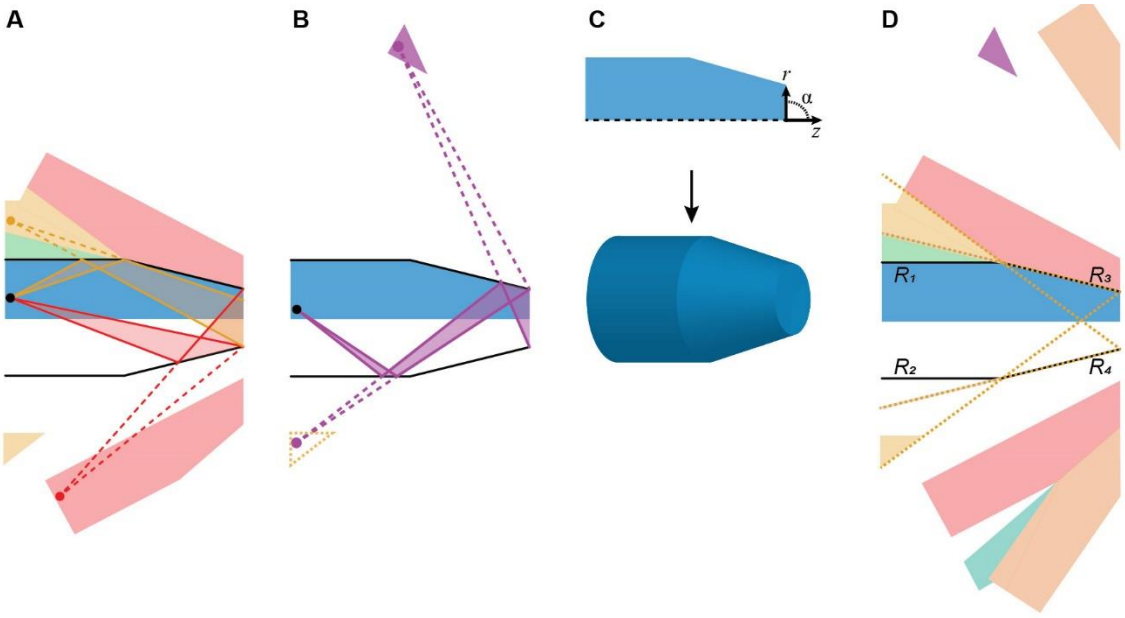

Figure 6.4: Full analytical geometric diode model. (**A**) Schematic representation of the integration regions (color-coded) and trajectories used to determine the transmission ratio δ. The black dot represents an example grid point used to begin trajectories. The red and yellow lines emanating from it demonstrate example single-reflection ballistic charge trajectories. These trajectories are calculated by the model to determine if a charge carrier would pass through the constriction. The blue region is the integration region associated with trajectories that do not reflect before passing through the constriction. All other colored sections correspond to a different type of integration region generated via reflection transformations and geometric constraints. The green region is from trajectories that reflect once off of the top uniform diameter section (and there is an additional one (not shown for conciseness) that reflects once off the bottom uniform diameter section). The red region is generated from reflections off either of the tapered sections. The yellow region is formed from trajectories near the vertex that do not span the full width of the constriction. (**B**) Example of a two-reflection trajectory as calculated by the model. The purple triangle outside of the NW is a region of integration constructed by consecutive reflection transformations. The dash-outlined yellow region is the single reflection region of integration that is reflected a second time to generate the purple region associated with the shown trajectories. (**C**) Representation of the 3D nature of the model achieved through rotational symmetry. In simulations of 3D geometric diodes, the integral can be simplified by utilizing cylindrical symmetry. Calculations can be done in 2D slices then rotated around the axis of the NW. (**D**) Representation of all integration regions associated with trajectories between 0 to 2 reflections. The dashed yellow lines indicate the geometric constraints that determine if trajectories are physically permissible, and are either partial, or full trajectories. R_1-R_4 correspond to the operators assigned to each linear segment of the NW surface.

The initial regions of integration, as shown in Fig. 6.4A, are determined by considering all potential trajectories that can pass through the constriction undergoing either no surface reflection or a single surface reflection. For trajectories that undergo a reflection, mirror plane

symmetries are used to convert all potential trajectories into linear trajectories that originate from regions of integration external to the NW geometry, but which can always be converted to internal integration regions upon reflection. The mirror symmetries are described using mirror plane operators, R_k, $k \in \{0,1,2,3,4\}$, where k = 1-4 correspond to linear surface segments of the NW geometry (see labels in Fig. 6.4D), and R_k applies a reflection transformation to an integration region. R_0 is the identity operator that corresponds to direct transmission through the constriction without reflection. Each integration region is also subject to geometric constraints to ensure that the associated trajectories are physically permissible. These constraints also divide the integration regions into those with trajectories that span the full width of the constriction ('full trajectories') and those with trajectories that span only a part of the constriction ('partial trajectories'). Fig. 6.4A shows the integration regions generated by a single R_k, and Fig. 6.4D displays the lines (yellow and black dashed) used to define the geometric constraints. The lines are formed by extending the tapered segments and by drawing a new line from either end of the constriction so that they intersect the opposite vertex where the uniform and tapered segments meet. In Fig. 6.4A, the green region contains single reflections off the upper uniform surface segment with full trajectories, the red regions are single reflections off the angled surface segments with full trajectories, and the yellow sections are single reflections off either the uniform sections or the angled sections with partial trajectories**.**

To account for more than one specular reflection, additional regions of integration are constructed by applying more than one reflection operator, R_k, to the initial internal regions of integration. Multiple operators may be applied in succession to generate linear trajectories that describe multiple reflections. Any integration region involving multiple reflections, derived using sequential reflection operators (*e.g.* $R_kR_{k'}$ for two reflections) is also subject to the physical

geometric constraints. Fig. 6.4D shows all the resulting integration regions for zero, one, and two reflections, although the model can account for arbitrary numbers. For each region of integration, the angular distribution that can pass through the constriction, as defined by α_{si} and α_{sf}, is calculated by drawing line segments from each spatial position to the upper and lower end points of the NW constriction and reflecting the resulting angles back to the internal geometry to define the angular limits. For integration regions with partial trajectories, the line segments are drawn not to the end points of the constriction but rather to the physically accessible end points along the NW constriction.

The effect of the high electric field within the ratchet, which substantially alters the momentum distribution of charge carriers to produce directed transport and nonlinear behavior, is accounted for using a Gaussian angular probability distribution function as:

$$G(\alpha) = \frac{\sqrt{2}}{\sqrt{\pi}\,\sigma\left(erf\left(\frac{\mu+\pi}{\sqrt{2}\sigma}\right) - erf\left(\frac{\mu-\pi}{\sqrt{2}\sigma}\right)\right)} exp\left[-\frac{(\alpha - \mu)^2}{2\sigma^2}\right], \tag{6.5}$$

where μ is the center of the distribution function (with $\mu = 0$ for all simulations, corresponding to a direction parallel to the *z*-axis), σ is the standard deviation of the distribution, and *erf* is the error function. The expression is normalized over the domain $-\pi$ to π, and the same probability distribution is used in the forward and reverse bias directions.

To simulate the DC current asymmetry, we take motivation from the Landauer-Büttiker (LB) formalism to qualitatively interpret the experimental DC current asymmetry in terms of the transmission of quasi-ballistic charge carriers through the constriction of the sawtooth geometry.[1,17] We emphasize that the LB formalism is merely motivation for a model that allows qualitative interpretation of experimental results, and the description herein is not meant as a replacement of a full-fledged model that would quantitatively describe the quasi-ballistic nature

of the charge carriers in the experimental system. In this formalism, the current through lead i can be expressed as:

$$\left(\frac{h}{2e}\right) I_i = (N_i - R_i)\mu_i - \sum_{j \neq i} T_{ji}\mu_j \quad , \tag{6.6}$$

where N_i is the number of propagating modes in lead i, R_i is the reflection coefficient for lead i, T_{ji} is the transmission coefficient from lead j to lead i (*i.e.* $j \rightarrow i$), and μ_i is the chemical potential at lead i. Normalization requires that

$$N_i = R_i + \sum_{j \neq i} T_{ij} \, . \tag{6.7}$$

In the case of the two-terminal NW geometric diode with current lead 1 at the beginning of the taper on the side of the ratchet and current lead 2 at the beginning of the taper on the side of the constriction, current conservation indicates that $I_1^m = -I_2^m$, where superscript m denotes forward bias (m = +) or reverse bias (m = –) and is needed because the high-electric field within the ratchet substantially alters the charge carrier momentum distribution, placing the system in a nonlinear regime. Using eqs. 6.6 and 6.7, the current through lead 1 can be expressed as:

$$I_1^m = \left(\frac{2e}{h}\right)\left(T_{12}^m \mu_1^m - T_{21}^m \mu_2^m\right). \tag{6.8}$$

The simulated DC current asymmetry, δ, can be expressed as the magnitude of the ratio of the current in forward and reverse bias in which lead 1 and lead 2 have the same chemical potential (*i.e.* $\mu_1^+ = \mu_2^-$) in forward and reverse bias, respectively. This condition corresponds to the experimentally measured ratio of forward and reverse bias current at the same magnitude of applied bias, $|V_{app}|$. Thus, δ can be expressed as:

$$\delta = -\frac{I_1^+}{I_1^-} = -\frac{\left(T_{12}^+\mu_1^+ - T_{21}^+\mu_2^+\right)}{\left(T_{12}^-\mu_1^- - T_{21}^-\mu_2^-\right)} \approx \frac{T_{12}^+\mu_1^+}{T_{21}^-\mu_2^-} = \frac{T_{12}^+}{T_{21}^-} \quad , \tag{6.9}$$

where the two right-hand expressions assume that $T_{12}^+ \gg T_{21}^+$ and $T_{21}^- \gg T_{12}^-$. These two assumptions should be valid in the highly non-linear regime produced with a high electric field within the ratchet geometry, which substantially alters the momentum distribution of the electrons to yield a vanishingly small transmission coefficient for the motion of electrons against the applied field.[22] Thus δ represents the ratio of transmission coefficients from forward and reverse bias. Moreover, a billiard ball model of ballistic electron motion,[1] as described by eq. 6.4, can be used to determine the transmission coefficients, where $T_{ij}^m = N_i P_{ij}^m$. Substituting $T_{12}^+ = N_1 P_{12}^+$ and $T_{21}^- = N_2 P_{21}^-$ into eq. 6.9, we arrive at the final expression for δ,

$$\delta = \frac{N_1 P_{12}^+}{N_2 P_{21}^-} = \frac{P_{12}^+}{P_{21}^-}. \tag{6.10}$$

For the two-terminal geometric diode, the number of propagating modes in leads 1 and 2 is necessarily the same (*i.e.* $N_1 = N_2$), leading to the simplified expression on the right-hand side of eq. 6.10. Thus, the ratio of probabilities in the forward and reverse direction (calculated by eq. 6.4) can be used to predict δ for qualitative comparison to experiment. It is therefore a valuable metric for understanding the geometric diode performance as a function of geometry.

The value of σ correlates to the applied voltage on the diode. A smaller σ correlates to higher voltages because it decreases the angular distribution of the charge carrier starting angles. A tighter angular distribution means they are pointed more down the axis of the geometry. Figs. 6.5A and B show plots of δ versus σ for two different NW geometries, demonstrating that the δ is strongly dependent both on σ and on the NW geometry. High values of δ can be predicted by this model depending on the exact distribution function and NW geometry.

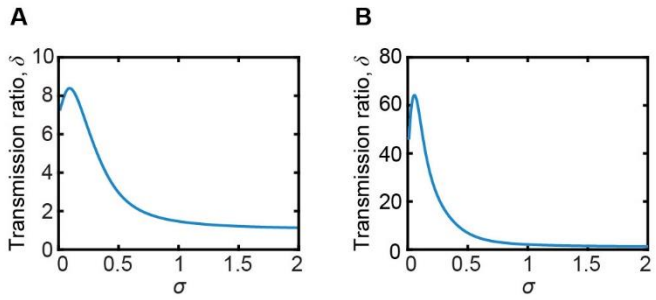

Figure 6.5: Transmission ratio δ from the analytical geometric diode model. (**A**, **B**) Plots of transmission ratio δ versus the standard deviation, σ, of the angular distribution function, G, used in the analytical model with a geometry of φ = 90°, d = 10 nm, and L = 400 nm (panel A) and geometry of φ = 90°, d = 1 nm, and L = 400 nm (panel B).

6.2.2.3 Analytical Model Results

Now let's examine how δ is affected by geometry and how those correlations compare to experiment. Figure 6.6A shows that as ratchet length is increased, δ is also increased, but only up to a certain point, and then δ plateaus. This is because as ratchet length increases, the funnel shape becomes increasingly like a tube. When L is very long, the charges are essentially traveling through a uniform tube, so increasing L has marginal returns on δ. It also shows that a smaller d leads to a higher possible δ. Figure 6.6B shows the dependence of δ on constriction length (l, the synonymous geometric parameter to ratchet length, but on the other side of the funnel). As constriction length (l) is shortened there is a higher possible δ that can be achieved. Similarly to L, it is not until very small values of l are realized that high values of δ can be achieved. This is essentially reverse of the L because high values of l lead to a tube geometry, and the smaller it gets, the closer φ gets to 90° (which is ideal). It is not until there is essentially a wall (very low l) on the constriction side that high values of δ are seen. Figure 6.6B also shows that as neck diameter, d, is decreased, the maximum values of δ are increased. However, looking at any individual parameter does not tell the whole story of what is happening with the geometric dependence. All of the geometric parameters affect each other.

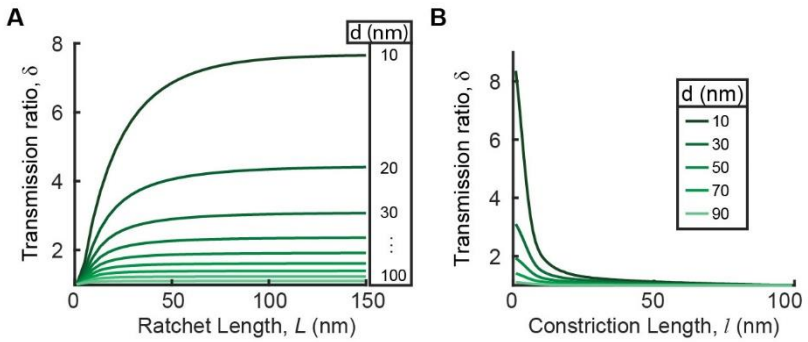

Figure 6.6: Analytical simulation geometric parameters. (**A**) Transmission ratio vs ratchet length, L¸ at different values of neck diameter, d. Outer diameter, D, is 100 nm. Constriction length (l) is 1 nm. (**B**) Transmission ratio vs constriction length (l, synonymous to ratchet length, but on the other side) at different values of neck diameter, d. Outer diameter, D, is 100 nm. Ratchet length is 100 nm.

As a method to combine geometric parameters (because they all affect each other anyway), the value of *f*-number (N) is examined, where $N = f/D$ and f is the effective focal length of the ratchet (Fig. 6.2) and $N = (2\tan(\theta))^{-1}$. N effectively combines the values of L, D and d. Then on the other side of the funnel, constriction angle, φ, is used to combine d, D, and l. Figure 6.7A displays δ for different values of φ at a fixed L as a function of N. For relatively large values of φ and N values above ~5, the model predicted that as N decreased, δ increased. For N below ~5, however, δ approached unity because d approached zero. The model also showed that δ depended strongly on the initial angular distribution, and substantially higher values could be achieved by varying this distribution (Fig. 6.5). Moreover, for a fixed N, decreasing φ decreased δ because a smaller φ corresponded to an increasingly symmetric sawtooth structure. In Fig. 6.7A, a standard deviation of 0.5 radians is used, as it approximates the expected momentum distribution when accounting for field effects. The trends for δ are in qualitative agreement with champion experimental devices that exhibited a trend of increasing DC asymmetry with decreasing N (Fig. 6.7B). More work is actively being done to improve this simulation. Namely to match it more closely to the LB formalism, add voltage dependence, have carriers inject just from a line instead of all of the area, add chemical potentials, and try to calculate reasonable

values for current.

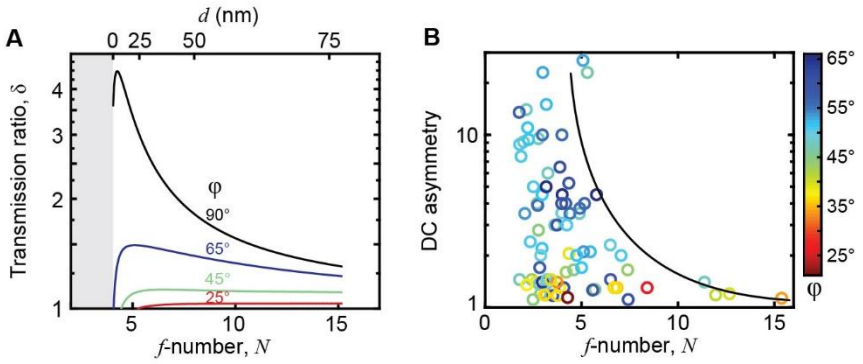

Figure 6.7: Transmission ratio vs *f*-number. (**A**) δ calculated as a function of *N* (lower axis) with *D* = 100 nm and *L* = 400 nm assuming φ of 90° (blue), 65° (green), 45° (orange), and 25° (red), where MFP is 0.3*D*. The *d* corresponding to values of *N* are shown on the upper axis. (**B**) *Reproduced from Fig. 4.5B for clarity in comparison* - Experimental values of DC asymmetry at $|V_{app}|$ = 1 V collected from 81 single-NW devices plotted as a function of *N*. Data points are color-coded according to the constriction angle φ. The black line is a guide to the eye.

6.2.3 Monte Carlo Modeling

Note that the Monte Carlo was largely built by Max Umantsev. Monte Carlo methods are a class of numerical techniques that rely on repeated random sampling within a probability distribution of possible inputs to solve conceptually deterministic problems. Due to their dependence on randomness, such methods require a large number of samples in order to produce reasonable approximations. A Monte Carlo simulation can be considered as a computational experiment with a number of variables which may not be feasibly obtained through physical experimentation. A typical algorithm randomly generates an input for each variable from its respective probability distribution over a predefined domain and outputs the result of a deterministic computation. Each variable repeatedly samples from its respective distribution until thousands of possible initial conditions have been simulated, which results in the probability of occurrence for different events.

In order to simulate carrier trajectories in the bulk of a semiconductor, a Monte Carlo method prescribed by Lundstrom in *Fundamentals of Carrier Transport*[3] has been adapted to our

geometric diodes. The prescription assumes room-temperature Si and considers four types of energy-dependent electron scattering processes: acoustic deformation potential (ADP) scattering, equivalent intervalley scattering by phonon absorption, equivalent intervalley scattering by phonon emission, and ionized impurity scattering. The total scattering rate, $\Gamma(p)$, is the sum of the rates due to these four mutually independent processes and, after repeatedly sampling from possible carrier trajectories, determines the average flight-time of a carrier between scattering events. Due to its dependence on carrier energy (which varies over time) the total scattering rate is actually also a function of time, $\Gamma(p(t))$. By approximating this function as a constant, Γ_0, and considering an additional, fictitious scattering type, known as *self-scattering*:

$$\Gamma_{self}(p) = \Gamma_0 - \Gamma(p), \ \Gamma_0 > \Gamma(p). \tag{6.11}$$

Where Γ_{self} is the self-scattering rate and Γ_0 is the constant total scattering rate. A single free flight and scattering event is simulated by generating four random numbers: r_1, r_2, r_3, r_4, where each number is selected from a uniform distribution from 0 to 1. First, r_1 is used in conjunction with Γ_0 to determine the free flight time until the next scattering event (real or self-scattering):

$$t_c = -\frac{1}{\Gamma_0} ln(r_1). \tag{6.12}$$

Where t_c is free flight time between scattering events. The free flight time is used to determine the carrier's position and momentum, in accordance with Newton's laws, just before the next scattering event.

The scattering type is identified by comparing r_2 to the partial sums of the fractional contributions of all *k+1* (there are *k* real scattering mechanisms, plus one self-scattering

mechanism) scattering mechanisms (in order of decreasing contribution) to the total scattering rate and selecting mechanism *j* if:

$$\frac{\Sigma_{i=1}^{j-1}\Gamma_i}{\Gamma_0} \leq r_2 < \frac{\Sigma_{i=1}^{j}\Gamma_i}{\Gamma_0}, \;\; j = 1,2,\ldots,k+1. \tag{6.13}$$

Where Γ_i is the i-th most likely scattering mechanism at a given energy. In our case the maximum number for k is 4 because of the 4 real scattering types. If the scattering type is self-scattering, the simulation determines a new free flight time and the carrier continues on its trajectory uninterrupted by any real scattering mechanisms. The final state after scattering is determined by the energy change associated with the scattering mechanism, assuming a spherical parabolic energy band:

$$p(t_c^+) = p' = \sqrt{2m^*[E(t_c^-) + \Delta E]}, \tag{6.14}$$

in conjunction with r_3 and r_4, which determine the orientation of the momentum vector after scattering. Where t_c^+ is the time the instant after a scattering event, t_c^- is the time the instant before a scattering event, ΔE is change in energy, and m^* is the effective mass of the carrier. By considering a rotated coordinate system where the primary coordinate (device/field axis) is directed along the initial momentum, the azimuthal angle β and the polar angle α are determined by:

$$\beta = 2\pi r_3 \quad \& \quad cos(\alpha) = 1 - 2r_4. \tag{6.15}$$

In the rotated coordinate system where the x-axis is pointing along the initial momentum, the momentum vector is:

$$p_r' = p' < cos(\alpha), sin(\alpha)cos(\beta), sin(\alpha)sin(\beta). \tag{6.16}$$

Where p_r' is the momentum after scattering in the rotated coordinate system. This process is repeated until statistical relevance is achieved.

As it stands, this model accounts for varying dopant concentrations when considering the scattering rate, but only at room temperature. The MFP is determined by considering a free carrier in the bulk of a semiconductor under no field. The trajectory is simply a straight line due to the lack of a field and boundaries, so the length of the free path between scattering events is simply the distance between two points in a 3D space. By considering the trajectory of one carrier after N scattering events, where N is sufficiently large, for a given doping level, the MFP is simply the average length of all free paths between scattering events for the trajectory. This MFP is later used to define the starting disk for carriers in an attempt to simulate only ballistic carriers.

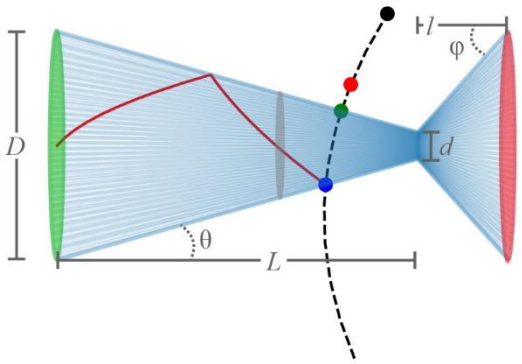

Figure 6.8: Monte Carlo Intro Schematic. 3D Schematic illustration of ballistic conduction through a geometry. Important geometric parameters are shown in grey. Green disk is where carriers begin. Red disk is where they end. The grey disk is an example of where a start disk could start if it does not start where the cone meets *D*. The blue lines are the 3D boundary. The red line is the previous path of the carrier. The blue dot is the current location of the carrier having just hit a wall. The black dotted line is the projected parabolic path from field driven transport. The green dot is where the carrier will reflect next. The red and black dots are possible solutions (scattering, end of free flight time) that are non-physical because they happen beyond the boundary.

To simulate a device we can introduce a non-zero field and boundaries. The field results in the line segments of a path becoming parabolic. For a given free flight time, a parabola is

generated for the carrier trajectory at that time, and the times of intersection with each cone and each plane are solved (Fig. 6.8); immediately, we can eliminate solutions that are imaginary, less than or equal to zero, or greater than the free flight time. Plugging in the remaining times in the equation for the parabola identifies all points of intersection with the geometry by eliminating points that are not on the device boundary (points on an end plane within the radial limits of the device are considered to be on the device boundary, however the trajectory is not reflected). If there are no remaining points, the carrier did not intersect the boundary at any point during its free flight time; otherwise, the point of intersection is that with the earliest time of intersection. By determining the point of intersection on the geometry, the normal to the surface is readily available and determines the momentum vector after reflection by subtracting from itself twice the projection of the momentum vector on the normal. A boundary intersection is considered probabilistically independent from a scattering event, so the new free flight time is the remaining free flight time after the intersection. This continues until the free flight time has been exhausted.

The relevant geometry for our geometric diodes is two intersecting cones (Fig. 6.8) that serve as boundaries for charge carriers. In this model, a trajectory is specularly reflected at the point of intersection with the boundary. With the trajectory between scattering events being a segment of a parabola in 3D space parametrized by time. At the end of each cone is a start disk and end disk that represent the degenerately doped sections. If a charge carrier makes it to the end disk or is back-reflected into the start disk it is treated like that charge is collected at a contact and that run is ended. The non-degenerately doped regions on either side of the constriction point of a geometric diode may each be considered as segments of (usually) different cones, determined by the length of the region and the radii of the constriction and the wire (Fig. 6.8).

In an attempt to mimic experiment and to more precisely study ballistic transport, MFP is calculated, and the start disk is placed at or within one MFP of the constriction. On the sawtooth side the start/end disk is placed at one MFP (even if that is not the location where the cone has the same diameter as the outer diameter, *D*) which should be close to where the doping transitions from non-degenerate to degenerate doping due to the nature of the exponential decay of the doping level in the sawtooth structures. On the constriction side, the start/end disk is placed at the end of the cone (where the cone diameter is D) because the constriction side is much shorter and should ideally be a wall. At these length scales specular reflections off of the wall should dominate the real scattering mechanisms. Because the length scales are so small within one MFP, turning the field on or off has minimal effect on the charge carrier flight, and in turn the results of the model. Therefore, for the model as of now, we will only present work that has start/end disks within one MFP of the constriction and has field turned off. Note that there are still field effects in the form of initial charge carrier direction and velocity, field effects are just turned off once the carrier has entered the geometry.

6.2.3.1 Monte Carlo Results

Results are collected similarly to the analytical model. A large number of charges are assigned random start positions on the start disk and then sent through the geometry. The amount of charges that make it to the end disk vs the amount that are back reflected is calculated as a transmission probability (TP) for that carrier traveling in that direction in that geometry. Then the start disk, end disk, and direction of initial momentum (dictated by the field direction) are flipped and that TP is calculated. The ratio of these TPs is calculated as a corollary to experimental DC current asymmetry.

Different combinations of geometric parameters were modeled to understand the geometric dependence of the transport behavior that produces asymmetry as expressed by the ratio of TP. TP ratio and δ in the analytical model are ostensibly the same, but different names are used for clarity. To explore the effects of geometry on the ratio of TP, one geometric parameter could be varied while the rest of the structure is held constant. Sweeping through a range of values for one parameter could allow for comparison of the resulting ratios of TP. However, this would not fully capture the geometric dependence because there is strong independence among certain parameters. Instead, values for multiple parameters were swept over, and heatmaps were used to create a more complete and accurate picture of the geometry (Fig. 6.9 and 6.10). To mimic ballistic systems, the start disk position is set equal to or less than one MFP of the constriction, and simulations were run with no electric field after the carrier is injected. Instead the electric field manifests itself in the initial injection velocity and angular distribution of the carriers.

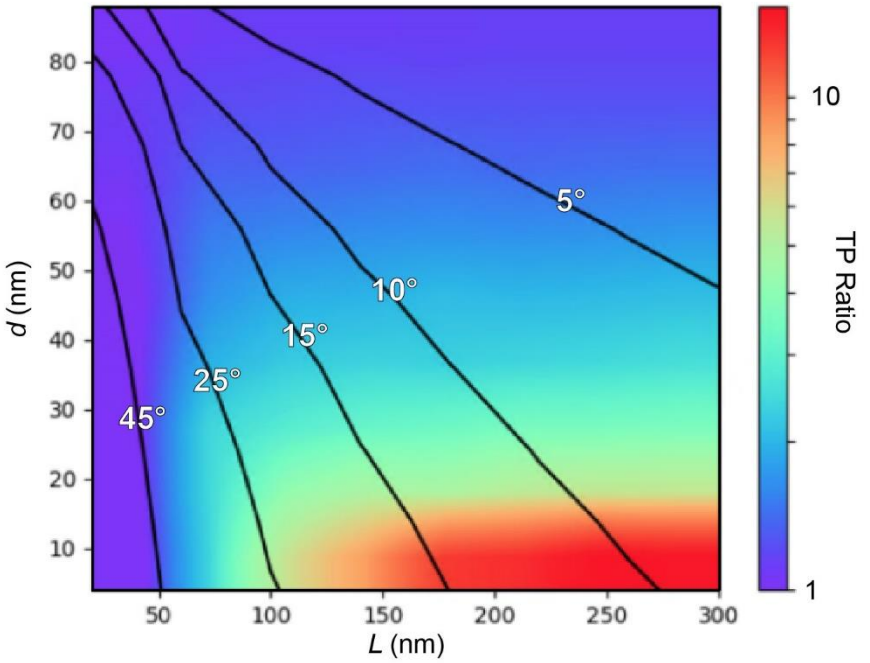

Figure 6.9: Simulated Ratio of TP vs ratchet side geometry. Heat map of ratio of TP for a geometric diode structure with varying *d* and *L* for fixed *D* = 100 nm and *l* = 3 nm. The start/end

disk on the ratchet side is fixed at one MFP from the constriction, and the start/end disk on the constriction side is fixed at *l*. Black contour lines are θ. Electric field within the geometry is turned off.

Figure 6.9 displays a heat map of the simulated ratio of TP on the parameters *d* and *L* with θ contour lines where θ is a combination of important parameters as shown by $\theta = \tan^{-1}(D-d/2L)$ (*D* and *l* are fixed at 100 nm and 3 nm respectively). Sweeping over values for *d* and *L*, the interdependence of the parameters and the ratio of TP is observed. Looking at larger values of *L* around 250 nm, as *d* decreases the ratio of TP starts at 1 and increases by more than an order of magnitude as carriers are being more effectively funneled in one direction and blocked in the other. However, at smaller values of *L* around 25 nm, the ratio of TP is similar for all values of *d* because the geometry is nearing a symmetric "bowtie" shape. At smaller values of *d* around 10 nm, as *L* increases the ratio of TP similarly starts at 1 and increases by over an order of magnitude. Because *d* is fixed, this is caused by a ratchet side that is becoming shallower and nearing resemblance of a tube while the constriction side still looks like a wall with a small aperture in it. The ratio of TP plateaus as *L* increases though because lengthening *L* has a diminishing effect on making the funnel of the ratchet side more shallow. However, at higher values of *d* around 80 nm, the ratio of TP is again around 1 for all values of *L* because *d* is not small enough to have a considerable effect on asymmetry in transport of carriers. In general, the ratio of TP increases as values of *L* increase and *d* decrease simultaneously. The heatmap highlights this interdependence of the effect of *d* and *L* on the ratio of TP. Together the *d* and *L* parameters contribute to the angle θ of the structure on the ratchet side. Following the same trend as *L* increases at smaller values of *d* around 10 nm, the ratio of TP increases as θ decreases. Following any θ contour line from top to bottom, as *d* decreases and *L* increases, the ratio of TP increases. Physically, this increase in the ratio of TP can be mostly explained by the direction in

which carriers traveling straight down the wire axis are reflected when they hit the structure. For carriers traveling straight down the wire axis, θ greater than 45° cause carriers to be retro-reflected back to the start disk. Conversely, as angles become smaller than 45°, carriers are more likely to be reflected forwards towards the constriction. The carriers are then more likely to go through the constriction and reach the end disk, thus increasing the ratio of TP. However, this trend is only applicable when the constriction is small enough to also block most of the carriers on the constriction side of the structure.

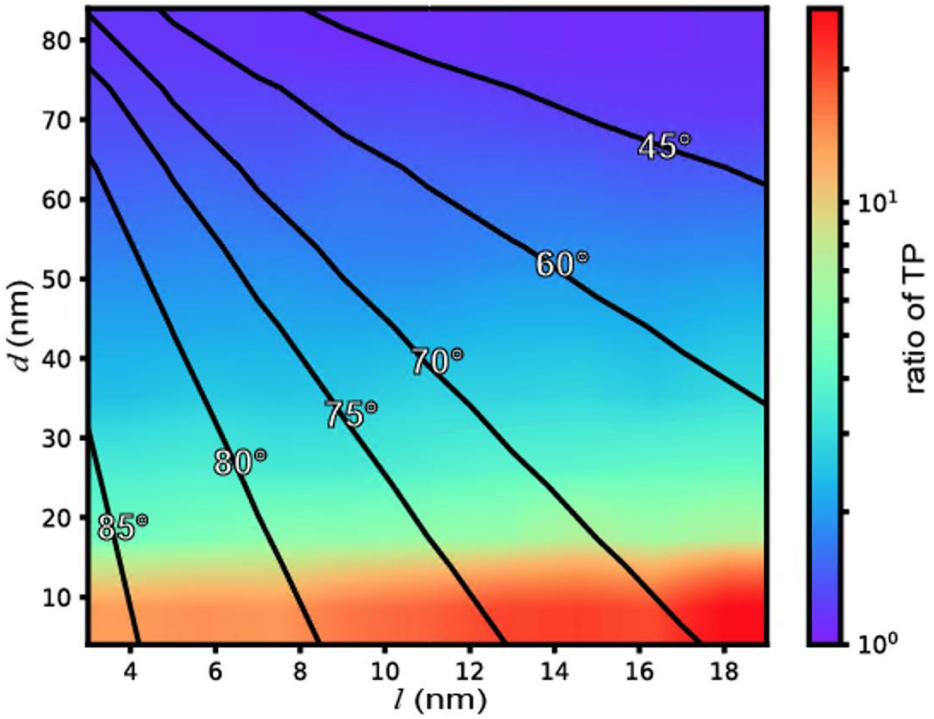

Figure 6.10: Simulated Ratio of TP vs constriction side geometry. Heat map of the ratio of TP for a geometric diode structure with varying *d* and *l* for fixed *D* = 100 nm and *L* = 200 nm. The start/end disk on the constriction side changes with *l* within one MFP from the constriction, and the start/end disk on the ratchet side is fixed at one MFP from the constriction. Black contour lines are φ where $\varphi = \tan^{-1}(D\text{-}d/2l)$. Electric field within the geometry is turned off.

Figure 6.10 displays a heat map of the simulated ratio of TP on the parameters *d* and *l* with φ contour lines where φ is a combination of important parameters as shown by $\varphi = \tan^{-1}(D\text{-}d/2l)$ (*D* and *L* are fixed at 100 nm and 200 nm respectively). Sweeping over values for *d* and *l*,

the interdependence of the parameters and the ratio of TP is observed. At all values of *l*, the ratio of TP increases as *d* decreases because the shrinking constriction becomes more effective at blocking carriers approaching on the constriction side. For larger values of d, greater than 20 nm, the ratio of TP is similar for all values of *l* because the constriction is large enough that the distance from which the carrier is injected will not have an effect on its transmission probability. However, for smaller values of *d*, less than 20 nm, the ratio of TP increases as *l* increases because the constriction is small enough such that only carriers injected in perfect alignment with the constriction are likely to be transmitted. As the precision of the carrier position becomes more important to the transmission probability at these smaller constriction sizes, the distance from which the carrier is injected has more effect on the ratio of TP. Larger *l* values correspond to carriers injected farther from the constriction, providing the carrier a greater distance over which to possibly scatter out of alignment, thus decreasing the transmission probability on the constriction side and increasing the ratio of TP. Despite these systems being deemed ballistic because the geometries are less than or equal to the MFP, MFP is still an average value, not a hard cut-off for the observation of scattering events. Therefore, there is still a non-zero probability of scattering. This dependence on scattering is the source of the difference in geometric effects of *l* on the ratio of TP between the Monte Carlo and analytical simulations. In general, the ratio of TP increases as values of *l* increase and *d* decrease simultaneously. The heatmap highlights this interdependence of the effect of *d* and *l* on the ratio of TP. Together the *d* and *l* parameters contribute to the angle φ of the structure on the constriction side. Following the same trend as *l* increasing at values of *d* smaller than 15 nm, the ratio of TP increases as φ approaches 45°. Physically, this increase in the ratio of TP can be mostly explained by the direction in which carriers traveling straight down the wire axis are reflected when they hit the

structure. For carriers traveling straight down the wire axis, φ smaller than 45° cause carriers to be reflected forwards towards the constriction. Conversely, as angles become larger than 45°, carriers are more likely to be retro-reflected back to the start disk. The carriers injected on the constriction side are then more likely to be reflected away from the constriction and return to the start disk, thus increasing the ratio of TP. However, this trend is only applicable when the constriction is small enough to also block most of the carriers on the constriction side of the structure. While this conclusion may seem counterintuitive because the analytical simulation shows that a φ of 90° results in the greatest ratio of TP, it is important to consider that carriers injected further from the constriction have more time to scatter off axis. Therefore, larger *l* values within one MFP of the constriction that contribute φ angles closer to 45° produce the greatest ratios of TP. Work on the Monte Carlo model is ongoing.

6.3 Conclusion

We've shown that finite-element modeling is an effective method to describe the electrostatics within the geometric diode. However, because Comsol cannot account for the ballistic nature of the carriers, it cannot currently predict the current asymmetry seen in experimental devices. It does show that the degenerate sections of the NWs can act as electron reservoirs that inject charges into a small ballistic region around the constriction.

Taking motivation from the LB formalism, an analytical model was created to account only for the ballistic nature of the charge carriers. The model uses the probability of carriers making it through the aperture from one side or the other to create a transmission ratio that can be compared to experimental DC current asymmetry. The predictions of geometric dependence on transmission ratio from the model align with the geometric dependence of DC current

asymmetry in experiment when surface treatments are not considered. More work is being done on the analytical model to map it more closely to the LB formalism.

To further confirm the ballistic nature of the charge carriers, a Monte Carlo model was built to model charge carrier movement while also being able to consider scattering events and more semiconductor physics. The model sends charges through different geometric diode geometries and measures their transmission probability. The model was adapted to also take motivation from the LB formalism. When the ratio of these TPs are compared to the analytical model and experiment there is excellent agreement, except for the nature of the constriction side. Modeling and deeper understanding of devices physics serve to further confirm the ballistic or quasi-ballistic nature of the charge carriers in the experimental system. More work is currently being done on understanding the MFP, temperature, and fields effects on the model.

CHAPTER 7: CONCLUSIONS

Room-temperature electron ratchets can be formed when a structure has asymmetry that is near the MFP of a charge carrier. These electron ratchets asymmetrically manipulate the flow of ballistic charge carriers to form a diode, a "geometric" diode. Geometric diodes use their shape to manipulate their electronic properties and create their diode behavior. Here we demonstrated the formation of 3D geometric diodes formed from Si NWs that are able to operate at room temperature.

First we studied the growth of the NWs using a computer-controlled CVD system. The ENGRAVE method was used to encode dopants, and then shape NWs with sub-10 nm precision. These precisely tuned NW geometries were used to form funnel, or sawtooth shapes to act as geometric diodes. These sawtooth shapes were made in various different geometries, with different surface coatings, and in both *n*- and *p*-type Si. The wet-chemical etch process to shape the wires is the most unreliable step in it's current form. Efforts should be made to improve the process, like creating a flow cell etching system to hopefully increase reproducibility.

To study how all of these different geometries and fabrication methods affect the electron ratcheting and diode behavior, the NWs were measured under DC voltage. DC current asymmetry at 1 V was used as a metric to define how "good" a specific diode was. It was shown that generally as *f*-number decreased (neck diameter decreased, and ratchet length increased) asymmetry went up, but this trend was distorted likely by non-ideal etching and impurities. When a native oxide is allowed to fully form, or the wire is coated in alumina the asymmetry increases dramatically (up to ~1600). All data mentioned is for *n*-type wires, but a small number

of *p*-type wires were created to compare and their asymmetry was quite high (~100's) despite holes having a larger effective mass. More work should be put in to understand the nature of the surface of the nanowires and their doping level and how they contribute to diode performance. This could include gating the surface using a metal oxide gate[93] or using a liquid ion gate.[94,95]

To further confirm the electron ratcheting effect within the geometric diodes, their behavior under AC was measured. Broadband AC rectification was measured up to 40 GHz. Measurement of higher frequencies was limited by instrumentation. The theoretical frequency response is ~1 THz based on the flight time of the carriers through the ballistic region. There were attempts to measure higher frequencies using free-space measurements at 28 THz and 600 GHz, but initial testing from both did not show rectification. However, there are many improvements which can be done to both measurements to conduct a better test. Additionally our collaborators have a free-space signal source at 94 GHz that could be used to measure the response of the wires. The demonstrations of high-speed rectification does show that geometric diodes could be used as ultra-fast signal processors, long wavelength energy harvesters, or THz sensors.[33,34,45,46,96] They could also potentially be used as both in a rectenna setup.[35,79,97,98] An interesting example of a unique device that could be made with the NW geometric diodes would be an all-in-one full-wave rectifier (Fig. 7.1).[22,99] In this setup the diodes can be used to generate power from both sides of the AC signal, so energy harvesting can theoretically be around 90% if all other things are optimized (which admittedly has a long way to go).

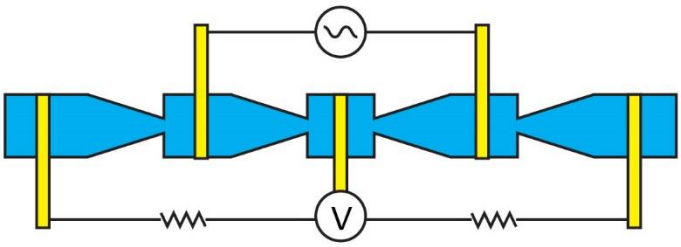

Figure 7.1: NW full wave rectifier schematic. Schematic of a full wave rectifier made from NW geometric diodes. The blue is the NW and the yellow are the metal contacts. Two diodes point right and then two diodes point left. Voltage is measured in the middle across loads that go to the ends. The AC signal is applied in-between each set of diodes facing the same direction.

Modeling the NW systems offered a deeper understanding of the complex physics at play. Finite-element modeling was used to examine the electrostatics of the device, but it neglected the potential for ballistic behavior of charges and therefore was unable to accurately predict the experimental current asymmetry. It was able to show that the degenerate sections of the NW could potentially act as charge reservoirs to inject carriers into a quasi-ballistic region around the constriction. Because of this an analytical model was built to simulate how ballistic particles move through a given geometry. This model was able to create ratios of transmission probabilities that nicely mapped onto experimental values of DC current asymmetry at a given geometry. In addition, a Monte Carlo model was built that works similarly to the analytical model, but includes more device physics like scattering events. This model also agrees with the analytical model (except for the nature of the constriction because of scattering) and experiment further confirming the quasi-ballistic nature of the charge carriers in the NW geometric diodes. However, more work needs to be done on both the analytical and Monte Carlo models to align them more closely with the underlying physics.

Si NW geometric diodes made from the ENGRAVE process offer an unpredicted level of control for ballistic geometric diode systems. They offer a unique way to study ballistic systems operating at room-temperature that allow us to gain deeper understanding of ballistic charge

carriers, which will become increasingly important as our technology shrinks further down into the nanoscale. More work should also be done with these devices at low-temperatures, possibly down to mK levels to study their potential quantum nature.[4,67] Finally, as a potential method to scale these devices up, an array of "geometric diode nubs" (Fig 7.2) could be created. Short Si NWs would be grown in an array defined by lithography on a conductive substrate. On the growth substrate, the Au catalyst would be etched away and then the NW would be etched to reveal the sawtooth structure. Then insulator could be deposited and the tip of the insulator could be etched away by possibly using a polymer resist. Then a degenerately doped semiconductor shell could coated over the whole thing. This method could be more useful in an industrial setting because it removes the e-beam lithography and more easily facilitates the creation of a pixel array for something like a THz sensor.

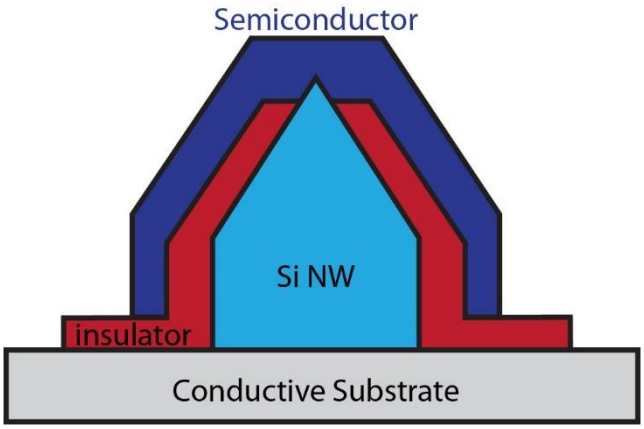

Figure 7.2: Nub geometric diodes. Schematic of a nanonub geometric diode that could be a more industrially friendly fabrication method. Si NW in light blue on a conductive substrate (grey). Insulator (red), deposited degenerate semiconductor (dark blue).

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