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Published in:
2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)

DOI (link to publication from Publisher):
10.23919/IPEC-Himeji2022-ECCE53331.2022.9807242

Publication date:
2022

Document Version
Publisher's PDF, also known as Version of record

Passivity-Based Design for High-Order Harmonic Voltage Emulation of Grid Emulators

Zejie Li*, Fangzhou Zhao, Xiongfei Wang
Department of Energy, Aalborg University, Aalborg, Denmark
*E-mail: zl@energy.aau.dk

***Abstract*— The high-order (i.e., 50th~ 100th) harmonic voltage emulation is increasingly required for future grid emulators. To mitigate adverse control interactions between grid emulator and converter under test, this paper proposes a passivity-based design method for the harmonic resonant controllers of grid emulators. This method selects the phase compensation angles of resonant controllers based on the theory of constrained piecewise linear fitting. Compared to conventional passivity-based design, the proposed method avoids complicated mathematical derivations and achieves precise harmonic voltage control with the passive harmonic impedance till the critical frequency of voltage control loop. The effectiveness of the proposed method is validated by experimental results.**

Keywords*— Harmonic emulation, passivity-based design, compensation angle, constrained piecewise linear fitting

I. INTRODUCTION

Harmonic voltage generation is a crucial functionality of grid emulators to analyze the impact of background harmonics in realistic grids on the performance of device under test (DUT). Currently, typical grid emulators can generate 2nd~50th harmonics [1]. However, the increasing use of wide-bandgap power devices tends to inject higher-order (beyond 50th) harmonics into power grids. Consequently, higher-order (i.e., 50th~100th) harmonic voltage emulation is to be required for future converter-based grid emulators [2].

The resonant controller has been commonly used for selective harmonic voltage/current control of inverters [3], [4]. Numerous research works have been reported on the design of harmonic resonant controllers. A major issue of the higher-order harmonic resonant controller is the phase lag caused by the time delay of digital control system, which poses two important challenges: 1) the inaccurate control of harmonics with steady-state errors [5]-[8], and 2) the negative harmonic resistance at the output of inverter, which may destabilize the interconnected electrical system [9], [10].

To counteract the phase lag at the harmonic frequency, the phase compensation angles (CAs) are commonly used with the harmonic resonant controllers. Several methods of designing CAs have been reported, yet most of them are directly based on the time delay of digital control system ignoring the uncertainties of loads or power grids [5]-[8]. These methods have been proven effective to mitigate the steady-state tracking error, yet they can still give rise to a negative harmonic resistance at the inverter output [9].

To avoid introducing negative harmonic resistance, the frequency-domain passivity theory is used to design the CAs of harmonic resonant controllers [9], [10]. Although a closed-form analytical solution of CAs is developed in [9], [10], the mathematical derivation is complicated.

This paper proposes an alternative passivity-based design method of resonant controllers for grid emulators. The approach not only avoids complicated mathematical derivations but realizes also passive harmonic impedance till the critical frequency of voltage control loop, i.e., $1/(4T_D)$, where T_D denotes the time delay of control loop. Experimental tests are conducted to verify the correctness of the presented method.

II. SYSTEM DESCRIPTION

A. Control Scheme and Time-Delay Indentification

Fig. 1 illustrates the general diagram of a grid emulator connected with a DUT, where u_o and i_o are the phase voltage and current at the point of common coupling (PCC), respectively. A L filter (L_s) instead of LC filter enables to widen bandwidth of voltage control to emulate higher harmonics. The anti-aliasing low-pass filter (LPF) is utilized to mitigate high-frequency noise. In particular, the DUT is the grid-following based wind turbine system.

The single-loop voltage control with active damping (AD) in $\alpha\beta$-frame is used for the grid emulator [11], as shown in Fig. 2, where R_{cf} is AD realized by the current feedforward control. The AD is adopted to enhance disturbance rejection and mitigate the medium-frequency negative resistance, similar to the single-loop voltage-controlled inverter with the LC filter [12].

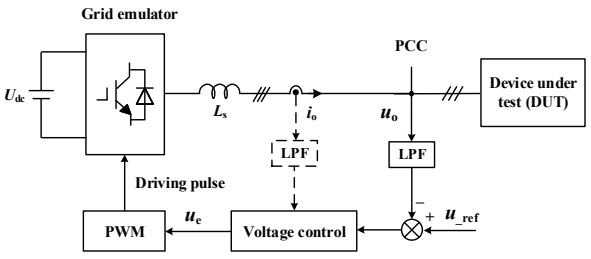


Fig. 1. General diagram of the grid emulation system.

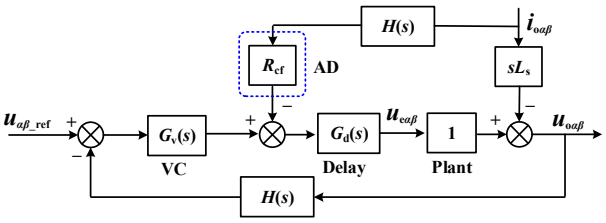


Fig. 2. Control diagram of the single-loop voltage control with AD.

$H(s)$ denotes the LPF, which is expressed as

$$H(s)=\frac{1}{1+T_{\mathrm{LPF}}s}\approx e^{-sT_{\mathrm{LPF}}} \tag{1}$$

where T_{LPF} is the time constant of the LPF, which is equivalent as a delay link.

$G_{\mathrm{d}}(s)$ represents the time delay link of digital control system, which is given by

$$G_{\mathrm{d}}(s)=e^{-sT_{\mathrm{d}}} \tag{2}$$

where the time delay T_{d} consists of computation delay, PWM delay and communication delay.

$G_{\mathrm{v}}(s)$ is the voltage controller (VC) including the fundamental and resonant controllers, which is given by

$$G_{\mathrm{v}}(s)=\frac{K_{\mathrm{r1}}s}{s^2+\omega_1^2}+\sum_{h=3,5,7,\cdots}\frac{K_{\mathrm{rh}}\left(s\cos\varphi_h-h\omega_1\sin\varphi_h\right)}{s^2+\left(h\omega_1\right)^2} \tag{3}$$

where the fundamental angular frequency ω_1 is equal to $2\pi f_1$. f_1 is the emulated fundamental frequency. φ_h denotes the phase-lead compensation angle (CA). Conventional design of φ_h is expressed as [9]

$$\varphi_h=h\omega_1T_{\mathrm{D}}=N_{\mathrm{c}}h\omega_1T_{\mathrm{sa}},\quad T_{\mathrm{D}}\approx T_{\mathrm{d}}+T_{\mathrm{LPF}} \tag{4}$$

where T_{D} is the total time delay. T_{sa} is the sampling period. N_{c} is the compensation coefficient.

It is therefore necessary to identify firstly the sampling frequency and time delay for the high-order harmonic emulation. According to technical specifications of typical grid emulators (e.g., Chroma 61845 and ACS6000 based grid emulator), the AC800PEC controller adopts a 50 kHz sampling frequency for 3 kHz harmonic generation to reduce harmonic accuracy loss [13]. Therefore, considering cost, the sampling frequency of grid emulator for future 100th harmonic emulation is selected as 60 kHz. It is assumed that the communication delay in the grid simulator is same to that of AC800PEC controller, i.e., 50 μs [14]. The cutoff frequency of the LPF is 15 kHz to filter out high-frequency noise such that T_{LPF} is 10.6 μs. Besides communication delay and T_{LPF}, the computation delay is one sampling period T_{sa} and the PWM delay is half of the sampling period $0.5T_{\mathrm{sa}}$ [15]. Therefore, the total time delay is given by

$$T_{\mathrm{D}}\approx T_{\mathrm{d}}+T_{\mathrm{LPF}}=85.6\ \mu\mathrm{s}\approx 5T_{\mathrm{sa}} \tag{5}$$

B. Parameter Tuning of Active Damping

According to Fig. 2, the output impedance of grid emulator is derived as

$$Z_{\mathrm{GE}}(s)=\frac{sL_{\mathrm{s}}+R_{\mathrm{cf}}G_{\mathrm{d}}(s)H(s)}{1+G_{\mathrm{v}}(s)G_{\mathrm{d}}(s)H(s)} \tag{6}$$

Since the harmonic resonator only affects the behavior

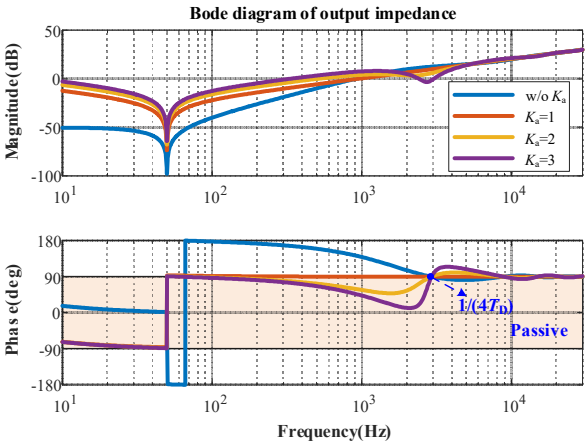


Fig. 3. Bode diagram of output impedance under various K_{a}.

of output impedance near harmonic frequency point [16], the sign of real part of the output impedance, without considering harmonic resonant controllers, is given by

$$\mathrm{sgn}\left\{\mathrm{Re}\left\{Z_{\mathrm{GE}}(j\omega)\right\}\right\}=\mathrm{sgn}\left\{\left(R_{\mathrm{cf}}+\frac{\omega^2L_{\mathrm{s}}K_{\mathrm{r1}}}{\omega_1^2-\omega^2}\right)\cos\left(\omega T_{\mathrm{D}}\right)\right\} \tag{7}$$

To guarantee the passivity of output impedance, R_{cf} should satisfy

$$R_{\mathrm{cf}}\geq\frac{\left(\pi/\left(2T_{\mathrm{D}}\right)\right)^2L_{\mathrm{s}}K_{\mathrm{r1}}}{\left(\pi/\left(2T_{\mathrm{D}}\right)\right)^2-\omega_1^2}\approx L_{\mathrm{s}}K_{\mathrm{r1}}K_{\mathrm{a}},\ K_{\mathrm{a}}\geq 1 \tag{8}$$

System parameters are shown in Table I. Fig. 3 shows the bode diagram of output impedance for grid emulator under various K_{a}, where K_{r1} is 5000 to guarantee control bandwidth of VC is not less than 1 kHz. A trade-off exists between provided the positive resistance before critical frequency $1/(4T_{\mathrm{D}})$ and introduced the negative resistance after $1/(4T_{\mathrm{D}})$. Hence, tuning K_{a} as 2.5.

III. Passivity-Based Design of Harmonic Resonant Controllers

In this section, the problem of conventional CAs ($h\omega_1T_{\mathrm{D}}$) of resonant controllers for high-order harmonic emulation is identified. A modified harmonic impedance passivity metric and the theory of constrained piecewise linear fitting are presented to design proper CAs.

A. Conventional Design Method

The single-frequency harmonic emulation is first considered. K_{rh} is selected as $0.1K_{\mathrm{r1}}$ to guarantee a short settling time of the harmonic emulation. According to (3) and (4), the harmonic impedance passivity is primarily affected by the compensation coefficient N_{c}. Since the time delay is $T_{\mathrm{D}}=5T_{\mathrm{sa}}$, N_{c} is 5 as the conventional design of CAs. Fig. 4 shows the bode diagram of output impedance with $N_{\mathrm{c}}=5$. Through the harmonic-order traversal from 3rd to 99th, it is found that the CAs are not sufficient to compensate phase lag caused by time delay and harmonic impedance passivity is not guaranteed when the harmonic order h is larger than 23rd.

Accordingly, the over-compensation angles (e.g., $N_{\mathrm{c}}=8$) are used and the bode diagram of output impedance is shown in Fig. 5. The over-compensation N_{c} enhances

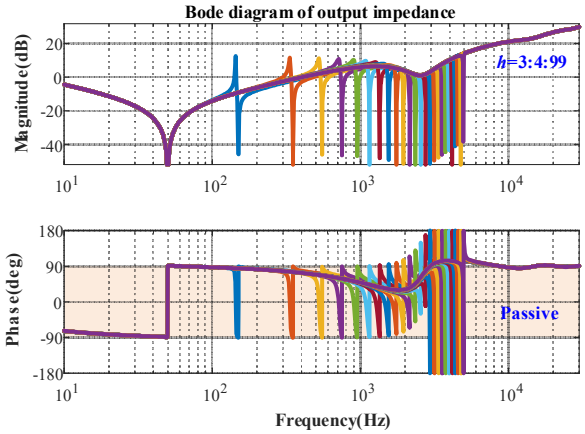


Fig. 4. Bode diagram of output impedance (N_c=5).

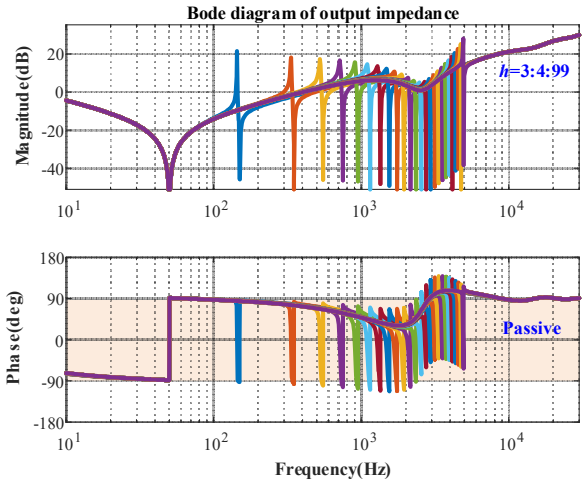


Fig. 5. Bode diagram of output impedance (N_c=8).

high-frequency harmonic impedance passivity but leads to the capacitive-negative resistance before critical frequency $1/(4T_D)$. Therefore, selecting a proper CA is crucial for the high-order harmonic emulation.

B. Modified Harmonic Impedance Passivity Metric

The frequency-domain output impedance of grid emulator can be expressed as

$$Z_{GE}(j\omega) = M_z\cos(\theta) + jM_z\sin(\theta) \tag{9}$$

where M_z and θ are the magnitude and the phase response of output impedance, respectively.

The output impedance magnitude M_z at each harmonic frequency is relatively small but larger than zero. Thus, $\cos(\theta)$ is adopted to represent the passivity behavior and $\sin(\theta)$ is used to denote the performance of inductive and capacitive impedance, as shown in Fig. 6. According to the impedance-based stability analysis, it is defined that the harmonic impedance non-passive region (NPR) represents the possible instability-frequency range. Obviously, $\cos(\theta)>0$ denotes NPR=0.

C. Proposed Design Method

From Fig. 5 and Fig. 6, it is clear that the harmonic non-passivity problem after critical frequency $1/(4T_D)$ is inevitable since an inductive-negative resistance is caused by time delay. Moreover, the grid-following based DUT usually shows the low-frequency capacitive and

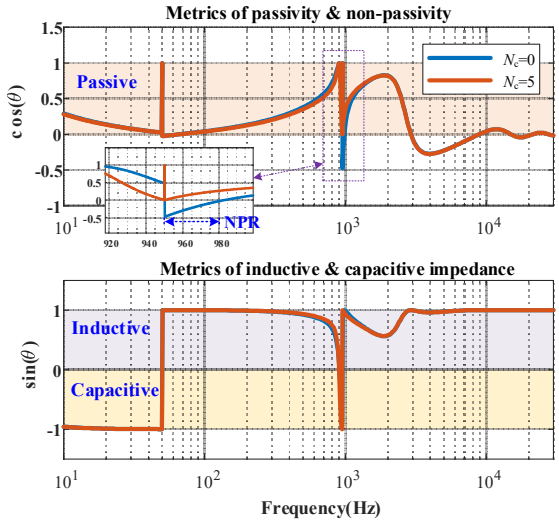


Fig. 6. Metrics of passivity and impedance behavior.

high-frequency resistance-inductive impedance [16]. Hence, according to the impedance-based stability analysis, the grid emulator should guarantee the harmonic impedance passivity ($\cos(\theta)>0$) before critical frequency and have no high-frequency capacitive impedance with negative resistance ($\cos(\theta)<0$, $\sin(\theta)>0$) beyond the critical frequency.

Fig. 7 shows the impact of compensation coefficient N_c for 99th harmonic emulation on the established metrics. There have been uncertain values of $\cos(\theta)$ and $\sin(\theta)$ at each harmonic frequency point. Hence, before and after harmonic frequency, two piecewise constraints for harmonic impedance passivity are defined as

$$\cos(\theta_{hp}) = \cos(\theta_{hf_1+f_k}) > 0 \quad (h < h_c) \tag{10}$$

$$\begin{cases} \cos(\theta_{hn}) = \cos(\theta_{hf_1-f_k}) > 0 \\ \cos(\theta_{hp}) = \cos(\theta_{hf_1+f_k}) > -D_{max} \end{cases} \quad (h > h_c) \tag{11}$$

where f_k is 0.5~1 Hz to ensure the accuracy of harmonic impedance passivity. h_c is the critical harmonic order. D_{max} is the maximum negative $\cos(\theta)$ for the high-order harmonic beyond h_c. (h_c=57, D_{max}=0.5 in this article)

Based on the harmonic impedance passivity metrics and the theory of constrained piecewise linear fitting [17], a design flow of CAs is proposed in Fig. 8. The over-compensation step S_{Nc} is 0.05 and initial N_c is 5, which

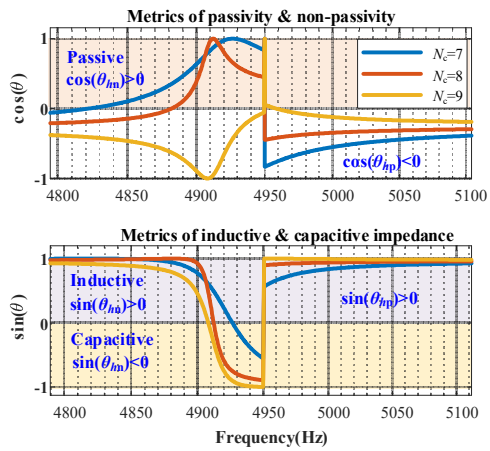


Fig. 7. Impact of N_c on modified passivity metrics under h=99.

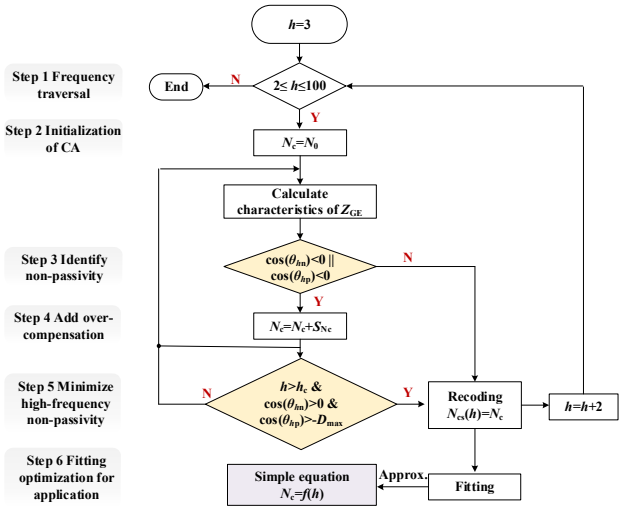


Fig. 8. CA design based on the constrained piecewise linear fitting.

can guarantee that the method does not fall into an endless loop and the proper CAs can be selected.

Furthermore, a first-order piecewise fitting function between obtained N_c and h is utilized for simplicity, as shown in Fig. 9. To improve the accuracy of harmonic impedance passivity, the fitting function contains four stages, which is given by

$$\begin{cases} N_{c1} = 5 \quad (3 \le h \le 23) \\ N_{c2} = 0.0828h + 2.93 \quad (25 \le h \le 39) \\ N_{c3} = 0.2337h - 3.095 \quad (41 \le h \le 57) \\ N_{c4} = -0.0313h + 11.19 \quad (59 \le h \le 99) \end{cases} \tag{12}$$

N_c of stage 1 is same as the conventional-compensation mode. The passivity-based design of CA is highly dependent on the output impedance profile, which is not always equal to the conventional CA ($h\omega_1 T_D$). To realize the high-order harmonic impedance passivity, the CA of each harmonic resonator becomes larger with the increase of h before the critical frequency $1/(4T_D)$, and the maximum CA is about $2h\omega_1 T_D$.

Based on the fitting function, the bode diagram of output impedance is shown in Fig. 10. The presented CAs can guarantee the single-frequency harmonic impedance

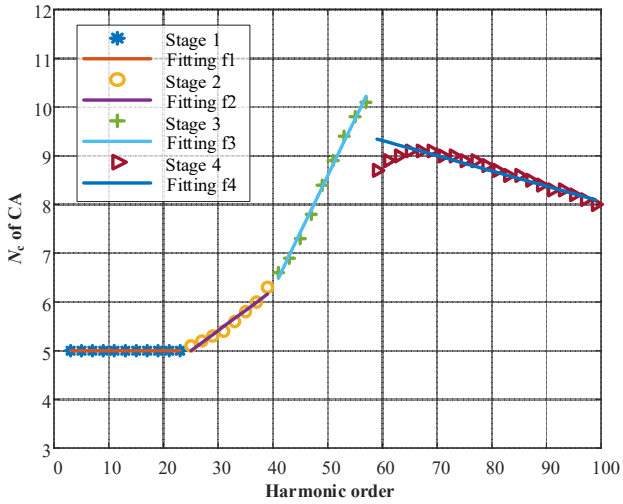


Fig. 9. The first-order piecewise fitting between N_c and h.

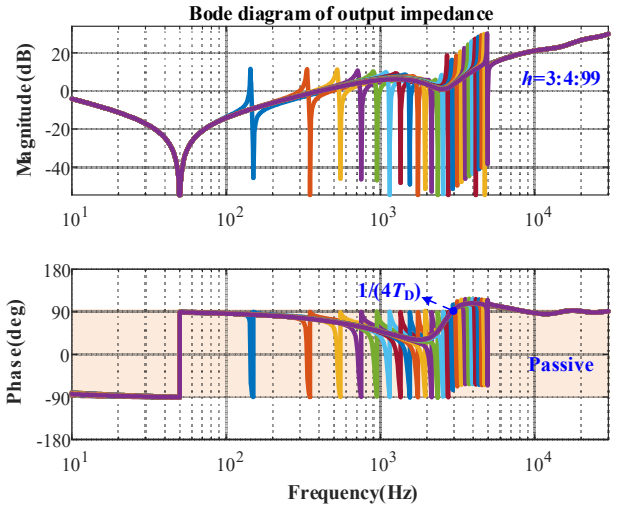


Fig. 10. Bode diagram of output impedance (Presented N_c).

passivity within critical frequency $1/(4T_D)$ and mitigate the high-frequency capacitive-negative impedance.

IV. Experimental Results

To validate the effectiveness of the theoretical analysis, a down-scaled experimental test by the three-phase pulse-width modulation (PWM) inverter with L filter is conducted, as shown in Fig. 11. Regarding the experimental setup, each phase utilizes the PEB-SiC-8024 module and output voltage is sensed by the voltage hall (LV20-P). The control hardware is the B-Box rapid prototyping controller (RCP), which features a Zynq-based Cortex-A9 ARM processor and a programmable Kintex-grade FPGA (Xilinx Zynq). The experimental parameters are shown in Table I. To simplify analysis, various passive loads are employed and the correctness of presented CAs of three cases (Stage 2,3,4) in Fig. 9 will be verified compared with conventional CAs.

TABLE I Experimental Parameters of the Grid Emulator

Symbol	Meaning	Value
V_{PCC}	PCC voltage (l-l, rms)	220 V (1 p.u.)
P_o	Rated power	1.5 kW (1 p.u.)
L_s	AC inductance	5 mH (0.05 p.u.)
f_{sw}	Switching frequency	15 kHz
f_{sa}	Sampling frequency	60 kHz
T_D	Total time delay	85.6 μs

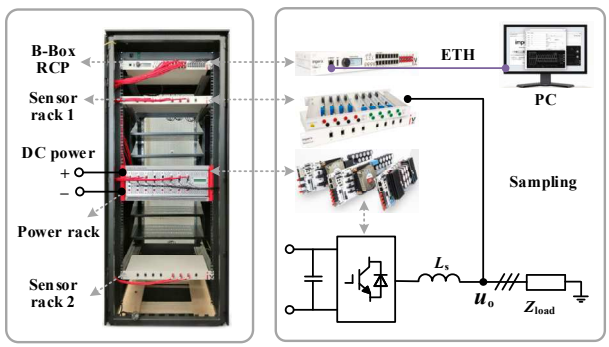


Fig. 11. Experimental setup of three-phase PWM inverter with L filter.

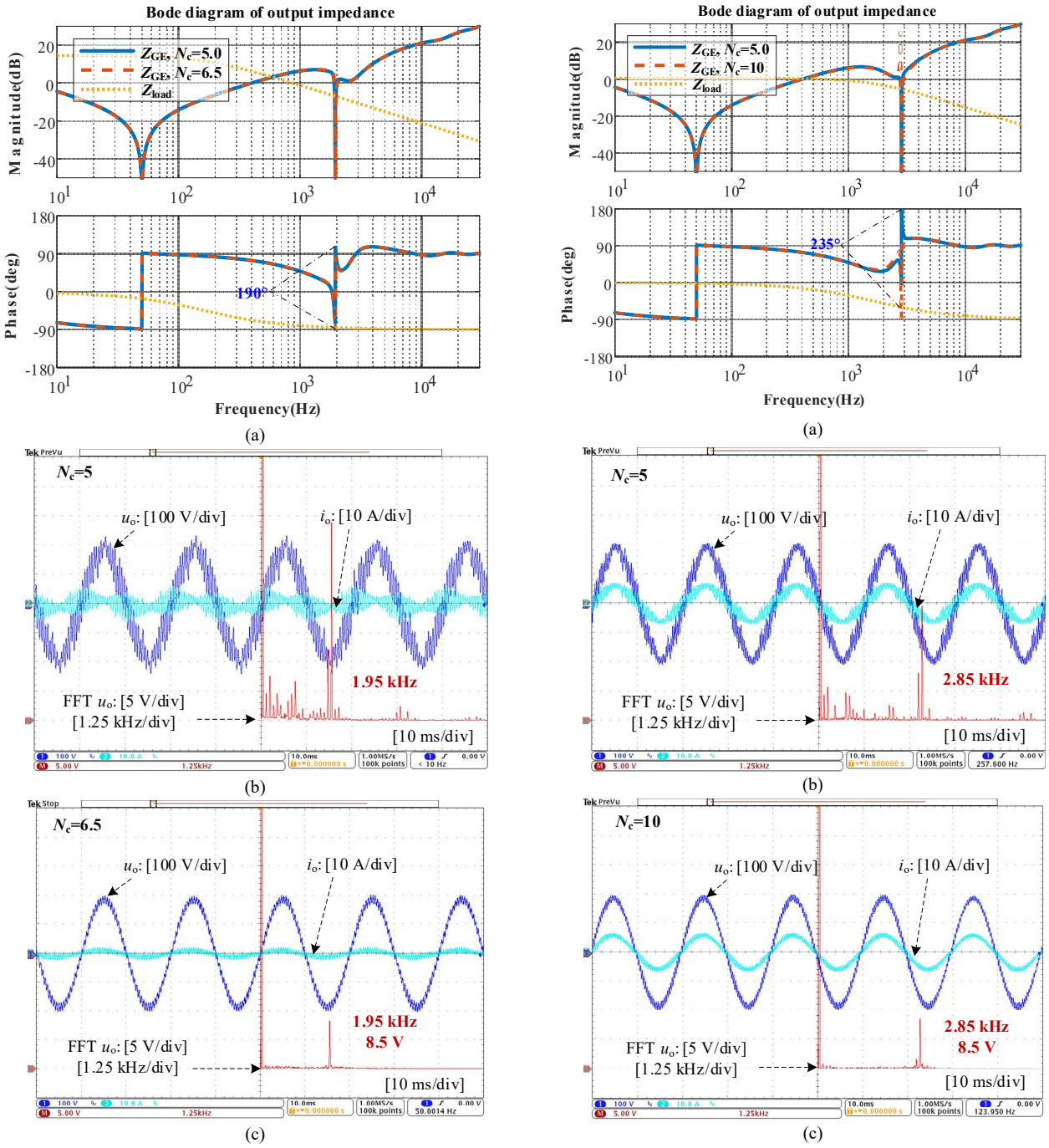


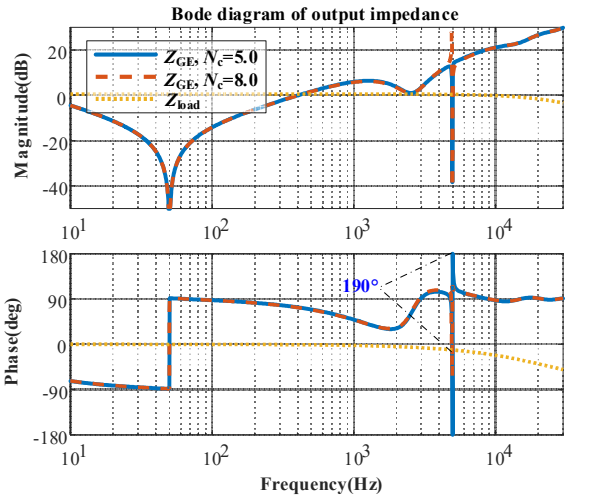
Fig. 12. Bode diagram of output impedance and experimental results for Case I (Stage 2). h=39, R_{load}=160 Ω, C_{load}=5 μF. (a) Bode diagram. (b) N_c=5. (c) N_c=6.5.

Fig. 13. Bode diagram of output impedance and experimental results for Case II (Stage 3). h=57, R_{load}=32 Ω, C_{load}=3 μF. (a) Bode diagram. (b) N_c=5. (b) N_c=10.

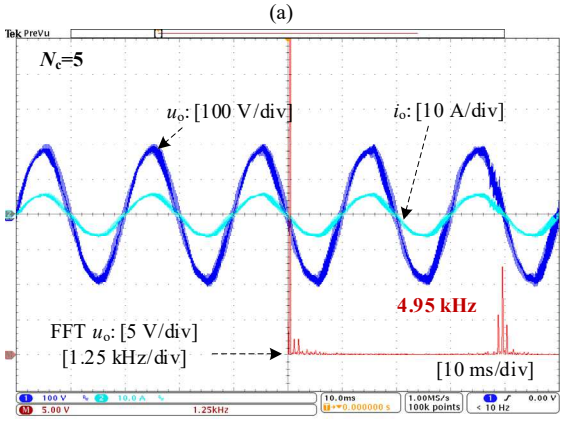
Fig. 12(a) plots the output impedance of grid emulator (GE) with 39th harmonic resonator, as well as a paralleled *RC* load (R_{load}=160 Ω, C_{load}=5 μF). It is clear that the load impedance intersects the GE impedance in the non-passivity region if the conventional CA is used, which leads to phase difference between GE and load is 190°, such that system is unstable. This stability analysis is further validated by the experimental results, as shown in Fig. 12(b), where u_o and i_o are the phase voltage and current. To avoid the overmodulation, emulated harmonic reference value is set as 5% of fundamental frequency magnitude. It can be seen that the oscillations in the voltage and current of grid emulator amplify the magnitude of 19th harmonic and introduce serious low-frequency harmonics. In contrast, system is stabilized with presented CA, as shown in Fig. 12(c).

Fig. 13 shows the bode diagram of output impedance and experimental results for 57th harmonic emulation with another paralleled *RC* load (R_{load}=32 Ω, C_{load}=3 μF). Compared with the conventional CA, the GE can operate stably with presented CA. Furthermore, the experimental results have confirmed the correctness of theoretical analysis.

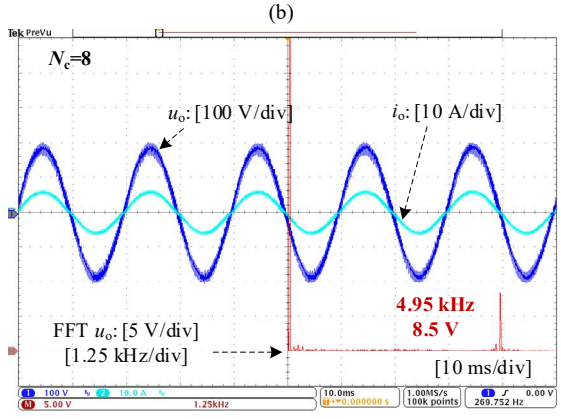
Similarly, Fig. 14 shows the bode diagram of output



(a)



(b)



(c)

Fig. 14. Bode diagram of output impedance and experimental results of Case III (Stage 4). h=99, R_{load}=32 Ω, C_{load}=0.2 μF. (a) Bode diagram. (b) N_c=5. (c) N_c=8.

impedance and experimental results for 99th harmonic emulation. The undercompensated effect of conventional CA destabilizes system with a specific load. In contrast, using presented CA, system can stably generate the high-order harmonic.

V. Conclusions

This paper presents a passivity-based design guideline of the resonant controllers with compensation angles for 2nd~100th harmonic emulation in the grid emulator. Experimental results have confirmed conventional CAs fail to assure the impedance passivity at high-order harmonic impedance passivity frequencies, whereas the proposed method can guarantee the harmonic impedance passivity within the critical frequency $1/(4T_D)$ of voltage control loop.

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