Multi-Sampling With Real-Time Update PWM for Time-Delay Minimization of FPGA-Based Voltage-Controlled Converters

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Multi-Sampling With Real-Time Update PWM for Time-Delay Minimization of FPGA-Based Voltage-Controlled Converters

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***Abstract*—Time delay usually limits control bandwidth and deteriorates the stability of digital control system. This paper presents the mechanism and optimization of the multi-sampling with real-time update PWM method for time-delay minimization. The relationship between modulation-wave update latency and digital delay is firstly analyzed by the graphical illustration, revealing that desired implementation of equivalently eliminating computation delay will be limited by large update latency. Further, to minimize update latency, the FPGA is employed to realize the resonant controller based voltage control, thanks to its advantage of fast-paralleled calculation. Compared with traditional multi-sampling with multi-update PWM, the presented method further reduces the digital delay by up to 66%. Its effectiveness is validated by the platform of a single-loop voltage-controlled converter with an inductor (*L*)-filter.**

Keywords—Multi-sampling, real-time update PWM, time delay, FPGA, voltage-controlled

I. INTRODUCTION

The time delay of digital control system caused by analog-sampling circuit, analog-to-digital (AD) conversion, digital computation, and pulse width modulation (PWM) could be classified into the analog delay and digital delay. The analog delay is primarily generated by the sampling sensor, while the digital delay mainly contains computation (unit) delay and PWM delay [1], [2]. These delays tend to deteriorate the dynamic response of control system and introduce the negative resistance, which further threaten system stability [3]. Therefore, the minimization of time delay to guarantee the wide-frequency passivity of digital control system is urgently needed [4].

Regarding the analog delay, the response time of current sensor is generally smaller than 1 μs, while typical response time of the hall voltage sensor is from 10 μs to 100 μs, which has a significant impact on the high-bandwidth voltage control. Increasing primary-measured resistance of voltage sensor is a simple and effective solution to reduce the analog delay even though at the expense of certain measurement accuracy [5]. On the other hand, numerous works have been reported to directly reduce the digital delay from the view of modulation and sampling. To reduce the computation delay, shifting the sampling instant towards to the instant of modulation-wave update method is proposed in [6]. Unfortunately, the high-frequency switching ripple and aliasing phenomenon are introduced simultaneously. The dual-alternate sampling with real-time update PWM is proposed to eliminate the computation delay in [7]. It significantly improves the system robustness without introduced switching ripple but it is only appropriate for the single-phase system. Moreover, removing computation delay is only effective when the update latency is smaller than a quarter of sampling period. The fast current control by reconstructing the architecture of PI controller with real-time update modulation wave in the digital signal processor (DSP) is proposed to minimize the update latency [8]. It can be applied in the three-phase system but the relationship between update latency and digital delay is not discussed. Furthermore, the above-mentioned methods only reduce the computation delay, and the PWM delay still exists in the system. The multi-sampling with multi-update method shows the attractive advantage to reduce the computation delay and PWM delay simultaneously [9-11]. However, the time delay is only reduced to 1.5 times switching period divided by sampling rate ($1.5T_{sw}$/N), and minimizing the digital delay by increasing sampling rate relays on the processing speed of digital controller.

To fill these gaps, the multi-sampling with real-time update PWM and voltage control implemented in FPGA are utilized to further reduce the digital delay compared with the traditional multi-sampling method. The graphical evaluation of adopted method is carried out and the impact of the modulation-wave update latency on reduced digital delay is revealed. The experiments are conducted to confirm the effectiveness of theoretical analysis.

II. SYSTEM DESCRIPTION

Fig. 1 shows the general diagram of three-phase voltage source converter (VSC) with *L*-filter operating in standalone mode. The single-loop voltage control based on the resonant controller (RC) is adopted for time delay analysis [12]. Regarding the experimental setup, the half-bridge adopts the PEB-SiC-8024 module and the control hardware is the B-Box rapid prototyping controller (RCP) from Imperix. The B-Box RCP consists of a dual-core ARM Cortex-A9 processor and a programmable Kintex-grade FPGA.

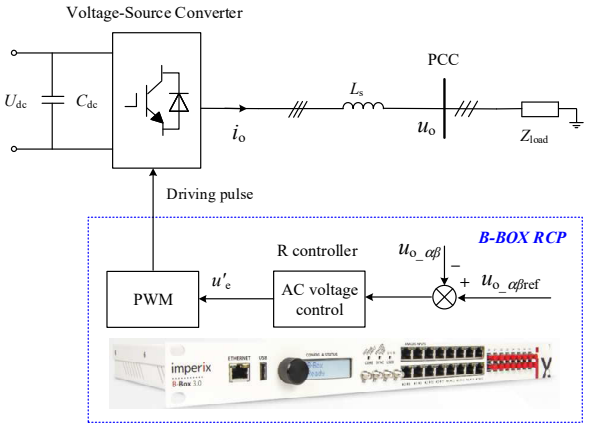

Fig. 1. Diagram of the single-loop voltage-controlled VSC.

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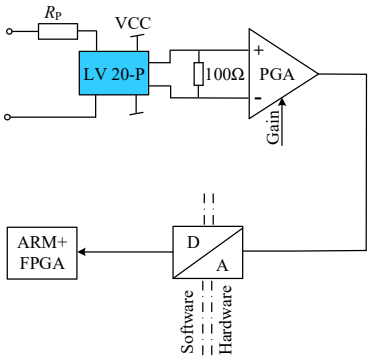


Fig. 2. Voltage-sampling specifications.

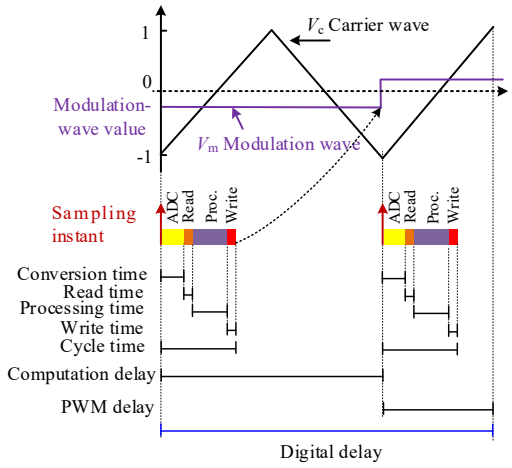


Fig. 3. Definition of the digital delay based on single-sampling mode.

Fig. 2 shows the sampling system, which contains the voltage sensor (LEM LV20-P), AD8251 power gain amplifier (PGA) and AD converter (ADS8568). Generally, the sensor delay of the LV20-P is 16 μs when the primary-measured resistance R_p is 25 kΩ as required [5]. The settling time of AD8251-PGA is 785 ns, which could be neglected.

Fig. 3 shows the definition of digital delay based on the single-sampling with single-update mode, which contains computation delay and PWM delay. The computation delay (one-step sampling instant T_{sa}) is time duration between the sampling instant and modulation-wave update instant. The PWM delay is caused by zero-order hold (ZOH) effect, resulting in an average delay of $0.5T_{sa}$ [10]. Generally, the PWM strategy is realized by the FPGA and control algorithm is implemented by the ARM. Each cycle time contains four parts: AD conversion time, read time of sampling signals from FPGA to ARM, processing time of control strategies and write time of PWM signals from ARM to FPGA. Moreover, the conversion time from analog data to digital data through ADS8568 is 2 μs. The cycle time must be smaller than T_{sa} to guarantee control strategies could be completed during one interrupt period.

III. Analysis and Optimization of Time-Delay Reduction

In this section, to reduce above digital delay, the multi-sampling with real-time update PWM is adopted. The graphical illustration is firstly utilized to reveal the relationship between update latency (i.e., cycle time) and computation delay. Moreover, the optimization of reduced update latency and sensor delay is carried out.

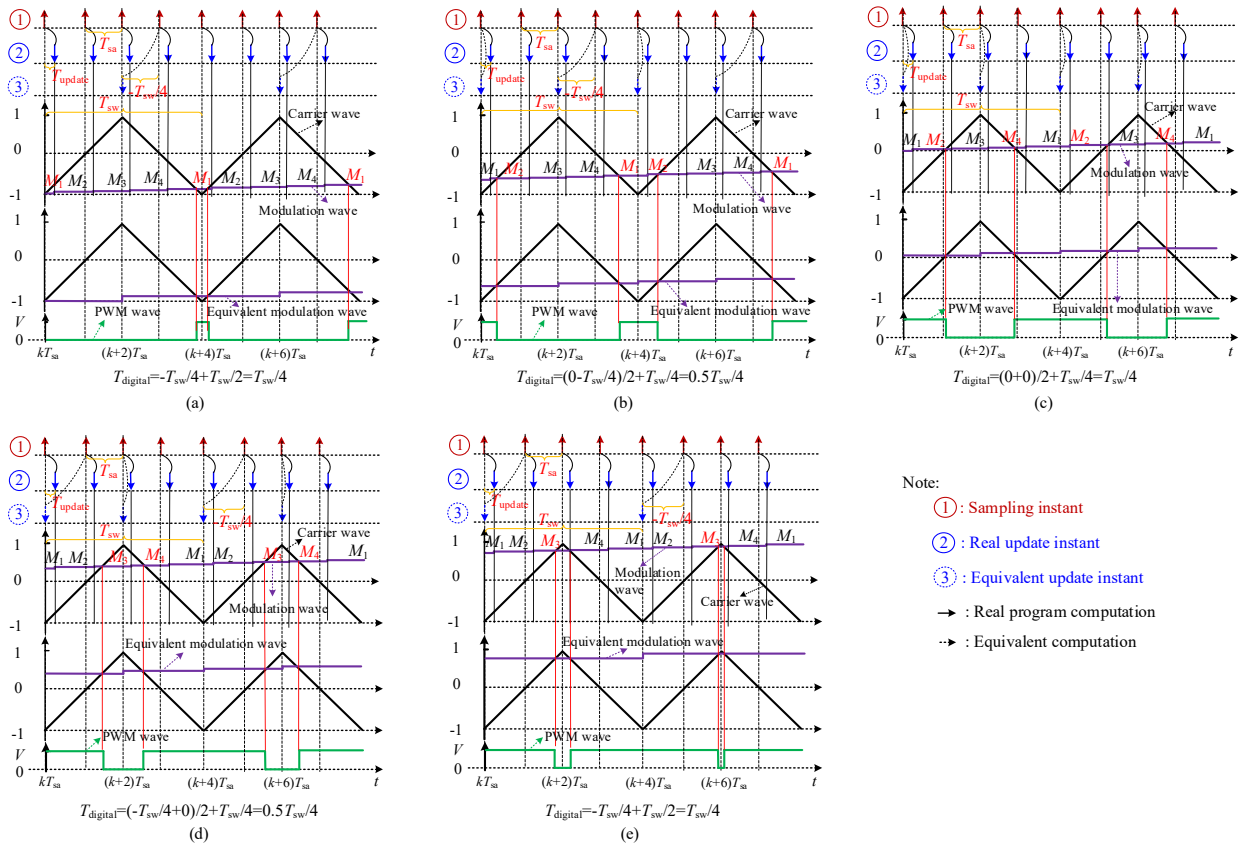
A. Graphical illustration of multi-sampling with real-time update PWM

Taking four-sampling with real-time update mode as an example, the modulation wave is updated immediately 4 times within each switching period T_{sw} once the control cycle is completed. It is defined that the update latency is $T_{update}=\lambda T_{sa}$ ($0<\lambda\leq1$). Obviously, the update ratio $\lambda=1$ is for the multi-sampling with multi-update PWM method. According to geometric deduction and graphical evaluation, the rule of digital delay is divided into three stages when the update ratio is $0<\lambda<0.5$, $\lambda=0.5$ and $0.5<\lambda<1$, respectively, as shown in Fig. 4~6.

Regarding Fig. 4, there are always two or one (near peak) effective modulation signals $M(k)$ which determine the intersection position between the triangular carrier wave and modulation wave on each switching period. Since the frequency of modulation wave is much smaller than the frequency of carrier wave, only five cases need to be considered. According to the voltage-second balance principle, the four-sampling with real-time update mode can be equivalent to single-sampling with single-update mode or double-sampling with double-update mode with back-shift sampling instant. Regarding Fig. 4 (a), this case is transformed into the single-sampling with peak-of-carrier-update mode. Based on geometric deduction, the front and back effective modulation signals are always M_1 and M_1 respectively when the range of $M(k)$ is $-1\sim(\lambda-1)$. The equivalent computation delay of back M_1 is $-T_{sw}/4$, which realizes the equivalent phase lead performance. Since the PWM delay of single-sample mode is $T_{sw}/2$, the digital delay is $-T_{sw}/4+T_{sw}/2=T_{sw}/4$. Other cases and corresponding ranges of modulation signals are shown in Table I. Especially, the digital delay is always $T_{sw}/4$ when the λ is equal to 0.5.

TABLE I. Delay of Four-Sampling With Real-Time Update Mode

Cases	**Range of $M(k)$ ($0<\lambda<0.5$)**	**Effective $M(k)$**	**Digital delay**
(a)	$-1\sim(\lambda-1)$	M_1 and M_1	$T_{sw}/4$
(b)	$(\lambda-1)\sim(-\lambda)$	M_2 and M_1	$0.5T_{sw}/4$
(c)	$(-\lambda)\sim\lambda$	M_2 and M_4	$T_{sw}/4$
(d)	$\lambda\sim(1-\lambda)$	M_3 and M_4	$0.5T_{sw}/4$
(e)	$(1-\lambda)\sim1$	M_3	$T_{sw}/4$
Cases	**Range of $M(k)$ ($\lambda=0.5$)**	**Effective $M(k)$**	**Digital delay**
(I)	-1~-0.5	M_1 and M_1	$T_{sw}/4$
(II)	-0.5~0.5	M_2 and M_4	$T_{sw}/4$
(III)	0.5~1	M_3	$T_{sw}/4$
Cases	**Range of $M(k)$ ($0.5<\lambda<1$)**	**Effective $M(k)$**	**Digital delay**
(A)	$-1\sim(-\lambda)$	M_1 and M_1	$T_{sw}/4$
(B)	$(-\lambda)\sim(\lambda-1)$	M_1 and M_4	$1.5T_{sw}/4$
(C)	$(\lambda-1)\sim(1-\lambda)$	M_2 and M_4	$T_{sw}/4$
(D)	$(1-\lambda)\sim\lambda$	M_2 and M_3	$1.5T_{sw}/4$
(E)	$\lambda\sim1$	M_3	$T_{sw}/4$



$T_{digital}$=-T_{sw}/4+T_{sw}/2=T_{sw}/4 (a)

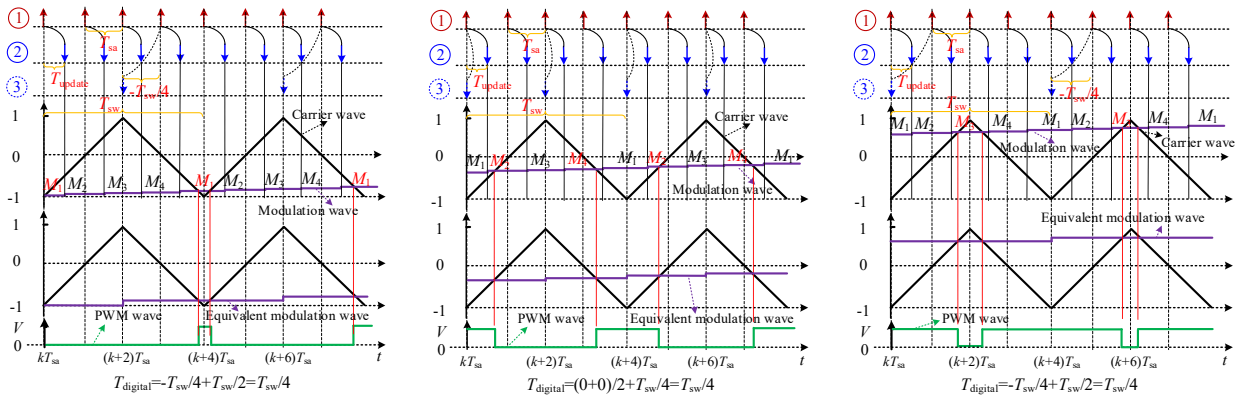
$T_{digital}$=(0-T_{sw}/4)/2+T_{sw}/4=0.5T_{sw}/4 (b)

$T_{digital}$=(0+0)/2+T_{sw}/4=T_{sw}/4 (c)

$T_{digital}$=(-T_{sw}/4+0)/2+T_{sw}/4=0.5T_{sw}/4 (d)

$T_{digital}$=-T_{sw}/4+T_{sw}/2=T_{sw}/4 (e)

Fig. 4. Four-sampling with real-time update PWM ($0<\lambda<0.5$).

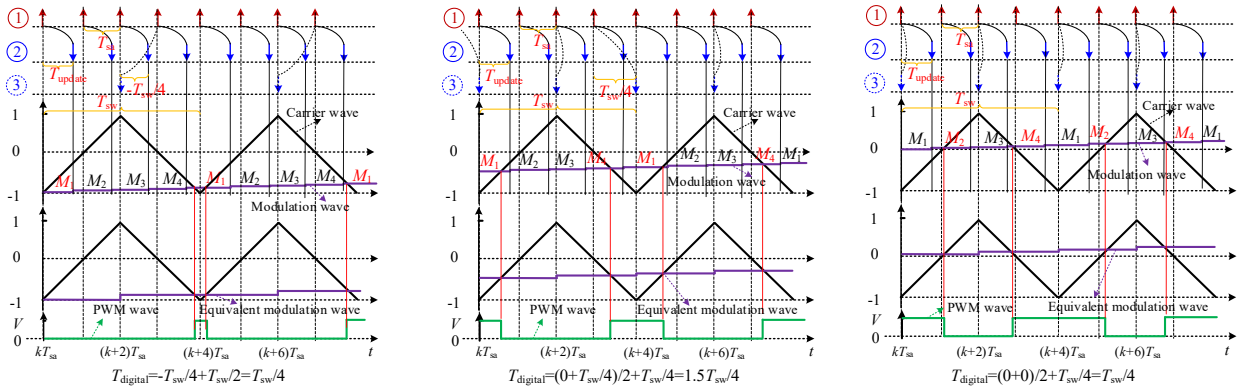


$T_{digital}$=-T_{sw}/4+T_{sw}/2=T_{sw}/4 (a)

$T_{digital}$=(0+0)/2+T_{sw}/4=T_{sw}/4 (b)

$T_{digital}$=-T_{sw}/4+T_{sw}/2=T_{sw}/4 (c)

Fig. 5. Four-sampling with real-time update PWM (λ=0.5).



$T_{digital}$=-T_{sw}/4+T_{sw}/2=T_{sw}/4 (a)

$T_{digital}$=(0+T_{sw}/4)/2+T_{sw}/4=1.5T_{sw}/4 (b)

$T_{digital}$=(0+0)/2+T_{sw}/4=T_{sw}/4 (c)

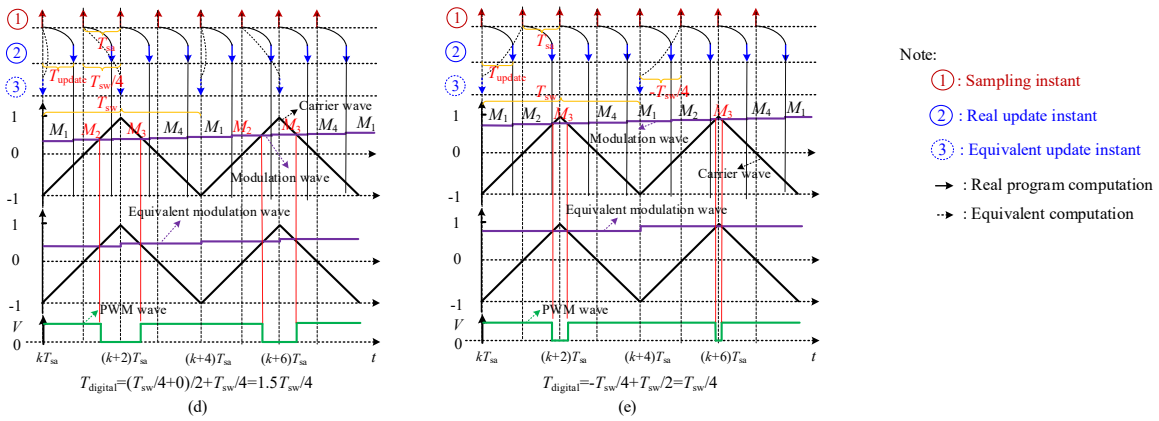


Fig. 6. Four-sampling with real-time update PWM ($0.5<\lambda<1$).

Taking the case of $0<\lambda<0.5$ as an example, the average digital delay during half period of modulation waveform (fundamental frequency 50 Hz) is shown in Fig. 7. Based on the periodic averaging method, the piecewise delays are transformed to the average digital delay, which is given by

$$\begin{aligned} T_{\text{digital}} &= \frac{T_{\text{sw}}}{4}\frac{t_{\text{sum}}}{0.01} \\ &= \frac{T_{\text{sw}}}{4}\left[1+\frac{\arcsin(\lambda-1)}{\pi}+\frac{\arcsin\lambda}{\pi}\right] \\ &\approx \frac{T_{\text{sw}}}{4}\left[1+\frac{\lambda-1}{2}+\frac{\lambda}{2}\right]=\frac{0.5T_{\text{sw}}}{4}+\lambda\frac{T_{\text{sw}}}{4} \end{aligned} \tag{1}$$

where t_{sum} is expressed as

$$\begin{aligned} t_{\text{sum}} &= t_1+0.5(t_2-t_1)+ \\ &\quad (t_3-t_2)+0.5(t_4-t_3)+(0.01-t_4) \end{aligned} \tag{2}$$

The same average digital delay as (1) can be obtained in the other cases $\lambda=0.5$ and $0.5<\lambda<1$. Accordingly, the average digital delay and total loop delay at any sampling rate are expressed as

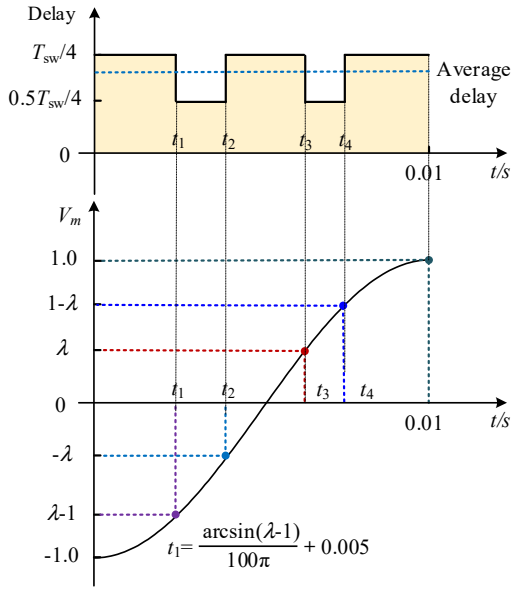


Fig. 7. Analysis of average digital delay ($0<\lambda<0.5$).

$$T_{\text{digital}} = \frac{0.5T_{\text{sw}}}{N}+\lambda\frac{T_{\text{sw}}}{N} \tag{3}$$

$$T_{\text{d}} = \frac{0.5T_{\text{sw}}}{N}+T_{\text{update}}+T_{\text{sensor}} \tag{4}$$

where N is the sampling rate. T_{d} and T_{sensor} are the total loop delay and voltage sensor delay, respectively. It is verified that (4) is satisfied when the sampling rate N is other values (e.g., 2, 8, etc.).

B. Optimization of update latency and sensor delay

As shown in (4), the minimized loop delay is limited by the update latency and sensor delay. The modulation-wave update latency of voltage control in ARM is monitored as 6.4 μs by the B-Box RCP in Fig. 8(a). With the subsequent increase of required control algorithms in ARM, the update latency will be larger, which worsens the dynamic behavior of the single-loop voltage control.

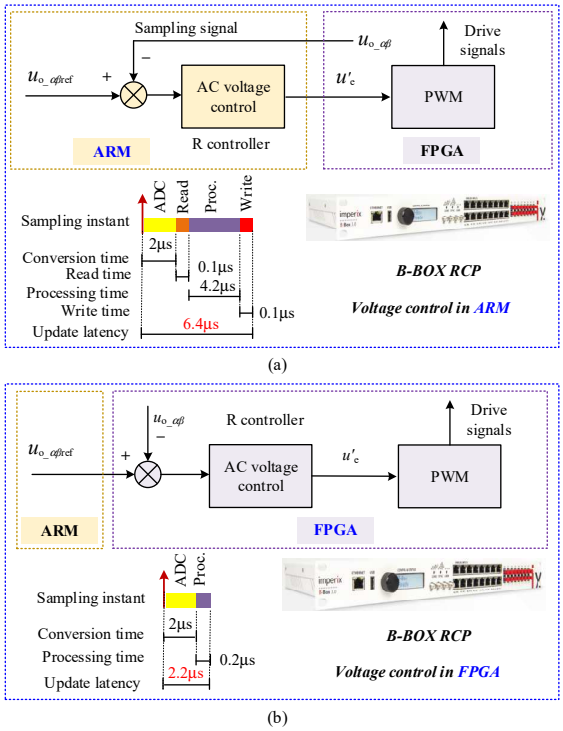


Fig. 8. Difference between voltage control in ARM and FPGA.

Therefore, the voltage control is distributed in the FPGA to minimize the update latency. As shown in Fig. 8 (b), thanks to the advantage of paralleled computation in FPGA, the update latency (2.2 μs) finally contains AD conversion time (2.0 μs) and FPGA processing time (0.2 μs). In this case, the computation delay is considered equivalently eliminated, and the digital delay is reduced by up to 66 % (2/3) compared with traditional multi-sampling method. In addition, the delay of voltage sensor is reduced to 4 μs using the 100 kΩ primary-measured resistor rather than 25 kΩ recommended in the datasheet of LEM LV20-P.

IV. Experimental Validation

Table II shows the experimental parameters and setting the resistor as the load to simplify analysis. The switching frequency and sampling rate are selected as 10 kHz and 8 to highlight the effect of reduced digital delay.

TABLE II. Experimental Parameters of the VSC with *L*-Filter

Description	Symbol	Value
AC line-to-line voltage (RMS)	u_o	220 V(1p.u.)
AC rated power	P_o	1.5 kW(1p.u.)
Fundamental frequency	f_0	50 Hz
Switching frequency	f_{sw}	10 kHz
Sampling rate	N	8
DC link capacitor	C_{dc}	594 μF(6p.u.)
AC inductor	L_s	6 mH (0.06 p.u.)
Load resistor	R_{load}	32 Ω (1p.u.)

A. Critical resonant gain analysis

Since time delay is difficult to be directly measured, the relationship between critical stability boundary and time delay is usually used to indirectly validate the effectiveness of reduced time delay [1]. Fig. 9 shows the block diagram of single-loop voltage-controlled VSC with *L*-filter in $\alpha\beta$-frame. The critical instability is mainly affected by the resonant gain K_r, time delay T_d and phase lag caused by the resistor load with L filter. Therefore, considering the impact of load resistance, the open-loop transfer function of single-loop voltage control is expressed as

$$T(\mathrm{s}) = \frac{K_r s}{s^2+\omega_1^2} e^{-T_d s} \frac{R_{load}}{sL_s + R_{load}} \tag{5}$$

To enhance accuracy at fundamental frequency and avoid extra time delay caused by discretization of the resonant controller, the Tustin with pre-warping discretized method is utilized in the digital control system. The discretized voltage control is given by [13]

$$G_v(z) = \frac{K_r \sin(\omega_1 T_{sa})}{2\omega_1} \frac{1-z^{-2}}{1-2z^{-1}\cos(\omega_1 T_{sa})+z^{-2}} \tag{6}$$

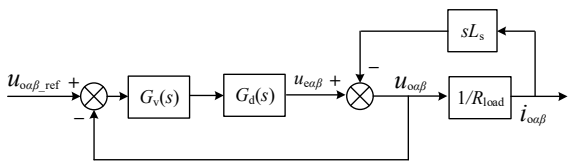


Fig. 9. Block diagram of the single-loop voltage-controlled VSC.

According to Nyquist stability criterion, the magnitude-frequency and phase-frequency response of open-loop gain $T(j\omega_c)$ at the critical-stable operating point should satisfy

$$\left|T(j\omega_c)\right| = \frac{K_r}{\omega_c} \frac{R_{load}}{\sqrt{R_{load}^2+\omega_c^2 L_s^2}} = 1 \tag{7}$$

$$\angle T(j\omega_c) = -\frac{\pi}{2} - \omega_c T_d - \arctan\frac{\omega_c L_s}{R_{load}} = -\pi \tag{8}$$

Therefore, the specific relationship among the critical resonant gain K_r, phase-crossover frequency f_c and total loop delay T_d is as follows

$$K_r = 2\pi f_c \sqrt{1+\frac{(2\pi f_c)^2 L_s^2}{R_{load}^2}} \tag{9}$$

$$T_d = \frac{\frac{\pi}{2} - \arctan\frac{2\pi f_c L_s}{R_{load}}}{2\pi f_c} \tag{10}$$

Above relationship is one-to-one correspondence, as shown in Fig. 10. With the decrease of time delay, critical resonant gain K_r and phase-crossover frequency f_c are larger, i.e., the larger oscillated frequency.

According to (4), T_d could be obtained respectively under three cases: traditional eight-sampling with eight-update PWM, adopted method with voltage control in the ARM and FPGA. After that, the corresponding K_r and f_c could be solved from (9) and (10) or found from Fig. 10, as shown in Table III.

TABLE III. Critical Parameters of Three Cases Under Eight-Sampling Mode

Cases	Critical K_r	Critical f_c	Total loop delay T_d based on (4)
(a)	45000	2.4 kHz	22.8 μs
(b)	70000	3.0 kHz	16.7 μs
(c)	84000	3.3 kHz	12.5 μs

*Case (a) denotes traditional eight-sampling with eight-update.
*Case (b) denotes eight-sampling with real-time update and the voltage control in ARM (T_{update}=6.4 μs as shown in Fig. 8(a)).
*Case (c) denotes eight-sampling with real-time update and the Voltage control in FPGA (T_{update}=2.2 μs as shown in Fig. 8(b)).

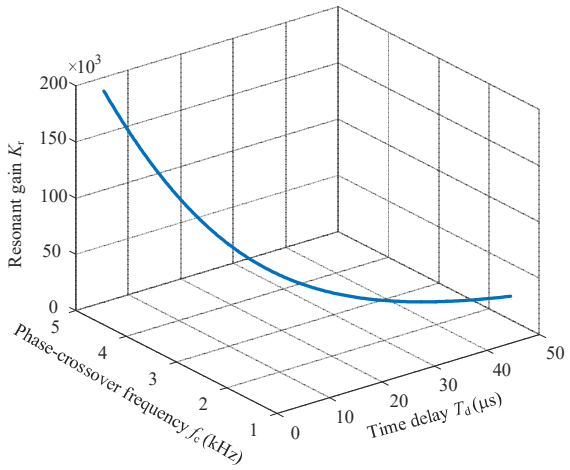


Fig. 10. Specific relationship among the resonant gain K_r, phase-crossover frequency f_c and time delay T_d.

B. Experimental results

Fig. 11 shows the states of phase-a voltage, phase-a current and FFT analysis. The resonant gain K_r is set as different parameters around above-critical K_r. The system becomes unstable with the increase of the resonant gain up to the value larger than the critical K_r. The oscillated frequency f_c and critical K_r of case(c) are larger than other cases. Moreover, when K_r is 80000, system under case(c) is stable while other cases are unstable, which validates the effectiveness of minimized time delay by the multi-sampling with real-time update PWM and voltage control distributed in FPGA. In summary, the experimental results are coincident with the theoretical analysis.

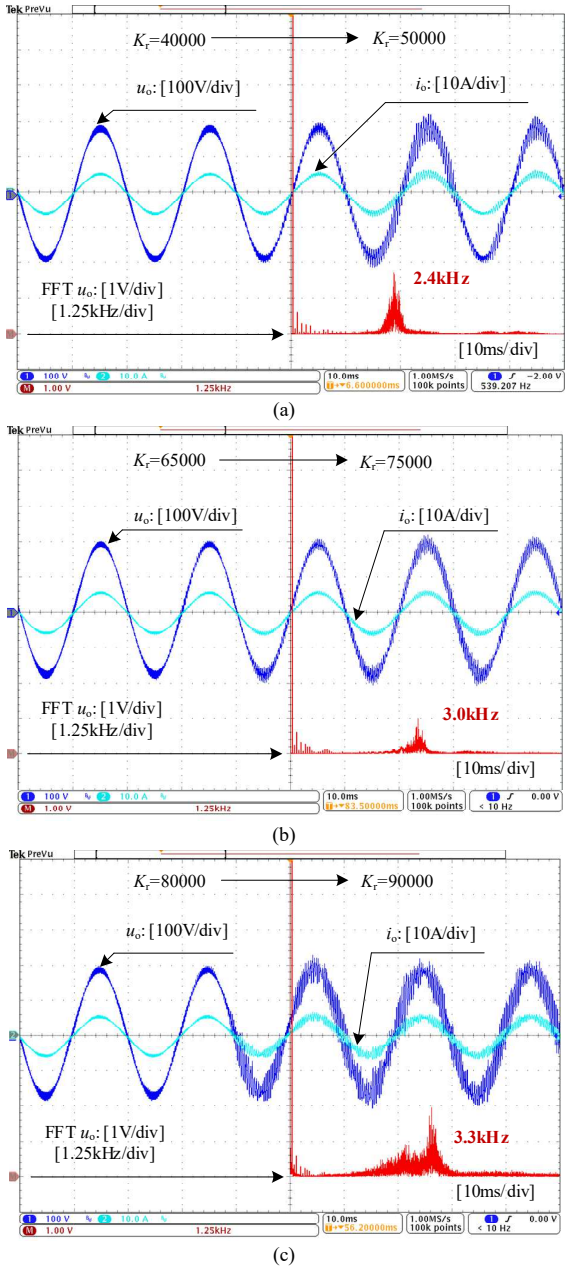


Fig. 11. The experimental results from stability to instability with different methods. (a) Traditional eight-sampling with multi-update mode (K_r from 40000 to 50000). (b) Voltage control in ARM (K_r from 65000 to 75000). (c) Voltage control in FPGA (K_r from 80000 to 90000).

V. Conclusion

This paper firstly reveals the mechanism of multi-sampling with real-time update PWM by graphical illustration and establishes the relationship between the modulation-wave update latency and average digital delay. The motivation of eliminating computation delay and minimizing digital delay is limited by the large update latency and sensor delay. The voltage control implemented in FPGA can minimize the update latency and reduce the digital delay by up to 66% compared with the traditional multi-sampling with multi-update PWM method. Finally, the correctness and effectiveness of the presented methods are indirectly verified by the experiments based on the critical-instability method.

Acknowledgment

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