Fast DC Fault Current Suppression and Fault Ride Through in Full-Bridge MMCs via Regulation of Submodule Capacitor Discharge

by

Munif Nazmus Sakib

A thesis

presented to the University of Waterloo

in fulfillment of the

thesis requirement for the degree of

Master of Applied Science

in

Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2022

Author’s Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

High Voltage Direct Current (HVDC) is more cost-effective than High Voltage Alternating Current (HVAC) for transmitting power over long distances, and therefore is ideal for bulk power transfer from wind, solar, hydroelectric, and tidal power plants located in offshore or remote locations to load centers. The use of Voltage-Sourced Converters (VSCs) in HVDC transmission systems offers greater flexibility when compared to their counterpart, Line Commutated Converters (LCCs), due to their smaller footprint, improved power quality, as well as decoupled active and reactive power control, voltage support, and black start capabilities. The most recent advancements in VSC technology have led to the emergence of a new converter topology known as the Modular Multilevel Converter (MMC). The simplest and most economical MMC cell structure is the Half-Bridge Submodule (HBSM), which is unable to prevent AC side contribution to DC side faults in HVDC systems. Therefore, DC fault protection in the HB-MMC requires either installation of expensive DC Circuit Breakers (DCCBs) or the opening of AC side breakers that are not adequately fast. Adding two extra switches to the HBSM results in the Full-Bridge Submodule (FBSM) configuration which ensures that, in the event of a DC side fault, there is a reverse voltage in the path of AC side current feeding the DC side fault through the antiparallel diodes in the SM switches. In addition, such fault blocking SMs capable of bipolar voltage generation equip the MMCs with Fault Ride Through (FRT) ability, thus allowing them to remain connected to both AC and DC networks during DC faults while operating as Static Compensators (STATCOMs) and exchanging reactive power with the AC network. A comprehensive review of notable fault blocking SM configurations and fault ride through techniques is presented in this thesis.

In the event of a DC side fault, the fault current contributions are initially made by SM capacitor discharge, which occurs before the fault is detected, followed by the AC side contribution to the DC side fault. While the AC side currents can be regulated using fault blocking SMs with bipolar voltage generation capability, the initial discharge of the SM capacitors results in high DC fault currents, which can take several milliseconds to be brought under control. A method to actively influence the rate of rise of the DC fault current by regulating the discharge of SM capacitors in an HB-MMC system has been presented in the literature. In this thesis, the approach has been modified and adapted to a FB-MMC system. The discharge direction of the FBSM capacitors is inverted following the detection of a DC side fault which leads to a reversal in the fault current direction and a fast drop-off towards zero. The conventional FRT procedure where the DC fault is cleared by making adjustments to the MMC

arm reference voltages followed by STATCOM operation of the MMC is initiated after the detection of zero-crossing of the DC fault current. The proposed control scheme provides significantly faster DC fault current suppression compared to the case where the conventional FRT procedure is initiated immediately upon DC fault detection. Simulations performed on a point-to-point FB-MMC test system are used to verify the theoretical analysis and to evaluate the DC-FRT performance of the proposed scheme.

Acknowledgements

First and foremost, I would like to express my sincere gratitude to my supervisors, Dr. Sahar Azad and Dr. Mehrdad Kazerani for their knowledge, guidance, and encouragement throughout my degree. This work would not have been possible without their support and valuable suggestions.

I would also like to express my thanks to Dr. Kankar Bhattacharya and Dr. Magdy Salama for serving on my thesis committee and providing valuable feedback.

A special thanks to Dr. Azad and Dr. Kazerani for providing financial support. I would also like to extend my gratitude to the University of Waterloo and the Government of Ontario for providing additional financial support through the President's Graduate Scholarship (PGS) and the Ontario Graduate Scholarship (OGS) programs.

Dedication

To my family who has always been there for me

Table of Contents

List of Figures

List of Tables

List of Abbreviations

AAC Alternate Arm Converter

ACCB Alternating Current Circuit Breaker

ACTSM Active Clamped T-Type Submodule

AFBSM Asymmetrical Full-Bridge Submodule

CDSM Clamped Double Submodule

CSM Composite Submodule

CDSM Clamped Double Submodule

DCCB Direct Current Circuit Breaker

DRBSM Double Reverse Blocking Submodule

FRT Fault Ride Through

FLCCSM Five-Level Cross Connected Submodule

FBSM Full-Bridge Submodule

HBSM Half-Bridge Submodule

HBHMC H-Bridge Hybrid Modular Converter

HCMC Hybrid Cascaded Multilevel Converter

HC-MMC Hybrid Cascaded Modular Multilevel Converter

HVAC High Voltage Alternating Current

HVDC High Voltage Direct Current

IGBT Insulated-Gate Bipolar Transistor

LCC Line Commutated Converter

MSM Mixed Submodule

MMC Modular Multilevel Converter

PCC Point of Common Coupling

SCSM Switched Capacitor Submodule

SFBSM Semi Full-Bridge Submodule

SM Submodule

SSHMMC Series Stacked Hybrid Modular Multilevel Converter

STATCOM Static Compensator

TLCCSM Three-Level Cross Connected Submodule

UFBSM Unipolar Full-Bridge Submodule

VSC Voltage-Sourced Converter

WSC Wave-Shaping Circuit

Chapter 1
Introduction

1.1 Background and Motivation

The extensive use of fossil fuels for electricity generation has significantly affected climate change and has accelerated the integration of renewable energy resources into the power grid. To comply with targets such as the European Union's goal of achieving carbon neutral status by 2050, it is conceivable that conventional fossil fuel-based power generation plants will gradually be replaced by renewable energy resources. However, taking advantage of huge supplies of renewable energy would require dedicating large areas of land (for large solar PV plants and onshore wind farms), and making installations in large bodies of water far away from the shore (for offshore wind farms). In both cases, the electricity has to be generated at locations far away from large urban centers, where most of the power consumption occurs. This necessitates an efficient means of transmitting the electricity generated in remote locations to the load centers leading to renewed interest in High Voltage Direct Current (HVDC) transmission systems. HVDC is more efficient than High Voltage Alternating Current (HVAC) for transmitting power over long distances, with reduced right-of-way requirements. This makes it an ideal choice for bulk power transmission from wind, solar, hydroelectric, and tidal plants located in far offshore or remote locations to load centers. In addition, HVDC systems offer better control over transmitted power when compared with HVAC systems [1].

The first HVDC link utilizing mercury-arc valves was commissioned in 1954 on the Swedish island of Gotland [2] to integrate wind power into the island grid. However, potential environmental hazards associated with mercury valves combined with the advent of newer HVDC technology led to the decommissioning of all mercury-arc valve based HVDC systems in the 21st century.

The invention of thyristor valves led to the development of Line Commutated Converters (LCCs) for HVDC systems. LCCs offered higher power capacity, higher reliability, and lower maintenance requirements when compared to converters based on mercury-arc valves. Such advantages enabled LCC technology to gain widespread recognition and extensive use in HVDC projects around the world. However, LCC-HVDC systems have serious drawbacks including a large footprint, as well as high harmonic filtering and reactive power compensation requirements. Advances in semiconductor technology led to the emergence of Voltage-Sourced Converters (VSCs) [3] that employ Insulated Gate Bipolar Transistors (IGBTs). VSCs were able to address some of the issues prevalent in LCCs and

offered smaller footprint, as well as decoupled active and reactive power control, voltage support, and black start capabilities. However, rather low voltage ratings of IGBT switches confined the application of conventional two and three level VSCs mostly to low and medium voltage systems.

Introduced in the early 2000s, the Modular Multilevel Converter (MMC) [4] is the latest advancement in HVDC transmission technology. MMCs consist of large numbers of switching cells called submodules (SMs) that are stacked in series to build up the desired operating voltage. Such a modular design allows for greater scalability and improves the quality of the output voltage, thereby eliminating the need for harmonic filters. Each of the SMs contains capacitor(s); so, the DC link capacitor, which is essential in VSCs, is no longer required. In addition, operation at a lower voltage and switching frequency leads to lower switching losses in the SMs. Due to such significant advantages, MMC has become the most promising technology in HVDC systems. However, the control of MMCs is more complex than the other converter technologies due to the requirement of balancing a large number of SM capacitors, as well as suppressing inner circulating currents.

Designing appropriate protection for HVDC systems is more challenging when compared to HVAC systems due to the lack of zero-crossing in the DC current and limitations in overload capability of semiconductor devices used in the converters. Like the conventional VSC, MMCs are vulnerable to DC side faults. The simplest SM structure in the MMC is the Half-Bridge Submodule (HBSM) which consists of two switches and a capacitor. The presence of freewheeling diodes in the HBSMs results in AC side contribution to DC faults. Direct Current Circuit Breakers (DCCBs) may be used to clear DC faults when HBSMs are used. However, DCCBs are expensive and have low technical maturity. The use of Alternating Current CBs (ACCBs) on the AC side is another option to clear DC faults; however, such breakers take a few cycles to trip and are, therefore, not adequately fast for HVDC systems protection. Recent research has focused on taking advantage of the inherent fault blocking capability of SMs such as the Full-Bridge Submodule (FBSM). Such SMs can introduce a reverse voltage in the path of fault current, thus driving the current down to zero. Furthermore, instead of blocking the fault current, certain fault-tolerant SMs may also be utilized as wave-shaping circuits to control the AC currents during the fault and provide reactive power support to the grid, thereby enabling the MMCs to work as Static Compensators (STATCOMs). However, when such MMCs are operating as STATCOMs, SM capacitor voltage balancing techniques may require modifications after DC fault occurrence. Furthermore, fault current suppression times will also need to be taken into consideration when such fault-tolerant MMCs are operated as STATCOMs to ride through the DC side fault.

Various studies have compared SMs with fault blocking capability that can be utilized in HVDC systems. Some have gone further to discuss the fault ride through ability of a certain subset of such SMs. However, very few have provided a comprehensive review of all the issues along with providing appropriate control designs for fast DC fault current suppression.

1.2 Objectives

To address the shortcomings in the past work regarding a thorough review of SM configurations with fault blocking and ride through capabilities for MMC-based HVDC systems, and control schemes for fast DC fault current suppression and STATCOM operation, the objectives of this thesis are as follows:

- Providing a comprehensive literature review on fault blocking configurations and fault ride through techniques in MMCs; and
- Designing an appropriate control scheme that can be utilized in fault-tolerant MMC configurations to facilitate fast DC fault current suppression while riding through DC faults.

1.3 Thesis Outline

To achieve the objectives of this research, the thesis is organized as follows:

- Chapter 2 presents a thorough literature review of MMCs from DC fault blocking and DC fault ride through viewpoints. In the first part, notable fault blocking MMC SMs are reviewed and compared. This is followed by a survey of DC fault blocking hybrid configurations. In the final part, a survey of MMC DC-FRT techniques in STATCOM operation mode with accompanying changes to SM capacitor energy balancing methods is presented.

- Chapter 3 attempts to address the gap in research on fast DC fault current suppression techniques during STATCOM operation mode. An existing state space-based averaging method to control the rate of rise of fault current by SM capacitor discharge in MMCs based on HBSMs is first analyzed and then modified to adapt for MMCs based on FBSMs. The developed scheme is tested on a point-to-point FB-MMC based HVDC system.

- Chapter 4 provides a summary of the thesis, lists the contributions made, and suggests avenues for further research.

Chapter 2
Literature Review

2.1 Introduction

HVDC transmission has received substantial attention and has gone through notable developments in the last few decades, particularly due to its suitability for renewable energy integration. LCCs used to be the predominant technology in HVDC systems, but VSCs have recently gained popularity due to their smaller footprint, as well as decoupled active and reactive power control, voltage support provision, and black-start capabilities. MMC is the most recent addition to the VSC family. MMCs are now being widely implemented in both medium and high voltage transmission systems since they address many of the limitations encountered in conventional VSCs, such as scalability to higher voltages by addition of more SMs, provision of smooth output voltage waveforms at a lower switching frequency, and elimination of low-order harmonics which typically require large filters [5], [6].

Designing appropriate protection means for HVDC systems is more challenging when compared to HVAC systems due to the lack of zero-crossing in the DC current and limitations in overload capability of semiconductor devices used in the converters. The latter is particularly true in the case of VSC-HVDC systems where IGBTs replace the thyristor switches that are prevalent in LCCs. As a result, high-speed protection is essential for HVDC systems to match the high rate of rise as well as the high steady-state value of fault current.

DC faults in the HVDC transmission system can be categorized into pole-to-ground and pole-to-pole faults [7], [8]. During pole-to-ground faults, the voltage of the unfaulted pole would rise to twice the rated value [9]. For unearthed or high impedance grounding systems on the DC side, pole-to-ground faults will not lead to overcurrent but will cause significant voltage stresses. Pole-to-pole faults on the other hand will give rise to very high DC side fault currents, especially in low impedance grounding systems.

MMCs consist of stacks of cells or SMs. The simplest and most economical SM topology is the HBSM. Due to the presence of freewheeling diodes in HBSMs, they are unable to prevent AC side contribution to DC faults. DCCBs may be used to clear DC faults when HBSMs are utilized [10]. DCCBs can be classified into three main types: mechanical, solid-state, and hybrid. Mechanical DCCBs [11], [12] are typically slow in clearing DC faults and this may lead to damage to the semiconductor

devices. Solid-state CBs [13], [14], [15] have a much faster response to faults, but they are significantly more expensive and have high on-state losses. Hybrid DCCBs are a combination of semiconductor devices and mechanical switches, featuring lower conduction losses; however, they are expensive and have a large footprint [16]. The use of ACCBs on the AC side is another option to clear DC faults. However, ACCBs take a few cycles to trip and are not adequately fast for HVDC systems protection [17].

Recent research has focused on taking advantage of the inherent fault blocking capability of SMs with modified designs. Such modifications can provide a reverse voltage in the path of fault current, thus driving the current down to zero. Furthermore, certain fault blocking SMs may also be utilized as wave-shaping circuits to control the AC currents during the fault and provide reactive power support to the grid. Full-bridge SM (FBSM) was developed by adding two switches to the HBSM structure to provide DC fault blocking capability. However, it has nearly double the conduction losses and device count when compared to the HBSM. Several SM configurations have been developed over the years that provide DC fault blocking capability with lower losses and device count than those of FBSM, giving rise to a class of DC fault blocking converters. Therefore, there is a crucial need for a comparative evaluation of various proposed SM configurations, rather than comparing them only against the FBSM, to identify a suitable configuration for any given application. Moreover, one of the most challenging tasks in an MMC is the energy balancing of the floating capacitors in the SMs. For proper operation, MMC control needs to regulate the total energy stored in the SM capacitors. This can be done either by controlling the voltages of the capacitors in the SMs [18] or by taking an energy-based approach where the total energy of the SMs in the converter arms and legs are regulated. The energy-based approach, first introduced in [19], has gained popularity in recent years since it achieves balancing by manipulating the circulating currents without affecting the output currents [20].

Several reviews, with MMCs as the focus, have been published in recent years. In [6], the development and future trends of MMC topologies were presented along with the technical challenges associated with notable MMC control methods. However, the DC fault tolerance of certain MMC SMs was not discussed in detail. Similarly, MMC modulation and control strategies were reviewed in [18]. Two modified SM configurations were proposed, as well, but details of DC-FRT mechanisms were not discussed. The authors in [21] have provided a general overview of the MMC with regards to modeling, control, notable topologies, and applications. DC side fault mitigation by utilizing fault blocking SMs was mentioned but not elaborated on. In [22], notable approaches related to fault diagnosis, fault

tolerance techniques, and MMC control during faults conditions were reviewed. Once again, an extensive analysis of DC fault blocking SMs and DC FRT techniques were not provided. In [23], SM configurations were discussed in terms of component requirements, conduction losses, and fault blocking ability. However, only a few SM configurations were discussed, and hybrid configurations were left out altogether. Reference [24] provided a more comprehensive review of DC fault blocking SMs as well as DC-FRT methods by utilization of the MMC as STATCOMs. Even though DC-FRT mechanisms of different topologies were discussed, the energy balancing strategies utilized during STATCOM operation were not addressed. Similarly, the focus of [25] was on the STATCOM operation of fault blocking configurations; however, only a small number of SM configurations were discussed, and the energy balancing issue was left untouched.

In this chapter, notable DC fault blocking SM and MMC configurations are reviewed and compared in terms of component requirements, conduction losses, and DC fault blocking capability. The ability of certain MMC configurations to ride through DC side faults and work as STATCOMs is also investigated along with arm and leg energy balancing strategies employed during DC fault operation.

2.2 MMC Structure and Operation

The generic structure of a three-phase MMC is shown in Figure 2.1(a). Each arm of the converter is comprised of N series-connected SMs along with an inductor. The purpose of the arm inductor is two-fold: filtering high-frequency components in the circulating current and limiting the fault current [26]. The SMs are made up of capacitors, and semiconductor switches and are capable of producing two or more voltage levels. Each MMC arm can generate the full DC link voltage, V_{DC}. The number of inserted SMs in the upper and lower arms is varied to generate a multilevel waveform at the AC terminals. The phase x terminal voltage, v_x ($x \in a, b, c$) in Figure 2.1(a), may be expressed in either one of the following ways

$$v_x = \frac{V_{DC}}{2} - v_{xu} - L\frac{di_{xu}}{dt}, \tag{2.1}$$

$$v_x = -\frac{V_{DC}}{2} + v_{xl} + L\frac{di_{xl}}{dt}, \tag{2.2}$$

where v_{xu} and v_{xu} denote the total upper and lower arm SM voltages, and i_{xu} and i_{xl} are the upper and lower arm currents in each phase. The modulation index m, is defined as the ratio of the peak value of the AC side phase-to-neutral voltage to half of the DC link pole-to-pole voltage,

$$m = \frac{\widehat{V}_x}{0.5V_{DC}}. \tag{2.3}$$

According to (2.3), operating in the overmodulation region ($m > 1$) is possible if the SMs can generate both negative and positive voltages. Operation in the overmodulation region is beneficial in cases of DC link voltage reduction, as explained in [27]. If a certain portion of SMs in the arm is allowed to generate a negative voltage state following a DC side voltage drop, the peak voltage obtained on the AC side can be kept nearly constant (leading to m becoming greater than 1). This would ensure continued converter operation even in cases of a significant reduction in DC side voltage. Furthermore, in [28] and [29], it has been shown that the normal operation of FB-MMC and mixed FB/HB-MMC systems in the overmodulation region reduces the energy storage requirement of the SM capacitors. This facilitates the reduction of converter size and cost.

The arm currents (i_{xu} and i_{xl}) in each phase of the MMC as shown in Figure 2.1(a) can be expressed as a combination of the AC output current i_x and a common-mode current i_{xz} [30],

$$i_{xu} = i_{xz} + \frac{1}{2} i_x, \tag{2.4}$$

$$i_{xl} = i_{xz} - \frac{1}{2} i_x, \tag{2.5}$$

where the common-mode current represents a combination of the DC bus current (I_{DC}) and AC circulating current components. The DC part of the common-mode current is responsible for active power flow through the converter while the AC part, which is a negative sequence current, causes power loss in the converter and needs to be suppressed [31]. Traditional vector control methods [32], [33], [34] are commonly implemented in MMC-HVDCs. Various modulation methods, such as the nearest level modulation [35], [36] and high-frequency carrier-based sinusoidal pulse width modulation techniques [37], [38], [39], [40] can be employed for the generation of the AC side waveforms. Since MMC SMs contain capacitors, voltage balancing [41], [42], [43] and sorting algorithms are also implemented to keep the capacitor voltages close to their nominal values.

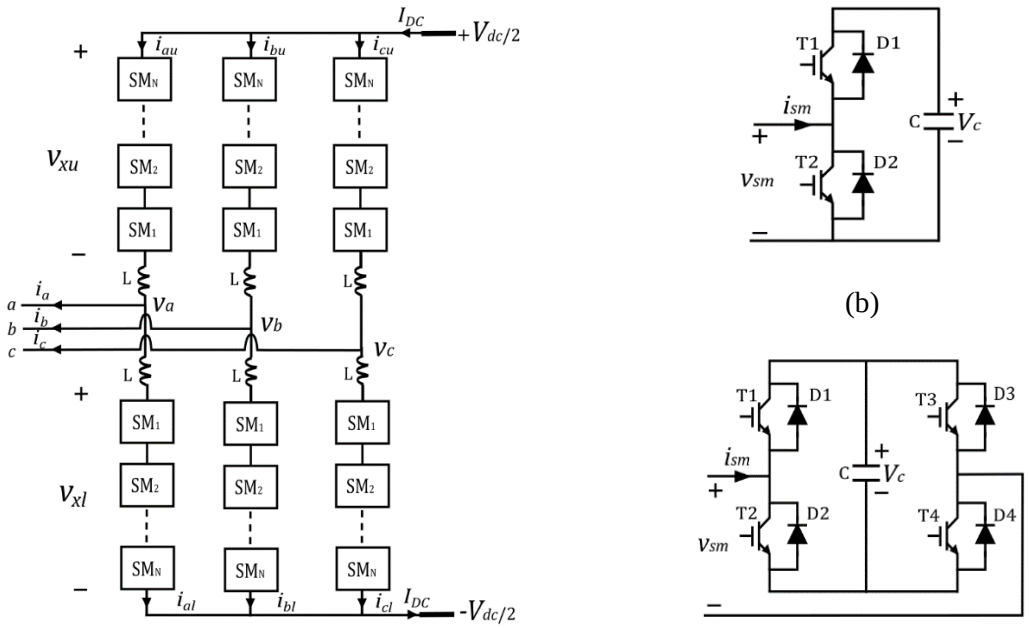


Figure 2.1 (a) Structure of a three-phase MMC; (b) the Half-Bridge SM (HBSM); (c) the Full-Bridge SM (FBSM)

The HBSM structure is depicted in Figure 2.1(b). It is capable of generating two voltage levels as shown in Table 2.1. The absence of a negative voltage state means that the modulation index is limited to a maximum value of 1 or 1.15 with selective harmonic elimination. On the other hand, the FBSM, shown in Figure 2.1(c), can generate three voltage levels: 0, V_c and $-V_c$, as shown in Table 2.2. Hence, the FBSM is a bipolar SM that can generate negative voltage states not only during fault blocking but also during normal operation [44], which is an essential feature when overmodulation capability is required in the converter.

Table 2.1 HBSM Switching States

Blocking State	
i_{sm}	v_{sm}
>0	V_c
<0	0
Normal Operation	
Switches ON	v_{sm}
T2	0
T1	V_c

Table 2.2 FBSM Switching States

Blocking State	
i_{sm}	v_{sm}
>0	V_c
<0	-V_c
Normal Operation	
Switches ON	v_{sm}
T1,T3	0
T2,T4	0
T2,T3	-V_c
T1,T4	V_c

A DC side fault event in MMC-HVDC systems can be divided into three stages [45], [46] [47], [48], [49] similar to VSC-HVDC systems [50]. In the first stage, the MMC is still able to generate the AC side voltages and therefore the AC side currents remain controlled. So, the fault current in this first stage consists mainly of a DC component due to the discharge of the SM capacitors. The main consequence of the discharge of the capacitors is that the MMC can no longer generate the AC side voltages and starts to lose control of the AC side currents. So, in the second stage, the AC side starts contributing to the fault; thus, there will be an AC component in the fault current in addition to the DC component. In the third stage, all IGBT switches in the SMs are blocked which prevents the further discharge of the capacitors. However, depending on the type of SM used, the AC side may still feed the DC side fault [51] due to the presence of freewheeling diodes in the SMs.

In the case of a pole-to-ground fault in the HB-MMC, for a positive SM current (i_{sm}>0 in Figure 2.2(a)), diode D1 and the capacitor in each of the SMs appear in the fault current path. The total capacitor voltage of the HBSMs in each MMC arm equals V_{DC}. Meanwhile, the peak AC voltage is equal to $V_{DC}/2$ from (1) and (2). Since the reverse voltage generated by the MMC arm is greater than the peak AC grid phase voltage, diode D1 is reverse biased and the fault current is suppressed. However, when is i_{sm}<0 (Figure 2.2(b)), the SM capacitors are bypassed entirely, and no reverse voltage is inserted by the SM capacitors in the current path. Therefore, the AC side source feeds the pole-to-ground fault on the DC side. Considering the case of a pole-to-pole fault in the HB-MMC, the fault current from a particular phase enters one of the arms, circulates through the fault, and returns via a different arm into another phase. For i_{sm}>0, the reverse voltage provided by each MMC arm equals V_{DC}, but since two arms are in operation, the total reverse voltage in the fault current path is $2V_{DC}$. At

the same time, the peak line-to-line AC side voltage is $\sqrt{3}V_{DC}/2$. Once again, as the reverse voltage from the MMC arms is greater than the peak-to-peak AC voltage, the fault current is suppressed. However, when the SM current direction reverses, all HBSM capacitors are bypassed, and the AC line voltage feeds the DC side fault. Regardless of the type of fault, the HBSM is incapable of blocking the AC grid contribution to the DC side fault. In the case of the FBSM, the presence of the two additional IGBTs along with their antiparallel diodes ensures that regardless of the arm current direction, the capacitor in each SM is inserted with the opposite polarity in the fault current path when a DC side fault occurs and all IGBTs in the SMs are blocked (Figures 2.3(a) and 2.3(b)).

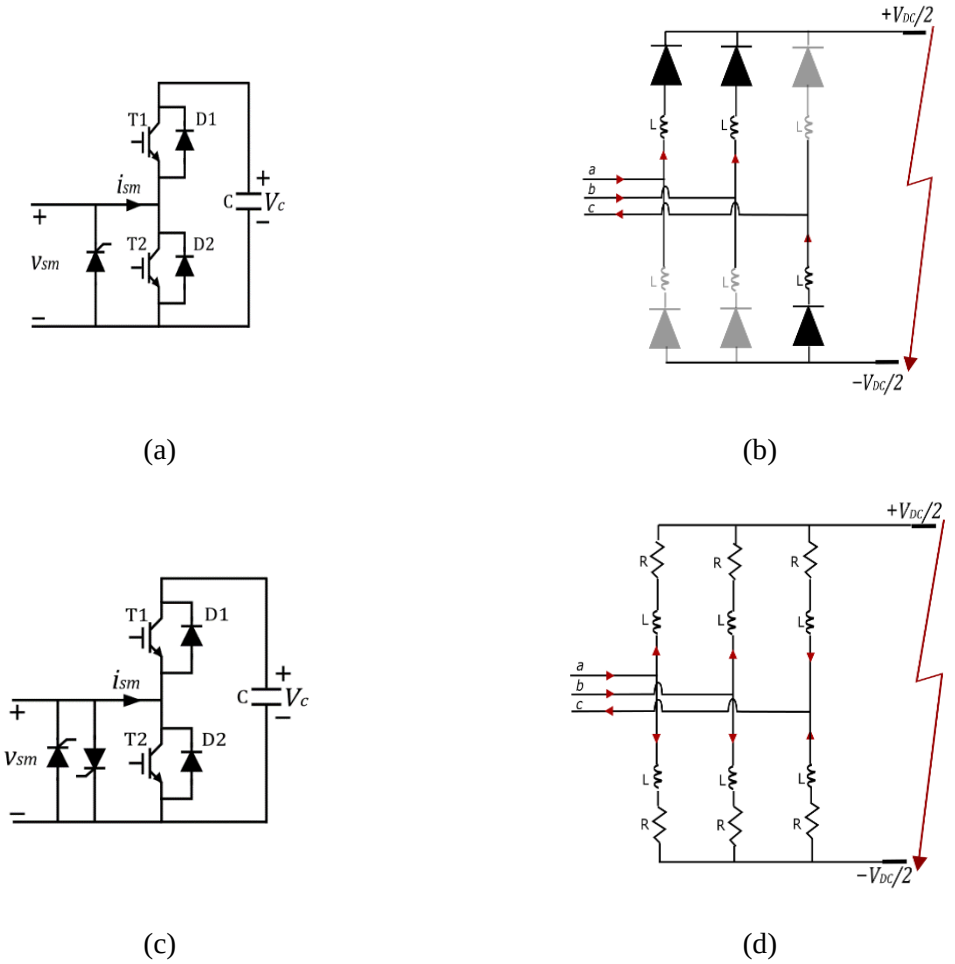
The increased power losses and device cost of additional switches in FBSMs have led some researchers to focus on modification of the HBSM configuration to protect the MMC from overcurrent. The single thyristor switch scheme [52], [53] (Figure 2.4(a)) adds a thyristor across the AC terminals of the traditional HBSM; this thyristor is fired once a DC side fault is detected (Figure 2.4(b)). Since thyristor current carrying capability is higher than that of diodes, this design helps to protect the diodes from overcurrent during a DC fault. The authors i [54] n proposed the double thyristor switch scheme (Figure 2.4(c)). When both thyristors are fired after the occurrence of a DC fault, the MMC arms are converted into six *RL* branches as shown in Figure 2.4(d). This effectively converts the DC side short circuit into an AC short circuit. The DC fault current decays to zero, but the AC short circuit currents continue to flow in the arms of the MMC and therefore such a design is only suitable for non-permanent faults.

(a) (b)

Figure 2.2 Fault current path: (a) HBSM for i_{sm} >0; (b) HBSM for i_{sm} <0

(a) (b)

Figure 2.3 Fault current path: (a) FBSM for i_{sm} >0; (b) FBSM for i_{sm} <0



(a) (b)

(c) (d)

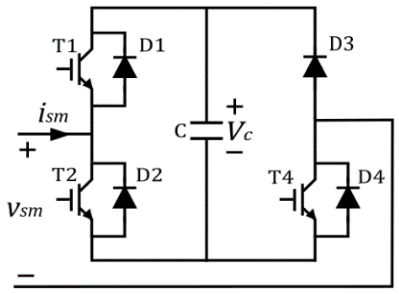
Figure 2.4 (a) Single thyristor switch scheme; (b) Single thyristor switch scheme equivalent circuit during pole-to-pole fault; (c) Double thyristor switch scheme; (d) Double thyristor switch scheme equivalent circuit during pole-to-pole fault

2.3 Fault Blocking SM Configurations

In the following subsections, the pros and cons of several noteworthy MMC SM configurations with fault blocking capability will be discussed.

2.3.1 SMs based on Standard HB and FB Structures

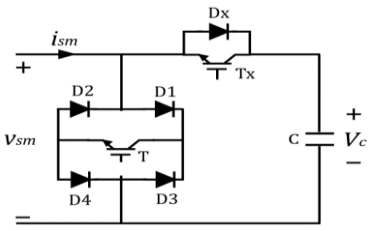
Removing a single IGBT from the standard FBSM results in the Unipolar Full-Bridge Submodule (UFBSM) structure [55], as shown in Figure 2.5. Since D3 is unidirectional, the SM is unable to generate a negative voltage during normal operation. Fault blocking operation remains intact, but overmodulation is no longer possible. This structure features a slightly lower device count than the FBSM albeit with similar conduction losses.



Blocking State	
i_{sm}	v_{sm}
>0	V_c
<0	-V_c
Normal Operation	
Switches ON	v_{sm}
T2,T4	0
T1,T4	V_c

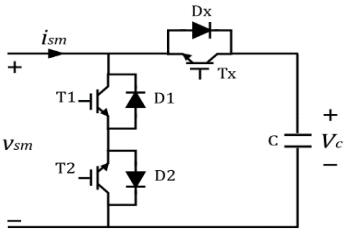
Figure 2.5 UFBSM

Authors in [56] proposed two types of SM by modifying the bypass switch in the traditional HBSM, as shown in Figures 2.6(a) and 2.6(b). The Type I SM inserts two diodes and one IGBT in the conduction path for the zero-voltage/bypass state. As a result, conduction losses in Type I are higher when compared to Type II SM, which inserts one diode and one IGBT in the conduction path for the zero-voltage/bypass state. Therefore, conduction losses of Type II SMs are comparable to those of the standard HBSM. The proposed structure achieves DC fault blocking by removing the gating signals to the IGBTs. For i_{sm}>0, the fault current is suppressed by the capacitors. For i_{sm}<0, the bypass switches that have been turned off, prevent the flow of the fault current. This implies that there is no alternate conduction path for the fault current which may create overvoltage and subsequent damage to semiconductor switches. For this reason, the authors proposed the use of RC filters at the AC terminals to provide a path for the fault current. However, the adoption of such filters would lead to an increase in the overall cost.



Blocking State	
i_{sm}	v_{sm}
>0	V_c
<0	--
Normal Operation	
Switches ON	v_{sm}
T	0
T_x	V_c

(a)



Blocking State	
i_{sm}	v_{sm}
>0	V_c
<0	--
Normal Operation	
Switches ON	v_{sm}
T1,T2	0
T_x	V_c

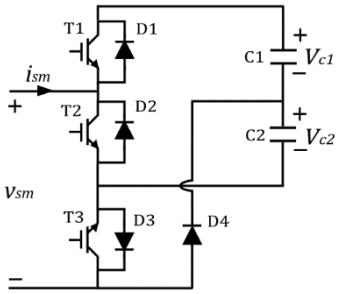
(b)

Figure 2.6 HBSM with modified bypass switch: (a) Type I; (b) Type II

2.3.2 The Clamp Circuit based Submodules

The Diode Clamp Submodule (DCSM) structure proposed in [57] (Figure 2.7) is formed by adding two diodes (D3 and D4) and an IGBT (T3) to the standard HBSM. The number of switches in DCSM is the same as that in UFBSM. Similarly, the DCSM does not support bipolar operation. Each SM has two capacitors but there are only two voltage levels available during normal operation. This is because there is no individual control over the insertion of the capacitors into the current path. To ensure an even comparison with other SM configurations, the total voltage ($V_{c1} + V_{c2}$) across the two capacitors in the SM is taken to be equal to V_c, implying that with identical capacitances the voltage across each would then be $V_{DC}/2N$. The IGBT T3 is always kept on during normal operation, which means there are two switches in the conduction path as is the case of the UFBSM/FBSM. During DC faults, the SMs are blocked. When i_{sm}>0, both capacitors are inserted into the current path to oppose the flow of the current leading to a total reverse voltage of V_{DC} being generated by each arm. For i_{sm}<0, the current is directed through diode D4 which inserts capacitor C2 into the current path with a total reverse voltage of $V_{DC}/2$ being inserted into the current path by each arm. For i_{sm}>0, both capacitors C1 and C2 are utilized for fault blocking while for i_{sm}<0 only capacitor C2 is available for fault blocking. Such an asymmetry during fault blocking leads to longer fault current suppression times [58]. One benefit of this SM is that the blocking voltage of T3, D3 and D4 needs to be only $V_{DC}/2N$, or half the maximum blocking voltage

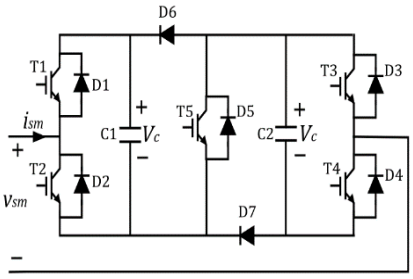
in an FBSM. UFBSMs/FBSMs require all switches to be capable of blocking the full SM voltage (V_{DC}/N).



Blocking State	
i_{sm}	v_{sm}
>0	$V_{c1}+V_{c2}$
<0	V_{c2}
Normal Operation	
Switches ON	v_{sm}
T2,T3	0
T1,T3	V_c

Figure 2.7 DCSM

The Clamped Double Submodule (CDSM) [58], shown in Figure 2.8, contains two capacitors and can generate three voltage states: $0, V_c$ and $2V_c$. The CDSM is incapable of generating negative voltages during normal operation. While two FBSMs use a total of four switches to generate the three voltage states, CDSM requires only three switches resulting in lower conduction losses. During faults, both capacitors are involved in the blocking operation when the SM current direction is positive. For the negative current direction, the SM capacitors are inserted in parallel and hence the reverse voltage generated per arm is $V_{DC}/2$. The equivalent circuit of a CDSM-based MMC during a pole-to-pole DC side fault is shown in Figure 2.9.



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T3,T5	0
T1,T3,T5	V_c
T2,T4,T5	V_c
T1,T4,T5	$2V_c$

Figure 2.8 CDSM

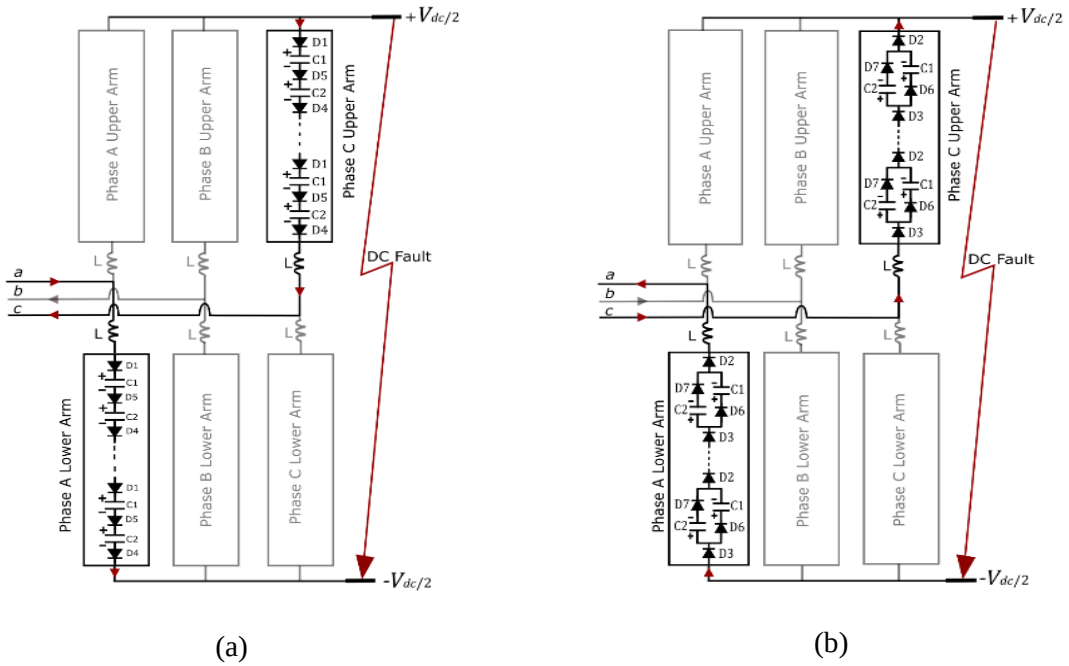
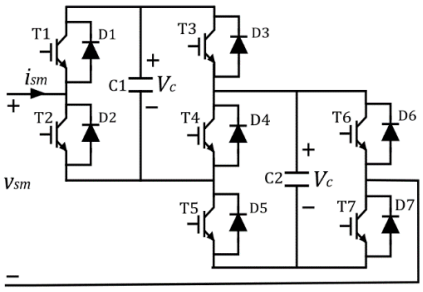


Figure 2.9 Fault current path for pole-to-pole fault in the CDSM-based MMC, showing one phase for (a) i_{sm} >0 and (b) i_{sm} <0

The Semi Full-Bridge Submodule (SFBSM) proposed in [59] and illustrated in Figure 2.10 is derived from CDSM. The diodes D6 and D7 in CDSM are replaced by active switches to facilitate bipolar operation. This structure allows the SM capacitors to be connected in parallel with either polarity resulting in a reduced number of voltage sensors, which is a definite advantage when sorting algorithms are utilized to ensure SM capacitor voltages in the arms remain nearly constant during MMC operation. For instance, the widely implemented algorithm presented in [60] sorts the SM capacitor voltages in order of magnitude. Afterward, depending upon the arm current direction and the number of SMs to be inserted in the arm, SMs with the lowest (highest) voltage magnitudes are selected to be in the current path to be charged (discharged). Implementation of such an algorithm requires all SM capacitor voltages to be monitored using voltage sensors. The number of required sensors is equal to the number of capacitors implying that the sorting algorithm will need a significantly high number of sensors for voltage balancing if each SM contains more than one capacitor. The utilization of the switching state enabling parallel connection of the two capacitors within each SM ensures both capacitors remain at the same voltage level such that only one voltage sensor per SM is sufficient to monitor the capacitor voltages.

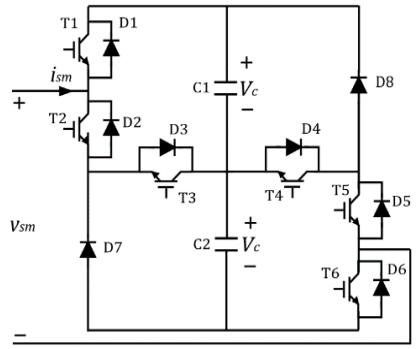
SFBSM on-state losses are comparable to those of CDSM, as three switches are sufficient to realize output voltage levels 0 and $2V_c$. It is only the parallel connection mode ($-V_c$, V_c) that involves the use of four switches. Fault blocking is asymmetrical with only capacitor C_1 available to suppress the fault current when i_{sm}<0.



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T5,T7	0
T1,T3,T6	0
T1,T3,T5,T7	V_c
T2,T3,T5,T6	$-V_c$
T1,T4,T7	$2V_c$

Figure 2.10 SFBSM

The Active Clamped T-type Submodule (ACTSM) proposed in [61] is unipolar with symmetrical DC fault blocking capability. The SM structure and switching states are shown in Figure 2.11. When either one of the capacitors is inserted into the current path, three switches are operational; however, when both capacitors are inserted, only two switches are required to be on. This is a definite advantage as two FBSMs require four switches to produce the $2V_c$ output level. Conduction losses in ACTSM are seen to be lower compared to those of other symmetrical fault blocking topologies, including the FBSM and the cross connected SMs that will be introduced later.



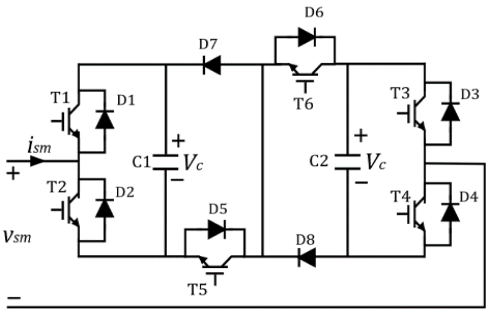
Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-2V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T3,T4,T5	0
T1,T4,T5	V_c
T2,T3,T6	V_c
T1,T6	$2V_c$

Figure 2.11 ACTSM

Among the clamped SMs, the SFBSM has the highest number of switches in the conduction path and therefore would exhibit the highest conduction losses. However, reduced voltage sensor requirement is a definite advantage in terms of cost. The CDSM has lower conduction losses but is only capable of unipolar voltage generation, making overmodulation impossible. Meanwhile, the ACTSM has comparable conduction losses when compared to the CDSM three and has bipolar voltage generation capabilities. The only drawback is the lack of the parallel SM capacitor insertion state when compared to the SFBSM.

2.3.3 The Cross Connected Submodules

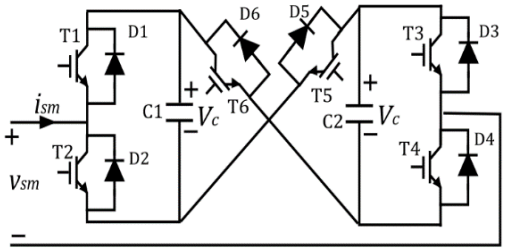
The Three-Level Cross Connected Submodule (TLCCSM) presented in [62] can be thought of as two HBSMs connected in series using a clamp circuit, as illustrated in Figure 2.12. Fault blocking is symmetrical; however bipolar operation is not possible due to the presence of diodes in the clamp circuit. Four switches need to be operational for the realization of all voltage states, making the conduction losses comparable to those of FBSMs. TLCCSM has a lower device cost compared to the FBSM as two of the IGBT switches are replaced with diodes.



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-2V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T3,T5,T6	0
T1,T3,T5,T6	V_c
T2,T4,T5,T6	V_c
T1,T4,T5,T6	$2V_c$

Figure 2.12 TLCCSM

The Five-Level Cross Connected Submodule (FLCCSM) [63] (Figure 2.13) is comprised of two HBSMs cross connected using two switches. All five output voltage levels 0, V_c, $2V_c$, $-V_c$ and $-2V_c$ require the operation of three switches, making conduction losses comparable to those of the CDSM. Bipolar voltage output enables operation in the overmodulation region if required. A major shortcoming of the FLCCSM is that the clamp switches need to withstand the combined voltage of the two SM capacitors ($2V_c$) and may require a series connection of two switches, which will lead to higher conduction losses than that of the FBSM.



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-2V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T3,T5	0
T1,T4,T6	0
T1,T3,T5	V_c
T2,T4,T5	V_c
T2,T4,T6	$-V_c$
T1,T3,T6	$-V_c$
T1,T4,T5	$2V_c$
T2,T3,T6	$-2V_c$

Figure 2.13 FLCCSM

The Series-Connected Double SM (SDSM) [64], also called Three Level SM in [55], is derived from FLCCSM by removal of the bidirectional switch T6 and replacing it with a unidirectional switch. The outcome is a slight reduction in device count while keeping DC fault blocking operation symmetrical; however, the SM becomes unipolar as a result.

The FLCCSM has a clear advantage over the TLCCSM in terms of conduction losses Moreover, it has bipolar voltage generation capability which is missing in the TLCCSM. However, if two IGBTs in series are installed in the clamp switches, then the FLCCSM would be inferior to the TLCCSM when conduction losses are compared.

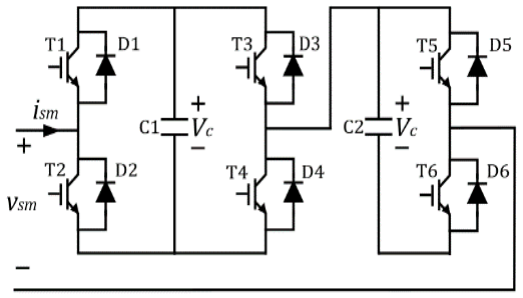
2.3.4 Other Fault Blocking SMs

This subsection presents fault blocking SM structures that do not fall under broader categories.

2.3.4.1 Mixed Submodules

The Mixed Submodule (MSM) [65], [66] is a series connection of an HBSM and any fault blocking submodule. The MSM provides asymmetrical fault blocking due to the presence of HBSMs but has overmodulation capability. The most common type of MSM is formed by combining HBSMs and FBSMs as illustrated in Figure 2.14. Generation of all voltage levels in such an MSM structure requires the operation of three switches, making on-state losses the same as in CDSM. However, when compared

to CDSM, it has one more IGBT and one less diode, resulting in a slight increase in the semiconductor device cost.



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$
Normal Operation	
Switches ON	v_{sm}
T1,T3,T5	0
T2,T4,T5	0
T2,T3,T6	0
T1,T4,T5	V_c
T1,T3,T6	V_c
T2,T4,T6	V_c
T2,T3,T5	$-V_c$
T1,T4,T6	$2V_c$

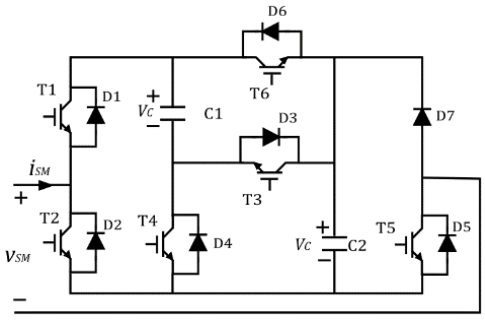
Figure 2.14 MSM

When a single capacitor cell structure such as the FBSM is used in an MSM as the fault blocking SM, replacing 50% of the HBSMs with FBSMs is sufficient to block both pole-to-pole and pole-to-ground faults on the DC side [66]. On the other hand, in an MSM configuration comprised of fault blocking SM containing two capacitors in the cell, the calculation to determine the minimum required number of fault blocking SMs is done differently as described in [62]. In MSM configurations, if double capacitor SMs with symmetrical fault blocking capability are utilized, 50% of the HBSMs in the mixed configuration will need to be replaced with fault blocking SMs for suppressing pole-to-ground faults while 44% replacement is enough for pole-to-pole fault current clearance [62]. If double capacitor SMs with asymmetric fault blocking capability are used, all SMs in the arms will need to be of the fault blocking type for suppression of pole-to-ground faults while an 88% replacement is sufficient when only pole-to-pole fault current suppression is desired.

2.3.4.2 Composite Submodules

The Composite Module (CSM) proposed in [67] is shown in Figure 2.15 along with its switching states. Like SFBSM, CSM has additional voltage states allowing the SM capacitors to be inserted in parallel with either polarity, which helps with capacitor voltage balancing. The conduction losses in this module

are lower than those of SFBSM since the number of switches in the conduction paths for 0 and $2V_c$ voltage states are lower than that in SFBSM by one.

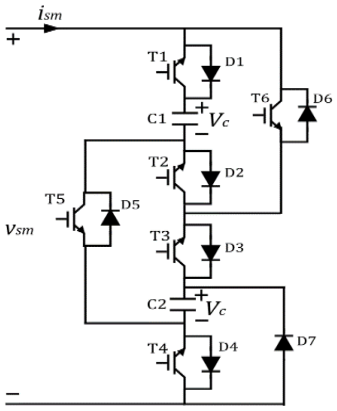


Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T5	0
T1,T4,T5	V_c
T1,T5,T6	V_c
T1,T4,T5,T6	V_c
T1,T3,T5	$2V_c$

Figure 2.15 CSM

2.3.4.3 Switched Capacitor Submodule

The motivation behind the development of the Switched Capacitor Submodule (SCSM) [68] was to reduce the total number of voltage sensors. The SCSM shown in Figure 2.16 does not support bipolar operation and provides asymmetrical fault blocking. The 0 and $2V_c$ voltage states are obtained using four switches. The V_c voltage state is obtained either by insertion of an SM capacitor into the circuit using three switches or by the parallel insertion of the SM capacitors (similar to the case of SFBSM) which would increase the number of conducting switches to five. It is noteworthy that the generation of all voltage states requires conduction through one extra switch compared to SFBSM.

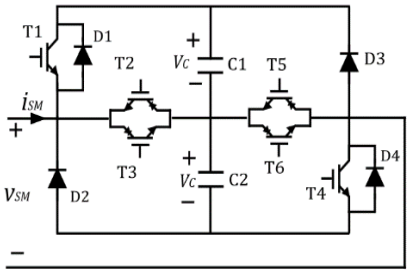


Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	V_c
Normal Operation	
Switches ON	v_{sm}
T2,T4,T5,T6	0
T1,T4,T5	V_c
T3,T4,T6	V_c
T1,T3,T4,T5,T6	V_c
T1,T2,T3,T4	$2V_c$

Figure 2.16 SCSM

2.3.4.4 Double Reverse Blocking Submodule

The Double Reverse Blocking Submodule (DRBSM) proposed in [69] is shown in Figure 2.17. The reverse blocking IGBT (RB-IGBT) unit consists of two antiparallel RB-IGBTs. Symmetrical fault blocking is provided with only two switches in on-state for any of the voltage states. This is an improvement over other SM configurations since conduction losses are comparable to HBSMs; however, the lack of overmodulation capability is considered a drawback.

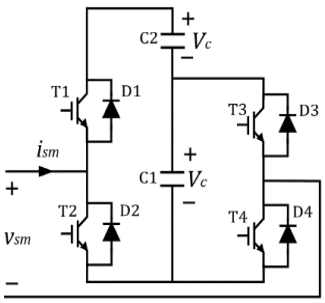


Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-2V_c$
Normal Operation	
Switches ON	v_{sm}
T2/T3,T5/T6	0
T1,T5/T6	V_c
T2/T3,T4	V_c
T1,T4	$2V_c$

Figure 2.17 DRBSM

2.3.4.5 Asymmetric Full-Bridge Submodule

The Asymmetric Full-Bridge Submodule (AFBSM) [70], shown in Figure 2.18, is a bipolar SM capable of asymmetrical fault blocking. During normal operation, only two switches need to be operational to attain the four voltage levels; hence, the advantage of this configuration is in its low conduction losses. However, switches T1 and T2 need to withstand the sum of the voltages of two capacitors. Therefore, they need to be rated at higher voltages or a series connection of two switches may be required, which would result in increased conduction losses.



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$
Normal Operation	
Switches ON	v_{sm}
T2,T4	0
T1,T3	V_c
T2,T3	$-V_c$
T1,T4	$2V_c$

Figure 2.18 AFBSM

2.4 Comparative Evaluation of different SM Configurations

A comparison of SM configurations in terms of device count, number of required voltage sensors, number of switches in the conduction path, overmodulation capability, and fault blocking symmetry is provided in Table 2.3. Among the SM configurations discussed in the previous section, configurations such as the SFBSM and SCSM, that allow parallel connection of capacitors, are desirable when employing a lower number of voltage sensors is important. The analysis suggests that further research on SCSM and SFBSM configurations would add significant value since employing a lower number of voltage sensors would lead to significant cost reduction. AFBSM is the preferred configuration if reducing conduction losses is a priority. However, fault blocking in AFBSM is asymmetrical leading to longer fault current suppression times. Meanwhile, the FLCCSM is capable of both overmodulation and symmetrical fault blocking. For both the AFBSM and the FLCCSM, the voltage ratings of IGBT switches need to be twice those for other SMs, leading to high cost and conduction losses. The MSM (with a mix of HB and FBSMs) and the CDSM configurations are similar to the FLCCSM in terms of device count and conduction losses. While the CDSM is unipolar, making overmodulation impossible, the MSM has bipolar voltage generation capability. Moreover, MSM with a mix of HB and FB modules would be commercially viable since significant research has already been conducted on the operation, control, and voltage balancing of such systems including operation in the overmodulation region.

Table 2.3 Comparison among different Fault Blocking SMs

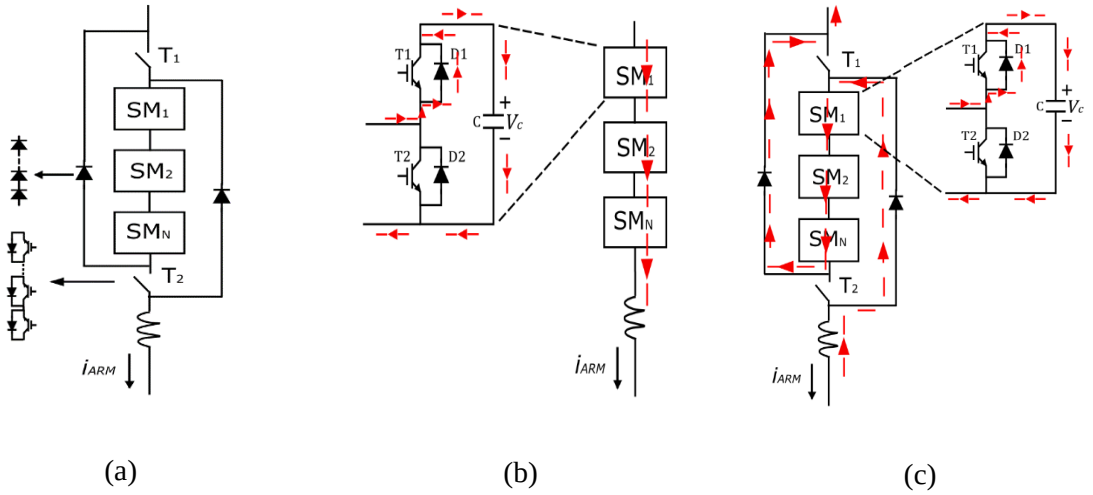
	FBSM (2 SMs)	**UFBSM (2 SMs)**	**DCSM (2 SMs)**	**CDSM**	**SCSM**	**SFBSM**	**CSM**	**TLCCSM**	**FLCCSM**	**ACTSM**	**AFBSM**	**Mixed SM**
No. of IGBTS	8	6	6	5	6	7	6	6	6	6	4	6
No. of diodes	8	8	8	7	7	7	1	8	6	8	4	6
No. of switches in conduction path for $0/V_c/2V_c$ states	4/4/4	4/4/4	4/4/4	3/3/3	4/5/4	3/4/3	2/4/3	4/4/4	3/3/3	4/3/2	2/2/2	3/3/3
No. of voltage sensors	2	2	2	2	1	1	1	2	2	2	2	2
Overmodulation	Yes	No	No	No	No	Yes	Yes	No	Yes	No	Yes	Yes
Symmetrical DC fault blocking	Yes	Yes	No	No	No	No	No	Yes	Yes	Yes	No	No

2.5 Hybrid Configurations

Hybrid MMC configurations aim to optimize converter performance in various ways, including combining two different SM configurations or making adjustments in the MMC structure. The majority of hybrid configurations involve the use of FBSMs in a two-level converter structure. The two-level VSC features low semiconductor device requirement compared to MMCs but requires the use of high-frequency pulse width modulation (PWM) to obtain a sinusoidal output voltage of acceptable quality. Moreover, the generation of only two voltage levels requires turning switches on and off under high currents and voltages, leading to high losses in the switches, especially at a high switching frequency. Furthermore, the two-level VSC is not capable of providing DC fault protection. Recent research in this area has involved the placement of FBSMs either on the AC or DC side of the two-level converter leading to various innovative designs. This section will describe such configurations and will touch upon noteworthy hybrid MMCs as well.

2.5.1 Improved HBSM-based MMC

Authors in [71] proposed an improved HBSM-based MMC (Figure 2.19 (a)) where the director switches (T_1, T_2) and diodes are installed around each arm. During normal operation, the director switches are kept closed and the operation of the improved HBSM-based MMC is identical to that of conventional HB-MMC. After the occurrence of a DC side fault, all IGBTs in the director switches and the HBSMs are blocked. For the positive arm current direction (Figure 2.19 (b)), the director switches are shorted, but the HBSM capacitors are capable of providing the necessary reverse voltage. When the current direction reverses, the antiparallel diodes in the director switches block the flow of the arm current. The current is then redirected into the opposite terminal of the MMC arm through the diodes connected in parallel to it such that the current flow direction through the SMs remains the same (Figure 2.19 (c)). This ensures continued blocking of the fault current by the HBSM capacitors. The director switches will thus need to withstand significant high voltage stresses during faults and ensure conduction through the alternate path.



(a) (b) (c)

Figure 2.19 (a) Improved HBSM-based MMC arm; (b) fault current path through one arm when i_{ARM} >0; (c) fault current path through one arm when i_{ARM} <0

2.5.2 Alternate Arm Converter

The Alternate Arm Converter (AAC) [72], [73], [74] is derived by placing the cascaded FBSMs on the DC side of the standard two-level converter. All six arms of the AAC have a chain link of FBSMs along with director switches, as shown in Figure 2.20. As in the two-level converter, the high-voltage director switches are operated in complementary pairs for each phase. The presence of the FBSM chains in the arms enables soft-switching of the director switches. Meanwhile, the complementary nature of the director switch operation implies that only one arm is in conduction at a time. Therefore, the upper arm FBSMs are used to construct the AC voltage waveform in the positive half cycle while the lower arm generates the voltage waveform in the negative half cycle. This implies conduction losses would be about half when compared to FB-MMC-based systems. In [75], a semiconductor loss comparison between the AAC and the HCMC was made where simulation results confirmed lower conduction losses in the AAC.

The number of required SMs in the AAC is reduced by half when compared to an equivalent FB-MMC. However, there needs to be a short overlap period, during which the conduction of switches is transferred from the upper arm to the lower arm in each phase and vice versa, to facilitate energy balancing in the arms. During this period, both arms conduct and form a path for current to flow between the DC rails. This circulating current can be used to achieve various control objectives such

as zero-current switching and arm energy balancing. With a short overlap period, the DC current contains a six-pulse ripple that needs to be filtered out. Besides, a short overlap period makes arm energy balancing challenging as the time window is limited. Several energy balancing methods based on a short overlap period are discussed in [76], [77], [78].

To address the energy balancing problem in the short overlap period, an Extended Overlap Alternate Arm Converter (EO-AAC) was proposed in [79] which resulted in a smooth DC current waveform and eliminated the large DC filter capacitor requirement. However, DC side inductors were still essential for current control. In [80], active filtering of the DC current based on internal energy control in the EO-AAC was proposed which eliminated the need for the DC side inductors, but soft-switching was not achieved. To address this issue, a zero-current switching method for the EO-AAC was proposed in [81].

An important advantage of the AAC over FB-MMC is in the minimum capacitor energy storage requirement to ensure SM voltage fluctuations are kept within set limits. It was shown in [82] and [83] that the capacitive energy storage requirement in the AAC is about one-third of that in FB-MMC even in the case of a short overlap period, with a large DC filter capacitor present. In the EO-AAC mode with no capacitive filters, there would be an extra 33% reduction in the energy storage requirements.

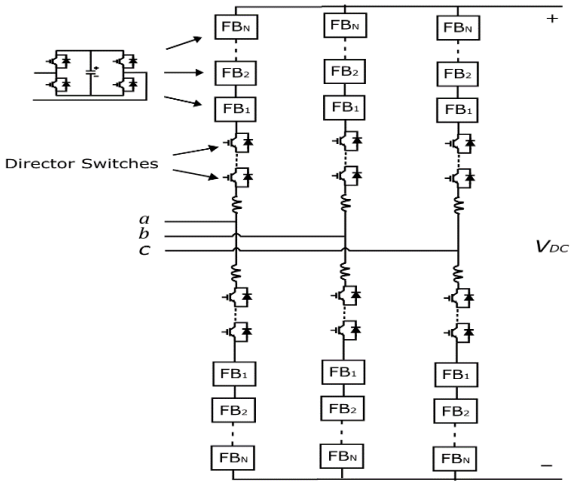


Figure 2.20 AAC

2.5.3 Hybrid Cascaded Multilevel Converters

Hybrid configurations with cascaded FBSM chains on either the AC or the DC side of the MMC are described in this subsection.

2.5.3.1 Hybrid Cascaded Multilevel Converters with AC side HBSMs

The authors in [5] and [84] presented a Hybrid Cascaded Multilevel Converter (HCMC) configuration that has a two-level VSC in the main power stage, which is connected in series with cascaded FBSMs on the AC side, as shown in Figure 2.21. Modulation and control schemes during normal and DC fault conditions for this design were proposed in [85]. This FBSM chain acts as an active filter or a wave-shaping circuit that eliminates the harmonic voltages produced by the two-level converter in the main power stage. The two-level converter produces a square wave output and the wave-shaping circuit compensates for the difference in the output of the two-level converter and the desired (sinusoidal) output voltage. The combined output voltage is an almost perfect sinusoid, which is a significant improvement over the output of the traditional two-level VSC. This allows the two-level converter to switch at a much lower frequency than would be possible in the absence of the wave-shaping converter. The fault blocking ability of the FBSM cells is utilized in the case of DC side faults to suppress the fault current. The cascaded FBSMs must block half the DC link voltage to provide short circuit protection against both pole-to-pole and pole-to-ground faults on the DC side. Since the cascaded SMs are placed on the AC side rather than on the arms, the total SM requirement is reduced to only a quarter compared to the FB-MMC while keeping voltage waveform quality and fault blocking ability intact. Placing the wave-shaping circuits on the AC side does not, however, solve the problem of high switching losses in the two-level converter. Even though the two-level converter switches can be switched at a low frequency, switching losses are still high. Moreover, as in the case of traditional two-level converters, large DC link capacitors are required in this configuration. Therefore, high inrush currents due to the recharging of the DC side capacitors during fault recovery is a drawback of this configuration and leads to high current stress on the switching devices. In [86], it was shown that the HCMC has lower conduction losses than the FB-MMC even when mixed SMs were utilized in the arms instead of HBSMs.

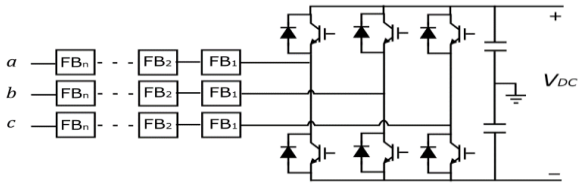


Figure 2.21 HCMC

The hybrid cascaded modular multilevel converter (HC-MMC) with HBSMs in the main circuit presented in [87] replaces the two-level converter in the main power stage of the HCMC with HBSMs. The wave-shaping circuit remains identical to that of the HCMC, as shown in Figure 2.22. In [88], a control technique to regulate the energy of the wave-shaping part, i.e., the FBSM chains, was proposed. HBSMs in the arms reduce the *dv/dt* stress on the switching devices and enable better reference voltage tracking for the AC side FBSM chains, thus improving switching synchronization between the two power stages. The FBSM chain in each phase only needs to block half the DC link voltage to facilitate wave-shaping and DC fault blocking, as explained previously. Since the two-level converter is replaced by HBSMs in the main power stage, high switching losses are avoided. In addition, the need to have a DC link capacitor is also eliminated. A drawback of this configuration is that the device count and conduction losses are higher than those of the HCMC due to the use of HBSMs in the main circuit.

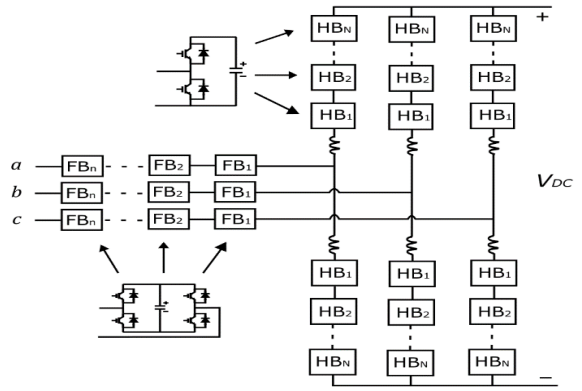


Figure 2.22 HC-HCMC

The H-Bridge Hybrid Modular Converter (HBHMC) [89] offers an improvement over the HCMC in terms of capacitor voltage balancing while the main difference between the two structures lies in the use of an H-bridge at the DC terminal in the HBHMC, as shown in Figure 2.23. H-bridge provides isolation or freewheeling mode for the load connected on the AC side. This gives an extra degree of

freedom for the FBSM capacitor voltage balancing. The HBHMC has two main parts, the main H-Bridge circuit (MHBC) and a wave-shaping circuit (WSC). To obtain three-phase AC voltage, three HBHMCs can be connected either in series or in parallel (Figure 2.24 (a) and (b)). Similar to the HMC with DC side cascaded cells, this configuration will only be suitable for back-to-back or short-distance HVDC transmission. In this configuration, DC fault blocking is provided by the FBSM chain.

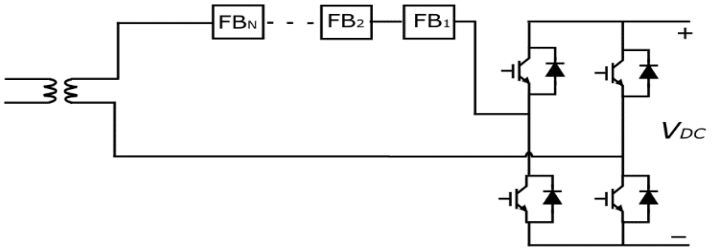
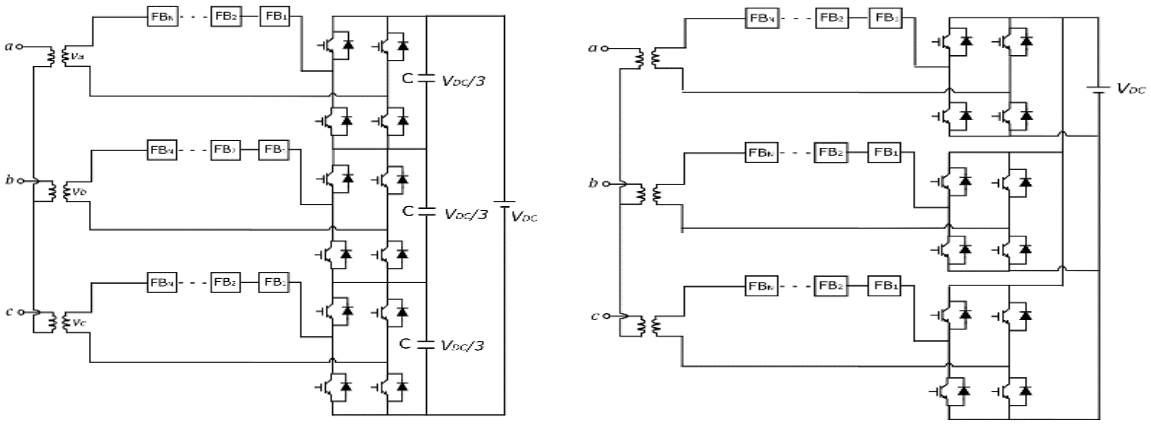


Figure 2.23 Single phase diagram of HBHMC



(a) (b)

Figure 2.24 (a) Series HBHMC; (b) Parallel HBHMC

2.5.3.2 Hybrid Cascaded Multilevel Converters with DC side FBSMs

The HCMC with DC side cascaded FBSMs, as shown in Figure 2.25, was presented along with a discussion on converter operation and control in [90], [91], [92] [93]. In this configuration, the total voltage across the cascaded FBSMs equals the full DC link voltage (V_{DC}). The difference between V_{DC} and the voltage generated by the FBSM chain produces a rectified voltage across the main H-bridge

circuit. The H-bridge circuit then reverses the polarity of this voltage during the negative half of each fundamental cycle to produce an AC signal. The use of the H-bridge at the AC terminal ensures that the converter generates the same voltage levels per phase as the traditional MMC but with half the number of SMs. Furthermore, the main H-bridge switches operate at the fundamental frequency and the switching occurs at near zero-voltage (soft-switching), keeping switching losses to a minimum. The cascaded FBSMs are capable of providing DC side short circuit protection. A disadvantage of this configuration is that it is only suitable for back-to-back or short-distance HVDC transmission. This is because the DC side voltage is half the peak-to-peak AC side voltage; therefore, the rated DC side current, for a given transmitted power, is double when compared to other hybrid configurations.

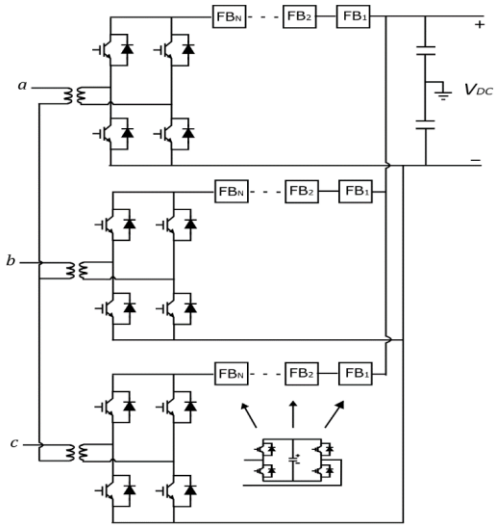


Figure 2.25 HMC with DC side FBSMs

2.5.3.3 Series Stacked Hybrid Modular Multilevel Converter

The authors in [94] proposed a three-phase, series-connected MMC (SCMMC) for HVDC applications to reduce the total number of required SMs when compared to the FBSM-based MMC. This structure is incapable of blocking DC side fault currents due to HBSMs in the arms. In [95], the Series Stacked Hybrid Modular Multilevel Converter (SSHMMC) was introduced (Figure 2.26). By replacing one-third of the HBSMs with FBSMs in this configuration, it is possible to incorporate DC fault blocking capability. The DC link voltage per phase in SSHMMC is $V_{DC}/3$. A clear disadvantage of this configuration is that the peak-to-peak voltages obtained on the AC side would also be reduced to one-third.

It is evident from Figure 2.26 that during a DC side fault, 6 out of the 12 arms of the converter are in the fault current path along with all three of the AC side sources. The three sources are balanced and sinusoidal; therefore, the maximum value of the AC side voltage at any instant of time is $2V_m$, where V_m is the peak value of phase voltage. Since the maximum AC side voltage is equal to the DC link voltage (per phase), V_m equals $V_{DC}/3$. Therefore, the total blocking voltage required to suppress the fault current is $2V_{DC}/3$. As mentioned previously, each arm of the converter can block $V_{DC}/3$. The 6 arms in series generate a total blocking voltage of $2V_{DC}$. Therefore, to block DC side faults, it is sufficient to have one-third of the SMs with symmetrical fault blocking capability. As a result, there is a reduction in the number of FBSMs required in the arms when compared to the traditional fault blocking hybrid MMC consisting of HBSMs and FBSMs with a 1:1 ratio.

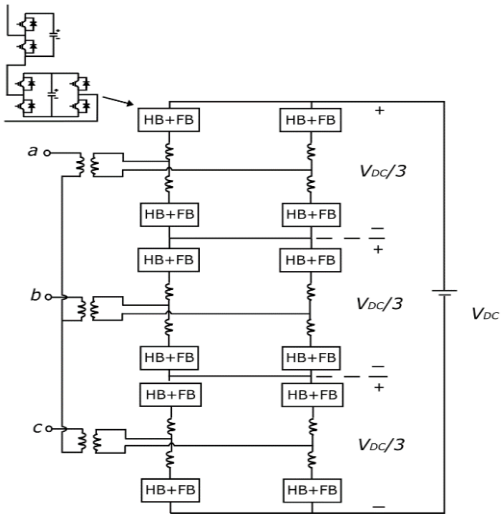


Figure 2.26 SSHMMC

2.6 Comparison of Hybrid MMC Configurations

A comparison of hybrid MMC configurations in terms of the total number of SMs and capacitors, total number of IGBTs, number of IGBTs in the conduction path, soft-switching, and overmodulation capabilities are summarized in Table 2.4. Director switch IGBTs were taken into consideration during the calculation.

Table 2.4 Comparison among different Hybrid MMC Configurations

	FB-MMC	HCMC	HC-MMC with HB Cells in Main Circuit	HCMC with DC Side Cascaded FBSMs	AAC	SSH-MMC	Series HBHMC	Parallel HBHMC
DC Link Voltage	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}
Voltage Stress Per Device	V_{DC}/N	V_{DC}/N	V_{DC}/N	V_{DC}/N	V_{DC}/N	V_{DC}/N	V_{DC}/N	V_{DC}/N
Maximum AC Phase Voltage	$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$	V_{DC}	$V_{DC}/2$	$V_{DC}/3$	$V_{DC}/3$	V_{DC}
Number of Voltage Levels	N+1	N+1	N+1	2N+1	N+1	2N/3 +1	2N/3 +1	2N+1
Total Number of SMs	6N	1.5N	7.5N	3N	3N	4N	N	3N
Total Number of Capacitors	6N	1.5N	7.5N	3N	3N	4N	N	3N
Total Number of IGBTs	24N	12N	18N	24N	15N	32N/3	8N	24N
Number of IGBTs in Conduction Path	12N	6N	9N	12N	4.5N	4N	4N	12N
Soft-switching	N/A	No	N/A	Yes	Yes	N/A	No	No
Overmodulation	Yes							

The AAC has some notable advantages over other configurations. It has a lower number of SMs compared to FB-MMC. It exhibits lower switching losses, especially in comparison to HCMC-based structures. Moreover, the capacitor energy storage requirements are much lower compared to FB-MMC systems which would provide significant benefits in terms of cell capacitor sizing. The drawbacks of the conventional AAC configuration include the requirement of a large DC side filter and challenges with arm energy balancing. The EO-AAC eliminates the need for the DC filter but is unable to facilitate soft-switching. Meanwhile, the HCMC topology has the lowest device count; however, HCMC with DC side cascaded HBSMs and the parallel HBHMC are only suitable for short-distance HVDC transmission. The series HBHMC and the SSHMC are more appropriate for low-power applications; however, the HBHMC is incapable of soft-switching. Therefore, the AAC remains the most promising

configuration in terms of commercialization if the aforementioned issues are alleviated through further research and development.

2.7 STATCOM Operation and DC Fault Ride Through

During a DC fault, the HVDC link voltage collapses, and active power cannot be transferred between the AC and DC sides. The MMC can be operated as a STATCOM to provide reactive power support to the AC system during this period. In the STATCOM operation mode, certain changes with regards to the control and arm/leg energy balancing in the MMC are required.

During normal operation of MMC, the reference voltages used for modulation of the upper and lower arms (v_{xu}^* and v_{xl}^*) are expressed as

$$v_{xu}^* = \frac{V_{DC}}{2} - v_x - v_{xz}, \tag{2.6}$$

$$v_{xl}^* = \frac{V_{DC}}{2} + v_x - v_{xz}, \tag{2.7}$$

where v_{xz} denotes the leg internal voltage which is generated due to the flow of circulating current. If all the SMs are blocked, the MMC cannot supply reactive power to the AC grid. If all the SMs are blocked, the MMC cannot supply reactive power to the AC grid. Instead, if the MMC is allowed to operate with the V_{DC} term in the arm reference voltage synthesized as zero [96], [97], then the DC fault will be cleared. Positive and negative excursions of the MMC arm voltages will enable them to operate as wave-shaping circuits and control the AC currents. As long as the SMs have bipolar voltage generation capability, the MMC can ride through the fault and operate as a STATCOM to provide reactive power support to the AC grid. The following subsections review some DC-FRT strategies and STATCOM operation mode of a selected subset of MMC configurations discussed thus far. The modifications of the arm/leg energy balancing controllers during STATCOM operation mode are discussed briefly as well.

2.7.1 Hybrid Arm-based Bipolar MMC

The hybrid-arm-based bipolar MMC [98] is a configuration where the arms connected to the ground pole are comprised of HBSMs while the arms connected to the positive and negative poles can be any type of fault blocking SM. The positive and negative poles are at $+V_{DC}/2$ and $-V_{DC}/2$, respectively, with respect to the ground pole. During both pole-to-pole and pole-to-ground faults, the fault blocking modules connected to the positive and the negative poles are blocked enabling the HBSMs to operate

as a STATCOM. Figure 2.27 shows such a bipolar MMC comprised of UFBSMs and HBSMs. This is a very simple and cost-effective way of achieving DC-FRT ability since the fault blocking SMs utilized do not need to have bipolar voltage generation capability for the MMC to clear the DC fault and work as a STATCOM.

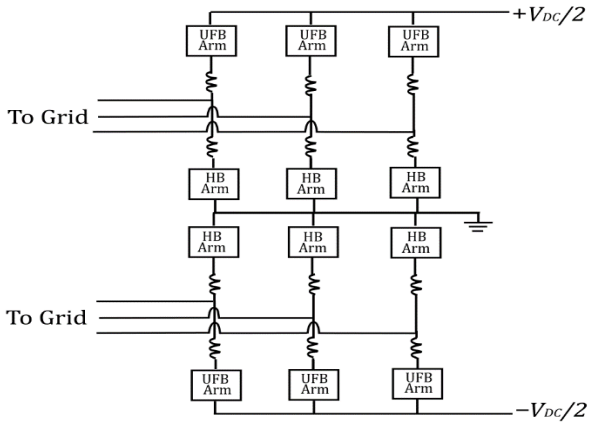


Figure 2.27 UFBSM-based hybrid arm bipolar MMC

2.7.2 STATCOM Operation Mode of the AAC

The bipolar voltage generation capability of the AAC enables it to operate as a STATCOM during DC faults. Two different modes of operation are presented in [99] depending on the conduction of the arms. The first mode of operation is similar to the normal operation mode of the AAC; the upper and lower arms of each phase conduct alternately. This mode will result in the current flowing through the DC side fault which is not desirable. In the second mode of operation, either all the upper arms or all the lower arms are utilized during the STATCOM operation. This implies that the upper or the lower arms can function as star-connected STATCOMs; the current will be constrained to flow within the arms and will not flow into the DC side.

2.7.3 STATCOM Operation of Unipolar SM Configurations

The CDSM is incapable of bipolar voltage generation rendering it unsuitable for STATCOM operation during DC faults. However, the authors of [100] identify switching states for bipolar operation of the CDSM, but only when the SM current direction is negative. This implies that the CDSM can operate as a STATCOM during DC faults if the arms are made to conduct alternately. The switching states for the STATCOM mode of the CDSM are shown in Table 2.5, where the “Positive” and “Negative” states

denote the bipolar SM voltages for i_{sm}<0. These switching states are utilized only when there is a DC side fault; the MMC is then able to clear the fault and work as a STATCOM. A disadvantage of such a STATCOM mode of operation is that it will have half the reactive power capability compared to MMCs containing bipolar SMs.

Table 2.5 CDSM STATCOM Mode Switching States

SM State	T1	T2	T3	T4	T5	i_{sm}	v_{sm}
Positive	1	0	0	1	0	<0	V_c
Bypassed	1	0	1	0	0	<0	0
Negative	0	1	1	0	0	<0	-V_c

The UFBSM is another fault blocking module that cannot generate bipolar voltages for both directions of SM current. However, alternate switching states with bipolar voltage output for i_{sm}<0 exist and are illustrated in Table 2.6. Therefore, DC fault clearance and STATCOM operation are made possible by alternate conduction of arms. Similar to the CDSM, a downside is that it will have half the reactive power capability compared to MMCs containing bipolar SMs.

Table 2.6 UFBSM STATCOM Mode Switching States

SM State	T1	T2	T4	i_{sm}	v_{sm}
Positive	1	0	1	<0	V_c
Bypassed	1	0	0	<0	0
Negative	0	1	0	<0	-V_c

In [101], the authors propose the STATCOM operation of a hybrid HBSM-SDSM with a mix of 30% of SDSM per arm. As mentioned earlier, the SDSM (Figure 2.28) is a unipolar module that cannot be operated as a STATCOM during DC faults if the switching states for normal operation are employed. Therefore, just as was the case with the CDSM and UFBSM, the arms are alternately blocked based on the current direction and an alternate set of bipolar voltage states is realized for i_{sm}<0. The switching states for the STATCOM operation mode of the SDSM are provided in Table 2.7. The line-line voltage generated by the alternate blocking and conduction of the arms during STATCOM mode is higher compared to the CDSM based STATCOM resulting in superior reactive power capabilities.

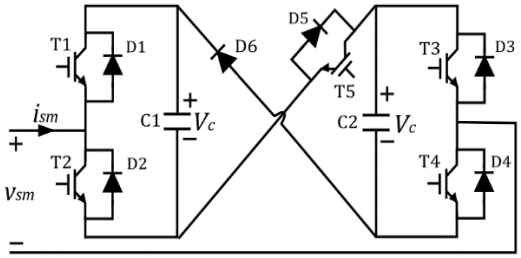


Figure 2.28 SDSM

Table 2.7 SDSM STATCOM Mode Switching States

SM State	T1	T2	T3	T4	T5	i_{sm}	v_{sm}
Positive	1	0	0	1	1	<0	$2V_c$
Positive	1	0	1	0	1	<0	V_c
Positive	0	1	0	1	1	<0	V_c
Bypassed	1	0	0	1	0	<0	0
Bypassed	0	1	1	0	1	<0	0
Negative	0	1	0	1	0	<0	$-V_c$
Negative	1	0	1	0	0	<0	$-V_c$
Negative	0	1	1	0	0	<0	$-2V_c$

2.7.4 Energy Balancing during STATCOM Mode of Operation

Capacitor energy balance in an MMC is essential to ensure proper operation of the converter and applies to both leg and arm. Voltage/energy balancing of the SM capacitors can be achieved either through non-energy- or energy-based methods. The non-energy-based algorithms are usually simpler to implement and do not require any modifications during DC faults in the MMC.

In the case of the UFBSM/HBSM-based bipolar MMC [98], the outer control loop was modified to facilitate converter energy control. The *d*-axis current reference was not obtained from the active power in the outer loop during STATCOM operation. Rather, a PI controller was utilized to generate the *d*-axis current reference such that the average capacitor voltage of the HBSMs was maintained near their

nominal ratings. This enabled control over the total energy flowing into the MMC during the STATCOM mode of operation. The conventional sorting algorithm was used to keep the capacitor voltages balanced within the arms.

In [19], an energy-based voltage balancing method was proposed whereby arm and leg energy in the MMC can be controlled by the injection of circulating currents. Expressions for the sum and difference of power flowing into the arms of an MMC are given by (2.8) and (2.9), respectively.

$$P_{x,sum} = P_{xu} + P_{xl} = V_{DC} i_{xz} - v_x i_x - 2 v_{xz} i_{xz}, \tag{2.8}$$

$$P_{x,diff} = P_{xu} - P_{xl} = 0.5 V_{DC} i_x - 2 v_x i_{xz} - v_{xz} i_x. \tag{2.9}$$

The first term in the right-hand side of (2.8) can be controlled by injection of a DC component in the circulating current (i_{xz}), allowing leg energy balancing to be carried out during normal MMC operation [19], [96], [102]. Meanwhile, the second term on the right-hand side of (2.9) can be utilized for arm energy balancing by the injection of a fundamental frequency component in the circulating current. However, in the event of a DC fault, V_{DC} is synthesized as zero to clear the fault and operate the MMC in STATCOM mode. Therefore, the $V_{DC} i_{xz}$ term in (2.8) becomes zero and leg energy control is no longer possible. In [96], a common-mode voltage (CMV) injection in the FB-MMC was proposed to carry out leg energy balancing during DC faults in the MMC. The CMV (v_{sn}) is defined as the potential difference that exists between the neutral points of the AC and DC sides. Expressions for the CMV and the AC side current are given by,

$$v_{sn} = V_c \sin(\omega t + \alpha), \tag{2.10}$$

$$i_a = I_s \sin(\omega t + \sigma), \tag{2.11}$$

$$i_b = I_s \sin\left(\omega t + \sigma - \frac{2}{3}\pi\right), \tag{2.12}$$

$$i_c = I_s \sin\left(\omega t + \sigma + \frac{2}{3}\pi\right). \tag{2.13}$$

The power generated in the MMC legs due to the injected common-mode voltage are given by

$$P_a^{\Sigma} = 0.5 V_c I_s \cos(\sigma - \alpha), \tag{2.14}$$

$$P_b^{\Sigma} = 0.5 V_c I_s \cos\left(\sigma - \alpha - \frac{2}{3}\pi\right), \tag{2.15}$$

$$P_c^{\Sigma} = 0.5 V_c I_s \cos\left(\sigma - \alpha + \frac{2}{3}\pi\right). \tag{2.16}$$

The three-phase powers are converted to the *dq* frame components and the reference for the CMV is obtained as follows

$$v_{sn}^{*} = Re\left\{\frac{P_d^{\Sigma*} + jP_q^{\Sigma*}}{0.5\left(i_{ds} + ji_{qs}\right)}\right\}, \tag{2.17}$$

where $P_d^{\Sigma*}$ and $P_q^{\Sigma*}$ represent the reference values of the leg powers in the dq frame, while i_{ds} and i_{qs} are the AC side *d*- and *q*-axis current components, respectively. By controlling the phase and amplitude of the CMV, it would then be possible to vary the power flowing into the legs of the MMC and continue to carry out leg energy balancing during the STATCOM operation mode.

When the CDSM-based MMC is working in STATCOM mode during a DC side fault [100], the arms conduct alternately. Thus, the equivalent circuit of the DC faulted CDSM-based MMC during STATCOM mode is different from when it is operating under normal conditions. The circulating current injection method for energy balancing is no longer feasible since no circulating current exists within the same phase due to the alternate conduction of the CDSM arms. Although the CMV injection method from [96] can be employed for leg energy balancing, a simpler strategy was represented in [100] where *dq* transformation is not required. As the RMS value of the capacitor voltages in an arm is indicative of the arm's energy level, in this strategy, the sum and difference of the arm power expressions for the conducting lower and upper arms, in terms of the RMS voltages of the SM capacitors, were split into two parts to denote powers flowing from the DC and AC sides into the conducting arms. The expression for the power flowing from the DC side into the conducting arms includes the CMV term. An increase in CMV leads to a decrease in the power flow in the conducting upper arm(s) and an increase in the power flow in the conducting lower arm(s), respectively; consequently, the difference in the energy levels between the conducting upper and lower arms will decrease. Similarly, a decrease in the CMV leads to an increase in the power flow in the conducting upper arm(s) and a decrease in the power flow in the conducting lower arm(s), respectively. The reference value of the CMV is obtained from a PI controller based on the difference in RMS voltages of the SM capacitors in conducting upper and lower arms. Therefore, the CMV reference can be adjusted based on the RMS voltage of SM capacitors, and no circulating current injection is necessary for arm energy balancing. In addition, the outer controllers are adjusted to control the total converter energy in the same way as in [98].

Authors in [103], [104] proposed an energy balancing approach based on either AC or DC power. The variation of energy in the SMs is dependent on the instantaneous AC power and the power exchanged with the DC bus. Based on the energy balance equation, a controller can be designed using the AC power or the DC power in the outer loop. The references generated by the outer loop are the AC grid currents and the circulating currents. When the outer controller is based on AC power, it is not possible to implement three separate loops for the grid currents. Therefore, only control of total MMC energy is possible as opposed to individual arm/leg energy balancing. In [105], this idea was expanded and implemented to achieve energy balancing during a DC fault. During normal operation, energy balancing was performed using DC power. After the occurrence of a DC fault, the energy balancing was shifted to AC power mode since the loss of the DC voltage made DC power-based control impossible. However, in the AC power-based control, leg/arm energy balancing is not feasible since any circulating current injection intended for balancing may not add up to zero and flow into the DC fault. Therefore, the authors suggest the use of coupling matrices to ensure that the AC components of circulating currents sum to zero and do not flow through the DC fault. This method has the added advantage of achieving low transient overvoltage in the arms during the fault in addition to DC fault clearance and reactive power injection into the AC grid.

To summarize, the CMV injection method for leg energy balancing can be applied to any SM configuration with continuous conduction of both arms in a phase. The capacitor energy-based method, which was originally developed for the CDSM-based STATCOM, can also be utilized for arm energy balancing during the STATCOM mode of operation of MMCs with other types of unipolar SMs. The AC power-based energy balancing method is more complex but can be used if better transient response/stability is desired.

2.8 Conclusion

In this chapter, a variety of noteworthy SM and hybrid MMC configurations, with DC fault blocking capability, were reviewed, and compared from different viewpoints, including the number of switches in the conduction path, fault blocking symmetry, voltage stress per device, device count, number of voltage sensors, overmodulation, soft switching, voltage balancing capability and control complexity. Based on the comparisons made, several configurations such as asymmetrical full-bridge submodule and mixed submodule were identified, which hold an advantage in terms of lower conduction losses or total semiconductor device count, while SM configurations such as semi full-bridge submodule and

switched capacitor were associated with better performance in terms of voltage balancing capability and control simplicity. When overmodulation is a requirement, mixed and asymmetrical full-bridge submodules are suitable choices. Meanwhile, the semi full-bridge submodule was identified as a proper candidate when a lower number of voltage sensors along with reduced control complexity is desired. Among hybrid topologies, the alternate arm converter was found to be the most efficient with a low device count, while the hybrid converter with cascaded DC side cells was recognized as a suitable configuration for short-distance HVDC transmission.

The STATCOM operation mode of the full-bridge MMC, alternative arm converter, hybrid MMCs, as well as MMCs based on unipolar SMs, such as clamped-double and unipolar full-bridge submodule, were discussed and compared in this chapter. This shows that the adjustment of the arm voltage reference enables bipolar SMs to work as wave-shaping circuits, allowing the provision of reactive power support to the AC grid during a DC fault. Furthermore, MMCs with unipolar SMs can also clear the DC fault and work as STATCOMs, if alternate switching states that enable bipolar operation exist for a certain direction of SM current. However, due to the alternate arm conduction during STATCOM mode, such unipolar SMs have half the reactive power capability of the bipolar SMs.

This chapter also provides a review of different methods used to provide arm and leg energy balancing in MMCs when they are operated as STATCOMs during DC faults. One of the most notable methods is common-mode voltage injection which can be applied to any SM configuration provided there is continuous conduction of both arms in a phase. The capacitor energy-based method for arm energy balancing during STATCOM operation of the clamped-double submodule can be applied to other unipolar SMs as well.

Chapter 3
Modified Scheme for Fast DC Fault Current Suppression

3.1 Introduction

Chapter 2 reviewed notable SM and MMC configurations capable of either blocking or riding through DC faults. While the blocking action by fault blocking SMs to facilitate fault current suppression can be achieved very quickly (usually within a few milliseconds) [18], it would prevent the MMCs from working as STATCOMs to provide reactive power support at the Point of Common Coupling (PCC). Bipolar SMs such as the FBSM are capable of clearing DC side faults and simultaneously allowing STATCOM operation of the MMCs as explained in the previous chapter. While this is advantageous from a PCC voltage stability standpoint, operation as a STATCOM comes with certain challenges. Firstly, SM capacitor voltage balancing is an issue if energy-based control approaches are utilized. Modifications to the balancing approach become essential to maintain energy balance in the arms/legs of the MMC. Secondly, it can take tens of milliseconds for the fault current to decay to zero after DC fault clearance and initiation of STATCOM operation due to the DC transmission line being a low damping system [8]. A damping method by utilizing an active resistance to absorb the inductive energy and accelerate DC fault current suppression was briefly discussed by the authors [8]. However, no details on the active resistance calculation method were provided. No other notable techniques to decrease oscillations and enable faster DC fault current suppression was found in the literature.

In this chapter, first, a state-space averaging approach to manipulate the DC fault current rise rate by controlled SM capacitor discharge in HB-MMC systems [106], [107] is analyzed. The authors' intent was to reduce the rate of rise of the DC fault current so that the size of the HVDC line reactors could be decreased, leading to lower costs. Since reduced SM discharge would by no means facilitate DC fault current suppression, such a method would not be useful in MMC-HVDC systems comprised of fault blocking SMs where the MMC capacitors are capable of either blocking the DC fault current or riding through DC faults while operating as STATCOMs. Therefore, a modification to the existing method was necessary for adoption by fault-tolerant MMC systems. This novel modified approach is presented in this chapter along with its theoretical underpinnings and simulation results that confirm its superior performance in riding through DC faults and suppressing fault current oscillations, compared to the conventional method of DC fault clearance and STATCOM operation of fault-tolerant MMCs.

3.2 Submodule Capacitor Discharge Control in HBSM-based MMC

Since the capacitors are the main source of the DC fault current during the initial stages, manipulation of the SM discharge rate in the MMC would be an effective means of limiting the DC fault current. A few methods involving SM capacitor discharge in HB-MMC systems, to achieve fault current control, have been proposed in the literature. One approach is to block the IGBTs and prevent SM discharge completely. Such an action would eliminate the SM capacitor contribution to the fault, but the diode freewheeling effect in HBSMs means the DC fault current, even though reduced, would not be completely suppressed. A significant disadvantage of the blocking action is that it would cause overvoltage across the arm inductors [108]. Another approach is to bypass the SMs entirely by using either the SM IGBTs [109] or double thyristor switches connected in parallel with the SMs [54]. The purpose of installing thyristors in parallel to the SMs is to protect the IGBTs from sustained high levels of fault current; thyristors typically have much higher current ratings than IGBTs. However, this bypass action would transform the DC side short circuit into an AC short circuit and lead to overcurrent on the AC side and in the MMC arms. Such deficiencies in both blocking and bypass approaches have led researchers to methods that provide a degree of control over the SM capacitor discharge.

In [106], [107] a method of controlled discharge based on state-space average modeling is proposed for HB-MMC systems. Each MMC arm inserts a certain proportion of N capacitors in the arms during each switching period. Thus, the number of inserted capacitors varies between 0 and N. Two independent circuits are defined as the base cases, both of which are depicted in Figure 3.1. Base circuit 1 represents the case when all of the SM capacitors are inserted into the circuit, while base circuit 2 portrays the opposite scenario, i.e. when all of the SM capacitors are bypassed. A variable D_1 is defined as the duty cycle for base circuit 1 during each switching period, T_s, while $(1 - D_1)$ represents the duty cycle for circuit 2. This variable D_1 represents the state of discharge of the SM capacitors. When $D_1 = 0.5$, 50% of all capacitors are inserted, and the circuit state corresponds to normal operation. When $D_1 = 0$, none of the capacitors are inserted, corresponding to the bypass state of the SMs. If the range of D_1 is assumed to vary between 0 and 1, then all possible states of the DC fault circuit can be comprehensively represented by the two base circuits. Therefore, establishing control over the variable D_1 would enable direct control over SM capacitor discharge, and thus the DC fault current. Since D_1 is an insertion parameter, it can be expressed by the ratio of the sum of the upper and lower arm voltages in a phase divided by the total generation capacity of the two MMC arms,

$$D_1 = \frac{v_{xu}+v_{lu}}{2V_{DC}}. \tag{3.1}$$

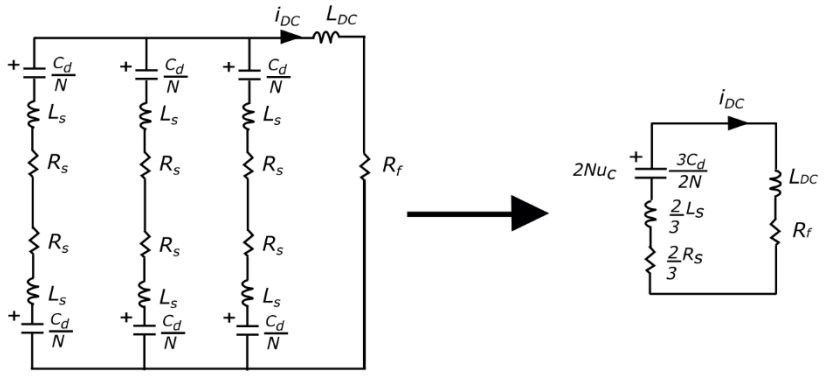
Neglecting the voltage drop across the arm inductors, the arm voltage expressions in phase *x* are given by,

$$v_{xu} = \frac{V_{DC}}{2} - v_x, \tag{3.2}$$

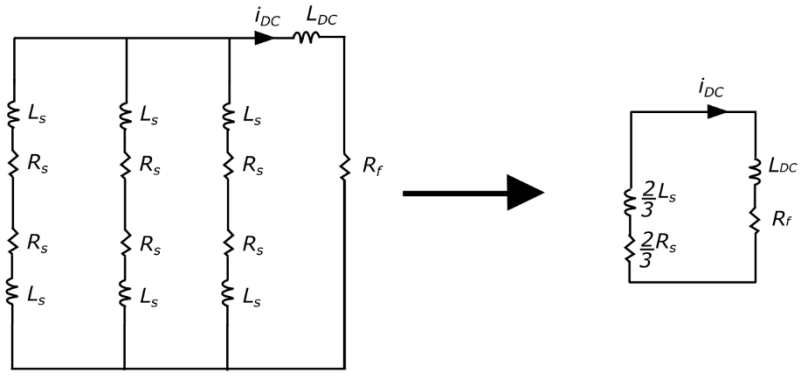
$$v_{xl} = \frac{V_{DC}}{2} + v_x. \tag{3.3}$$

In the expression for D_1, the AC terms in the arm voltages would cancel each other out, implying that the value of D_1 will be equal to 0.5 during normal operation. Thus, D_1 is the normalized DC component of the arm voltage reference. Since D_1 is 0.5 during normal operation, controlled capacitor discharge and subsequent fault current limiting action will be performed when D_1 is varied between 0 and 0.5.

From the equivalent circuits, it is apparent that only resistances, inductances, and capacitances of MMC, along with the inductance of DC line reactor and the fault resistance are parts of the model. The impedance of the DC line itself is excluded since it would vary according to the distance of the fault from the converter and therefore would interfere with the symmetry of the model when it is applied to the converter at the other end of the DC line.



(a)



(b)

Figure 3.1 Equivalent circuits for discharge control (a) Base Circuit 1 and (b) Base Circuit 2

The DC fault current i_{DC} (reactor current) and the averaged SM capacitor voltage u_c are selected as state variables of the state vector $x(t)$. Since the DC fault transient is short (a few milliseconds), the voltages of all SM capacitors are assumed to remain balanced. Then, an individual SM capacitor voltage u_c is used to represent the capacitor energy stored in the MMC. The state vector $x(t)$ can be expressed as

$$x(t) = \begin{bmatrix} i_{DC}(t) \\ u_c(t) \end{bmatrix}. \tag{3.4}$$

For a switching time-period denoted by T_s, the span of the first subinterval corresponding to base circuit 1 with all capacitors inserted would be $D_1 T_s$. The time span of the second subinterval for base circuit 2 with all capacitors bypassed would then be $(1 - D_1)T_s$. Applying Kirchhoff's voltage and current laws in base circuit 1, the following expressions involving the state variables can be obtained

$$2Nu_c(t) - L_e \frac{d}{dt} i_{DC}(t) - R_e i_{DC} = 0, \tag{3.5}$$

$$C_e \frac{d}{dt}\{2Nu_c(t)\} + i_{DC}(t) = 0, \tag{3.6}$$

where N is the number of SMs per arm, L_e is the equivalent inductance, R_e refers to the equivalent resistance, and C_e denotes the equivalent capacitance

$$L_e = \frac{2L_s}{3} + L_{DC}, \tag{3.7}$$

$$R_e = \frac{2R_s}{3} + R_f, \tag{3.8}$$

$$C_e = \frac{3C_d}{2N}. \tag{3.9}$$

Similar expressions can be derived for base circuit 2

$$-L_e \frac{d}{dt} i_{DC}(t) - R_e i_{DC} = 0, \tag{3.10}$$

$$C_e \frac{d}{dt} u_c(t) = 0. \tag{3.11}$$

The state-space expressions for base circuits 1 and 2, in matrix form, are given by (3.12) and (3.13), respectively.

$$\begin{bmatrix} L_e & 0 \\ 0 & C_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{DC}(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} -R_e & 2N \\ \frac{-1}{2N} & 0 \end{bmatrix} \begin{bmatrix} i_{DC}(t) \\ u_c(t) \end{bmatrix}, \tag{3.12}$$

$$\begin{bmatrix} L_e & 0 \\ 0 & C_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{DC}(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} -R_e & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{DC}(t) \\ u_c(t) \end{bmatrix}. \tag{3.13}$$

To combine the two sets of state-space equations, an averaged matrix **A** can be derived based on the duty cycles of the two base circuits as

$$\mathbf{A} = D_1 \mathbf{A_1} + (1\text{-}D_1)\mathbf{A_2} \tag{3.14}$$

$$= \begin{bmatrix} -R_e & 2ND_1 \\ -\frac{D_1}{2N} & 0 \end{bmatrix},$$

where

$$\mathbf{A_1} = \begin{bmatrix} -R_e & 2N \\ -\frac{1}{2N} & 0 \end{bmatrix}, \tag{3.15}$$

$$\mathbf{A_2} = \begin{bmatrix} -R_e & 0 \\ 0 & 0 \end{bmatrix}. \tag{3.16}$$

The complete time averaged expression can now be expressed as

$$\begin{bmatrix} L_e & 0 \\ 0 & C_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \langle i_{DC}(t) \rangle_{Ts} \\ \langle u_c(t) \rangle_{Ts} \end{bmatrix} = \begin{bmatrix} -R_e & 2ND_1 \\ -\frac{D_1}{2N} & 0 \end{bmatrix} \begin{bmatrix} \langle i_{DC}(t) \rangle_{Ts} \\ \langle u_c(t) \rangle_{Ts} \end{bmatrix}. \tag{3.17}$$

Differentiating the first equation in (3.17) with respect to time yields the following second-order differential equation:

$$\frac{d^2}{dt}\langle i_{DC}(t)\rangle_{Ts} + \frac{R_e}{L_e}\frac{d}{dt}\langle i_{DC}(t)\rangle_{Ts} - \frac{2ND_1}{L_e}\frac{d}{dt}\langle u_c(t)\rangle_{Ts} = 0. \tag{3.18}$$

From the second equation in (3.17),

$$\frac{d}{dt}\langle u_c(t)\rangle_{Ts} = -\frac{D_1}{2NC_e}\langle i_{DC}(t)\rangle_{Ts}. \tag{3.19}$$

Substituting (3.19) into (3.18) yields

$$\frac{d^2}{dt}\langle i_{DC}(t)\rangle_{Ts} + \frac{R_e}{L_e}\frac{d}{dt}\langle i_{DC}(t)\rangle_{Ts} + \frac{D_1^2}{L_eC_e}\langle i_{DC}(t)\rangle_{Ts} = 0, \tag{3.20}$$

with initial circuit conditions for the fault current and capacitor voltage at the time of DC fault occurrence given by

$$\langle i_{DC}(0^+)\rangle_{Ts} = I_{DC0}, \tag{3.21}$$

$$\langle u_c(0^+)\rangle_{Ts} = U_{c0}. \tag{3.22}$$

The characteristic roots of (3.20) are of the form:

$$p_{1,2} = -\frac{R_e}{2L_e} \pm \sqrt{\left(\frac{R_e}{2L_e}\right)^2 - \frac{D_1^2}{L_eC_e}}$$

The solution can be of three different types depending on the sign of the expression under the square root:

(1) Critically damped case ($D_1 = \frac{R_e}{2\sqrt{L_e/C_e}}$)

In this case, the solutions are equal and of the form

$$p_{1,2} = -\delta,$$

where

$$\delta = \frac{R_e}{2L_e}. \tag{3.23}$$

The general solution of such a differential equation is given by

$$\langle i_{DC}(t)\rangle_{Ts} = (A_1 + A_2t)e^{-\delta t} \tag{3.24}$$

Utilizing initial conditions,

$$\delta = \frac{R_e}{2L_e},$$

$$A_1 = I_{DC0}, \tag{3.25}$$

$$A_2 = \frac{4D_1U_{C0} - R_eI_{DC0}}{2L_e}. \tag{3.26}$$

(2) Overdamped case ($D_1 < \frac{R_e}{2\sqrt{L_e/C_e}}$)

In this case, the roots are of the form

$$p_{1,2} = -\delta \pm \sqrt{\delta^2 - \omega_0^2} = -\delta \pm \omega_r$$

where

$$\delta = \frac{R_e}{2L_e},$$

$$\omega_0 = \sqrt{\frac{D_1^2}{L_eC_e}}, \tag{3.27}$$

$$\omega_r = \sqrt{|\omega_0^2 - \delta^2|}. \tag{3.28}$$

The general solution to the equation is of the form

$$\langle i_{DC}(t)\rangle_{Ts} = \left\{A_3e^{(-\delta+\omega_r)t} + A_4e^{(-\delta-\omega_r)t}\right\}. \tag{3.29}$$

Utilizing initial conditions,

$$\delta = \frac{R_e}{2L_e},$$

$$\omega_0 = \sqrt{\frac{D_1^2}{L_eC_e}},$$

$$\omega_r = \sqrt{|\omega_0^2 - \delta^2|},$$

$$A_3 = \frac{2\omega_rL_eI_{DC0} + 4D_1U_{C0} - R_eI_{DC0}}{4\omega_rL_e}, \tag{3.30}$$

$$A_4 = \frac{2\omega_rL_e - 4D_1U_{C0} + R_eI_{DC0}}{4\omega_rL_e}. \tag{3.31}$$

The bypass condition with $D_1 = 0$ is an overdamped case. The solutions to the differential equation are then equal to

$$p_1 = 0,$$

$$p_2 = -2\delta.$$

From initial conditions,

$$A_3 = 0,$$

$$A_4 = I_{DC0}.$$

The differential equation changes from a second-order to a first-order with the solution

$$\langle i_{DC}(t)\rangle_{Ts} = I_{DC0}e^{-2\delta t} \tag{3.32}$$

This conforms with the *RL* representation of base circuit 2.

(3) Underdamped case ($D_1 > \frac{R_e}{2\sqrt{L_e/C_e}}$)

Due to small values of fault resistance, the underdamped case would occur most frequently while overdamped and critically damped cases would be rare. Therefore, the focus of this thesis will be SM capacitor discharge control in underdamped conditions. The test system parameters and selected duty cycle values would ensure underdamped conditions when the theoretical results are verified through simulation. For the underdamped case, the characteristic roots are complex conjugates:

$$p = -\delta \pm j\omega_r$$

The general solution of such a differential equation is of the form:

$$\langle i_{dc}(t)\rangle_{Ts} = Ae^{-\delta t}\{sin(\omega_r t + \beta)\} \tag{3.33}$$

Substituting (3.21) into (3.33) at $t = 0^+$ yields

$$A = \frac{I_{DC0}}{sin\beta}. \tag{3.34}$$

Differentiating (3.33) with respect to time gives

$$\frac{d}{dt}\langle i_{DC}(t)\rangle_{Ts} = A\{-\delta e^{-\delta t}sin(\omega_r t + \beta) + \omega_r e^{-\delta t}cos(\omega_r t + \beta)\}. \tag{3.35}$$

From the state space representation in (3.17),

$$\frac{d}{dt}\langle i_{DC}(t)\rangle_{Ts} = \frac{1}{L_e}\{-R_e\langle i_{DC}(t)\rangle_{Ts} + 2ND_1\langle u_c(t)\rangle_{Ts}\},$$

$$\frac{d}{dt}\langle i_{DC}(t)\rangle_{Ts} = \frac{2ND_1\langle u_c(t)\rangle_{Ts} - R_e\langle i_{DC}(t)\rangle_{Ts}}{L_e}. \quad (3.36)$$

Equating the right-hand sides of (3.35) and (3.36) yields

$$A\{-\delta e^{-\delta t}sin(\omega_r t + \beta) + \omega_r e^{-\delta t}cos(\omega_r t + \beta)\} = \frac{2ND_1\langle u_c(t)\rangle_{Ts} - R_e\langle i_{DC}(t)\rangle_{Ts}}{L_e}.$$

Utilizing initial conditions and substituting the expressions for A and δ yields

$$\frac{I_{DC0}}{sin\beta}\left(-\frac{R_e}{2L_e}sin\beta + \omega_r cos\beta\right) = \frac{1}{L_e}(-R_e I_{DC0} + 2ND_1 U_{C0}).$$

Rearranging the terms and simplifying, one gets

$$tan\beta = \left(\frac{2\omega_r L_e I_{DC0}}{4D_1 N U_{c0} - R_e I_{DC0}}\right),$$

$$\beta = arctan\left(\frac{2\omega_r L_e I_{DC0}}{4D_1 N U_{c0} - R_e I_{DC0}}\right). \quad (3.37)$$

Therefore, the parameters in the solution given by (3.33) can be expressed as

$$\delta = \frac{R_e}{2L_e},$$

$$\omega_0 = \sqrt{\frac{D_1^2}{L_e C_e}},$$

$$\omega_r = \sqrt{|\omega_0^2 - \delta^2|},$$

$$A = \frac{I_{DC0}}{sin\beta},$$

$$\beta = arctan\left(\frac{2\omega_r L_e I_{DC0}}{4D_1 N U_{c0} - R_e I_{DC0}}\right). \quad (3.38)$$

Now that the solution to the second-order differential equation for underdamped condition has been found, the next step would be to derive a simpler relationship between the fault current and the duty cycle. With that in mind, R_e is assumed to be zero, considering that the circuit resistance is small. By extension, δ also becomes equal to zero. Therefore,

$$\omega_r = \omega_0 = D_1\sqrt{\frac{1}{L_eC_e}}, \tag{3.39}$$

$$\beta = arctan\left(\frac{\omega_r L_e I_{DC0}}{2D_1 NU_{c0}}\right) = arctan\left(\frac{I_{DC0}}{2NU_{c0}}\sqrt{\frac{1}{L_eC_e}}\right). \tag{3.40}$$

The simplified expression for β is used to obtain the value for A making use of Pythagoras' Theorem:

$$A = \frac{I_{DC0}\sqrt{(2NU_{C0})^2 + \left(I_{DC0}\sqrt{\frac{L_e}{C_e}}\right)^2}}{I_{DC0}\sqrt{\frac{L_e}{C_e}}} = \sqrt{\frac{2}{L_e}\left[2C_e(NU_{c0})^2 + \frac{L_e I_{DC0}^2}{2}\right]}. \tag{3.41}$$

The initial capacitor and reactor energy can be written as

$$E_{C0} = 6 \times \frac{1}{2}NC_d U_{c0}^2 = 2C_e(NU_{c0})^2, \tag{3.42}$$

$$E_{L0} = 6 \times \frac{1}{2}L_s\left(\frac{I_{dc0}}{3}\right)^2 + \frac{1}{2}L_{dc}I_{dc0}^2 = \frac{L_e I_{dc0}^2}{2}. \tag{3.43}$$

Substituting the energy equations into the expression for *A* yields

$$A = \sqrt{\frac{2}{L_e}(E_{C0} + E_{L0})}. \tag{3.44}$$

The capacitor energy is typically much higher than the inductor energy. Hence, the expression for A can be simplified further to

$$A = \sqrt{\frac{2}{L_e}E_{C0}}. \tag{3.45}$$

Substituting (3.39), (3.40) and (3.45) into the expression for fault current and simplifying

$$\langle i_{DC}(t)\rangle_{Ts} \approx A\omega_r t + Asin\beta = \sqrt{\frac{2E_{C0}}{C_e}}\frac{D_1}{L_e}t + I_{dc0} = \frac{2D_1}{L_e}.NU_{dc0}.t + I_{dc0}. \tag{3.46}$$

Therefore, the rate of rise of the DC fault current can be obtained

$$\frac{di_{DC}(t)}{dt} = \frac{2D_1}{L_e}.NU_{dc0},$$

$$D_1 = \frac{L_e}{2NU_{c0}} \frac{di_{DC}(t)}{dt}. \tag{3.47}$$

Thus, varying the value of D_1 should vary the rate of rise of the DC fault current. As established previously, D_1 is the normalized DC component of the arm reference voltages. Therefore, it can simply be appended to the arm voltage references for the six arms of the MMC. To ensure symmetry when the value of D_1 is being varied after DC fault occurrence, a dynamic limiter with the range 0 to $2D_1$ is required. The arm reference voltages and the associated control diagram with D_1 control mode are shown in Figures 3.2 and 3.3 [107].

D_1 can be controlled either in an open or a closed loop manner. If it is controlled in a closed loop, then it would be possible to meet specific $\frac{di_{dc}(t)}{dt}$ targets. As evidenced by the results in [107], $\frac{di_{dc}(t)}{dt}$ is a parameter that can be used to facilitate DC breaker coordination in HB-MMC systems.

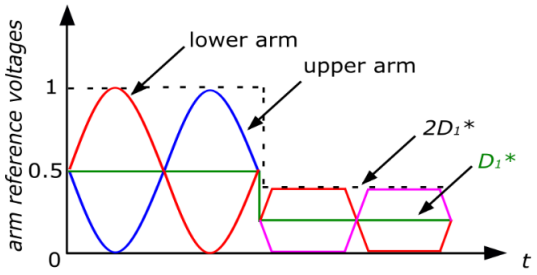


Figure 3.2 Arm reference voltages during SM capacitor discharge control in HB-MMC systems

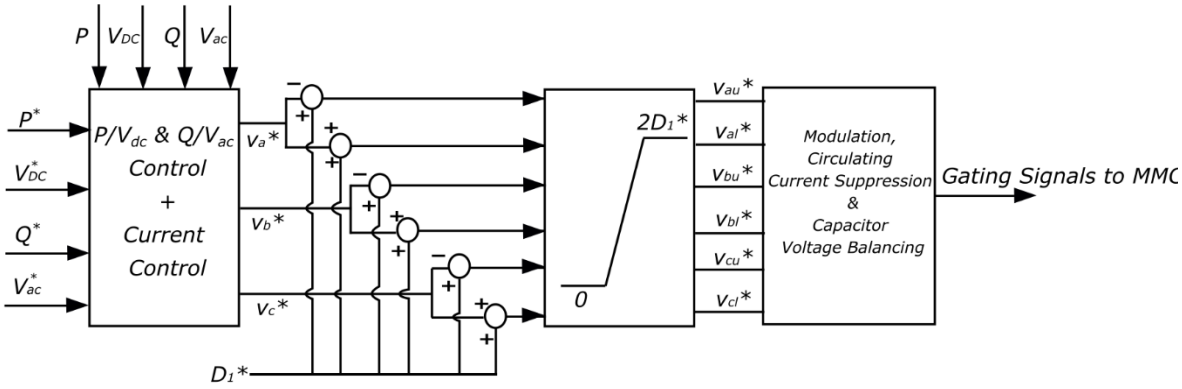


Figure 3.3 Control diagram for SM capacitor discharge control using D_1

It becomes necessary at this point to provide a brief overview of the MMC control system. MMCs are generally operated using traditional *dq* or vector control methods [32], [33], [34]. The control can be divided into upper- and lower-level controls. The upper-level controls are further divided into two parts: outer control and inner decoupled current control. The outer controller consists of two control loops, both using proportional-integral (PI) control blocks. One loop controls either the active power (P) or the DC side voltage (V_{DC}), while the second loop controls the reactive power (Q) or AC side voltage (V_{ac}). These outer controllers generate *d* and *q* axes current references which serve as inputs to the inner current control block as shown in Figure 3.4.

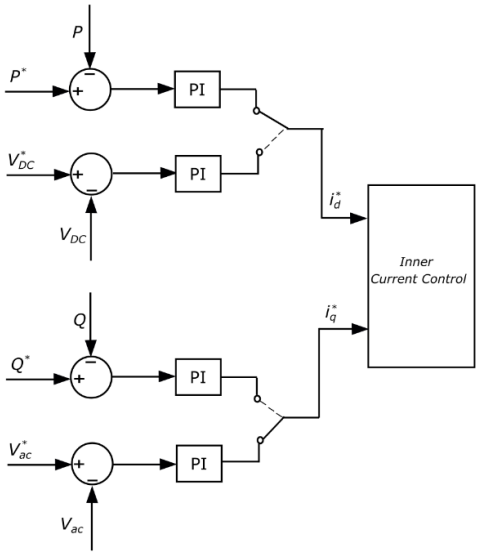


Figure 3.4 Outer control loops

In the inner decoupled current controller, shown in Figure 3.5, d and q axes current values (i_d, i_q) measured from the AC grid are regulated against their references (i_d^*, i_q^*) obtained from the outer controller by means of PI control. PI controller outputs are added to the measured grid voltage dq components and the cross-decoupling voltage terms $\omega L i_d$ and $\omega L i_q$ (L denotes the combined inductance of the converter and transformer). This generates the reference d and q axes components (v_d^*, v_q^*) of the AC voltage which are then transformed back to the abc reference frame (v_{abc}^*). This reference voltage is then fed into the lower-level control system.

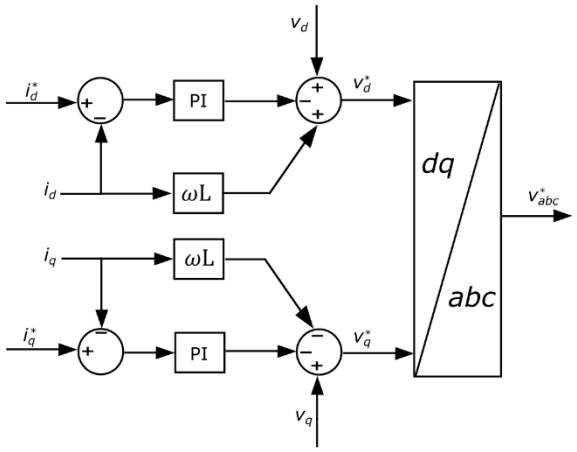


Figure 3.5 Inner decoupled current control loops

The lower-level control system is responsible for the modulation, circulating current suppression, and SM capacitor voltage balancing. The purpose of modulation is to determine the number of SMs to be inserted in the upper and lower arms of the MMC. Common modulation schemes include phase-shifted pulse width modulation, phase-disposition pulse width modulation, and nearest level control.

Switching mismatches between the upper/lower arms of the MMC and the ripple in SM capacitors voltages create a voltage difference between the arms of the phases. This voltage difference creates circulating currents to flow within the phases of the converter. Circulating currents do not affect the DC or AC sides of the MMC but distort arm current waveforms and cause increased power losses. The primary component in the circulating current is of negative sequence and rotates at twice the fundamental frequency. In [110], a controller is presented which can be utilized to suppress the circulating current primary component.

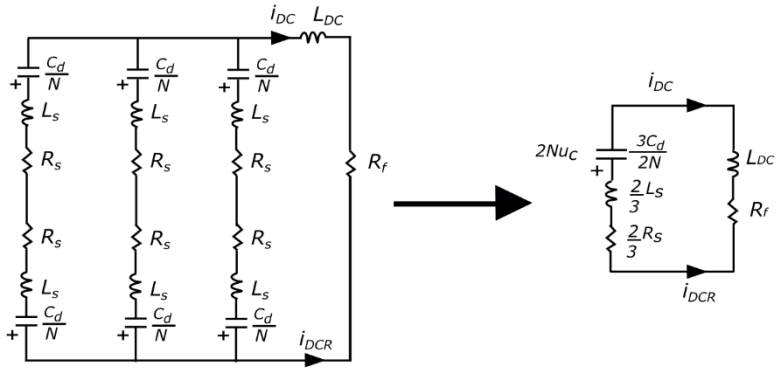
Continuous insertion into the current path inevitably leads to fluctuation in individual SM capacitor voltages. Voltage balancing of the SM capacitors can be achieved either through non-energy- or energy-based methods as mentioned in Chapter 2. Energy-based balancing methods generally have better performance during normal operation. However, they are usually more complex and require modifications during DC faults to continue to operate successfully. On the other hand, the widespread sorting algorithm used for even distribution of capacitor voltages in MMC arms as described in Chapter 2 is simple to implement and requires no changes during DC faults.

3.3 Submodule Capacitor Reverse Discharge Control

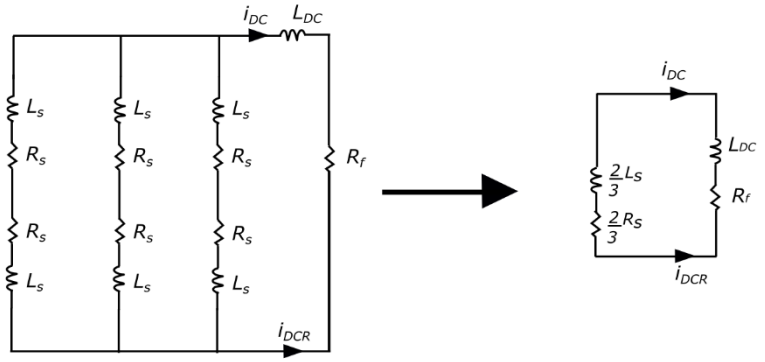
The manipulation of D_1 to influence the rate of rise of the DC fault current can be useful in HB-MMC systems since it would allow the HVDC line reactors to be reduced in size, leading to lower costs. In DC fault-tolerant systems, such as the FB-MMC, converters can either be blocked or the DC fault can be cleared and the MMCs operated as STATCOMs. The DC fault current would be reduced to zero very quickly when blocking action is performed in such fault-tolerant systems. However, the MMCs would lose the ability to provide reactive power support to connected AC systems which may lead to voltage instability. Operating the MMCs as STATCOMs is, therefore, more desirable from such a perspective. However, it can take tens of milliseconds for the fault current to decay to zero after clearance of the DC fault and initiation of the STATCOM mode, due to the slow damping of the fault current by the DC transmission line as mentioned previously. Conventional discharge control described in the previous section can only alter the rate of rise of the fault current, not its direction, and thus would be rendered useless in MMCs utilizing fault-tolerant SMs. Therefore, it becomes necessary to modify this discharge control method and apply it in a way that would improve the DC-FRT performance of fault-tolerant MMCs.

After a DC side fault occurs, but before the fault is detected, the SM capacitors will discharge whenever they are inserted into the current path, leading to a rapid rise in the DC fault current. In an FB-MMC system, the two extra switches in the FBSM would allow the SM capacitors to be inserted in either polarity into the current path. Capacitor discharge would occur regardless of the direction of insertion, but the difference will be in the direction of the discharge current. If the extra switches in FBSMs are utilized to reverse the direction of capacitor insertion immediately after fault detection, then it should result in a reversal of the direction of flow of fault current as well. Such a change in direction of the DC fault current will inevitably result in a zero-crossing that can be taken advantage of. A new

variable for the duty cycle will need to be defined to facilitate such a reverse discharge control scheme. Moreover, the state space formulations will need to be re-examined and modified where necessary to accommodate this reversal of capacitor insertion. Similar to the conventional discharge control mode described in the previous section, there will be two base circuits as shown in Figure 3.6.



(a)



(b)

Figure 3.6 Equivalent circuits for reverse discharge control (a) Base Circuit 1 (b) Base Circuit 2

Let the new duty cycle be represented by D_2. For a switching time-period denoted by T_s, the span of the first subinterval corresponding to base circuit 1, with all capacitors inserted in the reverse direction, would be D_2T_s. The time span of the second subinterval for base circuit 2, with all of the SM capacitors bypassed, would then be (1-D_2)T_s. It should be noted here that once the fault is detected and reverse discharge control mode is initiated, the SM capacitors will no longer be inserted in the conventional direction, and thus the previously defined duty cycle D_1 need not be considered in the base circuits. Two key differences can be observed in the new base circuits: 1) the capacitor in base circuit 1 has been

inserted in reverse as opposed to the previous case involving D_1, and 2) a second variable i_{DCR} for the DC fault current has been introduced whose direction is opposite to that of i_{DC}. Thus, the discharge of the capacitor which is controlled by the new duty cycle D_2 would affect i_{DCR} in the same manner as D_1 influenced i_{DC}. Therefore, the first state variable is changed from i_{DC} to i_{DCR},

$$w(t)=\begin{bmatrix} i_{DCR}(t) \\ u_c(t) \end{bmatrix}. \tag{3.48}$$

Since only the polarity of the capacitor insertion changes in base circuit 1, Kirchhoff's voltage and current equations would remain the same provided the new current direction i_{DCR} is utilized in the expression. Hence, for base circuit 1, the following expressions involving the state variables are obtained

$$2Nu_c(t) - L_e\frac{d}{dt}i_{DCR}(t) - R_e i_{DCR} = 0, \tag{3.49}$$

$$C_e\frac{d}{dt}\{2Nu_c(t)\} + i_{DCR}(t) = 0. \tag{3.50}$$

Similar expressions can be derived for base circuit 2

$$-L_e\frac{d}{dt}i_{DC}(t) - R_e i_{DCR} = 0, \tag{3.51}$$

$$C_e\frac{d}{dt}u_c(t) = 0.$$

It needs to be noted here that the expression involving the second state variable u_c remains the same since it does not contain a term involving the DC current.

Rewriting the equations in matrix form, one gets

$$\begin{bmatrix} L_e & 0 \\ 0 & C_e \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{DCR}(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} -R_e & 2N \\ \dfrac{-1}{2N} & 0 \end{bmatrix}\begin{bmatrix} i_{DCR}(t) \\ u_c(t) \end{bmatrix}, \tag{3.52}$$

$$\begin{bmatrix} L_e & 0 \\ 0 & C_e \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{DCR}(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} -R_e & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} i_{DCR}(t) \\ u_c(t) \end{bmatrix}. \tag{3.53}$$

The averaged matrix needs to be rewritten due to the introduction of the new duty cycle D_2

$$\mathbf{B}=D_2\mathbf{A_1} + (1\text{-}D_2)\mathbf{A_2} \tag{3.54}$$

$$= \begin{bmatrix} -R_e & 2ND_2 \\ -\frac{D_2}{2N} & 0 \end{bmatrix}.$$

The time-averaged state-space expression involving D_2 is given by

$$\begin{bmatrix} L_e & 0 \\ 0 & C_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \langle i_{DCR}(t) \rangle_{Ts} \\ \langle u_c(t) \rangle_{Ts} \end{bmatrix} = \begin{bmatrix} -R_e & 2ND_2 \\ -\frac{D_2}{2N} & 0 \end{bmatrix} \begin{bmatrix} \langle i_{DCR}(t) \rangle_{Ts} \\ \langle u_c(t) \rangle_{Ts} \end{bmatrix} \tag{3.55}$$

Differentiating the first of the two expressions in (3.55) with respect to time yields

$$\frac{d^2}{dt} \langle i_{DCR}(t) \rangle_{Ts} + \frac{R_e}{L_e} \frac{d}{dt} \langle i_{DCR}(t) \rangle_{Ts} - \frac{2ND_2}{L_e} \frac{d}{dt} \langle u_c(t) \rangle_{Ts} = 0. \tag{3.56}$$

From the second expression in (3.55),

$$\frac{d}{dt} \langle u_c(t) \rangle_{Ts} = -\frac{D_2}{2NC_e} \langle i_{DCR}(t) \rangle_{Ts}. \tag{3.57}$$

Substituting (3.57) expression into (3.56), yields

$$\frac{d^2}{dt} \langle i_{DCR}(t) \rangle_{Ts} + \frac{R_e}{L_e} \frac{d}{dt} \langle i_{DCR}(t) \rangle_{Ts} + \frac{D_2^2}{L_e C_e} \langle i_{DCR}(t) \rangle_{Ts} = 0. \tag{3.58}$$

The general solution of the differential equation is

$$\langle i_{DCR}(t) \rangle_{Ts} = A_R e^{-\delta t} \{ sin(\omega_{rR} t + \beta_R) \} \tag{3.59}$$

where

$$\delta = \frac{R_e}{2L_e},$$

$$\omega_{0R} = \sqrt{\frac{D_2^2}{L_e C_e}}, \tag{3.60}$$

$$\omega_{rR} = \sqrt{|\omega_{0R}^2 - \delta^2|}. \tag{3.61}$$

Expressions for A_R and β_R will need to be derived in a similar fashion from initial conditions. The initial condition involving the DC current will also need to be updated due to the change in state variable (the initial condition for voltage remains the same). Therefore,

$$\langle i_{DCR}(0^+) \rangle_{Ts} = -I_{DC0} \tag{3.62}$$

Substituting (3.62) into (3.59) at $t = 0^+$ yields

$$A_R = -\frac{I_{DC0}}{sin\beta} \tag{3.63}$$

Differentiating (3.59) with respect to time yields

$$\frac{d}{dt}\langle i_{DCR}(t)\rangle_{Ts} = A_R\{-\delta e^{-\delta t}sin(\omega_{rR}t + \beta_R) + \omega_{rR}e^{-\delta t}cos(\omega_{rR}t + \beta_R)\}. \tag{3.64}$$

From the first equation of the state space representation in (3.55), one gets

$$\frac{d}{dt}\langle i_{DCR}(t)\rangle_{Ts} = \frac{1}{L_e}\{-R_e\langle i_{DCR}(t)\rangle_{Ts} + 2ND_2\langle u_c(t)\rangle_{Ts}\},$$

$$\text{OR } \frac{d}{dt}\langle i_{DCR}(t)\rangle_{Ts} = \frac{2ND_2\langle u_c(t)\rangle_{Ts} - R_e\langle i_{DCR}(t)\rangle_{Ts}}{L_e}. \tag{3.65}$$

Equating (3.64) and (3.65) yields,

$$A_R\{-\delta e^{-\delta t}sin(\omega_{rR}t + \beta_R) + \omega_{rR}e^{-\delta t}cos(\omega_{rR}t + \beta_R)\} = \frac{2ND_2\langle u_c(t)\rangle_{Ts} - R_e\langle i_{DCR}(t)\rangle_{Ts}}{L_e}.$$

Utilizing initial conditions and substituting for A_R and δ yields,

$$-\frac{I_{DC0}}{sin\beta_R}\left(-\frac{R_e}{2L_e}sin\beta_R + \omega_{rR}cos\beta_R\right) = \frac{1}{L_e}(2ND_2U_{C0} + R_eI_{DC0}).$$

Rearranging the terms and simplifying,

$$tan\beta_R = \left(\frac{2\omega_{rR}L_eI_{DC0}}{4D_2NU_{c0} + R_eI_{DC0}}\right),$$

$$\Rightarrow \beta_R = arctan\left(\frac{-2\omega_{rR}L_eI_{DC0}}{4D_2NU_{c0} + R_eI_{dc0}}\right). \tag{3.66}$$

Therefore, the solution to the differential equation given by (3.59) can be completed by

$$\delta = \frac{R_e}{2L_e},$$

$$\omega_{0R} = \sqrt{\frac{D_2^2}{L_eC_e}},$$

$$\omega_{rR} = \sqrt{|\omega_{0R}^2 - \delta^2|},$$

$$A_R = -\frac{I_{DC0}}{sin\beta},$$

$$\beta_R = arctan(\frac{-2\omega_{rR}L_eI_{DC0}}{4D_2NU_{c0}+R_eI_{dc0}}).$$

Once again, R_e is assumed to be zero considering that the circuit resistance is small. This implies that δ will be equal to zero as well. Therefore,

$$\omega_{rR} = \omega_{0R} = D_2\sqrt{\frac{1}{L_eC_e}}, \tag{3.70}$$

$$\beta_R = arctan\left(\frac{-\omega_{rR}L_eI_{DC0}}{2D_2NU_{c0}}\right) = arctan\left(\frac{-I_{DC0}}{2NU_{c0}}\sqrt{\frac{1}{L_eC_e}}\right). \tag{3.71}$$

The simplified expression for β_R is used to obtain the value for A_R by making use of Pythagoras' Theorem

$$A_R = \frac{-I_{DC0}\sqrt{(2NU_{C0})^2+\left(-I_{DC0}\sqrt{\frac{L_e}{C_e}}\right)^2}}{-I_{DC0}\sqrt{\frac{L_e}{C_e}}} = \sqrt{\frac{2}{L_e}\left[2C_e(NU_{c0})^2+\frac{L_eI_{DC0}^2}{2}\right]}. \tag{3.72}$$

Substituting the inductor and capacitor energy equations from (3.45)-(3.46) into the expression for A_R yields

$$A_R = \sqrt{\frac{2}{L_e}(E_{C0}+E_{L0})}. \tag{3.73}$$

The capacitor energy is typically much higher than the inductor energy. Hence, the expression for A_R can be simplified further to

$$A_R = \sqrt{\frac{2}{L_e}E_{C0}}. \tag{3.74}$$

Substituting A_R into the expression for fault current,

$$\langle i_{DCR}(t)\rangle_{Ts} \approx A_R\omega_{rR}t + A_Rsin\beta_R = \sqrt{\frac{2E_{C0}}{C_e}}\frac{D_2}{L_e}t - I_{DC0} = \frac{2D_2}{L_e}.NU_{c0}.t - I_{DC0}. \tag{3.75}$$

Thus, an expression involving D_2 and the DC fault current i_{DCR} is found as

$$D_2 = \frac{L_e}{2NU_{c0}} . \left[\frac{di_{DCR}(t)}{dt}\right]. \tag{3.76}$$

Recalling that i_{DCR} is actually -i_{DC},

$$D_2 = -\frac{L_e}{2NU_{c0}} . \left[\frac{di_{DC}(t)}{dt}\right]. \tag{3.77}$$

The solution confirms that variations in the value of D_2 can be used to influence the rate of change of the fault current i_{DC}. However, the effect will be in the reverse direction when compared to the control over the rate of change of i_{DC} by variation of D_1in the conventional discharge control method. Figure 3.7 illustrates the change in MMC arm voltage references when control is switched to reverse discharge control mode after DC fault detection. The associated control diagram involving D_2 reverse discharge control is shown in Figure 3.8. It needs to be mentioned here that the arm reference DC component in the control diagram will be equal to 0.5 with no dynamic limiters during normal operation. During reverse discharge control, D_2 cannot simply be added to the arm reference voltage as was the case with D_1. This is because the SMs will be inserted in reverse and therefore the arm voltage range will need to change from [0,1] to [0,-1]. The DC component of the arm voltage references is equal to 0.5 during normal operation; this factor needs to be subtracted from the references in reverse discharge mode. Afterward, the value of D_2 is subtracted from the arm voltage references yielding a combined factor of (-0.5-D_2) at the summing junction in the control diagram. D_2 is subtracted instead of being added because it is the SM insertion parameter in the reverse direction.

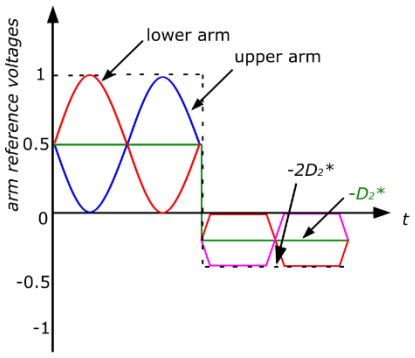


Figure 3.7 Arm reference voltages during reverse discharge control

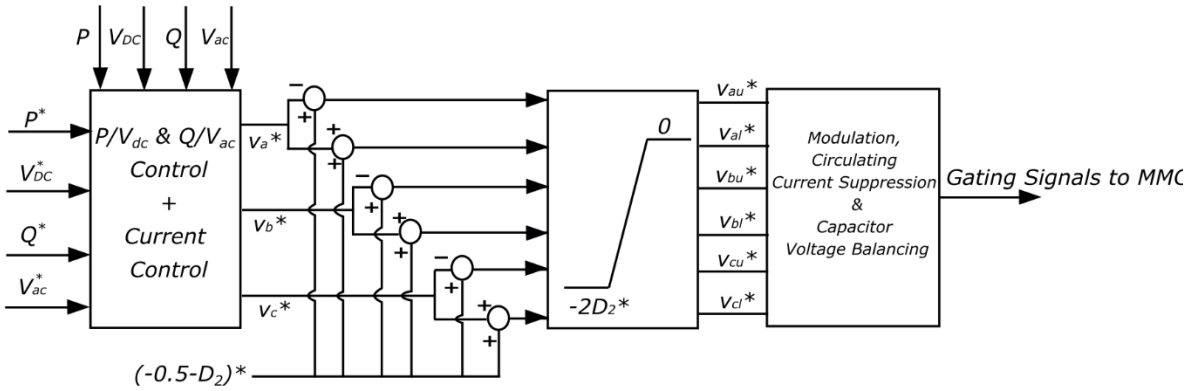


Figure 3.8 Control diagram for reverse discharge control using D_2

3.4 DC Fault Clearance and STATCOM Operation

As mentioned in Chapter 2, the DC side voltage needs to be synthesized as zero by the MMC arms after DC side fault detection to clear the fault and allow the MMC to operate as a STATCOM. This can be achieved by simply removing the DC component from the MMC arm voltage references. Figure 3.9 depicts the change in arm voltage references required to clear the DC fault and initiate STATCOM operation, while Figure 3.10 shows the associated control diagram. Another change is essential to ensure energy balance is maintained in the MMC while riding through the DC fault. This is done through a modification in the outer controllers as suggested by the authors in [98], [97], more specifically in the P/V_{DC} loop that provides the reference for the *d*-axis current.

When a DC fault occurs, active power cannot be transferred through the DC line. So, the active power reference should be set to zero. However, some active power will need to be provided to the SMs to account for losses in the switches. Therefore, the *d*-axis current reference should be provided by some other means instead of P/V_{DC}. This change is illustrated in Figure 3.11, where the *d*-axis current reference is obtained by employing a PI controller involving V_{SM}, the nominal SM capacitor voltage, and $v_{c,av}$, the average value of the measured capacitor voltages across all SMs in the MMC. Such an outer loop would ensure that the average capacitor voltage and therefore the total energy stored in the MMC capacitors is kept reasonably constant during the fault. The conventional sorting algorithm is kept in place to ensure equal voltage distribution in all six MMC arms.

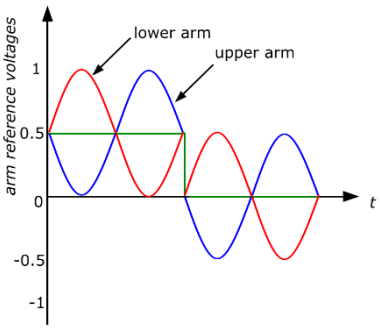


Figure 3.9 Arm reference voltages for DC fault clearance and STATCOM operation

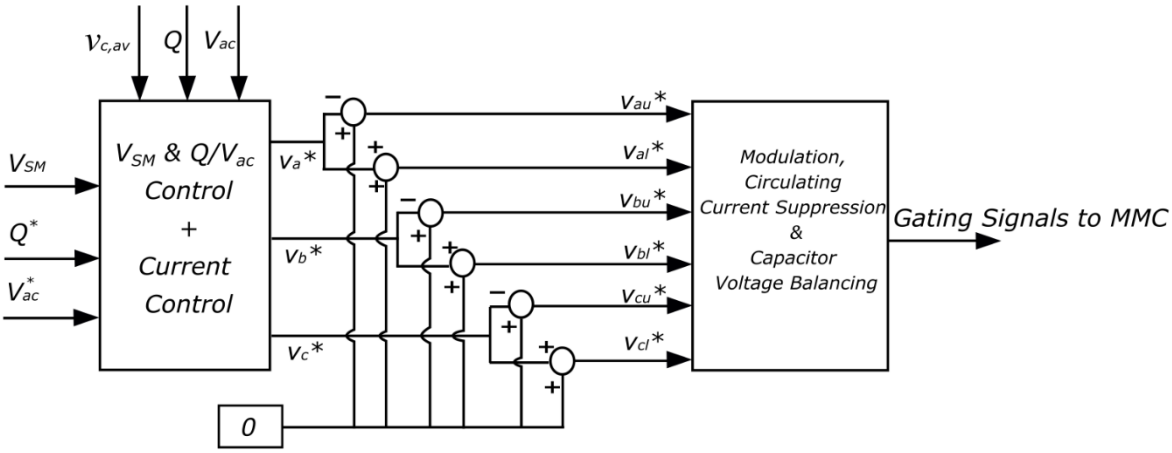


Figure 3.10 Control diagram for DC fault clearance and STATCOM operation

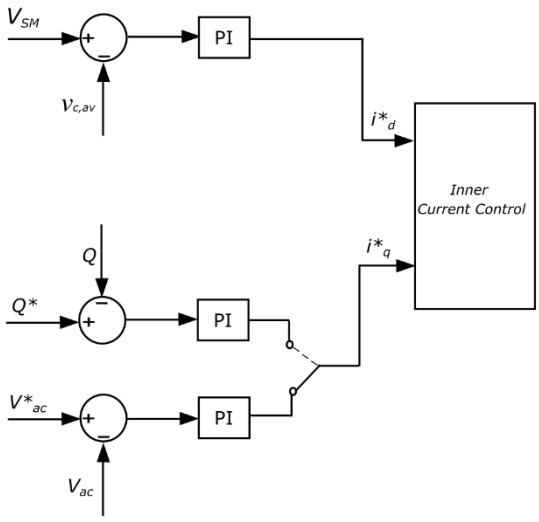


Figure 3.11 Outer controllers during STATCOM operation

3.5 Proposed Control Scheme

It has already been established that activating reverse discharge control after detection of DC fault will force the DC fault current to change direction and have a zero-crossing. Meanwhile, the conventional method of DC-FRT involves adjusting the MMC arm reference voltages to clear the DC fault and operating the MMC as a STATCOM to provide AC side reactive power support. However, DC fault current suppression by utilizing this conventional method usually takes tens of milliseconds due to significant oscillations in the DC current [8]. To overcome this issue, reverse discharge control mode may be utilized immediately upon fault detection to reduce the DC fault current to zero followed by the conventional method of DC fault clearance and initiation of STATCOM operation. Clearing the DC fault and initiating STATCOM operation at lower values of the DC fault current is likely to lead to lower oscillations and by extension, faster fault current suppression. The steps involved in the proposed control scheme are shown as a flowchart in Figure 3.12. The theoretical predictions are verified through simulations in PSCAD/EMTDC environment.

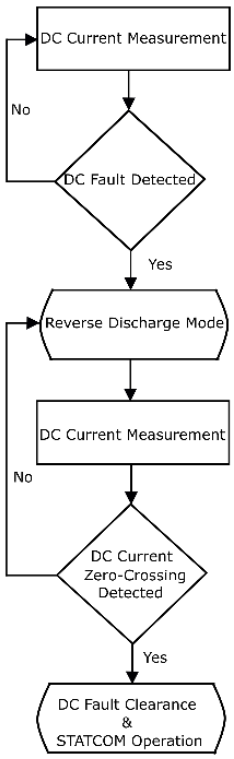


Figure 3.12 Flowchart for the proposed control scheme

3.6 Test System

The test system consists of a point-to-point HVDC connection, with FBSM-based MMCs at either end, as shown in Figure 3.13. The relevant parameters are given in Tables 3.1 and 3.2.

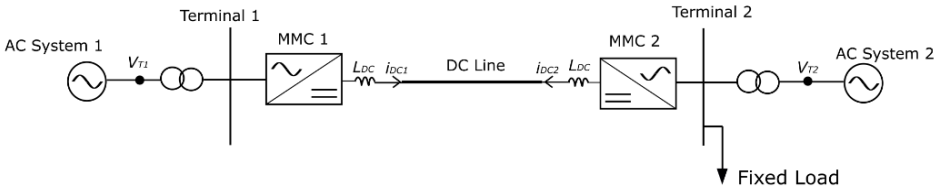


Figure 3.13 Test System

Table 3.1 Test System Parameters

Parameters	MMC 1	MMC 2
Operating Condition	-900MW Active power control	640kV DC side voltage control
Capacity (P_{rated})	1000 MW	1000 MW
SM Capacitance (C)	3 mF	3 mF
Carrier Frequency (f_c)	300 Hz	300 Hz
Number of SMs per arm (N)	76	76
IGBT and diode on-state resistance (R_d)	0.005 Ω	0.005 Ω
Arm inductance (L_s)	50 mH	50 mH
Arm resistance (R_s)	0 Ω	0 Ω
DC Line Reactor inductance (L_{DC})	50 mH	50mH
Nominal AC Voltage ($V_{AC,LL}$)	240kV	230kV
Transformer Reactance (X_t)	0.1 pu	0.1 pu
Transformer Turns Ratio	230 kV: 370 kV	230 kV: 370 kV

Table 3.2 Test System DC Transmission Line Parameters [111]

Item	Value
Resistance per unit length	0.009735 Ω/km
Inductance per unit length	0.0176 mH/km
Capacitance per unit length	0.001367 μF/km

The parameters for the equivalent circuit corresponding to the test system are calculated as

$$L_e = \frac{2L_s}{3} + L_{DC} = 83.33 \text{ mH},$$

$$R_e = \frac{2R_s}{3} + R_f = 1\ \Omega,$$

$$C_e = \frac{3C_d}{2N} = 59.21\ \mu\text{F}.$$

Table 3.3 shows critical damping mode values of D_2 for different values of the fault resistance and DC line reactor inductance. Considering that the test system fault resistance is 1 Ω and DC line reactor inductance is 50 mH, any value of D_2 over 0.013 will ensure an underdamped fault circuit.

Table 3.3 Critical values of D_2 with variation in R_f and L_{DC}

R_f (Ω)	L_{DC} (mH)	Critical D_2
1	50	0.013
1	100	0.009
1	200	0.0067
10	50	0.13
10	100	0.094
10	200	0.067

The selection of D_2 can be made according to inductor specifications since high *di/dt* can cause overvoltage in the inductors. If the inductors have an upper voltage limit, then D_2 can be used to meet specific *di/dt* targets. Unlike the case of discharge control with D_1 on HB-MMC systems, there are no DC breakers on the test FB-MMC system; therefore, breaker coordination by setting targets for *di/dt* is not applicable here.

In the test system, the FB-MMCs are controlled by the conventional *dq* method described earlier in the chapter. The circulating current suppression controller described in [110] is implemented as well. Terminal 1 controls the DC voltage while terminal 2 controls the active power. The DC line voltage is 640 kV and transfers 900 MW of power, which results in a DC current of 1.5 kA. The fixed power load draws an active power of 150 MW and reactive power of 150 MVAR per phase. A permanent pole-to-pole fault is applied in the middle of the 300 km-long DC line at t=3 s, with a fault resistance of 1 Ω. As soon as the fault occurs, the fault current increases rapidly due to the discharge of FBSM capacitors. The fault detection delay is assumed to be 2ms. After the fault is detected, both MMCs are put into D_2 reverse discharge control mode. When the measurement of the DC line current at the corresponding terminal reaches zero, the DC fault is cleared by adjusting the MMC arm reference voltages and STATCOM operation is initiated to provide AC side voltage support. The outer control loop controlling the *d*-axis current reference in both MMCs is switched to V_{SM} control to ensure energy balance.

3.7 Simulation Results

Figure 3.14 shows the DC currents at both terminals after the occurrence of a pole-to-pole DC fault and subsequent D_1 discharge control mode initiation. This serves as a check that D_1 discharge control does indeed work to reduce the rate of rise of the DC fault current.

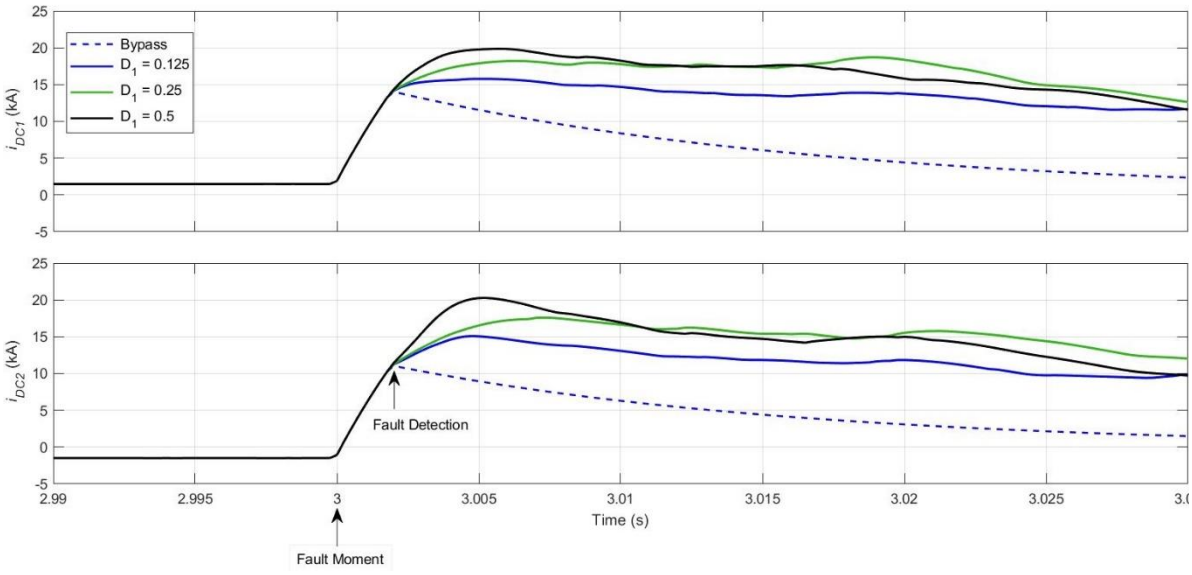


Figure 3.14 DC currents at the terminals during discharge control mode

A similar test involving D_2 reverse discharge control (without clearing the DC fault and initiating STATCOM operation after the zero-crossing) is performed as well. The results are shown in Figure 3.15. The DC current waveforms clearly show that initiating reverse discharge brings about a quick zero-crossing and that higher values of D_2 result in steeper slopes for both i_{DC1} and i_{DC2}.

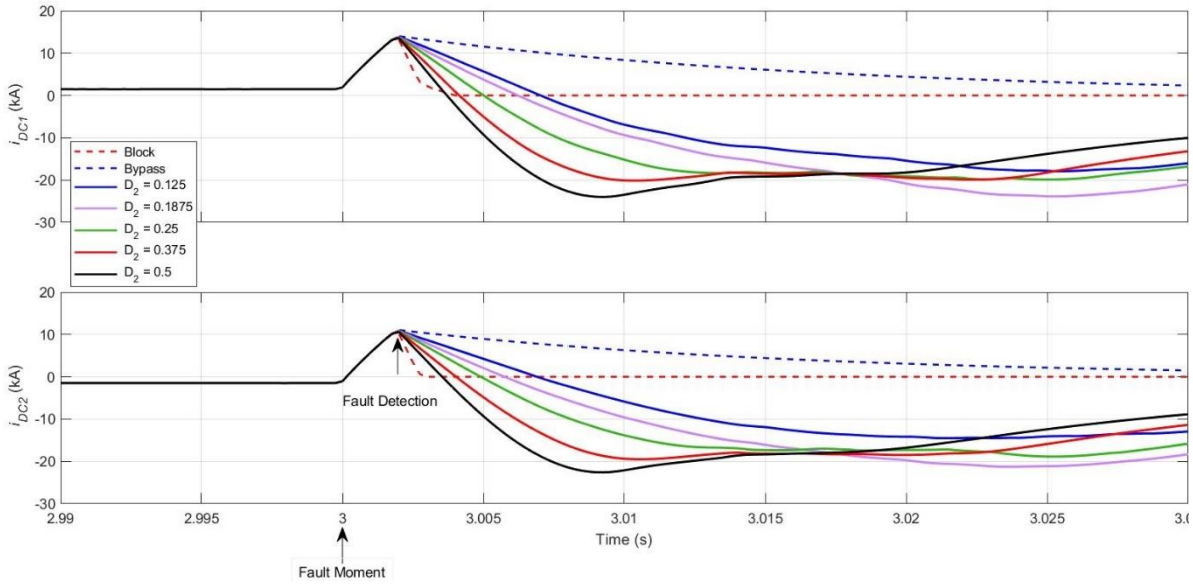


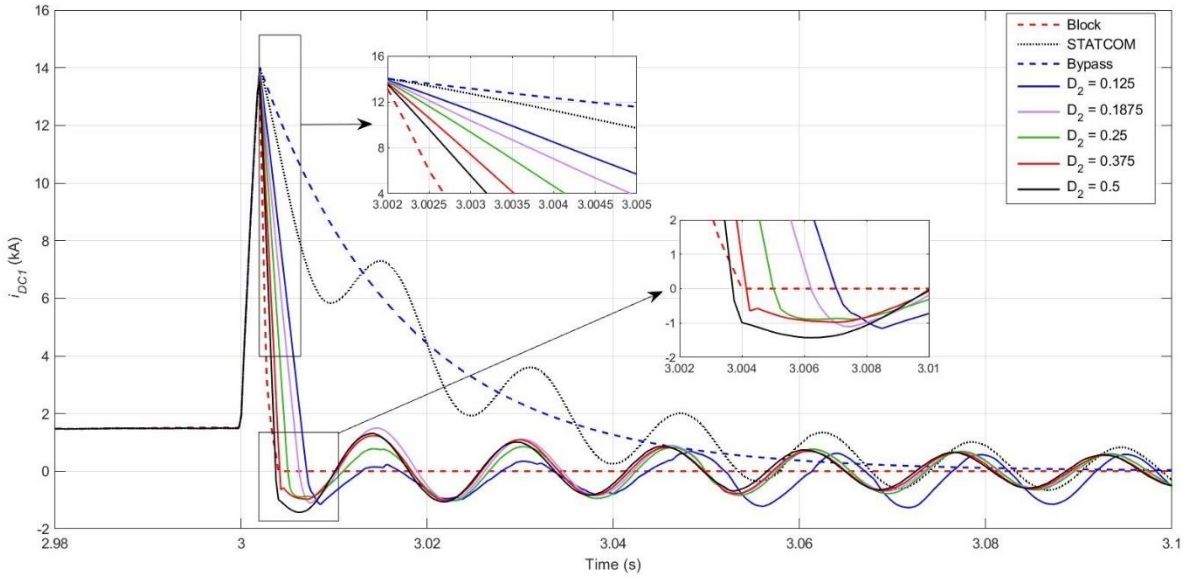
Figure 3.15 DC currents at the terminals during reverse discharge control mode

3.7.1 DC side Current

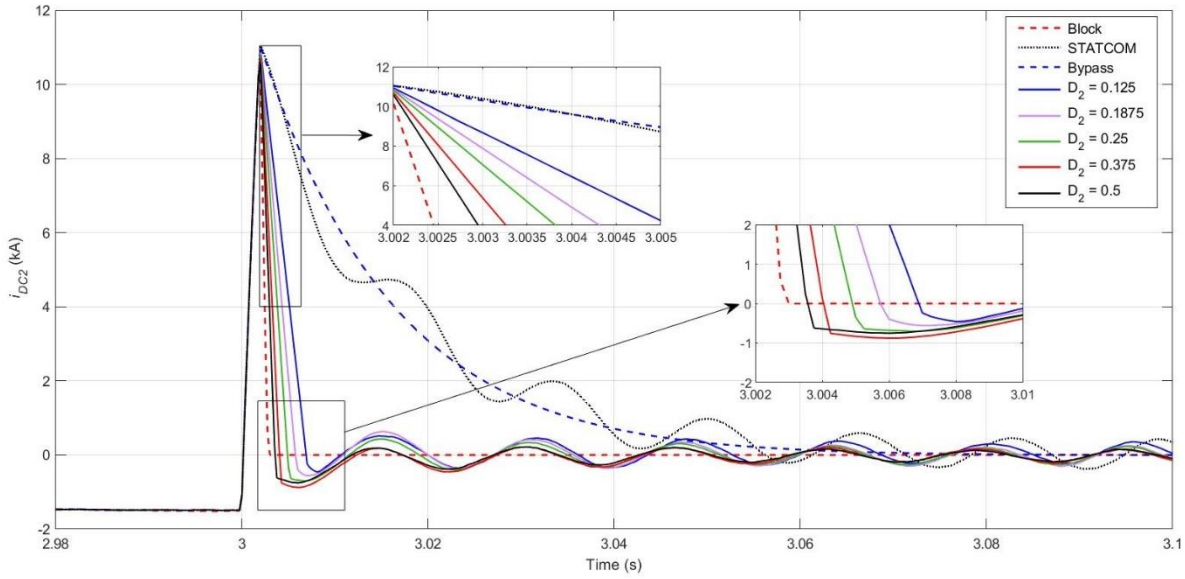
Now that both control methods have been shown to effectively influence the slope of the DC fault current, the next step would be to check the viability of the proposed scheme where reverse SM discharge control is followed by DC fault clearance and STATCOM operation after fault current zero-crossing. The value of D_2 is varied between 0.125 and 0.5 and the DC currents measured at both MMCs are plotted in Figure 3.16. DC current values for cases when the MMCs are blocked, bypassed, and when DC fault clearance/STATCOM operation (indicated as "STATCOM" in the plots) is initiated immediately upon DC fault detection are added to the plots to provide an effective comparison with existing DC-FRT methods.

The results show that blocking the MMCs is the fastest way to suppress the fault currents while the bypass mode is the slowest. Furthermore, Figure 3.16 shows that higher values of D_2 result in higher values of DC fault current falling slopes. Therefore, reverse discharge control with higher values of D_2 cause the DC current to cross zero in shorter timeframes. Once the current zero-crossing is detected, the DC fault is cleared by adjusting the MMC arm voltage references and STATCOM operation is initiated. Due to the fault being cleared at lower values of the DC current, the proposed control scheme is seen to be significantly superior in terms of fault current suppression times when compared to the

conventional DC-FRT procedure, in which DC fault clearance/STATCOM operation is initiated immediately upon detection of the DC side fault.



(a)



(b)

Figure 3.16 DC current at: (a) Terminal 1; (b) Terminal 2

The calculated values of $\frac{di_{DC}(t)}{dt}$ (from the linearized equation) and the simulated values for both MMCs are provided in Table 3.4. The simulated $\frac{di_{DC}(t)}{dt}$ values represent slopes in the first 1ms after reverse discharge mode initiation for higher accuracy. Since the MMCs have identical parameters, calculated values of the slopes are common for both.

Table 3.4 Calculated and simulated values of DC current slope during reverse discharge control

D_2	$\frac{di_{DC}(t)}{dt}$ (Calculated) (kA/ms)	$\frac{di_{DC1}(t)}{dt}$ (Simulated) (kA/ms)	$\frac{di_{DC2}(t)}{dt}$ (Simulated) (kA/ms)
0.125	-1.92	-2.57	-2.25
0.1875	-2.88	-3.44	-2.98
0.25	-3.84	-4.42	-3.75
0.375	-5.76	-6.23	-5.31
0.5	-7.68	-7.96	-6.91

3.7.2 AC side Currents

Figures 3.17-3.19 show the AC side currents for terminal 1, terminal 2, and MMC 2 (since the fixed load creates a node at terminal 2). The blocking mode can suppress the fault current through the MMC very quickly, although this mode cannot provide voltage support to the AC grid. As expected, the bypass mode (D_2=0) results in very high AC side currents. This is because when the SMs are bypassed, the DC side fault is transformed into an AC side short circuit leading to drops in the DC and hence the AC side voltages at the terminals. Lower D_2 values imply a higher proportion of SMs are bypassed, thus resulting in higher transient peaks in the AC side currents. No noticeable differences are observed in the AC side current waveforms between the conventional DC-FRT procedure where the fault is cleared and STATCOM operation initiated immediately upon fault detection and the proposed scheme when high D_2 values are utilized.

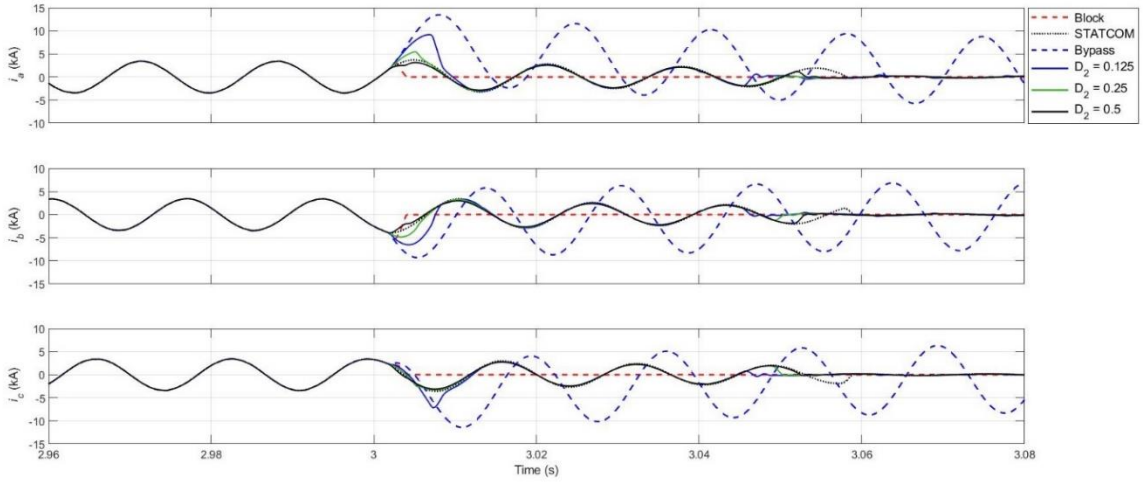


Figure 3.17 AC side currents at Terminal 1

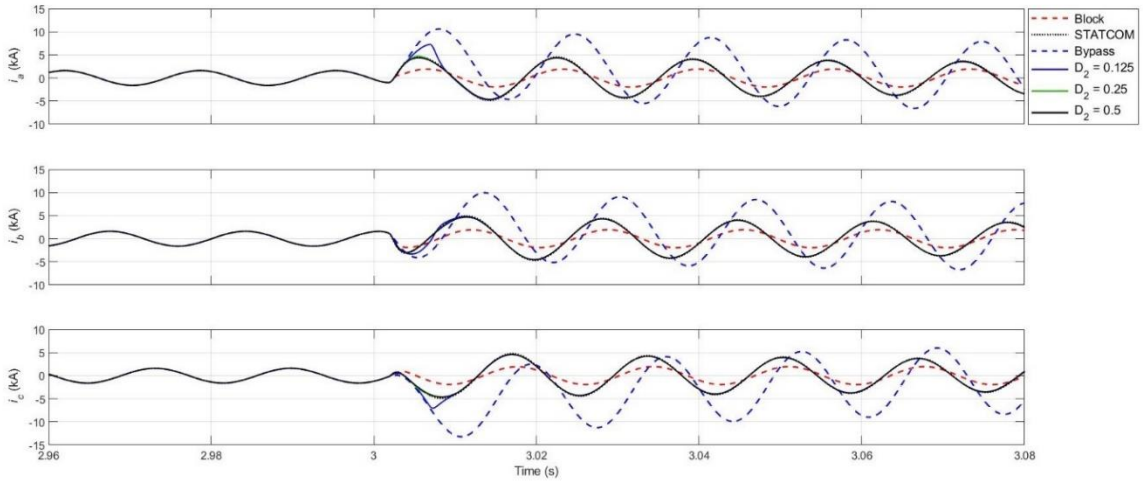


Figure 3.18 AC side currents at Terminal 2

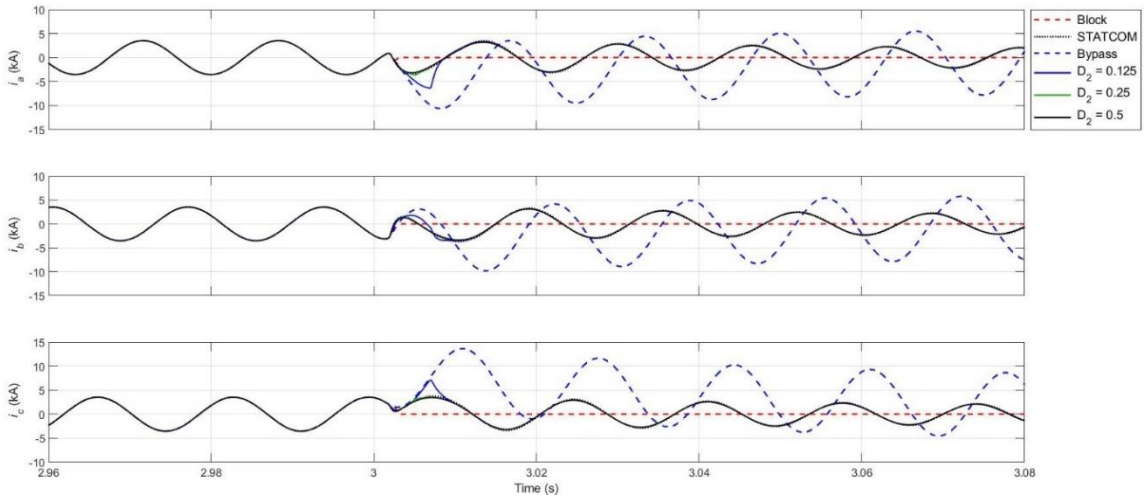
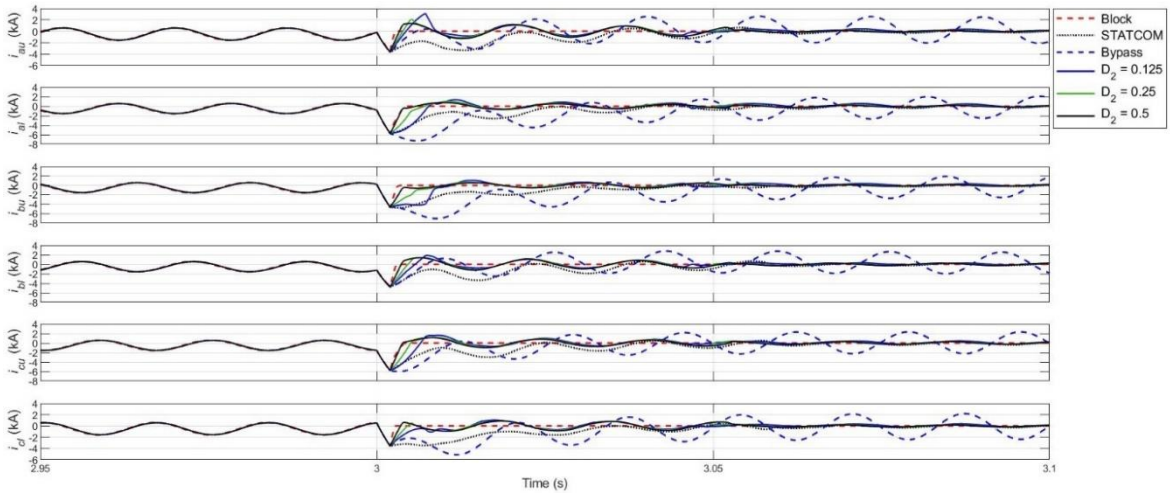


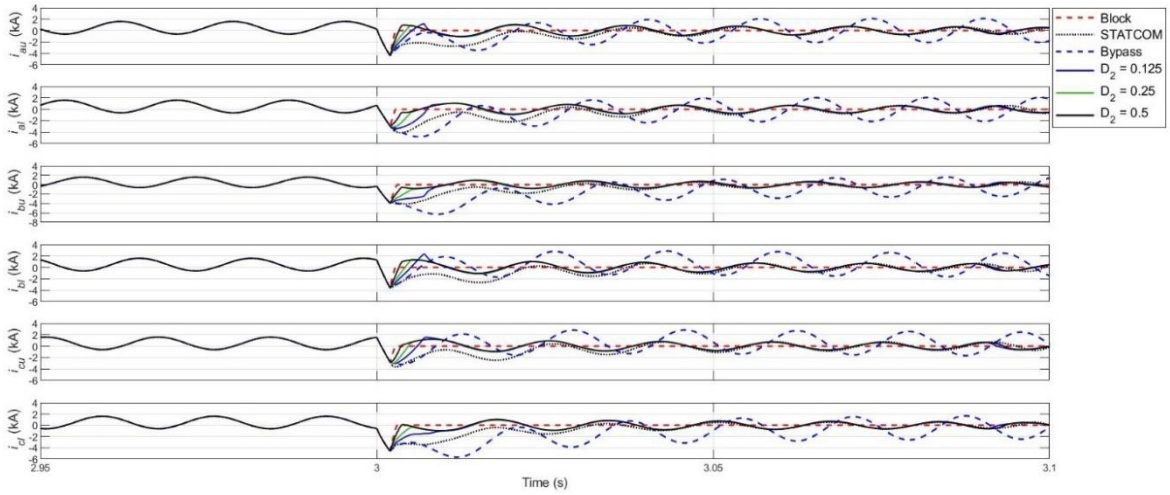
Figure 3.19 AC side currents at MMC 2

3.7.3 Arm Currents

Figures 3.20 show the arm currents in all six arms of both MMCs. Blocking the IGBTs results in very fast suppression of the MMC arm currents. Meanwhile, the bypass mode results in the highest arm current amplitudes. This is to be expected since bypassing the SMs converts the DC side short circuit to an AC side short circuit. These high AC side currents do not flow into the DC fault; instead, they circulate within the MMC arms. The proposed scheme is seen to keep better control over the arm current transient peaks compared to conventional DC fault clearance/STATCOM operation mode, provided high D_2 values are utilized. This is a direct consequence of reduced oscillations in the DC side current since approximately one-third of the DC current flows through each leg of the MMC. It should be noted that lower D_2 values will lead to higher transient fluctuations in the arm currents and, therefore, IGBT ratings must be taken into account when the selection is made. For example, the ABB 5SNA 3000K452300 [112] has a peak collector current rating of 6 kA, which can be withstood for a maximum of 1ms.



(a)



(b)

Figure 3.20 Arm currents of (a) MMC 1 and (b) MMC 2

3.7.4 Terminal Voltages

Figure 3.21 shows the line-line RMS voltages at both terminals before and after DC side fault occurrence. In bypass mode, the DC side fault transforms into an AC side short circuit leading to significant voltage drops at the terminals. In blocking mode, terminal 1 is unaffected while terminal 2 shows a significant drop. This is because there are no loads connected at terminal 1 and the AC system is strong. Therefore, reactive power support from MMC 1 is not needed during the fault. This is not the

case for terminal 2, where a fixed load that draws a constant power of 150MW and 150 MVAR per phase is connected. Since MMC 2 is blocked, it cannot provide reactive power support leading to a drop in terminal 2 voltage. As for the performance of the proposed scheme with high D_2 values, the results are similar to the conventional DC fault clearance/STATCOM operation mode. Lower D_2 values result in greater fluctuations due to higher voltage drop at the terminal during reverse discharge control.

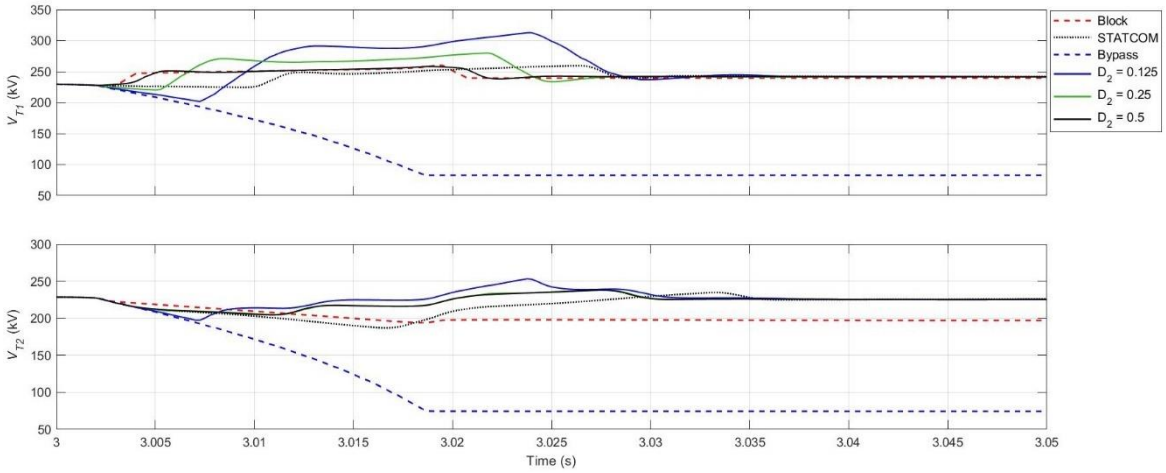
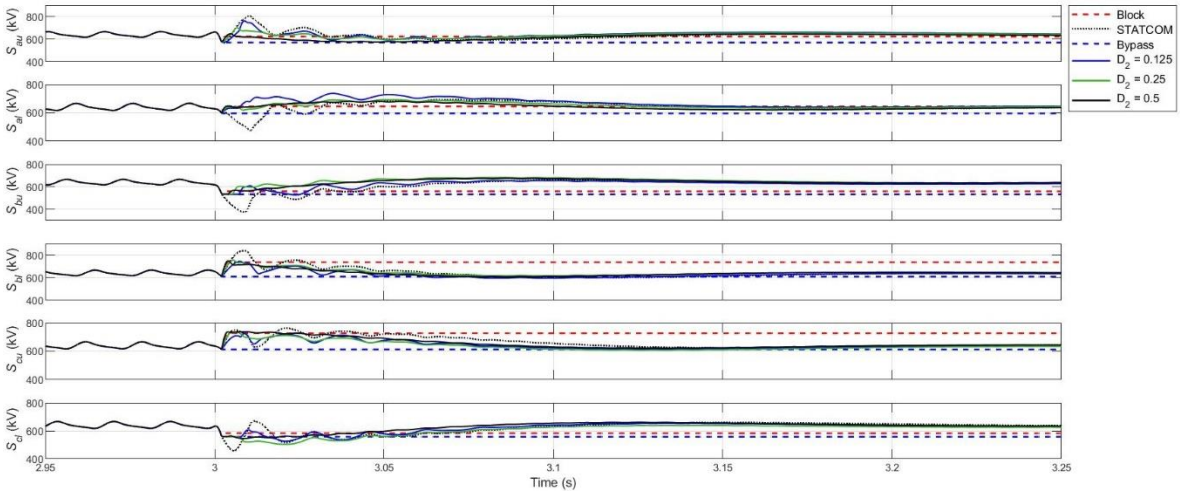


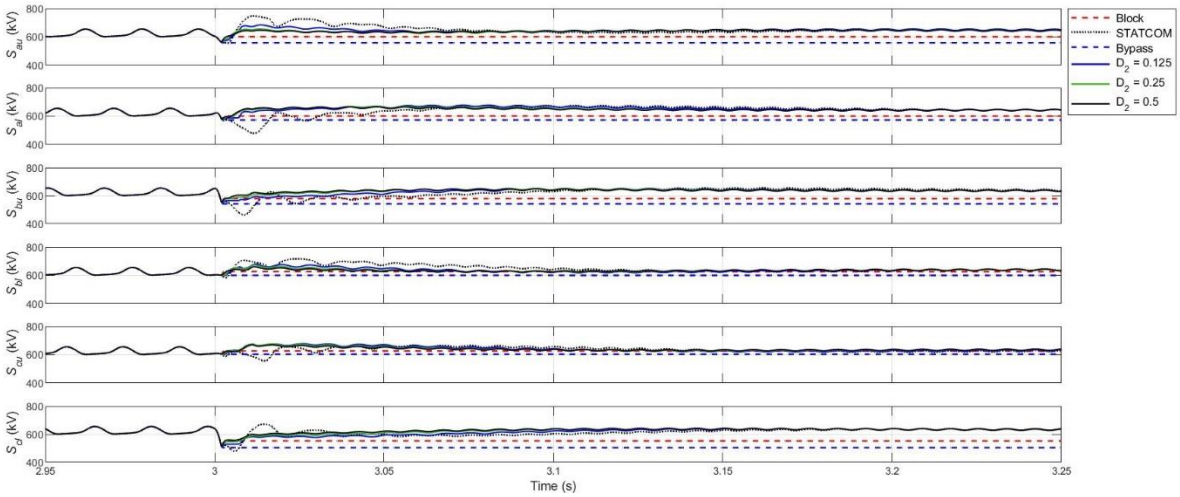
Figure 3.21 Line-to-line RMS voltages at Terminals 1 and 2

3.7.5 Capacitor Voltages

Figure 3.22 shows the sum of the capacitor voltages (S_{xu} and S_{xl} where x=a,b,c) for all the arms of both MMCs. In the blocking mode, there is no current flow through MMC arms and the SM capacitor voltages remain constant throughout the fault. The outcome is similar in the bypass mode where the arm currents do not flow through the SM capacitors. The results also indicate that in the proposed control scheme, the modified V_{SM} control loop along with the conventional sorting method keeps the arm energies very well balanced. In fact, the proposed control scheme maintains arm energy balance better than the conventional DC fault clearance/STATCOM mode of operation during the transient period provided that high D_2 values are utilized. This is because, in the conventional method, the arm current transient peaks are higher leading to greater fluctuations in the capacitor voltages.



(a)



(b)

Figure 3.22 Sum of capacitor voltages at (a) MMC 1 and (b) MMC 2

3.8 Conclusion

This chapter analyzed a state-space averaging approach to control the DC fault current rise rate through SM capacitor discharge regulation in HB-MMC systems. It then proposed a modified scheme that is suitable for use in FBSM-based MMCs or any MMC consisting of bipolar SMs. The goal behind the modification is to provide a simple method that can be utilized in fault-tolerant MMC systems to facilitate fast DC fault current suppression when the MMCs are operated as STATCOMs during DC

faults. The purpose of the original method is to reduce the rate of increase of the DC fault current during the discharge phase of the capacitors, thereby leading to a reduction in the size of HVDC line reactors. Therefore, it holds no value in MMC-HVDC systems comprising of fault blocking SMs where the SM capacitors can either block the DC fault current entirely or ride through the fault with the MMCs operating as STATCOMs. With the modified scheme presented in this thesis, the regulation of SM capacitor discharge is performed in the reverse direction, facilitating an immediate reversal in the DC fault current direction and a very fast drop-off towards the zero-crossing. DC fault clearance and STATCOM operation are initiated in the MMCs immediately after the detection of zero-crossing of the DC fault current. Extensive simulation studies verified the performance of the proposed control scheme and demonstrated how it reduced oscillations leading to significantly faster fault current suppression when compared to the conventional DC-FRT method.

Chapter 4
Conclusion

4.1 Summary

In this thesis, a variety of noteworthy SM topologies, as well as hybrid MMC configurations, with DC fault blocking capability, were reviewed and compared from different viewpoints. Configurations capable of riding through DC faults while operating as STATCOMs were also surveyed. Energy-based voltage balancing techniques for SM capacitors require modifications during DC faults; such modifications were discussed as well.

This thesis also developed a modified reverse SM capacitor discharge scheme that can be utilized during DC faults in bipolar SM-based MMCs to bring about a rapid reversal in the DC fault current direction. Such a rapid reversal leads to a fast drop-off in the DC fault current towards the zero-crossing. The DC fault is cleared and STATCOM operation is initiated immediately after zero-crossing of the fault current utilizing local DC current measurements from each MMC. The proposed scheme results in significantly faster fault current suppression when compared with the conventional scheme where DC fault clearance and STATCOM operation are initiated in the MMCs immediately upon detection of DC side faults. The theoretical analyses and the reliable performance of the proposed scheme are verified through simulations in the PSCAD/EMTDC environment.

4.2 Thesis Contributions

This thesis makes the following contributions:

- Performing a comprehensive literature review and critical analysis of fault blocking configurations and fault ride through techniques in MMCs; and
- Development of a fast DC fault current suppression scheme with fault ride through capability for fault blocking MMCs, which is based on reverse SM capacitor discharge control that can be utilized for rapid reversal in the direction of the fault current and initiating DC fault clearance/STATCOM operation after zero-crossing of the DC fault current.

4.3 Future Work

Further research can be conducted in the following areas:

- Investigating the performance of the proposed control scheme during DC faults on multi-terminal DC (MTDC) systems;
- Developing a method that would allow the DC line impedance to be incorporated into the state-space model of the MMC fault circuit.

References

[1] C.-K. Kim, V. K. Sood, G.-S. Jang, S.-J. Lim and S.-J. Lee, HVDC Transmission: Power Conversion Applications in Power Systems, Wiley-IEEE Press, 2009.

[2] U. Axelsson, A. Holm, C. Liljegren, M. Aberg, K. Eriksson and O. Tollerz, "The Gotland HVDC Light project-experiences from trial and commercial operation," in *16th International Conference and Exhibition on Electricity Distribution, 2001 Part 1: Contributions. CIRED. (IEE Conf. Publ No. 482), 2001, pp. 5 pp. vol.1*, 2001.

[3] O. E. Oni, I. E. Davidson and K. N. I. Mbangula, "A review of LCC-HVDC and VSC-HVDC technologies and applications," in *16th International Conference on Environment and Electrical Engineering (EEEIC), pp. 1-7*, Florence, 2016.

[4] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *IEEE Bologna Power Tech Conf. Proc., Bologna, Italy, 2003 vol. 3, p. 6*, Bologna, 2003.

[5] G. Adam, K. Ahmed, S. Finney, K. Bell and B. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 335-346, Feb. 2013.

[6] A. Dekka, B. Wu, R. L. Fuentes, M. Perez and N. R. Zargari, "Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631-1656, Dec. 2017.

[7] L. Ning, N. Tai, X. Zheng, W. Huang and M. H. Nadeem, "Detection and classification of MMC-HVDC transmission line faults based on one-terminal transient current signal," in *2017 IEEE Power & Energy Society General Meeting*, Chicago, IL, USA, 2017.

[8] S. Cui and S.-K. Sul, "A Comprehensive DC Short-Circuit Fault Ride Through Strategy of Hybrid Modular Multilevel Converters (MMCs) for Overhead Line Transmission," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7780 - 7796, Nov. 2016.

[9] J. Hu, K. Xu, L. Lin and R. Zeng, "Analysis and enhanced control of hybrid- MMC-based HVDC systems during asymmetrical DC voltage faults," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1394-1403, June 2017.

[10] T. Jonsson, P. Maiti and Y. Jiang-Häfner, "Converter technologies and functional requirements for reliable and economical HVDC grid design," in *CIGRE Canada*, Calgary, 2013.

[11] M. Hajian, L. Zhang and D. Jovcic, "DC transmission grid with low-speed protection using mechanical DC circuit breakers," *IEEE Transactions in Power Delivery*, vol. 30, no. 3, pp. 1383-1391, 2015.

[12] Z. He, J. Hu, L. Lin and R. Zeng, "Mechanical DC circuit breakers and FBSM-based MMCs in a high-voltage MTDC network: Coordinated operation for network riding through dc fault," in *International Conference on Renewable Power Generation (RPG 2015)*, Beijing, 17-18 Oct. 2015.

[13] M. Stumpe, P. Tünnerhoff, J. Dave, A. Schnettler, D. Ergin, A. Schön, K. Würflinger and F. Schettler, "DC fault protection for modular multi-level converter-based HVDC multi-terminal systems with solid state circuit breakers," *IET Generation, Transmission and Distribution*, vol. 12, no. 12, pp. 3013-3020, May 2018.

[14] A. Mokhberdoran, A. Carvalhoa, N. Silva, H. Leite and A. Carrapatoso, "Design and implementation of fast current releasing DC circuit breaker," *Electric Power Systems Research*, vol. 151, pp. 218-232, October 2017.

[15] C. Meyer and R. D. Doncker, "LCC analysis of different resonant circuits and solid-state circuit breakers for medium-voltage grids," *IEEE Transactions on Power Delivery*, vol. 21, no. 6, pp. 1414-1420, July 2006.

[16] S. Wang, C. Li, O. D. Adeuyi, G. Li, C. E. Ugalde-Loo and J. Liang, "Coordination of MMCs With Hybrid DC Circuit Breakers for HVDC Grid Protection," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 11-22, Feb. 2019.

[17] S.-M. Song, J.-Y. Kim, S.-S. Choi, I.-D. Kim and S.-K. Choi, "New Simple-Structured AC Solid-State Circuit Breaker," *IEEE Transactions of Industrial Electronics,* vol. 65, no. 11, pp. 8455 - 8463, Nov. 2018.

[18] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A Review," *IEEE Transactions on Power Delivery,* vol. 30, no. 1, pp. 37-53, Jan. 2015.

[19] A. Antonopoulos, L. Angquist and H.-P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," in *2009 13th European Conference on Power Electronics and Applications,* Barcelona, Spain, 8-10 Sep 2009.

[20] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 30, no. 1, pp. 4-7, Jan. 2015.

[21] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou and R. P. Aguilera, "Modular Multilevel Converters: Recent Achievements and Challenges," *IEEE Open Journal of the Industrial Electronics Society,* vol. 2, pp. 224 - 239, 2021.

[22] J. V. M. Farias, A. F. Cupertino, H. A. Pereira and S. I. Seleme, "On Converter Fault Tolerance in MMC-HVDC Systems: A Comprehensive Survey," *IEEE Journal of Emerging and Selected Topics in Power Electronics* , vol. 9, no. 6, pp. 7459-7470, 2021.

[23] M. N. Sakib, S. P. Azad and M. Kazerani, "A Review of DC Fault Blocking Converters for HVDC Transmission Systems," in *CIGRE Canada Conference,* Toronto, Oct. 2020.

[24] Y. Wan, M. Mao, L. Zhou, X. Xi, B. Xie and S. Zhou, "Review on topology-based dc short-circuit fault ride-through strategies for MMC-based HVDC system," *IET Power Electronics,* vol. 13, pp. 203-220, 2020.

[25] T. H. Nguyen, K. A. Hosani, M. S. E. Moursi and F. Blaabjerg, "An Overview of Modular Multilevel Converters in HVDC Transmission Systems With STATCOM Operation During Pole-to-Pole DC Short Circuits," *IEEE Transactions on Power Electronics,* vol. 34, no. 5, pp. 4137 - 4160, May 2019.

[26] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga and R. Teodorescu, Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems, Wiley-IEEE Press, 2016.

[27] N. Thitichaiworakorn, M. Hagiwara and H. Akagi, "Experimental verification of a modular multilevel cascade inverter based on double-star bridge-cells (MMCI-DSBC)," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, USA, Sept. 2012.

[28] Q. Song, W. Yang, B. Zhao, S. Xu, H. Rao and Z. Zhu, "Energy Storage Requirement Reduction Using Negative-Voltage States of a Full-Bridge Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, p. June 2019, 5243-5255.

[29] K. Wang, Q. Song and Xu, "Analysis and Design of the Energy Storage Requirement of Hybrid Modular Multilevel Converters Using Numerical Integration and Iterative Solution," *Energies*, no. 19, 2022.

[30] S. Du, A. Dekka, B. Wu and N. Zargari, Modular Multilevel Converters: Analysis, Control and Applications, Wiley, 2018.

[31] M. Hagiwara and H. Akagi:, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737 - 1746, July 2009.

[32] M. Durrant, H. Werner and K. Abbott, "Model of a VSC HVDC terminal attached to a weak AC system," in *Proceedings of 2003 IEEE Conference on Control Applications, 2003. CCA 2003.*, Istanbul, 25-25 June 2003.

[33] A. Farag, M. Durrant, H. Werner and K. Abbott, "Robust control of a VSC HVDC terminal attached to a weak AC system," in *Proceedings of 2003 IEEE Conference on Control Applications, 2003. CCA 2003.*, Istanbul, 2003.

[34] M. Durrant, H. H. Werner and K. Abbott, "Modelling and controller design for VSC-HVDC attached to an AC network," in *European Control Conference (ECC)*, Cambridge, Sep. 2003.

[35] P. M. Meshram and V. B. Borghate, "A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC)," *IEEE Transactions on Power Electronics,* vol. 30, no. 1, pp. 450-462, Jan. 2015.

[36] P. Hu and D. Jiang, "A Level-Increased Nearest Level Modulation Method for Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 30, no. 4, pp. 1836-1842, Apr. 2015.

[37] B. McGrath and D. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics,* vol. 49, no. 4, pp. 858-867, Aug. 2002.

[38] M. Huang, J. Zou and X. Ma, "An Improved Phase-Shifted Carrier Modulation for Modular Multilevel Converter to Suppress the Influence of Fluctuation of Capacitor Voltage," *IEEE Transactions on Power Electronics,* vol. 31, no. 10, pp. 7404 - 7416, Oct. 2016.

[39] G. S. Konstantinou, M. Ciobotaru and V. G. Agelidis, "Analysis of multi-carrier PWM methods for back-to-back HVDC systems based on modular multilevel converters," in *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*, Melbourne, 7-10 Nov. 2011 .

[40] B. Li, R. Yang, D. Xu, G. Wang, W. Wang and D. Xu, "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 30, no. 1, pp. 297 - 310, Jan. 2015.

[41] R. L. F., M. A. Pérez and J. Rodríguez, "DC voltage balance control in a modular multilevel cascaded converter," in *IEEE International Symposium on Industrial Electronics (ISIE)*, Hangzhou, China, 28-31 May 2012.

[42] X. Li, J. Li and W. Liu, "Capacitor voltage balancing control based on CPS-PWM of Modular Multilevel Converter," in *2011 IEEE Energy Conversion Congress and Exposition, ECCE*, Phoenix, 17-22 Sept. 2011.

[43] S. Du, J. Liu and T. Liu, "Modulation and Closed-Loop-Based DC Capacitor Voltage Control for MMC With Fundamental Switching Frequency," *IEEE Transactions on Power Electronics,* vol. 30, no. 1, pp. 327 - 338, Jan. 2015.

[44] G. P. Adam and I. E. Davidson, "Robust and Generic Control of Full-Bridge Modular Multilevel Converter High-Voltage DC Transmission Systems," *IEEE Transactions on Power Delivery,* vol. 30, no. 6, pp. 2468 - 2476, Dec 2015.

[45] B. Li, J. He, J. Tian, Y. Feng and Y. Dong, "DC fault analysis for modular multilevel converter-based system," *Journal of Modern Power Systems and Clean Energy,* vol. 5, no. 2, p. 275–282, 2017.

[46] Y. Wang, Z. Yuan, J. Fu, Y. Li and Y. Zhao, "A feasible coordination protection strategy for MMC-MTDC systems under DC faults," *International Journal of Electrical Power & Energy Systems,* vol. 90, pp. 103-111, Sep. 2017.

[47] G. Zhang, Y. Chen, C. Yue, L. Qi and J. Pan, "DC pole-to-pole short-circuit behavior analysis of modular multilevel converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, USA, 14-18 Sept. 2014.

[48] Z. Xu, H. Xiao, L. Xiao and Z. Zhang, "DC Fault Analysis and Clearance Solutions of MMC-HVDC Systems," *Energies,* vol. 11, no. 4, p. 941, Apr. 2018.

[49] Y. Wang, B. Yang, H. Zuo, H. Liu and H. Yan, "A DC short-circuit fault ride through strategy of MMC-HVDC based on the cascaded star converter," *Energies,* vol. 11, no. 8, p. 2079, Aug. 2018. .

[50] J. Yang, J. E. Fletcher and J. O'Reilly, "Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables," *IEEE Transactions on Industrial Electronics,* vol. 59, no. 10, pp. 3827 - 3837, Oct. 2012.

[51] G. Zhang, Y. Chen, C. Yue, L. Qi and J. Pan, "DC pole-to-pole short-circuit behavior analysis of modular multilevel converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, USA, 14-18 Sept. 2014.

[52] H. Zhang, L. Luo, L. Jia, L. Yang and S. Yang, "An Improved Sub-Module Topology for Protecting MMC Power Devices under DC-side Short Circuit Fault," in *2018 Chinese Control And Decision Conference (CCDC)*, Shenyang, China, 9-11 June 2018.

[53] K. Friedrich, "Modern HVDC PLUS application of VSC in Modular Multilevel Converter topology," in *2010 IEEE International Symposium on Industrial Electronics*, Bari, Italy, 4-7 July 2010.

[54] X. Li, Q. Song, W. Liu, H. Rao, S. Xu and L. Li, "Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 1, pp. 483-490, Jan. 2013.

[55] J. Qin, M. Saeedifard, A. Rockhill and R. Zhou, "Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385 - 394, Feb. 2015.

[56] K. H. Ahmed, G. P. Adam, I. A. Abdelsalam and A. A. Aboushady, "Modular multilevel converter with modified half-bridge submodule and arm filter for dc transmission systems with dc fault blocking capability," *IET Power Electronics*, vol. 11, no. 14, pp. 2253-2262, 2018.

[57] X. Li, W. Liu, Q. Song, H. Rao and S. Xu, "An enhanced MMC topology with DC fault ride-through capability," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria, 10-13 Nov. 2013.

[58] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, Sapporo, Japan, 21-24 June 2010.

[59] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga and H.-P. Nee, "Semi-full-bridge submodule for modular multilevel converters," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Seoul, Korea (South), 1-5 June 2015.

[60] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," *IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2903-2912, Oct.*, vol. 25, no. 4, pp. 2903-2912, Oct. 2010.

[61] X. Hu, J. Zhang, S. Xu and Y. Jiang, "Investigation of a new modular multilevel converter with DC fault blocking capability," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 1-5 Oct. 2017.

[62] R. Li, J. E. Fletcher, L. Xu, D. Holliday and B. W. Williams, "A Hybrid Modular Multilevel Converter With Novel Three-Level Cells for DC Fault Blocking Capability," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 2017 - 2026, Aug. 2015.

[63] A. Nami, L. Wang, F. Dijkhuizen and A. Shukla, "Five level cross connected cell for cascaded converters," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, France, 2-6 Sept. 2013.

[64] J. Zhang and C. Zhao, "The Research of SM Topology With DC Fault Tolerance in MMC-HVDC," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1561 - 1568, Jun. 2015.

[65] G. Adam, K. Ahmed and B. Williams, "Mixed cells modular multilevel converter," in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, Istanbul, Turkey, 1-4 June 2014.

[66] R. Zeng, L. Xu and L. Yao, "An improved modular multilevel converter with DC fault blocking capability," in *2014 IEEE PES General Meeting | Conference & Exposition*, National Harbor, MD, USA, 27-31 July 2014.

[67] J. Zhang, C. Jiang and Y. Han, "Modular multilevel converter composite submodule topology and control," *Journal of Engineering*, vol. 2019, no. 16, pp. 2643-2648, 2019.

[68] A. A. Elserougi, A. M. Massoud and S. Ahmed, "A Switched-Capacitor Submodule for Modular Multilevel HVDC Converters With DC-Fault Blocking Capability and a Reduced Number of Sensors," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 313 - 322, Feb. 2016.

[69] Y. Yao, Y. Zhang, X. Qu and W. Chen, "A Modular Multilevel Converter With Novel Double Reverse Blocking Sub-Modules for DC Fault Current Blocking Capability," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 4, pp. 740 - 744, Apr. 2020.

[70] A. Nami, J. Liang, F. Dijkhuizen and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18-36, Jan. 2015.

[71] X. Fang, C. Chen, Z. Wang, J. Xiong and K. Zhang, "An Improved Modular Multilevel Converter With DC Fault Blocking Capability Based on Half-Bridge Submodules and H-Bridge Circuit," *IEEE Transactions on Power Delivery*, vol. 35, no. 6, pp. 2682 - 2691, 2020.

[72] M. Merlin, T. Green, P. Mitcheson, D. Trainer, D. Critchley and R. Crookes, "A new hybrid multi-level Voltage-Source Converter with DC fault blocking capability," in *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, London, 19-21 Oct. 2010.

[73] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes and F. Hassan, "The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310 - 317, Feb. 2014.

[74] M. M. C. Merlin, P. D. Judge, T. C. Green, P. D. Mitcheson, F. Moreno and K. Dyke, "Alternate arm converter operation of the modular multilevel converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, USA, , 14-18 Sept. 2014.

[75] G. P. Adam, S. J. Finney and B. W. Williams, "Hybrid converter with ac side cascaded H-bridge cells against H-bridge alternative arm modular multilevel converter: steady-state and dynamic performance," *IET Generation, Transmission and Distribution*, vol. 7, no. 3, pp. 318-328, 2013.

[76] H. R. Wickramasinghe, G. Konstantinou and J. Pou, "Gradient-Based Energy Balancing and Current Control for Alternate Arm Converters," *IEEE Transactions on Power Delivery*, vol. 34, no. 4, pp. 1459 - 1468, Jun 2018.

[77] H. R. Wickramasinghe, G. Konstantinou, S. Ceballos and J. Pou, "Alternate Arm Converter Energy Balancing Under Parameter Variation," *IEEE Transactions on Power Electronics*, vol. 3, pp. 2996 - 3000, Apr. 2019.

[78] H. R. Wickramasinghe, G. Konstantinou and J. Pou, "Energy Balancing of the Alternate Arm Converter Under Parameter Variations," in *2018 IEEE 27th International Symposium on Industrial Electronics (ISIE)*, Cairns, QLD, Australia, 13-15 June 2018.

[79] M. M. C. Merlin, D. Soto-Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, D. R. Trainer and K. J. Dyke, "The Extended Overlap Alternate Arm Converter: A Voltage-Source Converter With DC Fault Ride-Through Capability and a Compact Design," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 3898 - 3910, May 2018.

[80] P. Vermeersch, F. Gruson, M. M. C. Merlin, X. Guillaud and P. Egrot, "A Stored Energy Control Based Active DC Filter for the Alternate Arm Converter with an Extended Overlap Period," in *21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Genova, Italy, 2019.

[81] S. Liu, M. Saeedifard and X. Wang, "Zero-Current Switching Control of the Alternate Arm HVdc Converter Station With an Extended Overlap Period," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2355 - 2365, Mar. 2019.

[82] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, F. J. Moreno and K. J. Dyke, "Cell capacitor sizing in modular multilevel converters and hybrid topologies," in *2014 16th European Conference on Power Electronics and Applications*, Lappeenranta, Finland, 2014.

[83] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electronics*, vol. 8, no. 3, pp. 350-360, March, 2015.

[84] G. Adam, S. Finney, B. Williams, D. Trainer, C. Oates and D. Critchley, "Network fault tolerant voltage-source-converters for high-voltage applications," in *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, London, UK, 19-21 Oct. 2010.

[85] Y. Xue, Z. Xu and Q. Tu, "Modulation and Control for a New Hybrid Cascaded Multilevel Converter With DC Blocking Capability," *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 2227-2237, Oct. 2012.

[86] X. Shi, S. Filizadeh and D. A. Jacobson, "Loss Evaluation for the Hybrid Cascaded MMC Under Different Voltage-Regulation Methods," *IEEE Transactions on Energy Conversion*, vol. 33, no. 3, pp. 1487-1498, Sep. 2018.

[87] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher and B. W. Williams, "Hybrid Cascaded Modular Multilevel Converter With DC Fault Ride-Through Capability for the HVDC Transmission System," *IEEE Transactions on Power Delivery,* vol. 30, no. 4, pp. 1853 - 1862, Aug. 2015.

[88] M. B. Ghat, A. Shukla and R. Mishra, "Variable Slope Trapezoidal Reference Signal Based Control for a DC Fault Tolerant Hybrid Modular Multilevel Converter With Cascaded Full Bridges," *IEEE Transactions on Industry Applications,* vol. 53, no. 4, pp. 3770 - 3781, Jul-Aug. 2017.

[89] M. B. Ghat and A. Shukla, "A New H-Bridge Hybrid Modular Converter (HBHMC) for HVDC Application: Operating Modes, Control, and Voltage Balancing," *IEEE Transactions on Power Electronics,* vol. 33, no. 8, pp. 6537 - 6554, Aug. 2018.

[90] D. Trainer, C. Davidson, C. Oates, N. Macleod, D. Critchley and R. Crookes, "A New Hybrid Voltage-Sourced Converter for HVDC Power Transmission," in *2010 CIGRE Paris*, Paris, 2010.

[91] G. P. Adam and B. W. Williams, "New emerging voltage source converter for high-voltage application: hybrid multilevel converter with dc side H-bridge chain links," *IET Generation, Transmission and Distribution,* vol. 8, no. 4, pp. 765-773, 2014.

[92] G. Adam, K. Ahmed and B. Williams, "Hybrid multilevel converter with dc side H-bridge chain links," in *2013 International Conference on Renewable Energy Research and Applications (ICRERA)*, Madrid, 20-23 Oct. 2013.

[93] G. Adam, I. A. Abdelsalam, K. Ahmed and B. Williams, "Hybrid Multilevel Converter With Cascaded H-bridge Cells for HVDC Applications: Operating Principle and Scalability," *IEEE Transactions on Power Electronics,* vol. 30, no. 1, pp. 65-77, Jan. 2015.

[94] Q. Hao, B.-T. Ooi, F. Gao, C. Wang and N. Li, "Three-Phase Series-Connected Modular Multilevel Converter for HVDC Application," *IEEE Transactions on Power Delivery,* vol. 31, no. 1, pp. 50-58, Feb. 2016.

[95] M. B. Ghat and A. Shukla, "Series-Stacked Hybrid Modular Converter with DC Fault Blocking Capability for HVDC Application," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 23-27 Sept. 2018.

[96] S. Cui, S. Kim, J.-J. Jung and S.-K. Sul, "Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, USA, 16-20 March 2014.

[97] E. Kontos, G. Tsolaridis, R. Teodorescu and P. Bauer, "Full-bridge MMC DC fault ride-through and STATCOM operation in multi-terminal HVDC grids," *Bulletin of the Polish Academy of Sciences: Technical Sciences*, vol. 65, no. 5, pp. 653-662, Oct. 2017.

[98] X. Yu, Y. Wei, Q. Jiang, X. Xie, Y. Liu and K. Wang, "A Novel Hybrid-Arm Bipolar MMC Topology With DC Fault Ride-Through Capability," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1404 - 1413, Jun. 2017.

[99] R. Feldman, A. J. Watson, J. C. Clare, P. W. Wheeler, D. R. Trainer and R. W. Crookes, "DC fault ride-through capability and statcom operation of a hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation," in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, Bristol, UK, 27-29 March 2012.

[100] X. Yu, Y. Wei and Q. Jiang, "STATCOM Operation Scheme of the CDSM-MMC During a Pole-to-Pole DC Fault," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1150 - 1159, Jun. 2016.

[101] K. A. Hosani, T. H. Nguyen and N. A. Sayari, "Fault-tolerant control of MMCs based on SCDSMs in HVDC systems during DC-cable short circuits," *International Journal of Electrical Power & Energy Systems*, vol. 100, pp. 379-390, Sep. 2018.

[102] J.-J. Jung, S. Cui, S. Kim and S.-K. SuI, "A cell capacitor energy balancing control of Modular Multilevel Converter considering the unbalanced AC grid conditions," in *2014 International*

Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), Hiroshima, Japan, 18-21 May 2014.

[103] S. Samimi, F. Gruson, X. Guillaud and P. Delarue, "Control of DC bus voltage with a Modular Multilevel Converter," in *2015 IEEE Eindhoven PowerTech*, Eindhoven, Netherlands, 29 June-2 July 2015.

[104] S. Samimi, F. Gruson, P. Delarue and X. Guillaud, "Synthesis of different types of energy based controllers for a Modular Multilevel Converter integrated in an HVDC link," in *11th IET International Conference on AC and DC Power Transmission*, Birmingham, UK, 10-12 Feb. 2015.

[105] E. Shahriari, F. Gruson, P. Vermeersch, P. Delarue, F. Colas and X. Guillaud, "A Novel DC Fault Ride Through Control Methodology for Hybrid Modular Multilevel Converters in HVDC Systems," *IEEE Transactions on Power Delivery*, vol. 35, no. 6, pp. 2831 - 2840, Dec. 2020.

[106] X. Li, B. Zhao, Y. Wei, X. Xie, Y. Hu and D. Shu, "DC fault current limiting effect of MMC submodule capacitors," *International Journal of Electrical Power & Energy Systems*, vol. 115, 2020.

[107] X. Li, Z. Li, B. Zhao, C. Lu, Q. Song, Y. Zhou, H. Rao, S. Xu and Z. Zhu, "HVdc Reactor Reduction Method Based on Virtual Reactor Fault Current Limiting Control of MMC," *IEEE Transactions on Industrial Electronics,*, vol. 67, no. 12, pp. 9991-10000, Dec. 2020.

[108] E. Kontos, G. Tsolaridis, R. Teodorescu and P. Bauer, "On DC Fault Dynamics of MMC-Based HVdc Connections," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 497-507, Feb. 2018.

[109] O. Cwikowski, H. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes and R. Shuttleworth, "Modular Multilevel Converter DC Fault Protection," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 291-300, Feb. 2018.

[110] "Guide for the Development of Models for HVDC Converters in a HVDC Grid," B4.57 CIGRE Brochure 604 (Working group), Dec 2014.

[111] S. Gao, H. Ye and Y. Liu, "Accurate and Efficient Estimation of Short-Circuit Current for MTDC Grids Considering MMC Control," *IEEE Transactions on Power Delivery,* vol. 35, no. 3, pp. 1541-1552, Jun. 2020.

[112] "Online: https://library.abb.com/d/5SYA1450," ABB.