FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING
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MASTER'S THESIS

FIBER WEAVE SKEW AND COPPER ROUGHNESS - EFFECTS ON TRANSMISSION LINE PERFORMANCE ON PCB

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Osmo Kitunen (2022) Fiber weave skew and copper roughness - effects on transmission line performance on PCB
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ABSTRACT

Designing manufacturable high performing transmission lines is an essential part of modern electronics design work. This thesis focuses on interconnect design and simulation while also examining how materials and manufacturing affects the designed interconnect. The goal of this work is to find how big and what kind of effects different design and manufacturing variables have and how to be mindful of all the relevant factors during the design phase. Specific focus areas are fiber weave effect and losses caused by copper roughness. In this thesis theory behind transmission lines on PCB is outlined first along with different material properties and relevant material test methods. Effects of different design parameters and material properties are then examined through simulations and literature.

Accurate simulation of fiber weave skew with readily available simulation tools is difficult, but fiber weave skew itself can be mitigated with design choices. Copper roughness can be modelled with various models. Multiple different ways to represent copper roughness in the scope of PCB design exist. These various roughness representations are examined extensively through examples. Copper roughness was found to have significant effects on signal integrity and different roughness models were found to perform very differently.

Keywords: signal integrity, impedance, etch factor, skin effect, dielectric constant, dissipation factor.

Osmo Kitunen (2022) Lasipunosajoitusvääristymän ja kuparin karkeuden vaikutukset siirtolinjojen suorituskykyyn piirilevyllä
Oulun yliopisto, tieto- ja sähkötekniikan tiedekunta, elektroniikan ja tietoliikennetekniikan tutkinto-ohjelma. Diplomityö 68 s

TIIVISTELMÄ

Modernin elektroniikkasuunnittelun yksi keskeisistä osista on massatuotantokelpoisten korkean suorituskyvyn, siirtolinjojen suunnittelu. Tämä diplomityö keskittyy yhteyssuunnitteluun ja siirtolinjarakenteiden simulointiin piirilevyllä. Valmistusprosessien ja materiaalien vaikutuksia siirtolinjoihin tarkastellaan myös. Työn tavoitteena on selvittää kuinka paljon ja millaisia vaikutuksia eri suunnittelu- ja materiaalivalinnoilla on sekä miten suunnittelija voi parhaiten ottaa eri seikat huomioon suunnittelun eri vaiheissa. Tarkemmin tarkasteltavat ilmiöt ovat kuparin pinnan karkeuden aiheuttamat häviöt ja piirilevyn eristemateriaalin lasikuitupunosrakenteen aiheuttama ajoitusvääristymä. Teoria piirilevyllä oleville siirtolinjoille on esitelty erilaisten materiaaliominaisuuksien ja materiaalien testausmenetelmien ohella ensin. Teoriaosuuden jälkeen eri suunnitteluparametrien ja materiaaliominaisuuksien vaikutuksia tutkitaan simulaatioiden ja kirjallisuuden pohjalta.

Lasipunosajoitusvääristymän simulointi helposti saatavilla olevilla simulointityökaluilla on haasteellista, mutta ilmiön aiheuttamia vaikutuksia on mahdollista pienentää erilaisilla suunnitteluratkaisuilla. Kuparin karkeuden mallintamiseen on tarjolla useita erilaisia simulointimalleja. Lisäksi kuparin karkeus voidaan esittää usealla eri tavalla. Erilaisia kuparin karkeuden esitystapoja piirilevykontekstissa on tarkasteltu kattavasti esimerkkien kautta. Kuparin karkeuden todettiin vaikuttavan signaalien vaimentumiseen merkittävästi ja eri karkeusmallien huomattiin palauttavan huomattavasti toisistaan poikkeavia tuloksia.

Avainsanat: signaalin eheys, impedanssi, etsauskerroin, skin-efekti, eristevakio, häviökerroin.

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FOREWORD

For my thesis work I wanted to make sure that the subject is genuinely interesting to me and also that the outcomes of the work are useful. I am convinced that this thesis has met both of those requirements. Working on this thesis has been a blast and a great learning experience. Initially I thought that I knew something about printed circuit boards, but it quickly turned out that my initial knowledge was greatly limited. At the beginning of this thesis work learning about all the various factors that need to be considered when designing a high-speed digital PCB felt overwhelming. Judy Warner, as the host of Altium OnTrack podcast said something along the lines: *"it is like drinking from a fire hose"* when she was discussing PCB materials with the Technical Marketing Manager at Rogers Corp, John Coonrod. That quote summarizes quite accurately how I felt when I tried to wrap my head around the subject of this thesis. However, as I delved deeper into the details, things started to make more and more sense and eventually I understood the big picture well enough that I could start compiling this thesis.

I would like to express my gratitude to everyone involved in the subject brainstorming phase and to everyone who shared their knowledge along the way and helped me to put this thesis together. Special thanks to my line manager Markus and to my technical Advisor Pekka, for supporting this work and sharing their ideas and expertise. I would also like to thank Nokia for offering me this thesis work opportunity.

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Osmo Kitunen

LIST OF ABBREVIATIONS AND SYMBOLS

5G	Fifth generation (mobile network)
BGA	Ball Grid Array - Surface mount component package type
BW	Bandwidth
CTE	Coefficient of thermal expansion
DC	Direct Current
Df	Dissipation factor
DIN	Deutsches Institut für Normung - German standardization organization
Dk	Relative dielectric constant
ED copper	Electro-Deposited copper
EM	Electromagnetic
EMI	Electromagnetic interference
ENIG	Electronless nickel immersion gold - surface finish for exposed conductors on a PCB
FEXT	Far-end crosstalk
FR-4	Common name for woven glass-reinforced epoxy PCB laminates. FR stands for "Flame retardant".
FWE	Fiber weave effect - same as glass weave effect
FWS	Fiber weave skew
GBd	Giga Baud - unit for signaling speed
GIGO	Garbage in Garbage out
GWE	Glass weave effect - same as fiber weave effect
GWS	Glass weave skew
HASL	Hot sir solder leveling - surface finish for exposed conductors on a PCB
IPC	Standardization organization specializing to standardizing printed circuit board design and manufacturing
ISI	Inter-symbol interference
JIS	Japanese Industrial Standards
NRZ	Non-return-to-zero - modulation for serial signaling one bit per unit interval
NEXT	Near-end crosstalk
PAM4	Pulse amplitude modulation 4-level - modulation for serial signaling two bits encoded to one UI
PCB	Printed circuit board
PI	Power Integrity

RA copper	Rolled-annealed copper
Ra	Roughness Average - surface roughness parameter
Rq	Same as Root Mean Square Roughness Average - surface roughness parameter
RMS	Root Mean Square
Rrms	Root Mean Square Roughness Average - surface roughness parameter
RTF	Reverse Treat Foil
Rz	Maximum height of the profile - surface roughness parameter with varying definitions
SI	Signal Integrity
UI	Unit Interval - Single symbol duration in serial communication
via	Plated structure connecting PCB layers together, not intended to be used as component mounting hole. [1]
VLP	Very Low Profile - surface finish name for copper foil.
ft	feet - imperial unit for length equal to 0.3048 meters
Oz	ounce - imperial unit for weight equal to 28.34 grams
C	symbol for capacitance
C_{mL}	mutual capacitance per unit length
C_L	capacitance per unit length of the signal trace
c	speed of light, 299 792 458 m/s
D1	dielectric thickness between transmission line and it's (top) reference plane
D2	dielectric thickness between transmission line and it's (bottom) reference plane
D3	distance between differential transmission lines. Edge-to-edge spacing
F	farad, unit for capacitance
f	symbol for frequency
f_{knee}	knee frequency, most of digital signal's spectral content of is below knee frequency
H	henry, unit for inductance
L	symbol for inductance
L_L	inductance per unit length of the signal trace
L_{mL}	mutual inductance per unit length
R	symbol for resistance
T	transmission line thickness
T_d	time delay

t_r	t_{rise} - rise time
V_a	voltage of the signal line
V_f	voltage at the far end of the quiet line
V_b	backward direction voltage noise on the quiet line
v	symbol for (signal) speed
W1	transmission line width top side
W2	transmission line width bottom side
δ	skin depth not to be confused with loss angle
ε_r	same as Dk
ρ	symbol for resistivity
$tan(\delta)$	tan of loss angle, Same ass dissipation factor

1. INTRODUCTION

High-speed digital data transmission is core functionality of any modern telecommunication or computing device. Demand for faster data rates with as little added cost as possible is here to stay. The number of connected devices increases, processors become faster, and demand for high bitrate content streaming keeps growing. The aforementioned are just few factors driving the need for speed also under the hood of the technology that keeps the wheels of the modern world turning. Fifth generation (5G) mobile networks can offer up to 1 Gbps data rates for individual users [2]. While the massive data rates delivered by 5G network equipment require sophisticated radio hardware, high performance radio hardware is more or less useless if it is not backed up with equally performing hardware all the way to the core network. Not to mention data centers that serve massive amounts of content over the internet. High speed interconnects are everywhere.

Signals travel between and within systems on different kinds of interconnects such as cables and PCB (Printed Circuit Board) traces. Each of these interconnects is a transmission line. Transmission line is just a signal conductor and a return path. Both of which influence equally to the transmission line performance unless the interconnect is transparent. Interconnect is called transparent if it has no effect on signal quality. Low speed signals i.e., signals with long rise times or short enough interconnects lead to interconnects looking transparent to the signal [3]. Practical high-speed transmission lines on PCB are basically never transparent. There are numerous factors that influence the interconnect performance on PCB: Solder joints between components and PCB, shapes of the solder lands, holes (vias and trough hole pins), connectors, PCB dielectric materials, copper properties, interconnect geometry and layers adjacent to the interconnect as well as other nearby interconnects on the PCB. This thesis will focus on the effects caused by PCB material properties and explore some ways to maintain signal quality as good as possible. The specific focus areas are fiber weave skew and signal degradation caused by copper roughness. Fiber weave skew is caused by non-uniform nature of common PCB materials: Dielectric properties are not constant across the entire PCB, which causes signals to behave differently in different points on the PCB. Copper roughness on the other hand refers to μm-scale bumps in the copper surface. These small variations in the conductive surface attenuate signals, especially the high frequency components. The presented mitigation strategies will be supported by literature and simulations where possible.

Transmission lines can be either single-ended or differential. In the scope of high-speed digital most interconnects are differential hence differential pair transmission lines will be examined in this thesis. Differential pair transmission line is essentially just two single-ended transmission lines used to transport a differential signal. While differential signaling offers benefits over single-ended signaling there are also some tradeoffs. Benefits of differential signaling include improved resilience to common mode crosstalk and discontinuities, possibility to use longer rise time drivers and possibility to use higher gain at the receiver. The cost of mentioned benefits is need for more PCB surface area and added complexity. One differential signal requires two conductors and a return path while one single-ended signal only needs one signal and a re-

turn path. Differential transmission lines offer more variables that require designer's attention. While this gives room for more versatile design decisions it also adds to the complexity of the design. [4]

Successful interconnect design requires materials understanding, knowledge on how transmission lines behave and awareness on how signals behave while propagating in a transmission line. These topics are described in sufficient detail for the purposes of this thesis in chapters 2 and 3. Ways to counter the performance degrading material effects using the available design variables is discussed in chapter 4, where topics outlined in earlier chapters will be examined from a more practical point of view. Some topics this thesis tries to clarify are:

- Design parameters that are crucial for signal integrity simulations
- The best format to input data to simulators
- Practical signal integrity effects due to imperfections in the PCB manufacturing process
- Is it worthwhile to consider certain effects or will they be negligible in comparison to other factors
- Scales of different effects and relationships between them
- The combined effects of different signal quality degrading factors

Design tool manuals can be very ambiguous when it comes to explaining what different options and parameters actually do. Trying to find an answer that should read directly in the tool's manual from different documentation sources can be a real chore. Lack of quick and easy access to accurate information on what one should input to the simulator, what different simulation options do and when to use each option available in a software is a factor that can worsen the simulation result quality.

2. CHALLENGES OF HIGH-SPEED DIGITAL ON PCB

This chapter outlines the general design considerations that constrain a high-speed transmission line. Material considerations are discussed in chapter 3 right after this chapter. High-speed digital signals are wideband from Direct current (DC) to some frequency defined by the shortest rise (or fall) time present in the signal. The data rate of the signal does not determine the signal bandwidth, but high data rate signals need short rise and fall times as the bit durations are short. Signal bandwidth can be approximated with

$$BW = \frac{0.35}{t_{rise}} \tag{1}$$

where BW is signal bandwidth and t_{rise} is signal rise time [4]. If rise time is given in nanoseconds the bandwidth will be in gigahertz. Equation (1) does not approximate the full spectral content of a signal but is rather an assumption of the midpoint of the spectral content associated with the rise time. The upper frequency limit of a digital signal is described with knee frequency

$$f_{knee} = \frac{0.5}{t_{rise}} \tag{2}$$

where f_{knee} is the knee frequency and t_{rise} is once again the rise time [5]. The knee frequency is the frequency below which most of the spectral content of a digital signal is. The wideband nature of digital signals imposes constraints to transmission line design as real transmission lines function as low pass filters to some extent. Real world conductors attenuate all frequencies, but different phenomena attenuate high frequencies more than low frequencies thus essentially turning transmission line into a low pass filter.

Along with as low loss as possible, conductors used for high-speed digital signals need to have constant electrical properties all the way from the transmitter to the receiver. Changes in interconnect impedance cause reflections that degrade signal quality. Propagation delay differences between signal conductors cause timing problems and intra-pair skew in differential signals. [4] Intra-pair skew can start causing bit errors with short bit durations. Modern serial differential communication protocols have bit durations that are less than 100 ps, for such short bits intra pair skew tolerance is poor.

Fast signals require that signal voltage levels are kept as low as possible. The lower the logic 1 voltage is the smaller is the slew rate required to achieve certain rise time [3]. Slew rate describes how much driver output can change its voltage level in a time unit [6]. Low voltage levels make signals more susceptible for interference from the surrounding environment as relatively small, coupled voltages can be significant at the receiver when compared to the actual signal. Crosstalk i.e., the undesired coupling between neighboring traces should be kept as low as possible by simply leaving enough space between conductors that should not be coupled [1]. A run-through of factors affecting high-speed digital designs is presented in table 2.1.

Table 2.1 High-speed design considerations

Design parameter	Describes	Constant with frequency	Ideal value
Trace Impedance	In this document the time domain input impedance of a trace	Yes	Constant. Matched to driver's output impedance. Usually 50 Ω.
Dielectric losses	Signal losses caused in the dielectric material to the propagating electromagnetic (EM) wave	No	As low as possible
Conductor losses	Signal losses due to conductor resistance, skin effect and copper surface roughness	No	As low as possible
Skew	Timing difference between signals	No	As low as possible
Crosstalk	Unwanted energy transfer between adjacent conductors due to mutual inductance and capacitance [1]	No	As low as possible
Propagation speed	Signal speed (speed of light in the dielectric material) in a transmission line, determined by dielectric constant of the substrate material	No	Constant

2.1. Transmission line impedance

Transmission line impedance is one key consideration in interconnect design. Usually, the desired impedance is close to 50 Ω, but not necessarily exactly that. The required impedance is defined by the signaling protocol usually with allowable impedance tolerance around 10% [7–9]. Table 2.2 lists impedances used by different protocols also more specific impedance tolerances are available on the table apart from USB4. Lower impedance generally yields lower crosstalk while higher impedance requires larger termination resistances which dissipate less power [3].

Table 2.2 Impedances utilized by common differential signaling protocols. Single-ended or differential impedance listed based on what was available in specifications.

Protocol	Single-ended impedance	Differential impedance
PCIe Gen 3 and 4 [10, 11]	$42.5\,\Omega\ \pm 5\%$	$85\,\Omega \pm 5\%$
DDR2, DDR3, DDR4 [8]	$50-60\,\Omega \pm 10\%$	$100\,\Omega \pm 10\%$
USB2 [9]		$90\,\Omega \pm 15\%$
USB4 [12]	$42.5\,\Omega$	
Ethernet [7]	$50\,\Omega \pm 10\%$	$100\,\Omega \pm 10\%$

Transmission line impedance is not just one value. Impedance is different in time and frequency domains moreover the time domain impedance of a transmission line may not be constant. In the scope of high-speed digital the time domain impedance is of a bigger interest than the frequency domain impedance. Frequency domain transmission line impedance is the steady state input impedance including all reflections that happen in the transmission line and it is useful for RF considerations. In the time domain the more interesting impedance is the impedance seen by the signal as it propagates in the transmission line, this impedance is called the instantaneous impedance. In a uniform transmission line i.e., transmission line that is physically uniform throughout its entire length the instantaneous impedance is the characteristic impedance. For non-uniform transmission lines characteristic impedance cannot be defined as there is no single impedance that would characterize the entire transmission line. Non-uniform transmission lines need to be broken into uniform sections if there is need to describe them in terms of characteristic impedance. The input impedance of a uniform transmission line in the time domain is initially the characteristic impedance of the transmission line and the termination impedance in the steady state. If a step stimulus is launched into a uniform transmission line the input impedance stays constant until the signal has propagated all the way to the end of the transmission line and back. The signal that travels back to the source provides information on how the transmission line is terminated as a reflection. If the input impedance stays constant indefinitely the transmission line is either indefinitely long or perfectly terminated. [3]

Materials and transmission line geometry determine the characteristic impedance. Dimensions relevant to transmission line impedance have been annotated in figure 2.1 and explained in table 2.3. To keep transmission line uniform and its impedance constant all the listed parameters need to stay constant. The easiest and most reliable way to obtain the transmission line impedance from these parameters is to plug values into an EM field solver and let a computer program solve the impedance. Trace edges are drawn concave to visualize the actual trace edge on a finished PCB. Trace edges become slightly trapezoidal and concave. The origin of finished conductor shape is explained in chapter 3. This trapezoidal conductor shape is described with a parameter called etch factor, which can be approximated with

$$Etch\ Factor = \frac{W2 - W1}{T} \tag{3}$$

Where W1, W2 and T are as defined in figure 2.1. The difference between W1 and W2 is called etchback. The amount of etchback will vary per fabricator and copper thickness. [13]

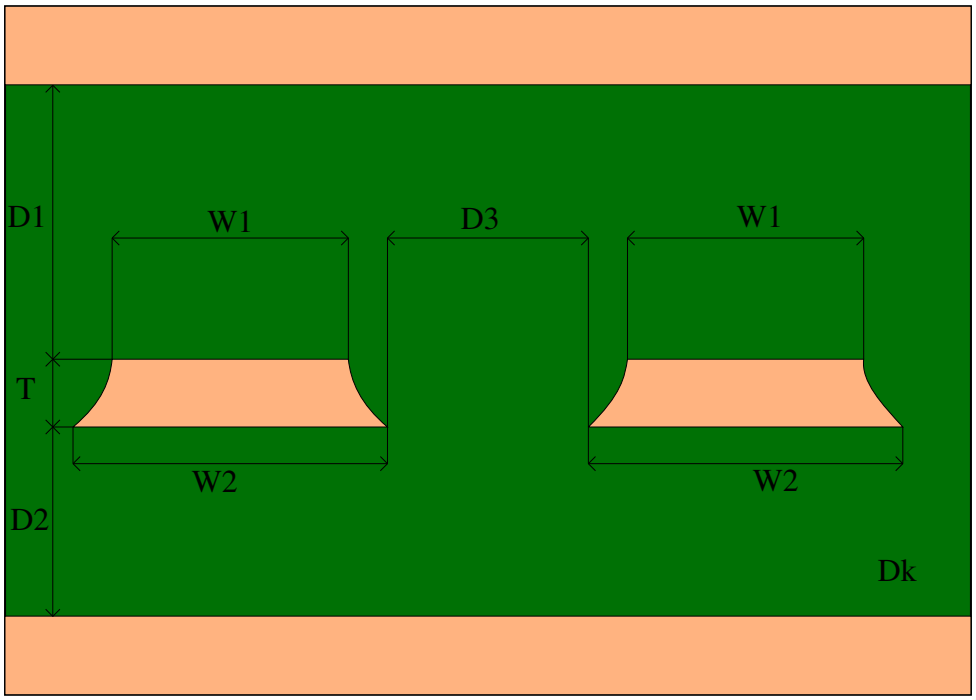


Figure 2.1. Dimensions affecting stripline trace impedance

Table 2.3 Symbols used in figure 2.1

Symbol	Description
D1	Distance between transmission line and reference plane in the case of a symmetrical stripline same as D2
D2	Distance between transmission line and reference plane in the case of a symmetrical stripline same as D1
D3	Distance between differential pair transmission lines, Edge-to-edge spacing. Can be used to adjust differential impedance.
W1	Transmission line width top side, one factor determining etch factor
W2	Transmission line width bottom side, one factor determining etch factor
T	Transmission line thickness, one factor determining etch factor
Dk	Relative permittivity of the dielectric material (green area) i.e., dielectric constant

Transmission line dimensions do not only affect the impedance of the transmission line but also have various effects. Distances to reference planes (D1 and D2) obviously affect the final PCB thickness. Additionally, as reference planes are brought closer to a trace the trace impedance will decrease as the coupling between the trace and its reference plane becomes stronger. To maintain the same trace impedance trace width needs to be shrunken assuming that dielectric material stays the same. Thinner traces take less physical space on the PCB but also are more lossy than wider traces. Differential impedance can be adjusted with trace edge-to-edge spacing D3, however edge-to-edge spacing only affects impedance if there is meaningful coupling between the traces. See figure 2.5.

Keeping transmission line's physical dimensions constant might seem like a trivial task. However, things get quickly complicated when routing a signal from a surface mounted device

to an internal signal layer and back to the surface of the PCB and to another device or possibly even a connector. How to keep impedance constant when changing PCB layers? Which layer should the signal be routed on to maximize performance and minimize via stubs (=unused remainders of a vias)? What needs to be considered when maneuvering transmission lines between other features on the PCB? How long trace can still work reliably for a certain signal? When it comes to bends and corners in the trace the most important thing is to keep the width of the trace constant by either chamfering corners or by using rounded corners/curved traces. With differential signals corners and bends result in length difference between the traces, which will cause skew that may need to be compensated. On the other hand, vias are a complicated matter by themselves. One particularly important thing to ensure smooth layer transitions using vias is to design current return paths the signal via is the solution as the via connected to reference planes will serve as current return path. Proper current return paths for layer changes also help to contain the electromagnetic interference (EMI) emissions of the board. Calculating via impedances is difficult and the best results are achieved using 3D EM field solver.

Discontinuities in current return path (e.g., gaps in reference plane, traces, component footprints, copper keep-outs around holes etc.) can cause impedance discontinuities. In case of a gap in a reference plane the reference plane effectively vanishes or jumps one layer further away, which will largely affect impedance. Figure 2.2 visualizes a differential stripline transmission line with a discontinuity in the reference plane. Return current will cross the gap by flowing somewhere else, which will spread out the EM field. Higher impedance section caused by the gap will also increase transmission line insertion loss and cause reflections. On high frequencies return currents travel as close to the signal conductor as possible due to skin effect. Effectively this means that return current flow on the reference plane(s) follows signal trace very closely. Skin effect is explored in further detail later in this chapter.

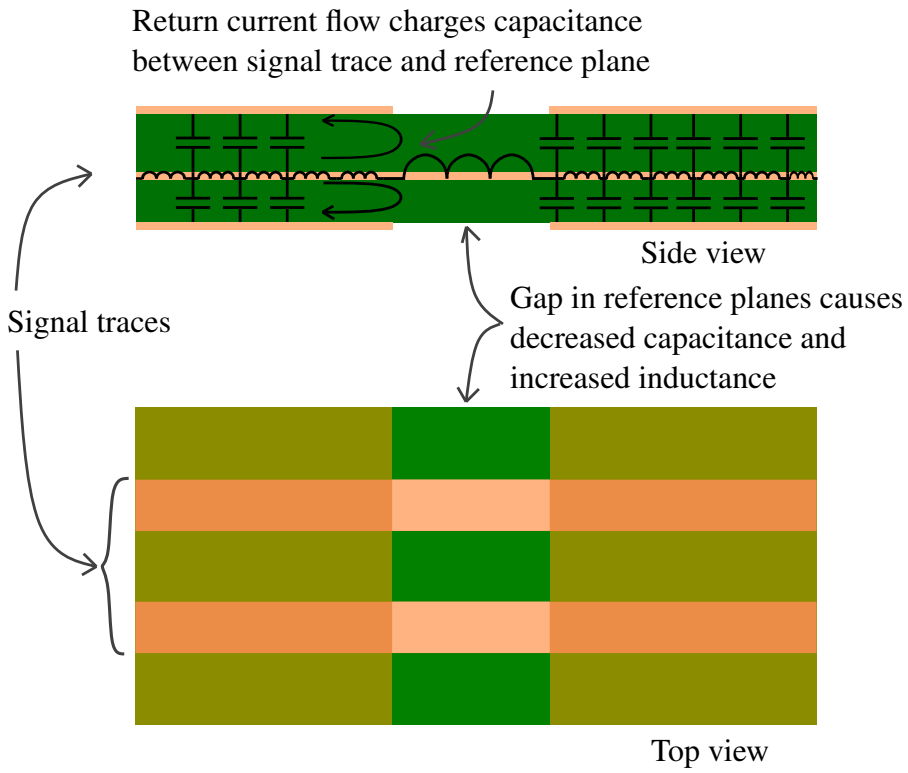
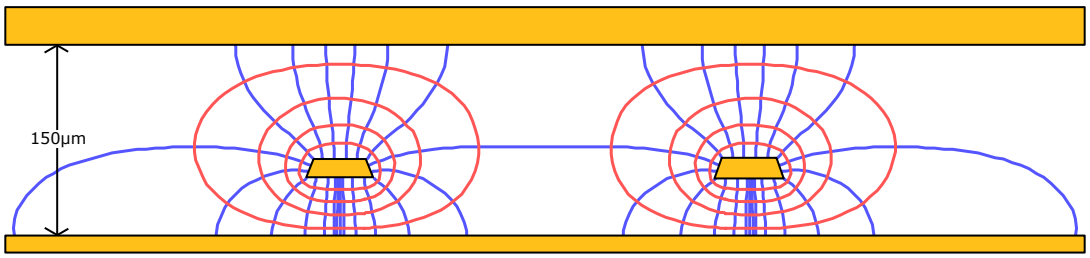


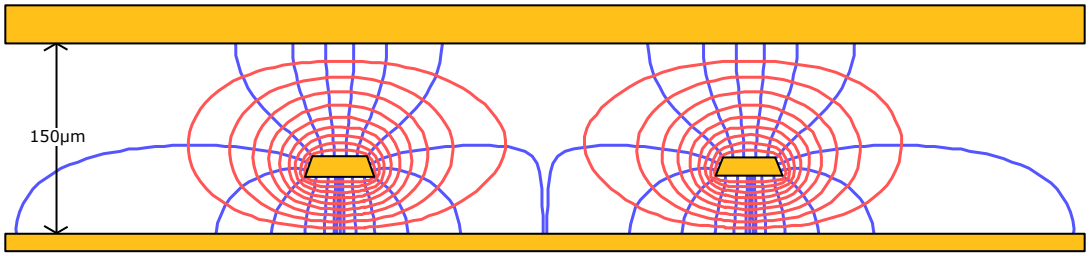
Figure 2.2. Reference planes needs to be present and continuous for a high-speed digital transmission line to work properly. This needs to be considered in the PCB layout phase.

For differential signals all factors mentioned above apply, however there are also other things to consider. Coupling between differential traces improves noise immunity and allows higher interconnect density on the PCB as traces are closer together. Increased coupling between two traces increases their mutual capacitance and inductance per length. Therefore, differential impedance of the interconnect decreases, which needs to be accounted for in the impedance planning design phase by either using narrower traces or by moving reference planes further away. If there is no coupling between two traces forming a differential pair the differential impedance will simply be two times the single-ended impedance. As the coupling between traces increases the differential impedance decreases, but single-ended impedance stays constant. This effectively means that common-mode signals and differential signals see different instantaneous impedances when propagating in the transmission line. Differential pair does not need to have any coupling between the traces, the only requirements are constant impedances and length matching to a degree determined by the bitrate of the signal [14]. [4]

In figures 2.3 and 2.4 electromagnetic fields in differential and common propagation modes are shown for two different asymmetrical stripline configurations consisting of two stripline transmission lines. Figures 2.3 (a) and 2.3 (b) show differential striplines with 50 Ω single-ended impedance and 100 Ω differential impedance and figures 2.4 (a) and 2.4 (b) show a differential transmission line with single-ended impedance around 66 Ω and differential impedance at 100 Ω. Magnetic fields are drawn in red and electric fields in blue. With reference planes further away the EM fields are spread more evenly to larger area, which means that the signal propagating in the transmission line couples more to nearby traces causing crosstalk.

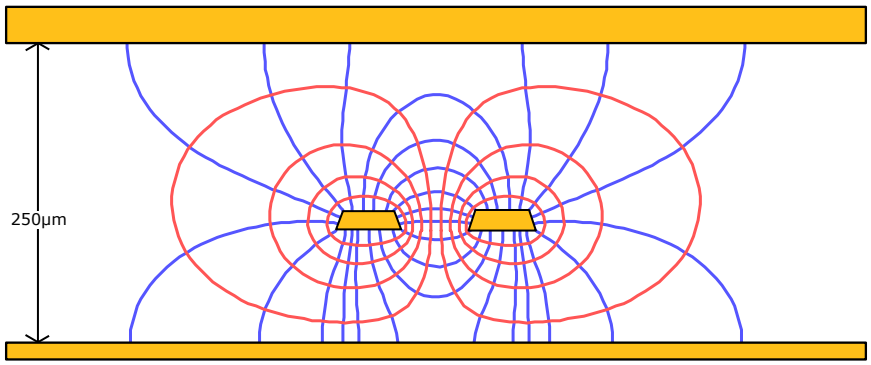


(a) Differential propagation.

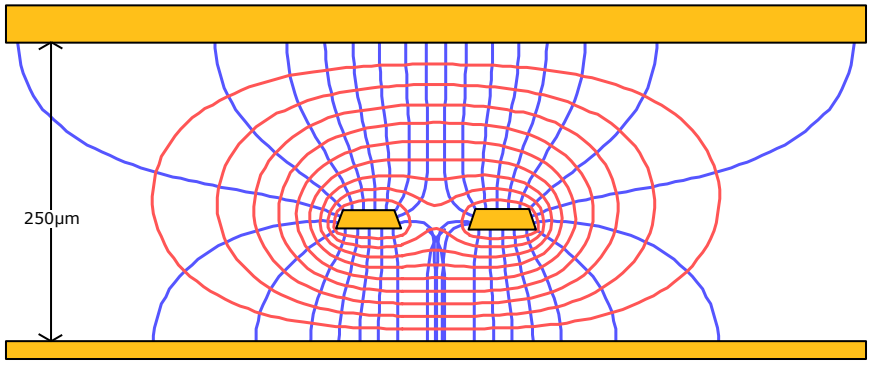


(b) Common mode propagation.

Figure 2.3. Reference planes close to traces, traces have strong coupling to reference planes. Wide trace edge to edge spacing to maintain 100 Ω differential impedance. Single-ended impedance 50 Ω.



(a) Differential propagation.



(b) Common mode propagation.

Figure 2.4. Reference planes far away, tight coupling between traces to maintain 100 Ω differential impedance and 66 Ω single-ended impedance.

Figure 2.5 visualizes the relationship of trace width and trace separation when aiming for certain differential impedance. The green curve plots all differential pair dimensions that result in a certain differential impedance with certain dielectric thicknesses. The actual numerical values for trace widths and separation depend on factors discussed above. Figure 2.5 aims only to show how differential impedance is affected by these two factors together.

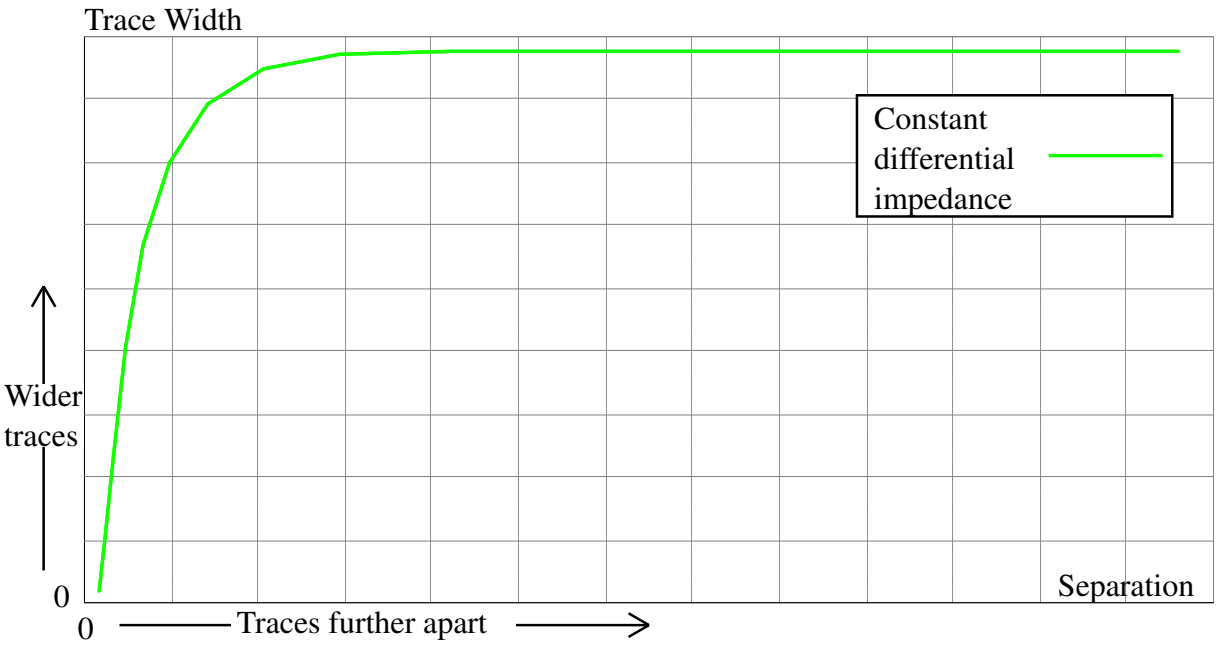
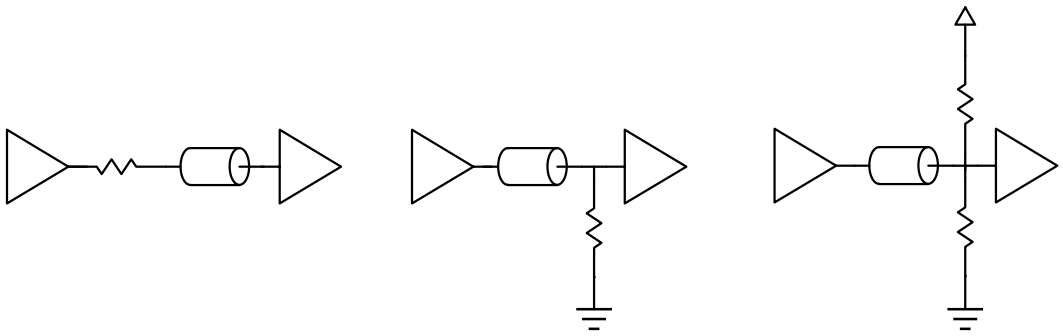


Figure 2.5. As long as there is coupling between the traces forming a differential pair, the differential impedance depends also on the distance between the traces.

2.1.1. Reflections

All changes in the instantaneous impedance seen by the signal will cause reflections. Whether these reflections will affect signal quality or not, depends on the application. If signal rise or fall times are less than twice the time delay of a transmission line reflections need to be considered [15]. If signal rise time is long compared to the time delay of a transmission line, reflections are not likely to be a big concern [3]. Some receivers designed for high-speed signals have internal terminations and thus do not require external termination resistors on PCB. High-speed transmission lines can be terminated by either parallel, series or Thevenin termination network [16]. The objective of terminating a transmission line is to minimize reflections i.e., undershoot and overshoot [17]. Overshoot caused by reflection can exceed the maximum voltage level tolerated by the transmitter circuit and cause damage and undershoot degrades signal quality by lowering the signal voltage [17]. Figure 2.6 presents different termination strategies suitable for high-speed transmission lines. Cylinders represent transmission lines, other symbols ought to be self explanatory.



(a) Series termination (b) Parallel termination (c) Thevenin termination

Figure 2.6. Series, parallel and Thevenin termination topologies

2.2. Crosstalk

Crosstalk is unwanted coupling between signals. Traces running close together on the same layer of PCB will couple together (edge coupling), and traces that are routed on adjacent layers on top of each other will couple together (broadside coupling). When traces run on different layers on top of each other they will couple mostly capacitively, and when traces are side by side on the same layer inductive coupling will dominate [16]. The amount of crosstalk introduced to the quiet line will increase as the length of the coupled section increases. Coupling gets stronger when the switching line is brought closer to the quiet line. The transmission line called *switching line* (sometimes also *aggressor*) has some signal propagating on it that couples to the transmission line called *quiet line* (sometimes also *victim*). As shown earlier the dielectric thicknesses between transmission line and reference plane affects the EM field distribution. Smaller distance to reference planes helps to contain the EM field and thus reduce the crosstalk between adjacent transmission lines. The amount of crosstalk depends on the mutual capacitance and inductance between the switching and quiet lines but also the capacitance and inductance between the individual traces and reference planes.

Far end cross talk (FEXT) produces a short voltage pulse whereas near-end cross talk (NEXT) produces longer voltage pulse. FEXT and NEXT can be calculated if enough data is available. FEXT i.e., the cross talk at the receiver end of the transmission line can be calculated with

$$FEXT = \frac{V_f}{V_a} = \frac{Len}{t_r}\frac{1}{2v}\left(\frac{C_{mL}}{C_L} - \frac{L_{mL}}{L_L}\right) \tag{4}$$

where FEXT is the far-end crosstalk coefficient as the ratio of voltage at the far end of the quiet line V_f i.e., the crosstalk voltage and the voltage of the signal line V_a. Len is the length of the coupled section, t_r is the rise time of the signal in the switching line, v is the speed of signal on the line, C_{mL} and L_{mL} are the mutual capacitance and mutual inductance per unit length. C_L and L_L are the capacitance and inductance per unit length of the signal trace. NEXT can be obtained similarly with

$$NEXT = \frac{V_b}{V_a} = \frac{1}{4}\left(\frac{C_{mL}}{C_L} + \frac{L_{mL}}{L_L}\right) \tag{5}$$

where V_b is the voltage noise on the quiet line in backward direction and other parameters as above in equation 4. Equations (4) and (5) show that strong coupling to reference planes i.e., high signal trace capacitance and inductance will reduce crosstalk. Extremely tight coupling to reference planes is however not a silver bullet to all crosstalk problems as higher trace capacitance means lower trace impedance and trace impedance obviously cannot be arbitrarily low. A rule of thumb for adjacent trace routing is that spacing between traces should be at least two times the line width to keep crosstalk at an acceptable level. [4]

Crosstalk's relation to trace to reference plane distance can be examined with a simple simulation in Siemens HyperLynx. Figure 2.7 shows the simulation schematic and figure 2.8 visualizes the trace edge-to-edge spacings and distances to reference planes for both simulated cases. Drivers U1 and U5 launch a step response with 10 ps rise time to the differential 30 cm long transmission lines connected to them. Outputs of U3.1 and U7.1 are stuck low, and all voltage variation seen at U4.2 and U8.2 is consequently due to crosstalk. Numbers 1, 2 and 3 written on transmission lines on figures 2.7 and 2.8 help to keep track which line is which, while also serving as capacitance and inductance matrix indexes later. Receivers U2, U6, U4.2n and U8.2n shown in the schematic have internal 50 Ω terminations to keep the schematic as simple as possible

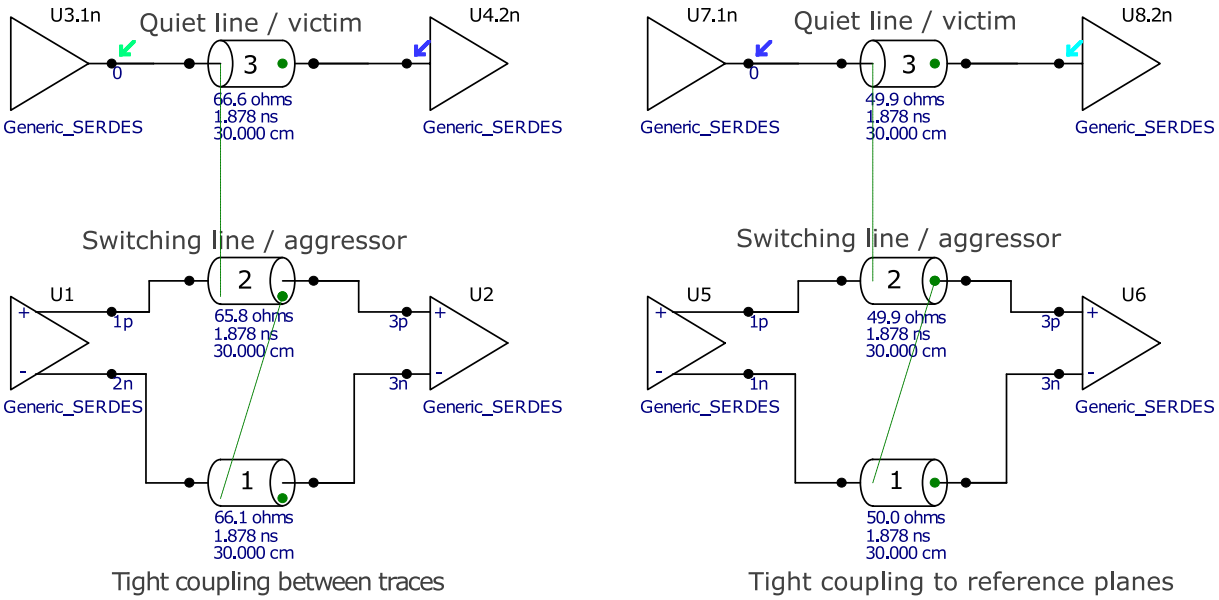
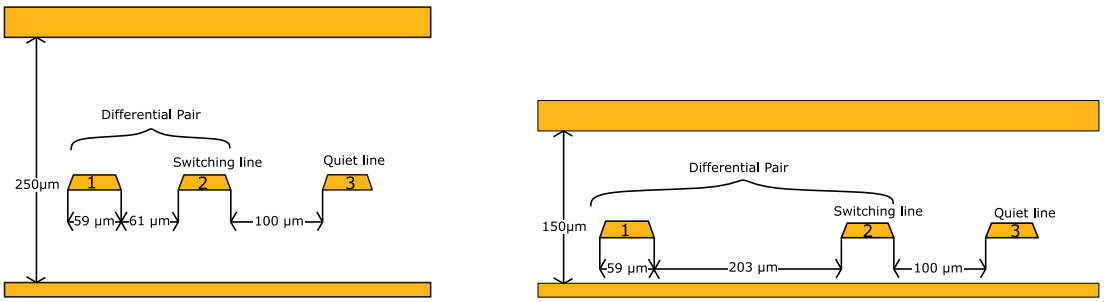


Figure 2.7. Simulation schematic for crosstalk simulation. Switching line is modelled as a transmission line from a differential pair and quiet line as a single-ended transmission line.



(a) Thick dielectric material and tight coupling between traces.

(b) Thinner dielectric material, tight coupling to reference planes and very little coupling between traces.

Figure 2.8. Cross section drawings for transmission lines in presented in figure 2.7

Capacitance and inductance matrices calculated with Siemens HyperLynx for situation in figure 2.8 (a) are

$$C = \begin{pmatrix} 100.663 & -24.348 & -0.647 \\ -24.348 & 103.077 & -13.981 \\ -0.647 & -13.981 & 96.060 \end{pmatrix} \quad L = \begin{pmatrix} 413.458 & 100.012 & 17.337 \\ 100.012 & 411.890 & 60.617 \\ 17.337 & 60.617 & 416.744 \end{pmatrix} \tag{6}$$

where the matrix indices match traces in figure 2.8 (a) from left to right, so that the switching line is index two and quiet line three and indexes run from left to right, top to bottom starting from one. Units for capacitance and inductance values are $\frac{pF}{m}$ and $\frac{nH}{m}$ respectively. For the situation in figure 2.8 (b) the mutual capacitances and inductances with the same indexing scheme are

$$C = \begin{pmatrix} 125.164 & -1.018 & -0.010 \\ -1.018 & 125.755 & -7.334 \\ -0.010 & -7.334 & 125.744 \end{pmatrix} \quad L = \begin{pmatrix} 312.995 & 2.544 & 0.172 \\ 2.544 & 312.586 & 18.229 \\ 0.172 & 18.229 & 312.595 \end{pmatrix} \tag{7}$$

HyperLynx seems to output Maxwell capacitance matrices as off-diagonal elements are negative. Maxwell capacitance matrix is the result of field solver calculations. Diagonal Maxwell capacitance matrix values are capacitances between a conductor and its return path and all other conductors. Off-diagonal values are mutual capacitances between traces. Values are negative to represent the sign of induced charges: positive voltage on conductor induces negative charge on adjacent conductor. A more useful version of capacitance matrix is the SPICE capacitance matrix where each value stands for a capacitance values between a pair of conductors. Diagonal elements of SPICE capacitance matrix are capacitances between conductors and their return paths and values stored in the matrix can be used to construct the equivalent spice circuit. In SPICE capacitance matrix off-diagonal values are numerically equal to Maxwell matrix but positive. Diagonal SPICE capacitance matrix values can be obtained from Maxwell capacitance matrix by summing values in each column of Maxwell capacitance matrix. The sum of a column is the diagonal value in SPICE matrix for the respective column. Values in inductance matrices are loop self-inductances and loop mutual inductances. [4]

SPICE capacitance matrix for tightly coupled traces (figure 2.8 (a)) is

$$C_{SPICE} = \begin{pmatrix} 75.668 & 24.348 & 0.647 \\ 24.348 & 64.811 & 13.981 \\ 0.647 & 13.981 & 81.432 \end{pmatrix} \tag{8}$$

where diagonal values have been derived from capacitance matrix in equation (6). Correspondingly SPICE matrix for the case where coupling is strong to the reference planes and weak between the differential traces is

$$C_{SPICE} = \begin{pmatrix} 124.127 & 1.018 & 0.010 \\ 1.018 & 117.403 & 7.334 \\ 0.010 & 7.334 & 118.4 \end{pmatrix} \tag{9}$$

where values have been derived from the capacitance matrix in equation (7). SPICE matrix values are applicable for FEXT and NEXT formulas in equations (4) and (5). The capacitance between the switching line and the reference planes, is in this case C_{22} and mutual capacitance between switching line and quiet line is C_{23} or C_{32}. Values for mutual inductance and self-inductance can be obtained directly from the matrices outputted by the simulator. Simulation result presented below cannot however be replicated simply by substituting values to equations (4) and (5) because in the simulations non-ideal behavior such as losses have been taken into account.

Overview of the Simulation results for the situation in figure 2.7 is shown in figure 2.9. As mentioned before switching lines have 10 ps rise time drivers. Dk on all dielectric layers is 3.5. Voltages at the transmitters of switching lines are V(U1-1p) and V(U5-1p), switching line receiver voltages are V(U2-3p) and V(U6-3p). Crosstalk voltages at the far-ends of the quiet lines are V(U4-2n) and V(U8-2n). Near-end crosstalk voltages are the remaining voltages: V(U3-1n) and V(U7-1n).

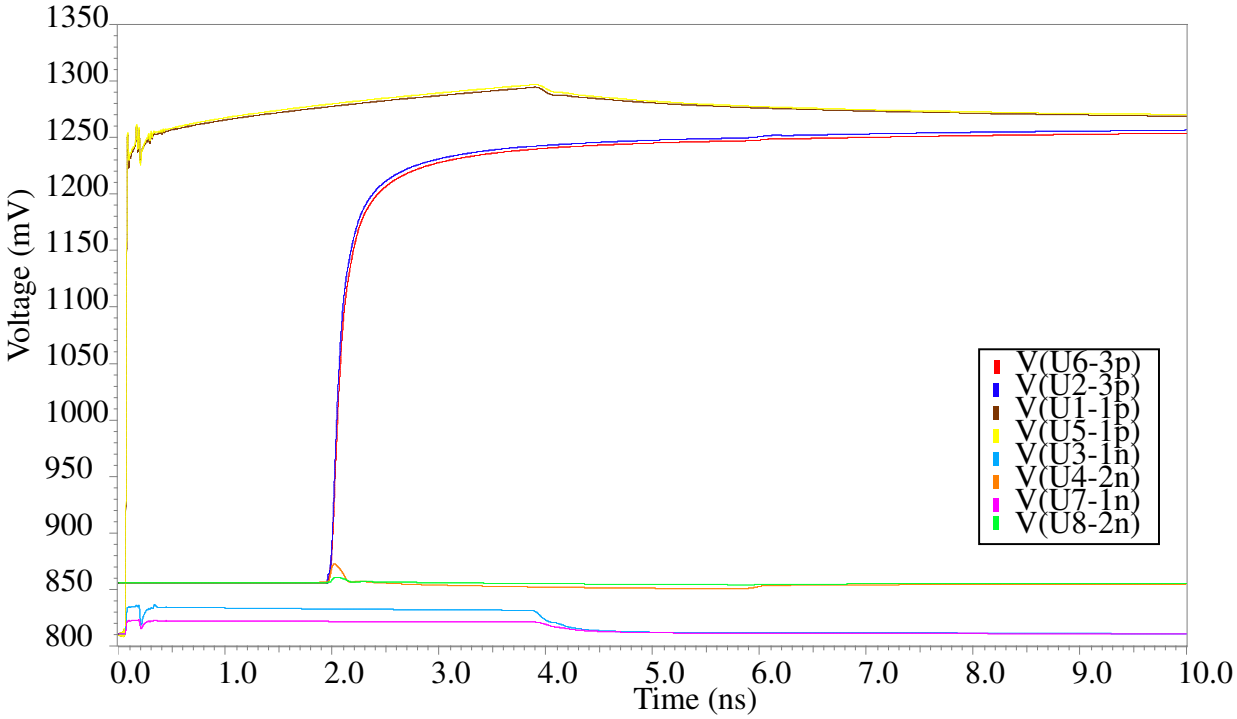


Figure 2.9. All voltages from the simulation schematic shown in figure 2.7.

A closer look at the crosstalk voltages is shown in figure 2.10. Waveform colors and labels match figure 2.9. Simulation results confirm that bringing reference planes closer to the traces help to reduce crosstalk. The voltage V(U8-2n) i.e., the far end crosstalk voltage of the configuration with tight coupling to reference planes is much lower than the crosstalk voltage of the configuration where coupling is tight between the traces and loose between traces and reference planes. Same holds true for the near-end crosstalk voltages.

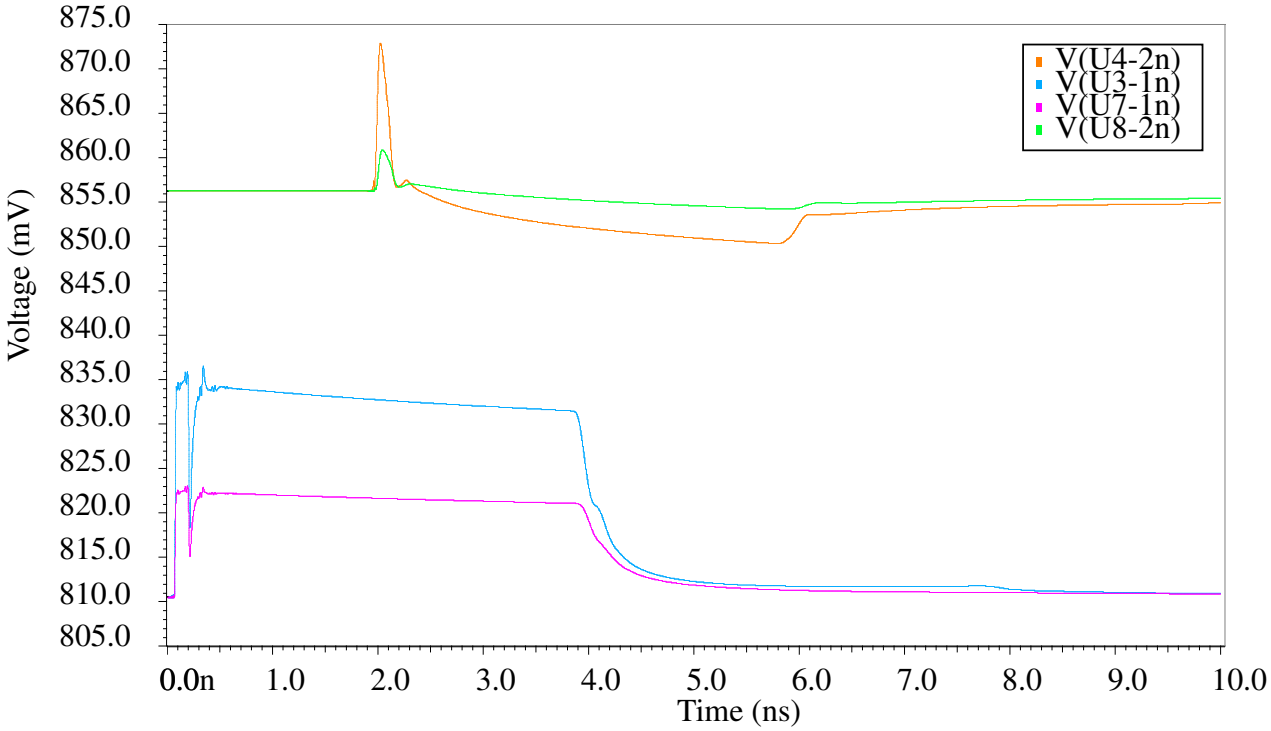


Figure 2.10. Far end and near end crosstalk simulation results. Waveform labels are same as used in figure 2.7.

2.3. Signal losses

All real interconnects are lossy, and losses are generally unwanted in the scope of digital signal transmission. If signal losses were constant on the whole frequency spectrum losses could be compensated with gain at the receiver. However as high frequencies are attenuated more in the transmission line signal rise times get longer and sharp edges become rounded. If the signal rise time is degraded so much that it starts to be comparable to the unit interval (UI) of the signal, inter-symbol interference (ISI) will occur as the signal won't have enough time to reach the desired voltage levels before symbol changes.

2.3.1. Dielectric losses

Dielectric losses are caused by leakage currents through the dielectric material. On DC the dominating mechanism is ionic motion. The amount of mobile charge carriers in dielectric materials is generally small and thus dielectric losses are low on DC. The dominating dielectric loss mechanism on AC is polarization of permanent dipoles. When electric field is applied to the dielectric material dipoles align with the electric field. If the electric field is caused by a sinusoidal voltage the orientation of dipoles will change with the electric field enabling AC current flow. Higher frequencies will cause dipoles to rotate more quickly increasing the leakage current. [4, 15]

2.3.2. Conductor losses

Conductor losses are caused solely by resistance on DC, but as frequency increases the loss caused by DC resistance is dwarfed by other loss mechanisms. While the resistivity of copper stays constant up to frequencies near 100GHz, skin effect forces the current to flow only in the

surface of the conductor which increases losses. Losses caused in conductors can be decreased by either using sorter conductors or by using wider conductors. High-speed materials tend to have lower Dk than regular FR-4 [18]. FR-4 is a common name for woven fiberglass reinforced epoxy resin laminates [19]. Low Dk allows using wider conductors for certain layer thickness and instantaneous impedance, resulting in lower loss interconnects. Conductor losses cause signal loss equally in the signal trace and in the return path.

2.3.3. Skin effect

Current's tendency to flow closer to the conductor surface on higher frequencies is called skin effect. The immediate consequence of this phenomena is that high frequency signals do not utilize all of the available cross-sectional conductor surface area. Smaller cross-sectional surface area increases the apparent resistance of the conductor, which in turn causes signal losses [20]. Ways to mitigate skin effect losses are discussed in chapter 4. Skin depth measures the depth in which current flows on a certain frequency and it can be approximated with

$$\delta = 2.1\sqrt{\frac{1}{f}} \tag{10}$$

where δ is the skin depth in μm and f is the (sine wave) frequency in GHz [4]. Equation (10) is plotted in figure 2.11 from 0.1 GHz to 100 GHz. Skin depth is on vertical axis and frequency on horizontal, logarithmic axis. On 100 MHz skin depth is only 6.64 μm, which is already less than half of the nominal thickness of 17 μm copper foil. On even higher frequencies copper surface profile starts also contributing to signal losses as copper foils used on PCBs have surface bumpiness that exceeds the skin depth. Skin depth approaches zero as frequency increases to hundreds of gigahertz. When skin depth is smaller than the conductor thickness, the conductor surface area seen by the propagating signal is smaller.

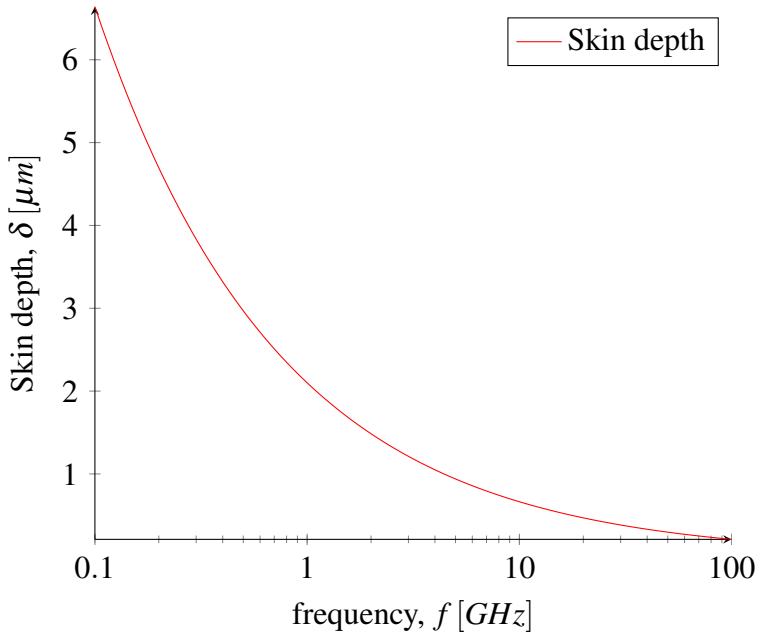


Figure 2.11. Skin depth as a function of frequency.

Skin effect originates from the same phenomena that causes return currents to flow right

below (and above) the signal trace. AC currents will travel paths that have the least inductance i.e., the lowest impedance. This phenomenon is amplified as frequency increases.

2.4. Propagation delay and Skew

Signal propagates in an interconnect at a finite speed that is considerably lower than the speed of light in a vacuum. Speed of signal in PCB dielectric is

$$v = \frac{c}{\sqrt{Dk}} \tag{11}$$

where c is the speed of light (roughly 300 000 000 m/s) and Dk is the relative dielectric constant of the material [3]. Propagation delay is then naturally

$$T_d = \frac{conductor\ \ length}{v} \tag{12}$$

where v is the speed of signal in the dielectric material and T_d is the time delay or propagation delay caused in the interconnect. Propagation delay alone does not degrade signal quality, it only adds latency to the signal transmission. However, if propagation delay is different between conductors forming a differential pair or different between other time sensitive signals, problems start to occur. Skew causes mode conversion in differential signals, which means that differential signals become common mode signals and vice versa. [20]

How much skew can be tolerated depends on the signaling baud rate and modulation. Pulse Amplitude Modulation 4-level (PAM4) is more sensitive to intra pair skew than non-return-to-zero (NRZ) modulation with the same data speed [21]. The allowable skew is decided by the rise time of the receiver and the signal speed in the transmission line [16]. Signal baud rate also gives some insight on the order of magnitude of skew that can be tolerated. For example, a 2.4 GB/s NRZ data stream has a unit interval of 416 ps [16]. When signaling rate is 26.5625 Giga baud (GBd) the unit interval is as short as 37.64706 ps [22]. It is safe to say that with no information about the receiver rise times the skew constraints are tight for high-speed signals. A signal travels 6 mm (Dk=3.5) in the UI of 26 GBd signal and skew cannot be even close to the whole unit interval. While trace length matching of PCB traces is a manageable issue skew is also generated by other factors. One of these is non-uniformity of the substrate material. This skew mechanism is called fiber weave effect and will be discussed later in further detail.

3. PCB MATERIAL PROPERTIES

PCBs are typically constructed of stacks of woven glass fiber sheets laminated together with epoxy resin with copper foil sheets in between the glass fiber layers. This chapter describes how dissimilar materials, material treatments and manufacturing processes affect parameters that influence signal integrity on PCB. The focus is on Glass fiber materials as they enable cost effective mass production with currently available manufacturing technology. Materials other than glass fiber can be used as PCB substrate, however these more exotic materials are out of the scope of this document due to worse availability and higher cost.

Figure 3.1 shows an example on how an eight-layer PCB layer construction i.e., build-up or stack-up can be done. Different layers have been labeled for the top side of the drawn stack-up. Resin has been drawn transparent to show glass weave structures inside layers. Core layers have a single glass fiber sheet while prepreg layers are constructed from two glass fiber sheets stacked on top of each other. In real application where two glass fiber sheets are used for one layer the fiber bundles would not likely be aligned as they are in the figure 3.1. Prepreg layers could also be constructed from only one glass fiber cloth and one core could on the other hand have two or more glass fiber cloths stacked together. Construction of each layer depends on what is available for the selected resin system.

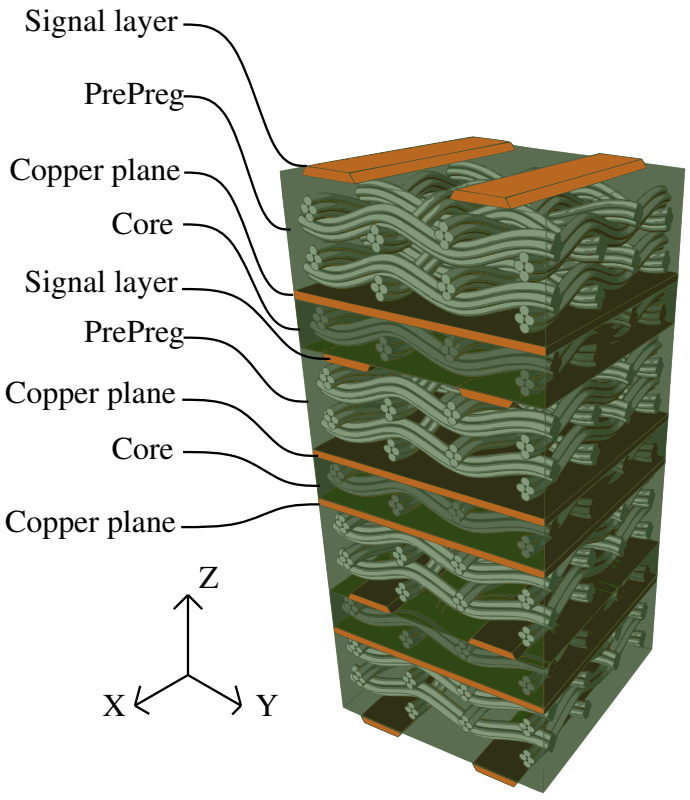


Figure 3.1. PCB layer construction visualization, not drawn to scale.

3.1. Core and Prepreg

PCB materials referred as core or copper-clad laminates are comprised of cured resin reinforced with glass fiber mesh. Core materials come with copper foil attached to both sides. These materials are cured during the laminate manufacturing process and thus their thickness will not vary during the PCB lamination process. Prepreg on the other hand is only partially cured before PCB lamination process and thus prepreg layer's final thickness depends on the amount of copper present on the adjacent surfaces. Both cores and prepregs can be ordered with various different glass styles. Glass weaves and epoxy resin have different dielectric properties which ultimately affects signal propagation on the finished PCB. [23]

Final prepreg thickness affects the thickness of the finished board as well as the impedances on the signal layer next to the prepreg layer. Some stack-up design utilities such as Siemens Z-planner and ICD Stack-up Planner do calculate the pressed prepreg thickness automatically, however sometimes it may be useful to estimate final prepreg thickness manually. IPC has defined laminate thickness tolerances for different laminate thicknesses and copper types in IPC 4101E WAM1 [24]. IPC is an international standardization organization standardizing electronics product development cycle [25]. One way to estimate final prepreg thickness is

$$T_{FinalPrePreg} = T_{InitialPrePreg} - [T_1(100\% - D_{Trace}\%)] - [T_2(100\% - D_{Plane}\%)] \qquad (13)$$

where $T_{FinalPrePreg}$ is the finished prepreg thickness, $T_{InitialPrePreg}$ is initial prepreg thickness, T_1 and T_2 are copper thicknesses of signal and plane layer respectively D_{Trace} is routing density for signal layer in percentage and D_{Plane} is the same for the plane layer [26]. The estimate in equation (13) is based only on initial prepreg thickness, copper layer thicknesses and copper layer densities, it does not account for resin content, which also affects the prepreg layer thickness [27].

3.1.1. Relative dielectric constant and loss tangent

Relative dielectric constant (ε_r) or (Dk) is probably the best-known dielectric property of PCB substrate materials. It is material's absolute dielectric constant divided by the dielectric constant of air. To be exact relative dielectric constant compares material's permittivity to vacuum permittivity, but air permittivity differs insignificantly from vacuum permittivity, thus it does not make sense to differentiate between vacuum and air in this context [5]. When referring to material properties relative dielectric constant is often simply called *Dielectric constant*. Dielectric constant creates capacitance between conductors influencing greatly to trace impedances. The dielectric constant seen by the finished transmission line on the PCB is not directly the data sheet value of Dk as surrounding materials influence the dielectric constant that is perceived by the transmission line. This perceived Dk is called effective dielectric constant. [4]

Dissipation factor (Df) is the same as tangent of the loss angle $(\tan(\delta))$ and it describes the amount of energy that is lost in the electromagnetic field traveling through dielectric material [16]. A great everyday demonstration of dissipation factor is a bowl that heats up in the microwave oven: Bowl's dissipation factor determines how much energy it will dissipate and turn to heat. Ideally one would want the food to heat up and not necessarily the bowl however if the bowl has high dissipation factor it may heat up significantly. Greek letter δ as loss angle is unrelated to δ as skin depth.

Dielectric properties are not constant across frequencies, both dielectric constant and dissipation factor vary slightly relative to frequency. Dk decreases as frequency increases and Df

increases slightly as frequency rises [28]. Material data sheets seem to agree on the increasing of Df with frequency while in Eric Bogatin's Signal and Power Integrity - simplified -book dissipation factor's frequency dependency is described as follows: *"At high enough frequency, the dipoles will not be able to respond as fast as at lower frequency and we would, therefore, expect the dissipation factor to decrease."* [4]. This sentence sounds contradicting in comparison to the measured Df values available in material data sheets. As Df test methods are well established and documented it should be safe to conclude that Df increases slightly with frequency - at least on the frequency band of interest in the scope of PCB design. Higher Df means bigger losses resulting in higher insertion loss and thus worse performance while lower Dk results in higher trace impedance. Dk and Df values measured with different frequencies are usually available in material data sheets. Dissipation factor's effect to dielectric losses is also heavily frequency dependent even if the dissipation factor itself would stay constant.

Figure 3.2 shows simulated attenuation per unit length in an asymmetric stripline transmission line. Figure 3.3 shows the construction of the simulated interconnect. Frequency is on the horizontal axis and attenuation on the vertical axis. The dielectric losses (green curve) start increasing rapidly on frequencies beyond 10GHz. Copper roughness effects have not been considered in the simulations for this graph. Resistive losses increase due to skin effect: current flows in the conductor surface only making the conductor effectively thinner. See section 2.3.3. Ways to measure dielectric constant and dissipation factor have been described in further detail in section 3.1.2.

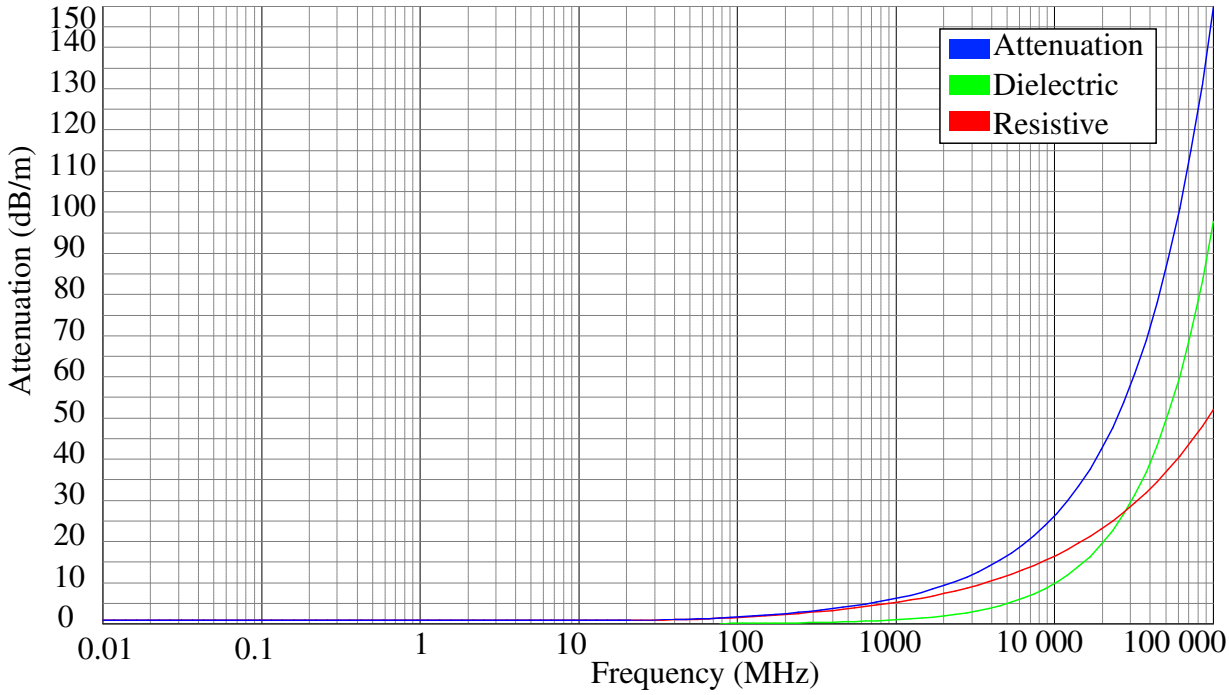


Figure 3.2. Attenuation per unit length HyperLynx

Prepreg thickness in figure 3.3 is 139 µm and core thickness is 102 µm, different features in the drawing are drawn roughly to scale with each other. Dielectric constants are 3.25 and 3.66 for prepreg and core respectively. Dissipation factor of prepreg material is 0.006, core material has slightly lower loss at 0.0056. Transmission line single ended impedance is around 50 Ω. The used material parameters are parameters of a real low loss multilayer PCB material from Shengyi [28]. The specific material is Shengyi S7439C/S7439CB.

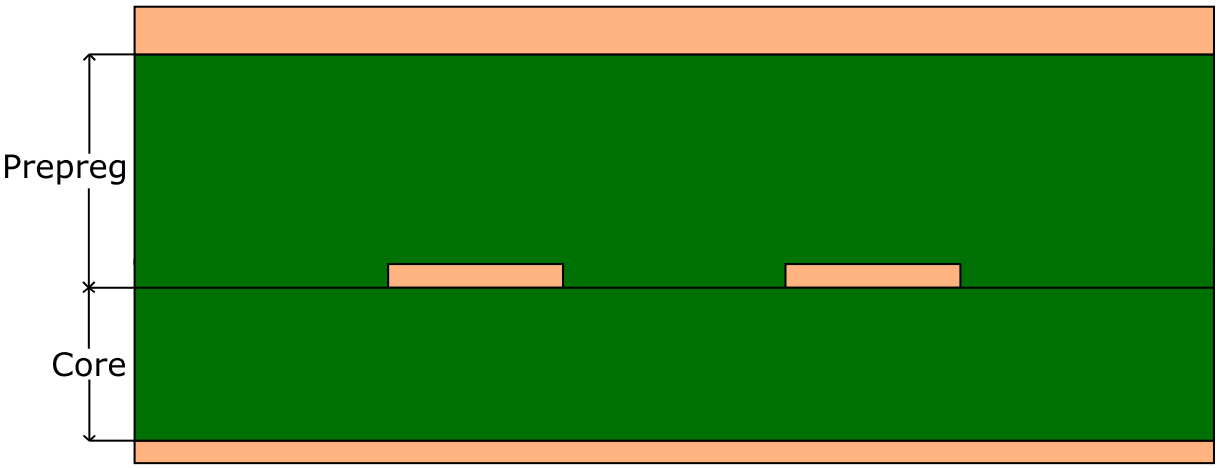


Figure 3.3. Cross section drawing of the stripline structure simulated in figure 3.2

3.1.2. Dk and Df test methods

An abundance of dielectric property test methods has been developed: IPC has defined 12 different test methods for measuring Dk and on top of the IPC test methods there are numerous test methods defined by other institutions as well [29]. Generally dielectric material test methods are divided to circuit and material test methods. This section will introduce a couple of common test methods: Clamped stripline test (material test method), Split-Cylinder Resonator (material test method) test and microstrip ring resonator test (circuit test method). Material test methods evaluate the dielectric purely without any PCB fabrication variables. Circuit test methods on the other hand evaluate materials based on circuit performance. Both test method categories are affected by different variables and measuring same material using different types of tests will result in different results. Moreover, some test methods evaluate material's properties in Z-direction while other tests evaluate the materials in the XY-plane. See figure 3.1 for coordinate axes reference. Most PCB materials are anisotropic, which means that material's dielectric properties are not homogenous in all directions [29]. Generally dielectric properties in Z direction are of a bigger interest for high-speed digital designs as stripline transmission lines couple to reference planes in Z direction. However as explained in section 2.1 differential pairs also couple to each other in XY direction thus is also worth mentioning that there should be mostly only resin from the prepreg layer between the differential pair and resin has lower Dk than glass.

The test method that seems to be most frequently used in laminate datasheets is the stripline test for Permittivity and Loss Tangent, specified in IPC TM-650 Test Methods Manual 2.5.5.5 [30]. This test method is sometimes called also "clamped stripline test" which is very descriptive name for this test. When performing this test, a resonator structure is clamped between two sheets of the material under test. A stripline structure is formed as the clamping surfaces double as reference planes. Due to this mechanical clamping configuration this test method may report lower Dk than actual as there might be some air trapped in the surface imperfections of the materials. The IPC TM-650 2.5.5.5 evaluates dielectric properties in Z-direction and up to 12.4GHz. Clamped stripline test is a material test method and it does not evaluate the performance of final applications, but rather the consistency of the material in general. The copper clad materials used to conduct this test are destroyed as all copper needs to be etched away before performing the clamped stripline test. [29, 30]

Split Cylinder Resonator Test specified in IPC-TM-650 2.5.5.13 needs similarly prepared

material as the clamped stripline test: all copper needs to be etched away before conducting this test. Unlike clamped stripline test the Split-Cylinder Resonator test evaluates material in the XY-plane. If results obtained by Split-Cylinder resonator test and clamped stripline test on a certain frequency are compared, information about the material anisotropy can be obtained. [29]

Microstrip Ring resonator test method is a circuit test method, which means that it is affected by variables associated with PCB construction such as copper thickness and roughness and manufacturing tolerances. Microstrip Ring resonator test is conducted by building a microstrip ring resonator on the material under test and measuring its performance. [29]

From the three mentioned test methods microstrip ring resonator and the clamped stripline tests are relevant for stripline and microstrip interconnect design where most coupling is to the reference plane(s). The clamped stripline test gives the best consistency as the material under test is the only variable in the test setup, but as stated earlier the obtained Dk values tend to be lower than material's actual Dk. However as clamped stripline test gives consistent results it is a good test method for comparing different materials. Clamped stripline test results are also influenced by the copper roughness, even though all copper is etched away. Rougher copper leaves the laminate surface rougher, and more air can be trapped between the laminate and the test fixture [31]. Microstrip ring resonator test on the other gives Dk value for the particular material and manufacturing combination. Manufacturing tolerances can cause the Dk extraction to be inaccurate, if they are not taken into account in the Dk extraction process [29]. Different test circuit designs can also yield different Dk results on the same material [31].

3.1.3. Glass Styles

Glass fiber cloth makes PCB materials durable and rigid. It also affects the electrical properties of the finished PCB. Different glass fiber cloths are distinguished with a three- or four-digit number. Unfortunately, there does not seem to exist any common rules regarding glass style numbers. Lack of a common glass style numbering scheme means that it is not possible to deduct dimensions and other features of a glass style solely based on the glass style number. In table 3.1 glass styles available for the earlier mentioned low loss material, Shengyi S7439C/S7439CB are listed [28]. Glass style properties apart from the spread-column are as presented in IPC 4412C [32]. Spread-column is based on [33] as IPC has not defined clearly what should be referred as spread glass [34]. Spread glass in general refers to glass fibers being distributed more evenly in the woven fabric. In standard glass the glass bundles are roundish and there are gaps between bundles, spread glass on the other hand has flattened glass bundles with smaller gaps between glass bundles. Fabric count per centimeter presented in standard has been converted to glass fabric pitch as pitch better describes the spacing between the glass bundles. Although it should be kept in mind that the glass fiber bundles may not always run straight, and the actual fabric pitch may change along the material. Glass used in electronics is usually so-called E-glass, which is electronics grade glass with low alkali content and low water absorption tendency [35]. There are also other glass types such as low dielectric constant glass (D-glass), High-strength glass (S-glass) and chemical glass (C-glass) [35]. Fabric thickness values presented on table 3.1 are marked as "Reference only" in the IPC standard. The thickness of the finished core materials will be presented in laminate manufacturers data sheet and prepreg material thickness will need to be determined based on the resin systems resin content and the amount of copper on the planes adjacent to prepreg layer. Figure 3.4 visualizes how glass bundles are arranged in standard glass like 106. Drawing represents side view of the fabric, in actual printed circuit board this fabric would be soaked in resin and laminated between copper planes from top and bottom.

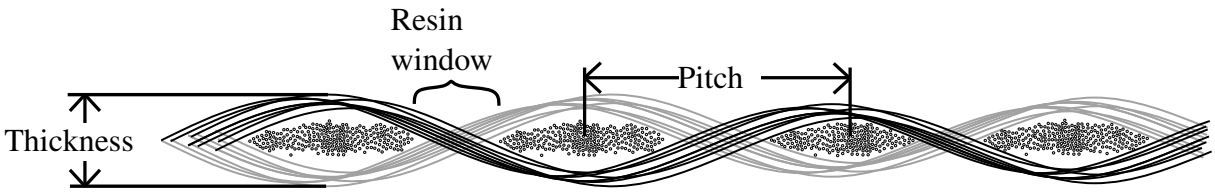


Figure 3.4. Side view drawing of non-spread glass fiber cloth, drawn neither to scale nor to represent any actual woven fabric.

Table 3.1 Approximate dimensions for a selection of glass styles

Glass Style	Thickness µm	Spread	Pitch X µm	Pitch Y µm
106	33	No	454.5	454.5
1067	43	Yes	362.3	362.3
1078	43	Yes	469.5	469.5
1080	53	No	423.7	540.5
3313	84	Yes	423.7	409.8
2116	94	No	423.7	438.6

Different glass styles obviously have different characteristics and tradeoffs. Bigger resin windows allow resin to flow freely through the glass fiber cloth generally allowing better adhesion to adjacent copper planes while more uniformly spread glass fiber bundles yield more uniform dielectric properties. Spread or flat glass was initially developed to improve consistency in laser-drilling process, but it also helps mitigating glass weave skew and improves resin distribution [34]. Improved resin distribution here probably means that the resin will flow nicely on the flat glass, if there is enough resin to fill everything. However if there is not enough resin on either side of the glass fabric flattened glass bears higher risk of leaving voids as the resin will have hard time flowing through the uniform glass bundles. In figure 3.5 different glass cloths listed in table 3.1 have been drawn proportionally to each other using dimensions presented in [33]. Glass style 2116 has been omitted from the drawing as dimensions were not available. It is clear that spread glass has significantly smaller resin windows: almost no white background can be seen through glass styles 1067, 3313 and 2116. Table 3.2 lists different terms used to describe glass styles based on Isola Group's documentation [33].

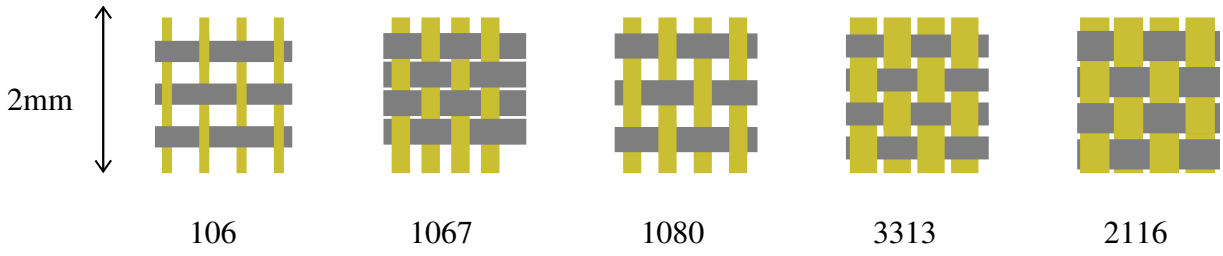


Figure 3.5. Visualization of different glass styles

Table 3.2 Glass definitions based on definitions from Isola Group S.a.r.l

Term	Definition
Spread Glass	Glass bundles are spread out, offers more uniform dielectric properties and is flatter than standard glass.
Expanded Weave	Glass that is spread in more than one direction.
Open Filament	Same as expanded weave
Open Weave	Same as expanded weave
Mechanically Spread (MS) Glass	Glass that is mechanically spread in both X and Y directions.
Square Weave	Glass that has balanced density and/or same glass pitch in both X and Y directions.
Flat Glass	Glass with fibers that have very little or no twist at all.

3.2. Copper foils

Copper foil is the part of printed circuit board that forms the bulk of conductors, thus its qualities greatly affect printed circuit board's electrical performance. Qualities of the copper foil between dielectric layers of the PCB also determine how well layers adhere together and ultimately how durable the finished PCB is. Copper comes in different thicknesses and surface finishes, common copper thicknesses are 70 μm, 35 μm, and 17 μm. Generally smoother copper has better electrical properties but worse mechanical properties: it adheres worse to the PCB laminate resulting in worse structural rigidity while electrical losses due to surface roughness are lower. Two different ways to manufacture copper foil can be utilized depending on the desired electrical and mechanical properties. These manufacturing methods are rolling and electrodeposition. Differences between rolled copper or rolled-annealed (RA) copper and Electrodeposited (ED) copper are discussed briefly below based on [36], [27] and [37].

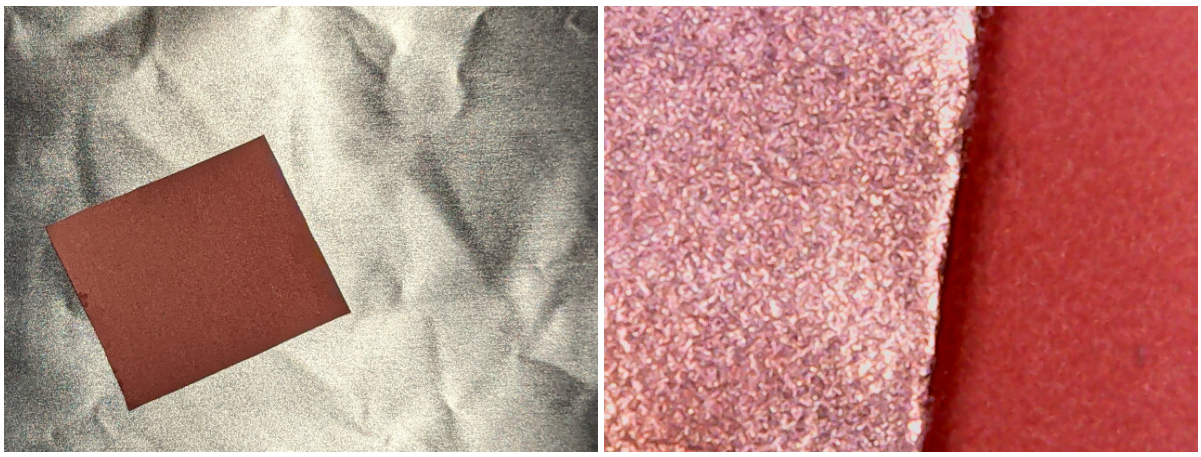
3.2.1. Rolled Copper

Copper foil can be manufactured by flattening a copper ingot to thin foil by series of rollers. Foil manufactured in this kind of process is called rolled copper or RA copper (rolled-annealed copper). Finished RA copper foil is very smooth, surface roughness is defined by the surface finish of the final rollers in the manufacturing process, but generally surface is smoother than ED copper surface and needs to be roughened to some extent before lamination in order to improve bonding to the PCB substrate. Due to the manufacturing process rolled copper has in-plane grain structure which allows it to withstand bending quite well thus allowing use in flexible circuits. Rolled copper is also able to withstand thermal stresses better than ED copper and might be useful material in applications that are expected to face rapid temperature changes.

3.2.2. Electrodeposited copper

More common and cheaper method of manufacturing copper foil is electrodeposition. Electrodeposited (ED) copper is manufactured by plating a titanium drum with copper using electrolysis. ED copper manufacturing process results in copper foil that has a shiny side and matte side. The shiny side is the drum side and its surface finish is determined by the drum's surface. The matte side is rougher and in the case of standard ED copper the matte side is treated and attached to the PCB core material. ED copper has vertical grain structure which makes etching

traces and other patterns to ED copper easier than to RA copper. In practice higher circuit density and tighter trace width tolerances can be achieved with ED copper. Figure 3.6 shows the difference between shiny and matte sides of ED copper.



(a) Shiny side up in the background. (b) Shiny side up on left

Figure 3.6. Shiny and matte sides of ED copper differ considerably from each other.

3.2.3. Reverse treated foil

Reverse treated foil copper (RTF) is ED copper that is bonded to the PCB core substrate from the shiny side. As the name implies the treatment is "reversed" in comparison to normal ED copper where the matte side is treated and adhered to the PCB core substrate. The treated side of RTF copper is after treatments rougher than initially but still smoother than the matte side enabling designers to exploit smaller conductor losses in high frequency applications by designing the stripline so that the closest reference plane is on the RTF side of the stripline and if possible, RTF side of reference plane is towards the stripline. This configuration will be explored in further detail in section 4.2.1.

3.3. Copper properties

This section will explore copper foil properties that are relevant to PCB design and signal integrity performance. The focus in this section is on properties for ED and RTF copper, but same properties should be applicable to rolled copper as well.

3.3.1. Copper thickness

Possibly the most evident variable related to copper foils is the thickness of the copper foil. As stated earlier the most common thicknesses are $70\,\mu m$, $35\,\mu m$, and $17\,\mu m$. Sometimes copper thickness values are given in ounces per square feet (Oz/ft^2). Mentioned common thickness values in ounces are 2 Oz, 1 Oz and 0.5 Oz. In reality copper foil thicknesses are usually less than the nominal thickness. IPC specifies minimum foil thicknesses for internal and external copper layers and different nominal thicknesses in IPC 6012E [38]. Relevant data from the IPC standard for internal layers has been replicated in table 3.3 and for external layers in table 3.4. Final thickness for internal layers is thinner than initial foil thickness because different treatments applied in the PCB lamination process thin down the copper. External layers, on the

other hand are thicker than the foil itself as plating is applied on top of the copper. Classes 1, 2 and 3 in table 3.4 refer to IPC performance classes defined in IPC-6011. Class 1 is General Electronic products, Class 2 Dedicated service electronic Products and Class 3 High Reliability Electronic Products [39].

Different copper thicknesses are suitable for different applications. For signal layers carrying high frequency i.e., high-speed signals using thick copper does not make sense as skin effect forces the current to flow in the surface layers of the conductor. Thick copper foils are mostly needed in power distribution networks as the voltages for processors and other digital devices can be low, yet the power consumption can be several hundreds of watts. In other words, tens of amperes of DC current may need to flow in some parts of some PCBs thus requiring high cross sectional conductor surface area to keep ohmic losses and heat output small. Thick copper works also as a better heat sink than thin copper. Typically, thinner foil has higher roughness on the matte side than thicker foils in the same product range. As an example, Rogers CU4000 Electrodeposited copper foil data sheet has a couple of microns higher roughness for 18µm thick standard foil than 35µm thick standard foil, however with Rogers' RTF copper called LoPro copper there is no difference in this particular case [40]. Copper thickness also limits achievable conductor width and spacing. With thicker copper it is more difficult to etch very small features mainly due to etch factor getting worse with thicker copper [41]. Etch factor worsens as copper thickness increases because etching is a chemical process that eats away all exposed copper: As the etching process progresses exposed copper is revealed from the "sides" of copper features being etched allowing etching chemistry also remove material in the unwanted horizontal direction. The thicker the copper foil is the longer the etch process needs to go on and longer etching leads to more etched exposed copper. Etch factor closer to zero means more square trace.

Table 3.3 Copper thickness tolerances as specified in IPC 6012E for internal copper layers.

Thickness (µm) [Weight $(oz./ft^2)$]	Absolute Copper Minimum thickness (µm)	Minimum Foil Thickness after Processing (µm)
17.10 [1/2 oz.]	15.40	11.4
34.30 [1 oz.]	30.90	24.9
68.60 [2 oz.]	61.70	55.7

Table 3.4 Copper thickness tolerances as specified in IPC 6012E for external copper layers.

Thickness (µm) [Weight $(oz./ft^2)$]	Absolute Copper Minimum thickness (µm)	Minimum Conductor Surface Thickness after Processing.	
		Class 1 & 2	Class 3
17.10 [1/2 oz.]	15.4	33.4	38.4
34.30 [1 oz.]	30.90	47.9	52.9
68.60 [2 oz.]	61.70	78.7	83.7

3.3.2. Copper roughness

Different ways to measure and present surface roughness are in use. In this section roughness measures that are most commonly used with copper foils are described. The units of measure-

ment often associated with PCB design are Ra, Rrms and Rz. Ra and Rrms are similar to each other whereas Rz takes completely different approach [42]. Ra and Rz interpret surface geometry very differently and while conversion coefficients between said units have been derived roughness values obtained by converting from different units may not be accurate at all. Ra roughness value lacks information Rz needs and vice versa [42, 43]. Conversion coefficients can be enough for rough estimations and will work better on some surface profiles than on others. Surface roughness units are described below based on [43] unless some other source is specified. For demonstrative purposes I have created a dummy roughness profile Z(x) shown in Figures 3.7 and 3.8. This roughness profile does not represent any real surface but hopefully helps to gain understanding on how different roughness values are obtained.

Ra is the roughness average value of the surface; this parameter is essentially the integral of the surface profile variation divided by the sample length. The analytical definition for Ra is

$$Ra = \frac{1}{L}\int_0^L |Z(x)|\,dx \tag{14}$$

where Z(x) is the surface profile variation and L is the length of the profile. With discrete samples Ra is calculated with

$$Ra = \frac{|Z_1| + |Z_2| + ... + |Z_n|}{n} \tag{15}$$

where $Z_1 ... Z_n$ are discrete samples taken from the surface and n is the total amount of samples. In figure 3.7 Z(x) is plotted with blue line, and the integral of the absolute value of Z(x) is in gray. If 200 equally spaced samples are taken from Z(x) over the entire visible profile result is Ra value of 0.87. In practice Ra is sum of samples within a sampling length divided by the number of samples.

Rrms or Rq roughness is similar to Ra but the result is a root mean square (RMS) value. Analytical definition of Rq is

$$Rq = \sqrt{\frac{1}{L}\int_0^L (Z(x))^2 dx} \tag{16}$$

with the same abbreviations as used in equation (14). For practical use cases Rq can be obtained from discrete samples with

$$Rq = \sqrt{\frac{Z_1^2 + Z_2^2 + ... + Z_n^2}{n}} \tag{17}$$

using same abbreviations as used in equation (15). The example profile has Rq of 1.08 based on 200 discrete samples.

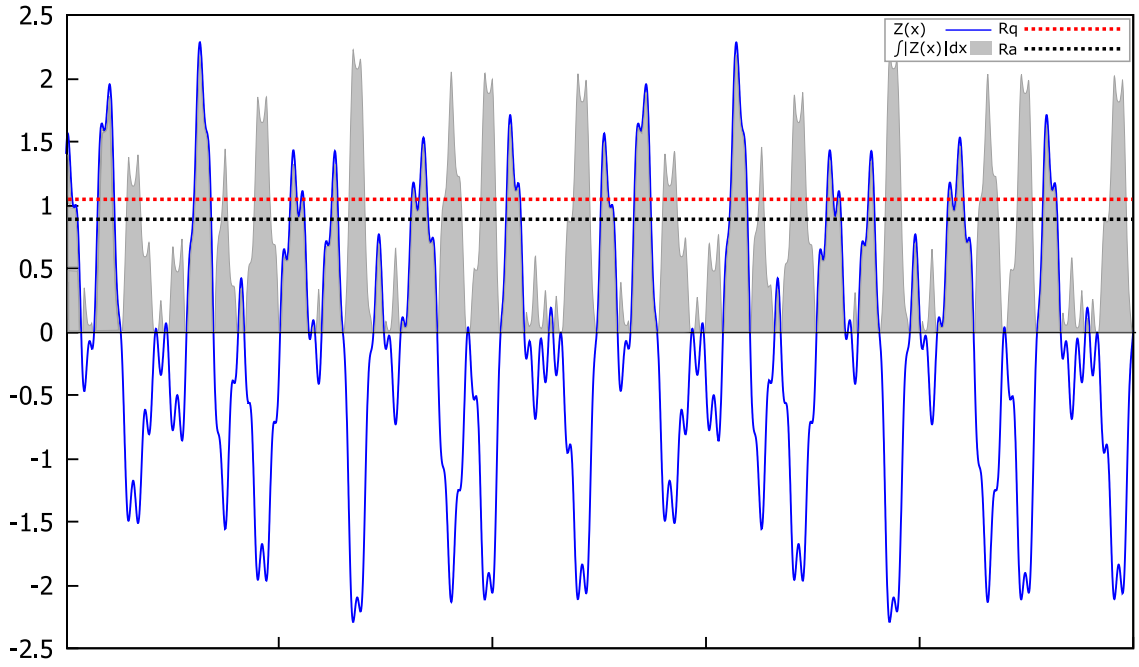


Figure 3.7. Ra and Rq roughness values plotted on the same graph with the roughness profile.

There are multiple definitions for Rz roughness as it has been defined differently by different standardization organizations. Having same symbol defined in multiple different ways is not ideal and creates confusion. Sometimes Rz values are presented with a note specifying which Rz definition is used, this is however not always the case. In my understanding Rz (DIN) is nowadays the most used definition for Rz and all Rz values will be RzDIN values in this document unless otherwise specified. Rz in ISO4287 standard is defined simply as sum of largest profile peak and valley within a sampling length [44, 45]. With the example dummy roughness profile Z(x) RzISO is 4.57. Rz is defined in JIS'94 as ten-point roughness profile, accounting five highest peaks and 5 lowest valleys within a sampling length. RzDIN is defined by first dividing the sampling length to five equal length sections and measuring the highest peak-to-valley distance within each of the five sections and calculating the average peak-to-valley height. In practice RzDIN can be obtained with

$$RzDIN = \frac{1}{5}\sum_{i=1}^{5}(Pi - Vi) \tag{18}$$

as sum of highest peak-to-valley distances divided with the number of samples. For the dummy roughness profile Z(x) RzDIN roughness of 4.04 can be obtained by using labels from figure 3.8.

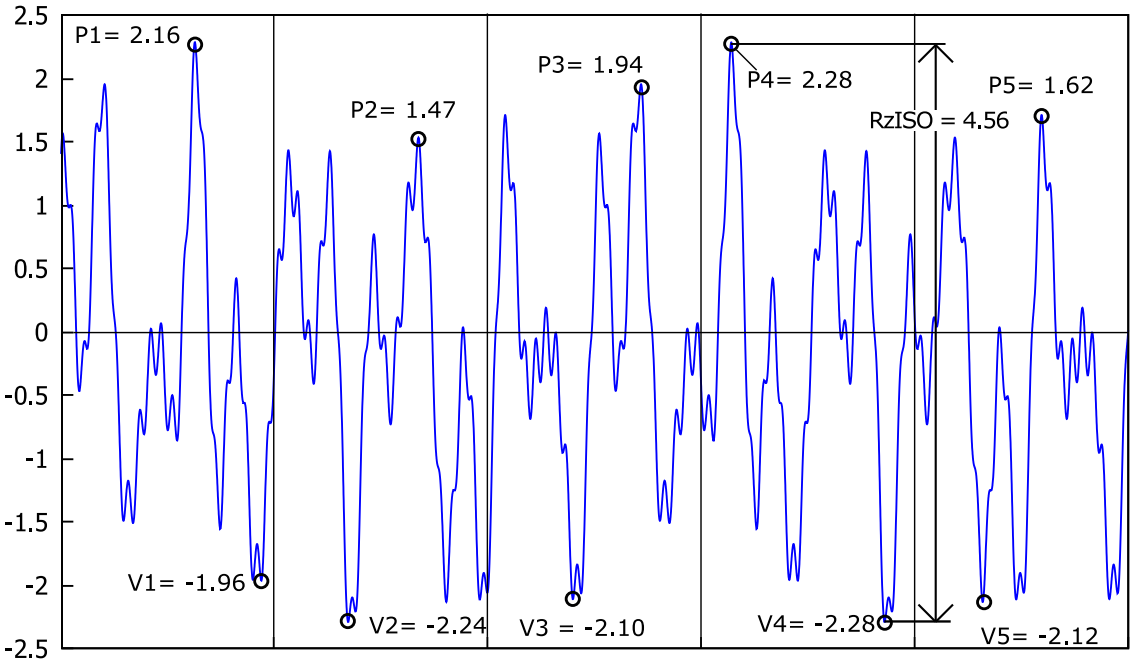


Figure 3.8. Roughness profile Z(x) with labels for Rz calculation.

3.3.3. Roughness unit summary

As described, different roughness units are obtained in different ways and carry different information. It is difficult to describe a three-dimensional surface accurately with single parameter thus multiple units have been defined for different purposes. IPC-TM-650 2.2.17A is a a test method specification for surface roughness measurement using a profilometer with a diamond stylus. The test method specification instructs to use Ra to evaluate *"The surface finish or roughness of foils"* while Rz shall be used to evaluate *"foil profile"* [30]. In summary Ra offers an overview of the surface and Rz reveals possible speaks in the surface profile. Roughness can be also measured accurately with optical non-contact measurement equipment. Table 3.5 summarizes key features of each roughness unit.

Table 3.5 Differences and use-cases of surface roughness units.

Unit	Describes	Used for
Ra	Average profile height. Returns lower value than Rq	Copper foil Untreated side roughness in material data sheets [46]
Rq/Rrms	Root mean square value of average profile height	Available occasionally in data sheets
Rz	Profile's average peak-to-valley height. Different definitions exist for Rz	Typically used to report treated side roughness after treatment [46]

As mentioned in section 2.3.3 copper foil surface roughness contributes to conductor losses. Rougher surface causes bigger losses. IPC 4562A standard specifies copper foil roughness pro-

files as shown in table 3.6 [47]. The roughness values specified in the standard are required on both sides of the copper foil for each grade. Roughness specifications by IPC are not currently up to the technology requirements [27]. Copper with smoother surfaces than what IPC specifies as Very Low Profile is manufacturable and in demand.

Table 3.6 Copper profiles as defined in IPC 4562A.

Foil Profile	Rz(DIN) µm
S (Standard)	N/A
L (Low Profile)	10.2
V (Very Low Profile)	5.1
X (No Treatment or Roughness)	N/A

Manufacturers have employed their own naming conventions for copper foils. Names that manufacturers use are not consistent across manufacturers and some manufacturer might have considerably smoother VLP copper than some other manufacturer. For example Isola presents some names for different surface roughness levels and respective roughness values which have been replicated in table 3.7 [48]. Isola is only presenting copper tooth heights which should be slightly higher, but relatively close to Rz roughness value of the surface. Rough copper slows propagating high frequency signal down and the lower propagation speed will be perceived as higher Dk [49]. In other words, copper roughness has an effect on dielectric material's effective Dk. Thinner dielectrics are affected more than thick materials [49].

Table 3.7 Copper foil definitions from Isola Group S.a.r.l

Name	Description
DSTF® (Drum Side Treated Foil)	Adhesion treatment is applied to shiny/drum side
RTF (Reverse Treated Foil)	Same as DSTF®
VLP	Very Low Profile Foil with Tooth < 5 Microns
e-VLP/H-VLP	Very Low Profile Foils
STD HTE (Standard Shiny Copper)	Adhesion treatment is applied to matte side

3.4. Solder mask and surface finishes

PCB top and bottom copper surfaces are different than internal copper layers as outer layers only have dielectric substrate material on one side and the outer copper surface if covered with solder mask. There are also different surface finishes and coatings for the copper itself. Solder mask typically has high Df and while Dk can be close to the Dk value of the substrate on the other side of the copper the solder mask thickness may not be too well controlled. Solder mask has an order of magnitude worse dissipation factor and water absorption properties when compared to substrate materials. Where substrate materials can have dissipation factors under 0.005 solder masks have Df in the range of 0.02. Moisture absorption for laminate materials is less than 0.3%, but for solder masks the respective value is 1-2%. Moisture absorbed in the dielectric increases loss tangent and can cause deviations to impedance. Thick solder mask

layer introduces more losses than thin layer. Lack of solder mask is, however always the option that leads to least dielectric losses for surface layers. [50]

Same weight copper foil on surface layers results in thicker final copper thickness than on internal layers as more copper needs to be deposited on the PCB to apply conductive layer to vias and plated holes. This additional deposited copper can have thickness variations, which will in turn cause variations in the etching process. [51]

Top and bottom layers also have an important function as mounting surface for components. The exposed copper areas need to be treated to promote solderability and to protect copper from oxidation. Some surface finishes can be applied to the whole board before solder mask, but it is more common and arguably better to apply surface finish selectively only to exposed copper areas after solder mask. Electronless nickel immersion gold (ENIG) forms a nickel coating to the copper, which increases insertion loss in comparison to bare copper. Hot air solder leveling (HASL) is not usable for high density boards. Immersion tin finish produces smooth surfaces and good press-fit performance. Immersion tin surface is however not very robust before assembly and it is susceptible to development of tin whiskers making it not suitable for fine pitch components. Immersion silver does not increase insertion loss of the interconnect as much as other surface finishes as it has similar conductivity as copper. Silver surface however tarnishes quickly when exposed to air thus the PCB needs to be soldered within a day after removal from storage. [51–53]

4. MITIGATING MATERIAL AND MANUFACTURING IMPERFECTIONS

Different material and design constraints need to be considered and simulated early and as accurately as possible with the available data. However not everything can be easily simulated due to rogue nature of some material properties and tolerances. To obtain accurate and dependable simulation results the input data needs to be correct. Garbage in, garbage out (GIGO) principle holds true in the scope of simulations: if input data to simulator is not correct the output from the simulator will surely not be of any use. Dielectric properties are fairly straight forward to set-up in simulation tools. Thickness, Dk and Df are needed for each dielectric layer. Some simulation tools allow inputting Dk and Df values for specific frequency. Dk, Df and the frequency are then used to create a broadband approximation of the material behavior. Prepreg layer thicknesses need to be estimated if the simulation software does not have prepreg thickness estimation feature. In case dielectric properties have been measured using multiple different test methods some research might be needed in order to select the best value to use. Conductor properties can be trickier to input as manufacturing processes affect conductor thickness, surface texture and final conductor shape. With sufficient understanding on PCB material's key properties and the expected circuit behavior preparing and executing simulations that actually model the intended design is possible and filling in all needed data does not feel overwhelming.

4.1. Fiber weave skew

Skew caused by Dk variations introduced by woven fiberglass structures is called fiber weave skew (FWS). Glass weave skew (GWE), Fiber weave effect (FWE) and glass weave effect (GWE) also refer to the same phenomenon. This phenomenon is hard to simulate or even approximate as the alignment and position of the glass weaves is unknown and varies between panels i.e., bare PCB base materials. Traces running perpendicular to the fiber weave structures i.e., horizontally or vertically relative to the panel always see the same repeating Dk variations. Assuming that the glass bundles run straight of course. Routing differential traces on the same pitch as the glass weave pitch or a multiple of the glass weave pitch should help to reduce Dk variations between traces. As both traces are always roughly above same kind of spot of the periodically repeating weave pattern. If differential pair is routed with some arbitrary pitch and one trace of a differential pair constantly sees resin windows and the other runs directly over a glass bundle the traces will constantly see different Dk values and thus have different signal propagation speeds [54]. Glass bundle position's relation to intra pair skew has been examined practically and it seems that high and low skew measurements do not always correlate to obvious patterns in weave alignment relative to traces [55]. Different propagation speeds within a differential pair will cause intra pair skew. If traces are not perpendicular to the panel but rather routed in a zig-zag pattern or if the whole design is rotated some degrees relative to the production panel fiber weave effect will be reduced to some degree. Figure 4.1 shows how

differential trace separation and angled routing relates to the glass weave in the laminate.

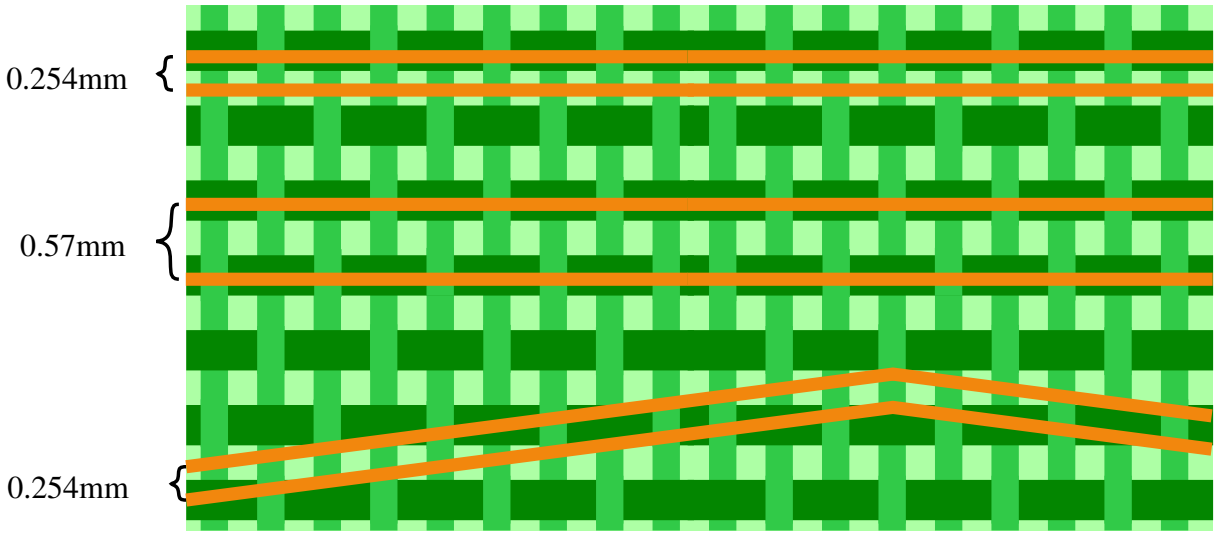
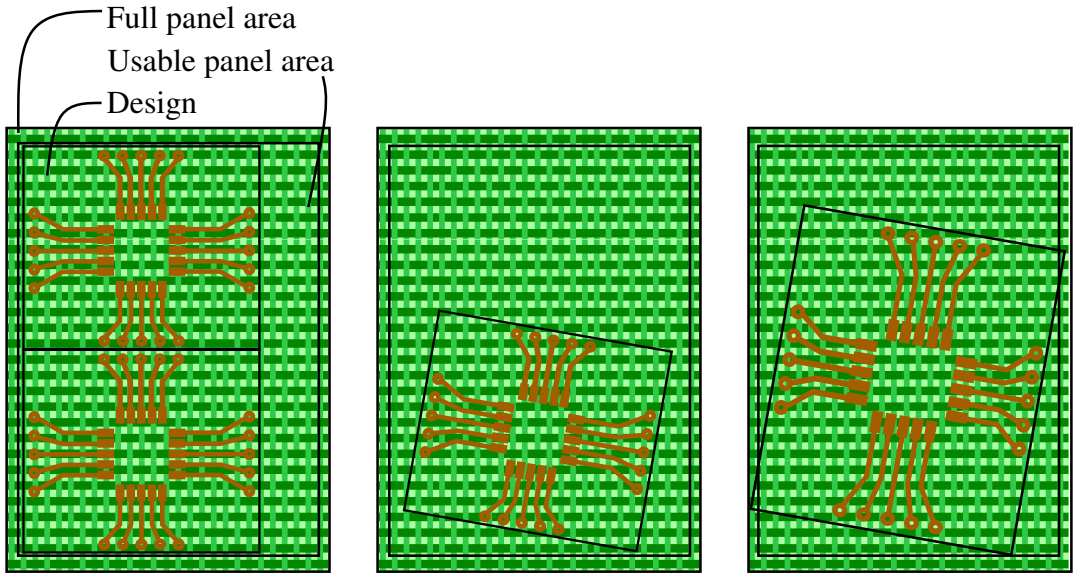


Figure 4.1. Different differential trace configurations on 1080 glass. All traces are 0.1 mm wide and glass weave and traces are drawn roughly to scale. Differential pair with no fiber weave effect considerations on top, same pitch as weave in the middle and zigzag routing on the bottom.

4.1.1. Production panel tilting and zigzag routing

FWE can be reduced effectively by rotating the PCB artwork relative to the manufacturing panel. The principle of PCB artwork rotation is shown in figure 4.2. Ten degrees of rotation has been shown to reduce skew between traces to less than three percent of the skew present with no rotation [55]. 45 Degree rotation was almost as effective as ten-degree rotation [55]. Rotating the entire PCB design is easy and applicable to almost all designs regardless, whether rotating the design was planned initially or not. The major downside of this skew mitigation technique is the added cost: Production panel surface area will be wasted if right angled design is rotated on a production panel. PCB production panel sizes are fixed and, in some cases rotating the design will force the fabricator to use a larger panel. Reduced area use efficiency can also reduce the number of individual PCBs that fit on a panel as shown in figures 4.2 (a) and 4.2 (b). If the design is already as big as the biggest available panel can support rotating the design is no longer an option as it will exceed the usable panel area as shown in figure 4.2 (c). It has been shown that weave can be as much as eight degrees off from the expected position [55]. If PCB design happens to be rotated as much and in the same direction as the weave, rotated design will suffer from higher skew than a design with no rotation on the same panel would.

Zigzag routing aims to achieve same effects as production panel tilting, but without actually tilting the whole design in the panel. Thus, zigzag traces can be used selectively only on traces that need to support high-speed digital signals. Zigzagging traces do reserve more board area but they may allow better use of the available production panel area than production panel tilting. However, the PCB area needed to implement certain function might increase if there is zigzagging high-speed traces are plentiful. Both zigzag routing and production panel tilting should not be used with the same design for obvious reasons: odds are that traces align with the fibers as the mitigation strategies potentially cancel each other partially out.



(a) Design not tilted in the production panel.

(b) Design tilted ten degrees relative to the production panel.

(c) Design that is close to the size of the usable panel dimensions won't fit to the usable panel area when tilted.

Figure 4.2. PCB design tilting relative to production panel. PCB fabricators use certain size panels on which the design needs to fit.

4.1.2. Glass fabric selection

Difference between glass and resin Dk is the underlying mechanism causing skew. Glass has higher Dk than the surrounding resin. Low Dk glass helps to minimize Dk differential between glass and resin, but it does not get entirely rid of FWE. Differences in the mechanical properties of glass and resin cause problems in PCB manufacturing process. Spread glass helps to mitigate unevenness in both electrical and mechanical domains, but not entirely without drawbacks. Spread glass does make the PCB lamination process more difficult as it restricts resin flow. Initially spread glass fabrics were introduced to help minimize tolerances in laser drilling process. Spread glass also helps to mitigate FWE. Multi-ply dielectric (i.e., dielectric layer consisting of more than one glass fiber sheet) is also effective way to reduce FWE with a small increase in PCB cost. Multi-ply dielectric reduces the probability of glass bundle alignment on neighboring glass fiber sheets thus shrinking resin windows while spread glass is flattened eliminating large gaps in the fabric. Both spread glass and multi-ply stack-up have been practically proven to be effective FWE mitigation strategies [56]. [34, 57]

Different resin systems come also with different Df values. Lower Df values yield lower insertion loss in interconnects thus enabling for example use of longer traces. Figure 4.3 shows how dissipation factor affects losses in a stripline transmission line. The simulated Df values range from extremely low Df = 0.003 to solder mask level high Df of 0.02. Each 0.001 increase in dissipation factor seems to increase insertion loss for about the same amount.

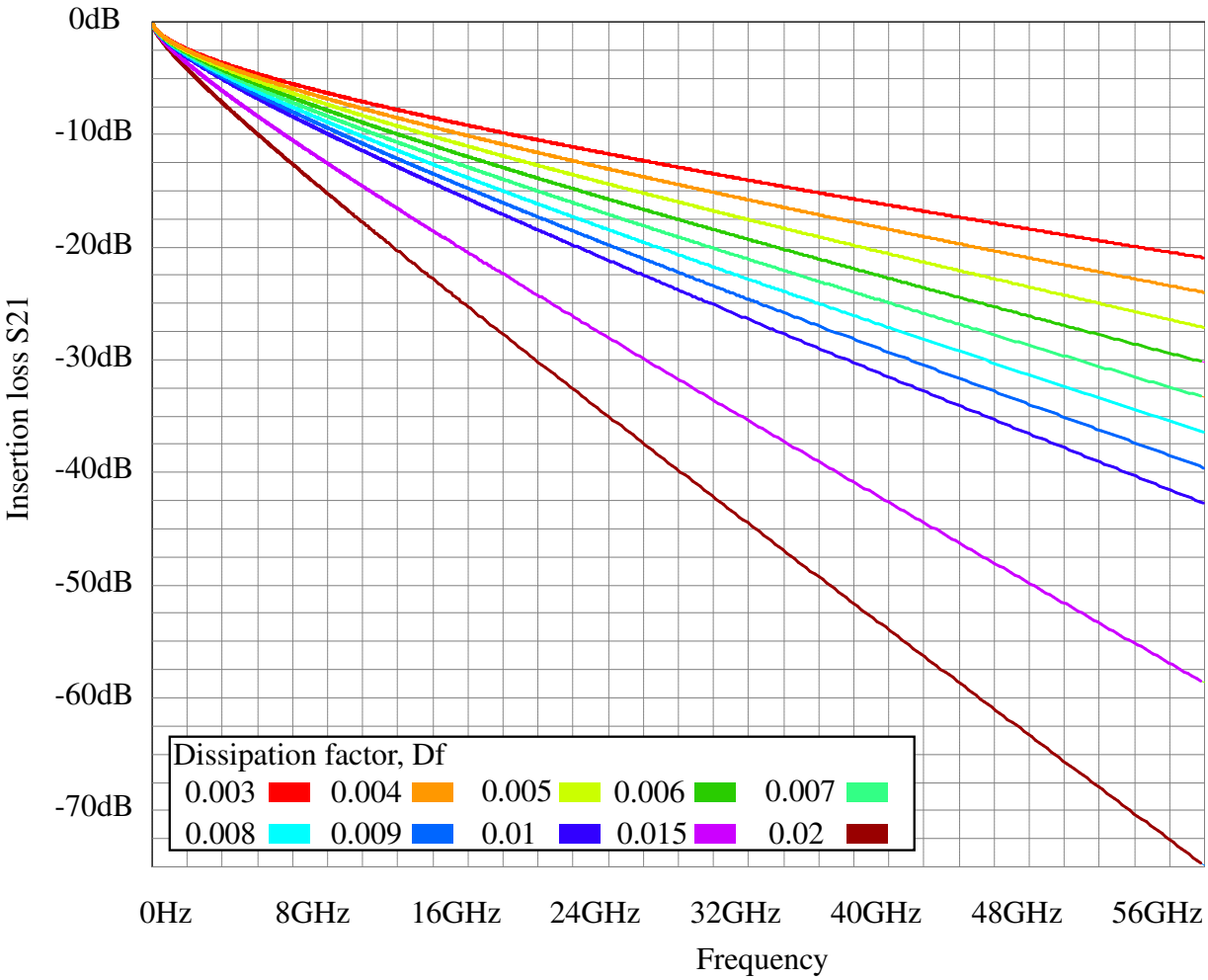


Figure 4.3. Insertion losses for different dissipation factor values. 30 cm asymmetrical 115 μm wide transmission line.

4.1.3. Using wider transmission line traces

Using as wide traces as possible is beneficial from a signal integrity point of view as wider traces cause less losses. Wide traces could also help to even out Dk variations caused by fiber weave effect although little research seem to have been conducted investigating this matter. It could be that for example a 10 μm difference in trace width is rather insignificant when it comes to fiber weave effect as 10 μm is a small distance compared to glass fiber bundle dimensions. However, at some point wider trace should start reducing skew caused by fiber weave effect. If traces are very wide compared to the glass bundles it could be assumed that there is no fiber weave skew. For example on a two layer, 1.6mm thick PCB a 50Ω single-ended trace is relatively wide (approximately 3mm when Dk=4). Finding how trace width affects FWE through practical means of building and measuring test vehicles would be an interesting experiment. Examining fiber weave effect by the means of building and measuring test vehicles is problematic due to the stochastic nature of fiber weave effect, effectively meaning that statistically significant amount of identical test vehicles would need to be built and measured to obtain meaningful results. Needless to say, building and measuring large amounts of test vehicles is expensive both in the terms of time and money.

Wide traces occupy more surface area from the PCB and do not fit in the tightest places such as underneath a high pitch BGA (Ball Grid Array) packages. It was also shown earlier

that when reference planes are further away from the trace EM fields are spread more broadly in the dielectric material, which is not favorable from crosstalk point of view. As discussed earlier, trace width is ultimately constrained by impedance requirements, dielectric constant of the substrate and the thickness of the dielectric layers between trace and its reference planes. While thicker dielectric layers allow wider traces to be used for certain impedance PCB cannot be indefinitely thick due to multiple reasons: Finished PCB is usually enclosed in some kind of mechanics that may constrain the physical dimensions of the PCB. Thermal expansion of the PCB determined by coefficient of thermal expansion (CTE) is additive and the thicker PCBs will thus expand more and experience mechanical strain during for example reflow soldering [23]. Using more material is also likely to add cost to the PCB.

Insertion loss simulation results for five different trace widths are shown in Figure 4.4. All simulated transmission lines are 30 cm long 50 Ω single-ended symmetrical stripline transmission lines. Dissipation factor of 0.006 was used in the simulations and Dk was 3.3. Different dielectric layer thicknesses were employed in order to arrive to the 50 Ω single-ended impedance. Dielectric layer heights and the corresponding trace widths to achieve 50 Ω impedance are shown in figure 4.5. According to the simulation results even a 10 μm increase in trace width yields multiple decibels lower insertion loss on high frequencies with the simulated 30 cm long transmission line.

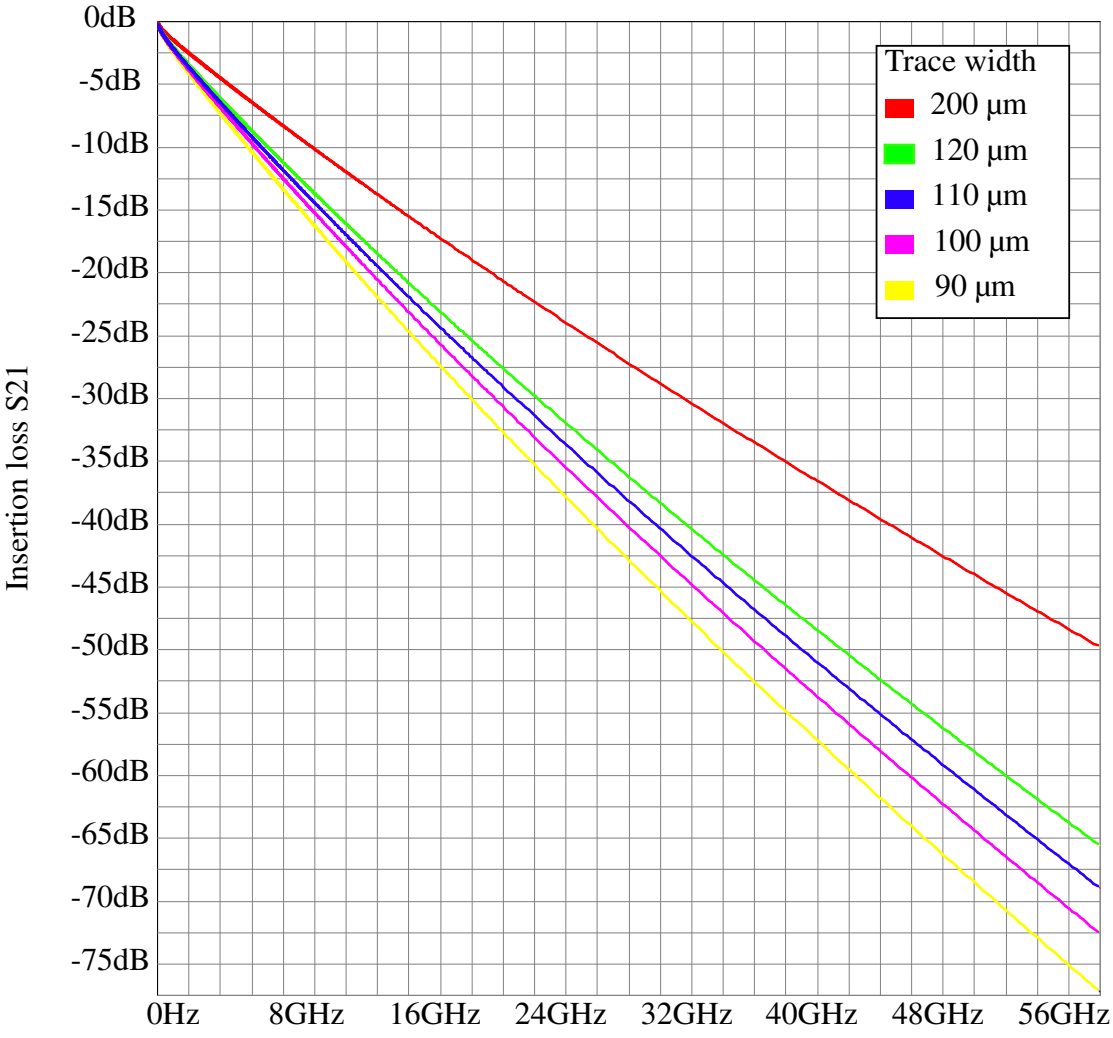


Figure 4.4. Insertion losses for five different conductor widths employed in a 30 cm transmission line.

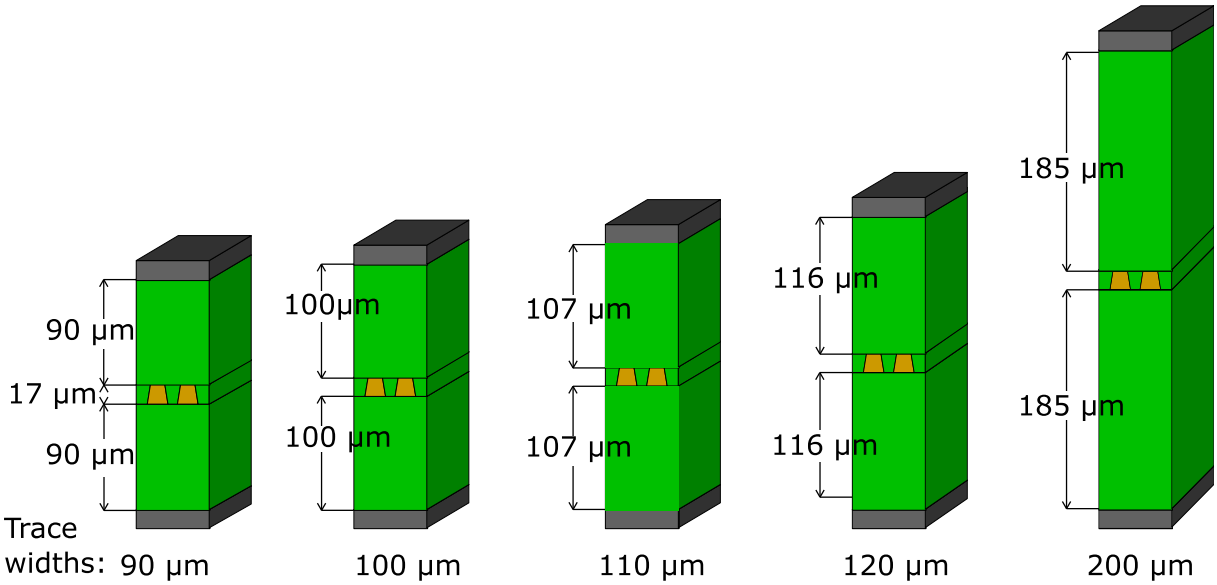


Figure 4.5. Layer heights for the insertion loss simulations presented in figure 4.4.

4.2. Conductor uncertainties

Imperfections and tolerances in the copper layers of a PCB affect the electrical performance as well as the structural rigidity of the PCB. Some of these effects are easier to account for than others. As described earlier wide traces attenuate signals less they can also be more consistently to etched as absolute etching tolerance is determined by the etching process and the tolerance relative to trace width is smaller when traces are wider. Copper roughness and etch factor are described below in better detail. However as a brief summary, etch factor can be queried from the PCB fabricator and accounted for in the design phase while accurate data for copper surface roughness may not be as straight forward to obtain.

4.2.1. Surface roughness

As detailed in chapter 3 copper surface roughness is a rather complex issue to represent with a single figure. Different roughness units describe surface differently and common sense suggests that using the correct roughness units should yield the most accurate results. In other words, roughness data should be obtained and fed to the simulator in format expected by the model used. The limiting factors are the available roughness data and knowledge on which unit to use for each model. HyperLynx for instance does allow to input roughness data in Ra, Rz or Rrms format for all available models and also performs conversions between roughness units with constant coefficients. Rrms can be approximated from Rz by assuming that the profile is triangular with peak-to-valley height of Rz [58]. The RMS height of the profile based on Rz is then

$$R_{rms} = R_z \frac{1}{2\sqrt{3}} \approx R_z \frac{1}{3.46} \tag{19}$$

where R_z is the measured roughness value and R_{rms} is an approximation for root mean square profile height [58]. HyperLynx also performs conversion to and from Ra, but it is unclear how the conversion is done behind the scenes. Table 4.1 presents a few different Rz values and converted Ra and Rrms values. Values for the dummy roughness profile presented in chapter

3 are also presented for comparison. The definition of Rz used by HyperLynx is not explicitly defined, but it is likely that the used definition is RzDIN.

Table 4.1 Converted values from Rz to Ra and Rms in HyperLynx and calculated values for dummy profile.

Hyperlynx				
Rz	Ra	Rz/Ra	Rrms	Rq/Rrms
1	0.23	4.3478	0.289	3.4602
4.04	0.931	4.3394	1.166	3.4648
5	1.152	4.3403	1.443	3.4650
10	2.304	4.3403	2.887	3.4602
Dummy profile from section 3.3.2				
Rz	Ra	Rz/Ra	Rrms	Rq/Rrms
4.04	0.87	4.6437	1.08	3.7407

Actual calculated roughness values from the dummy profile yield Rz/Ra ratio that is in the same order of magnitude as the Rz/Ra ratio produced by HyperLynx conversions. Consequently, HyperLynx would have done an ok job converting the roughness to a different unit in this particular case. How significant impact do the conversion errors have on the simulation results? Error caused by conversions is not likely to be very significant, considering that there are some tolerances also in the roughness measurement techniques. Roughness values can even be expressed as ranges in some foil datasheets [40].

Simulated insertion losses with different surface roughness values for a 115 μm wide, 30 cm long and 17 μm thick trace are presented in figure 4.6. Dissipation factor of the simulated dielectric material was 0.006. Simulation was conducted using Cannonball roughness model. Using Cannonball model is recommended in Siemens HyperLynx SI/PI User Guide. Differences between roughness models are described later in this chapter.

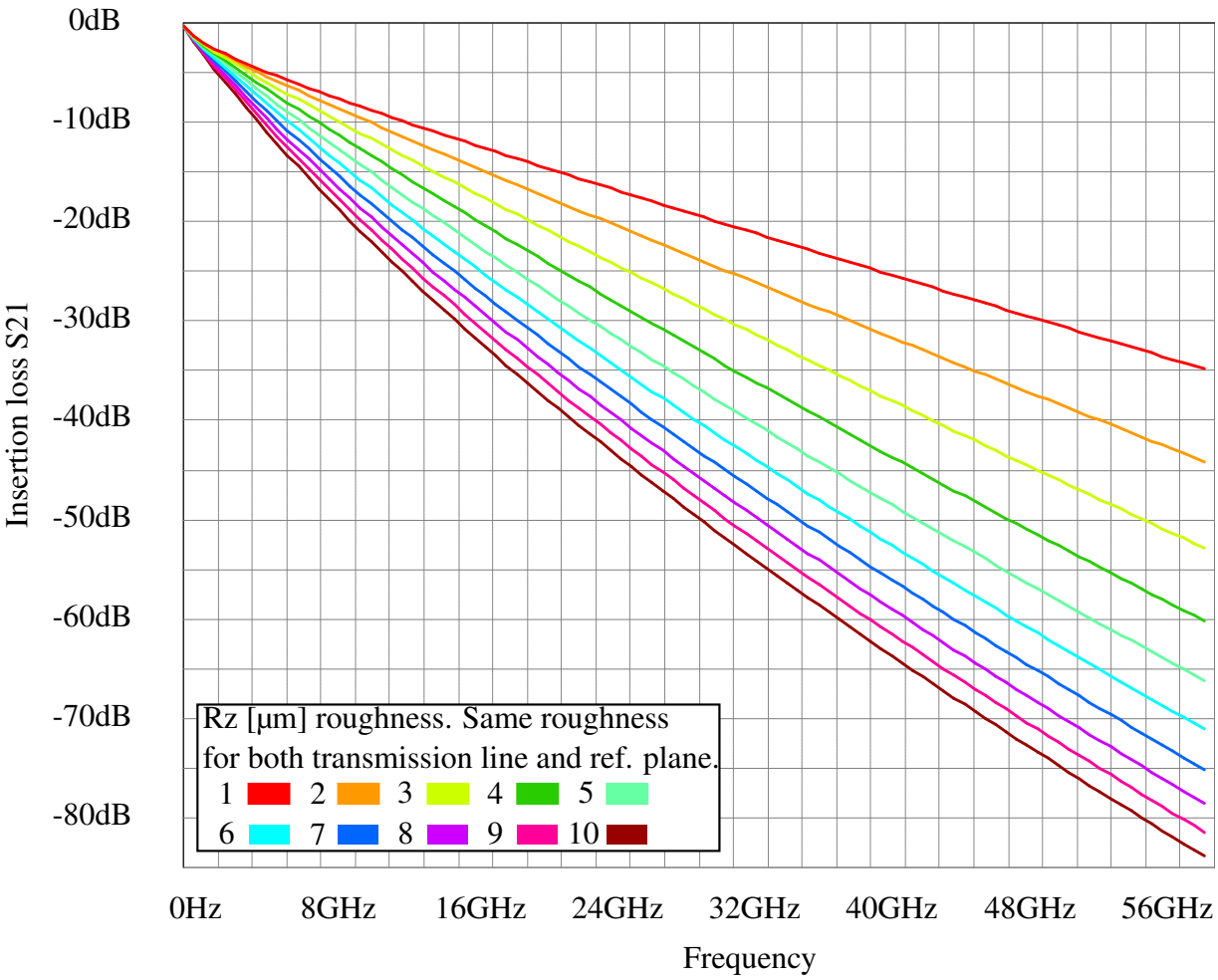


Figure 4.6. Insertion loss simulations with different surface roughness values for a 115 μm stripline trace.

Based on the insertion loss graphs in figure 4.6, roughness does affect insertion loss linearly: Rz roughness was increased in 1 μm increments but losses increase more with smoother surfaces i.e., when relative increase in surface roughness is bigger. It is difficult to point the root cause for this behavior without digging deep into the electromagnetic theory behind signal propagation, which is out of scope of this document. Losses caused by copper surface roughness are however significant and require attention regardless of the surface roughness value.

In reality copper foil surface roughness is different on either side of the foil. In figure 4.7 results for a simulation where the difference between ED and RTF copper was examined in time domain are presented. Chosen Rz roughness values for the simulation were 6.5 μm for the matte side and 4 μm for the shiny side of the foil. RTF foil is bonded to the PCB core material from the shiny side and ED copper from the matte side. If PCB stack-up is constructed so that core substrate is thinner than adjacent prepreg layer, RTF copper can provide an advantage over ED copper as the strongest EM fields are between the smoothest copper surfaces. Figure 4.8 visualizes two stack-ups with identical dielectric layers but one with RTF copper and other with ED copper. The copper surface features have been exaggerated to visualize the difference between the two options. Insertion loss in the simulated situation is somewhat lower for RTF copper than for ED copper which is to be expected based on initial hypothesis and time domain simulations.

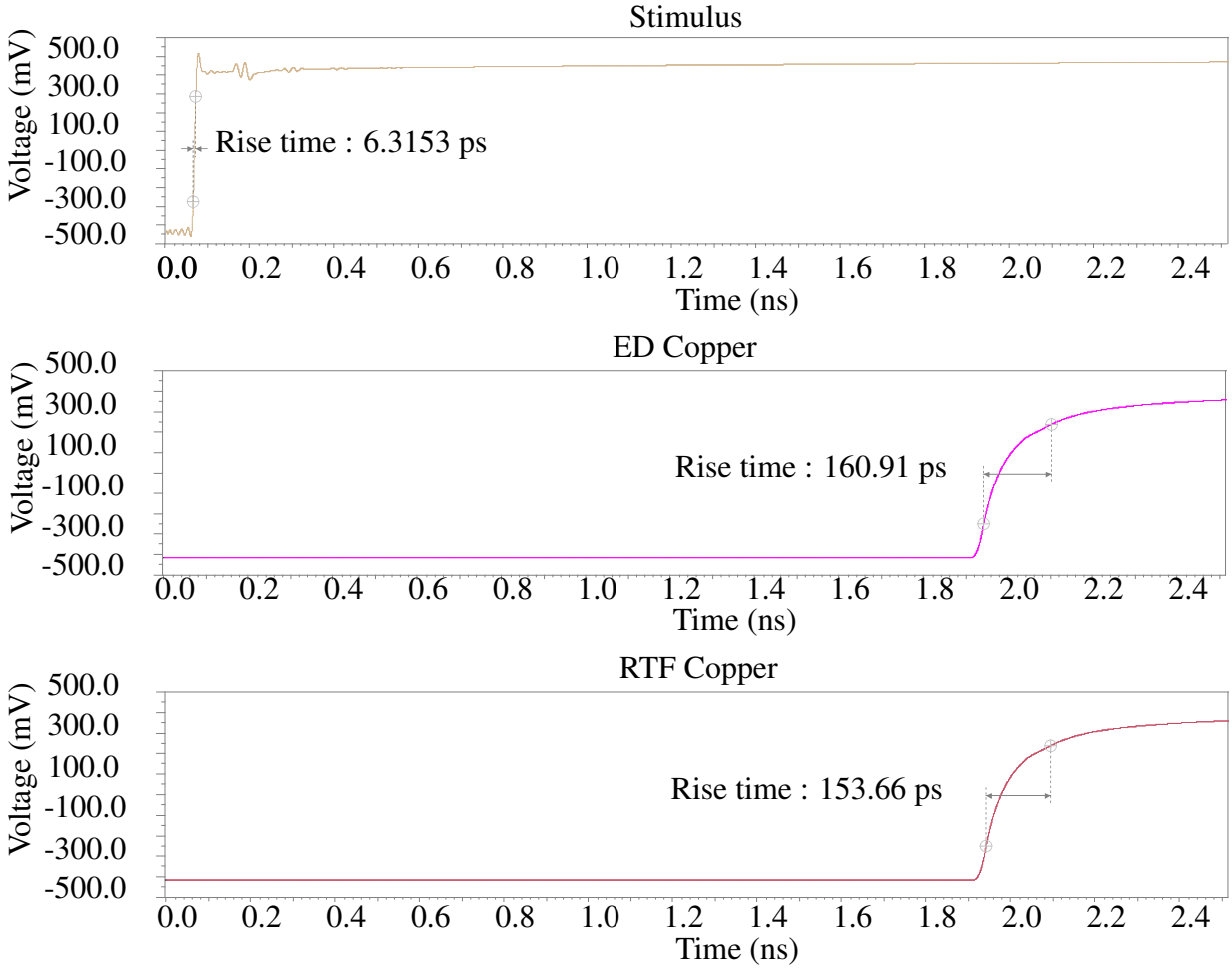


Figure 4.7. With 30 cm transmission line with the stack-ups presented in figure 4.8 the signal rise time (20% to 80%) at the end of the transmission line is about 5% shorter with RTF copper.

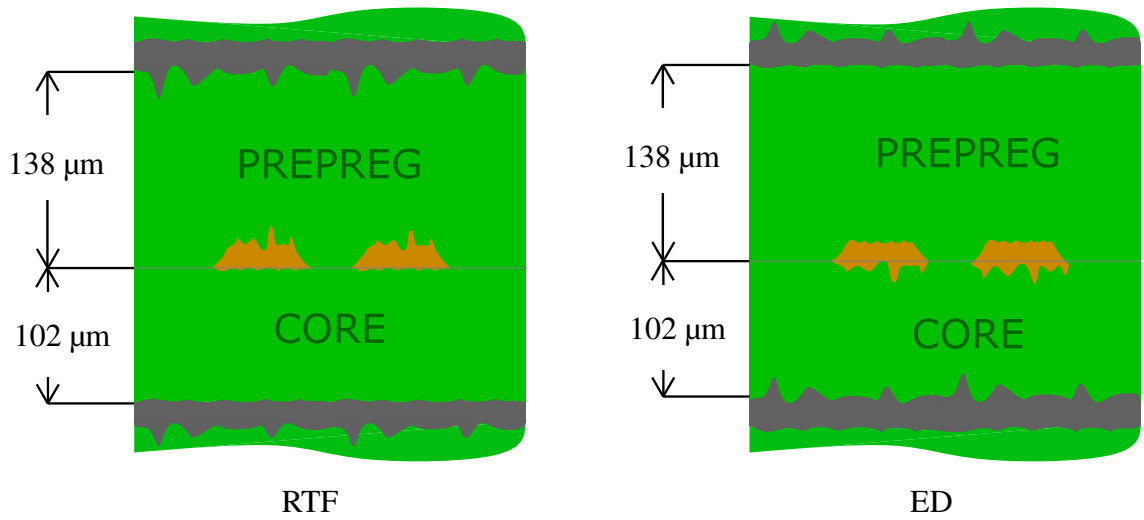


Figure 4.8. PCB stack-ups for comparison between RTF and ED copper. With RTF copper the smoothest available copper surfaces are supporting most of the current. Not drawn to scale.

Simulation results in figure 4.7 confirm that it does matter whether ED copper or RTF copper is used. Terminology used to differentiate between the two sides of copper foil can be unex-

pectedly confusing. Table 4.2 lists and explains a selection of different names that may be used when referring to copper foils. This list is by no means exhaustive as this terminology does not seem to be standardized and thus new terms may pop up anytime. Moreover it is not guaranteed that the listed terms will always be used as listed. Sometimes language barriers make understanding slightly ambiguous terms even more tricky. Copper foil datasheet roughness values may not represent the actual roughness of the same foil when it has been laminated inside a PCB. Various surface treatments meant to promote adhesion also alter the surface geometry. These processes are often manufacturer specific and very little documentation is available regarding their effects.

Table 4.2 Different terms used to differentiate between ED and RTF copper foil sides.

Term	Definition
Shiny side	Smoother side of ED copper. Drum side in the ED copper manufacturing process
Matte side	Rougher side of ED copper. Opposite side of the drum side in the the ED copper manufacturing process
Drum side	Same as shiny side
Treated side	The side of the copper foil that is attached to the PCB core substrate. For RTF copper this is the Shiny side.
Untreated side side	The side that is not facing the PCB core substrate i.e., this side is attached to the prepreg layer.
Bonding side	Same as treated side.
Resist side	Same as untreated side
Dielectric side	Same as treated side
Top side	Same as untreated side

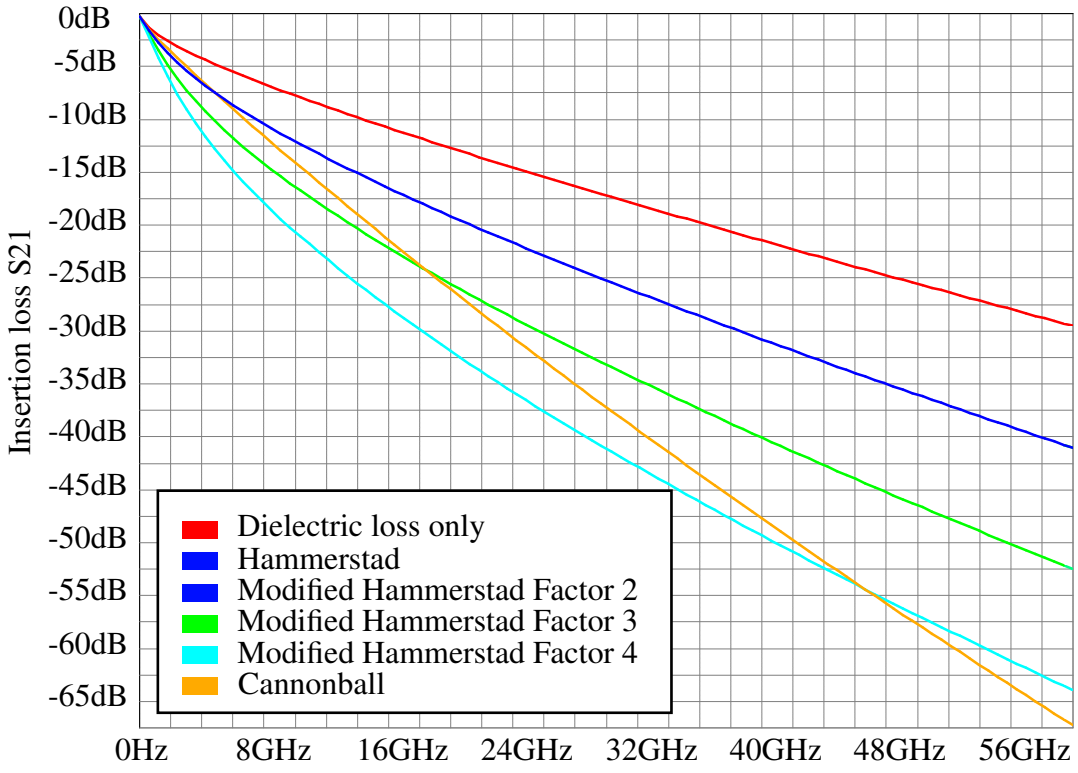
Modelling copper surface roughness takes things a step further as there are multiple models that aim to model copper's impact to high frequency signals. Modelling complex and relatively random geometries effectively and accurately based on one numerical parameter is no trivial task. Different roughness models have been listed and described superficially in table 4.3.

Table 4.3 Most common copper roughness models and their features.

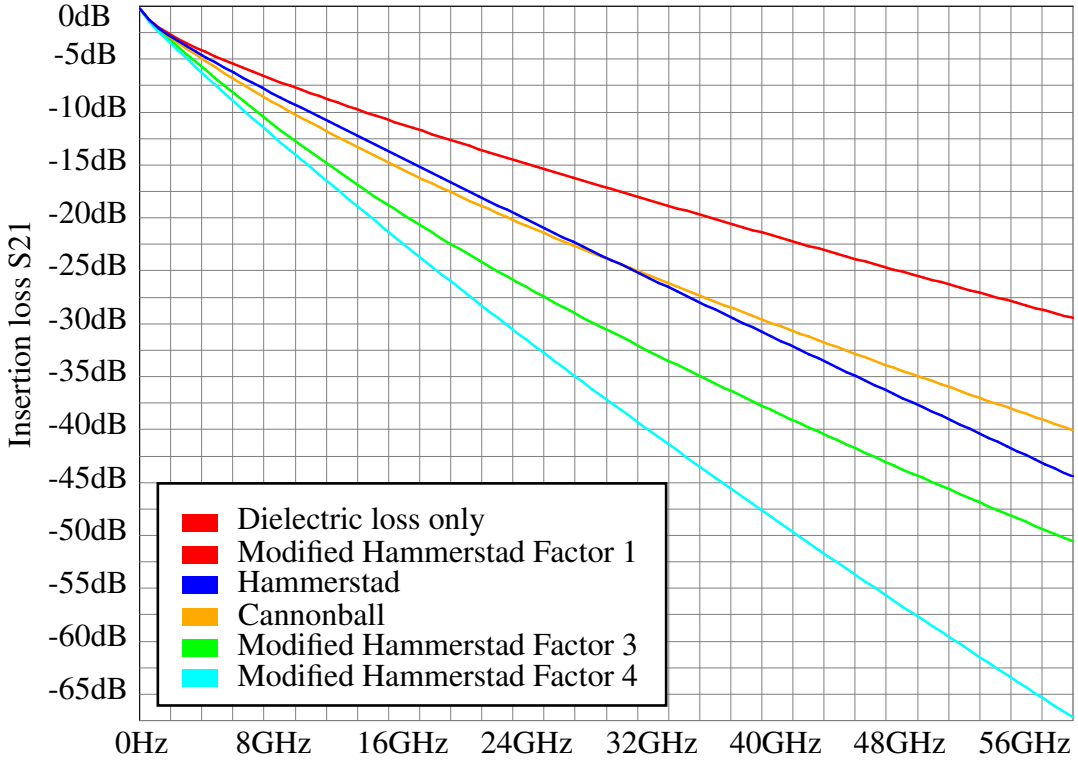
Model name	Features and limitations
Hammerstad model	Works on smooth surfaces (2 μm RMS roughness) on frequencies below 15 GHz
Modified Hammerstad	Suitable for high speed design. Needs RMS roughness value as well as scaling factor. Scale factor is usually not easily available. [59]
Hemispherical model	Uses random hemispherical protrusion to approximate surface roughness, works at least up to 30 GHz [60]. Not available in HyperLynx.
Huray snowball model	Accurate model that models the surface as stacked spheres uses three parameters to define the surface [58, 59]. Obtaining all needed parameters can be difficult. Not available in HyperLynx.
Cannonball model	Similar to snowball model, but needs only Rz roughness value to model losses [58]. Good for high speed digital design.

Differences between different copper surface roughness models have been examined through simulations shown in figure 4.9. Different models behave in diverse ways with different surface roughness input values. For the insertion losses in figure 4.9 (a) surface roughness value of $Rz = 5.1\,\mu m$ was used for all copper layers. Copper with Rz roughness of $5.1\,\mu m$ or less on both sides qualifies as Very Low Profile per IPC 4562A Metal Foil for Printed Board Applications -standard. See table 3.6. As can be seen from the simulation results, different models return significantly different losses with basically same input data. It is clear that some of the obtained results are closer to the reality than others. Loss modelled with Cannonball model is probably closest to the real losses as Cannonball model has been optimized for modelling losses based on single roughness value. Modified Hammerstad model can likely be tweaked to match reality relatively well if enough data about the copper surface is available. The original Hammerstad model is not able to model losses accurately on high frequencies. The accuracy of various roughness models has not been verified with measurements in this thesis.

In figure 4.9 (b) surface roughness is reduced to relatively smooth but still realistic Rz value of $2\,\mu m$. With copper roughness less than half of the first simulation Hammerstad and modified Hammerstad models return remarkably similar results as before where cannonball model returns significantly lower losses. Hammerstad models expect Rrms roughness as input and HyperLynx likely converts the Rz value to Rrms before inputting it to the model. Converted values are however not a big problem here as the simulations aim only to explore how models behave with different yet realistic inputs that could be available in a material datasheet. Using the same conversion coefficients as HyperLynx following Rz to Rrms conversions can be done: $Rz = 2\,\mu m \Rightarrow Rrms = 0.577\,\mu m$ and $Rz = 5.1\,\mu m \Rightarrow Rrms = 1.472\,\mu m$. Cannonball roughness model seems like the best choice for estimating losses caused by copper surface roughness especially if copper surface roughness is presented with one value in material datasheet.



(a) Different models return very different results. $Rz = 5.1\,\mu m$ on all copper surfaces.



(b) Smoother ($Rz = 2\,\mu m$) copper roughness changes loss estimations on low frequencies on all models. On higher frequencies Cannonball model shows the biggest differences in comparison to insertion losses in figure 4.9 (a).

Figure 4.9. Insertion loss simulation results simulated with HyperLynx where 30cm asymmetrical stripline transmission lines with different roughness models was simulated.

4.2.2. Etch factor

Etch factor is an unwanted manufacturing artifact that causes etched traces to have trapezoidal shape. The origin of etch factor was explained in section 3.3.1. Designed trace width is actually the width of the bottom side of the trace i.e., the width in the copper-substrate interface or W2 if labels from figure 2.1 are used. Etch factor impacts primarily trace impedance, however, bigger etch factor does also increase losses in the interconnect [61]. Table 4.4 lists how etch factor impacts impedance with different trace widths. Impact on losses is simulated in figure 4.10. Conductor roughness has been taken into account in using the Cannonball model and Rz roughness value of 5.1 μm

Table 4.4 Trace impedances for different etch factors, calculated in Siemens HyperLynx. Stack-ups are same as in figure 4.5

Etch factor	90 μm trace impedance	120 μm trace impedance	200 μm trace impedance
0 (Square)	48.7 Ω	48.9 Ω	49.3 Ω
0.2	49.2 Ω	49.3 Ω	49.5 Ω
0.4	49.6 Ω	49.6 Ω	49.7 Ω
0.6	49.9 Ω	49.9 Ω	49.9 Ω
0.8	50.3 Ω	50.1 Ω	50 Ω
1	50.6 Ω	50.4 Ω	50.2 Ω

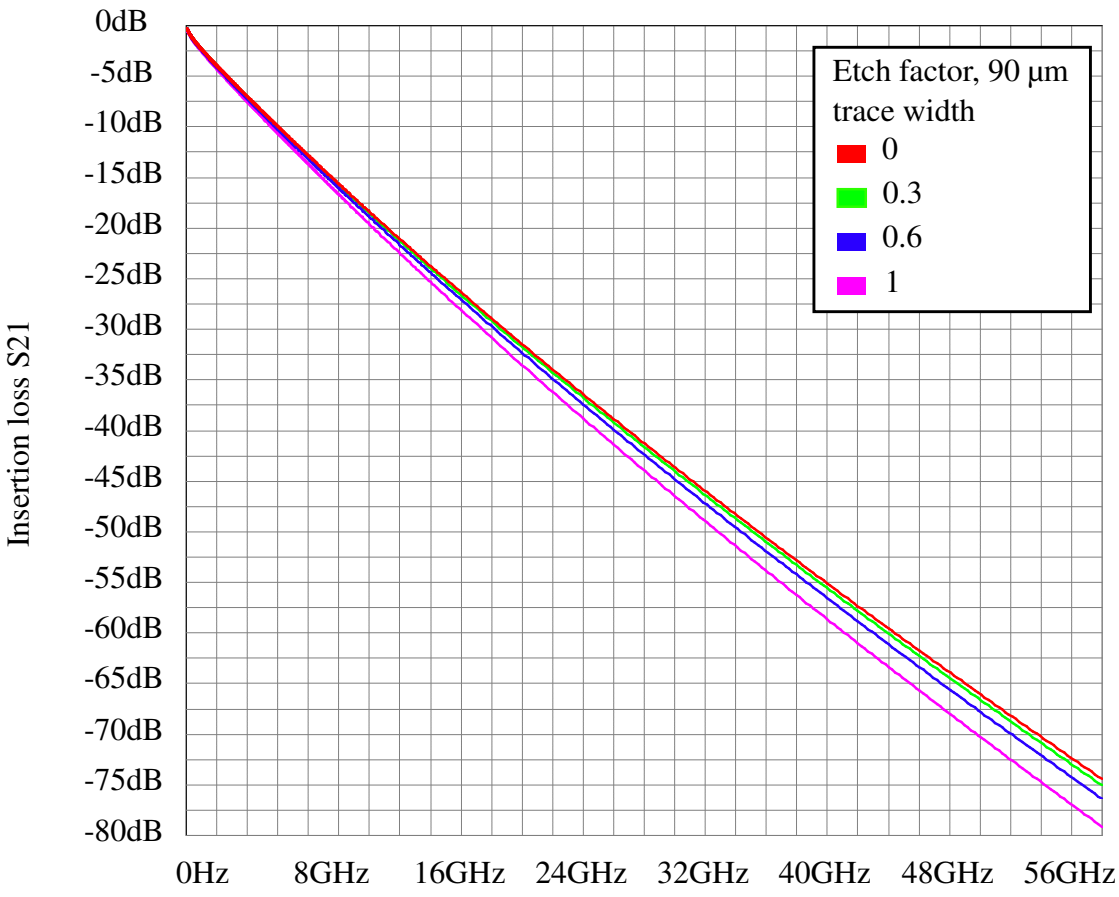


Figure 4.10. Conductor width in the simulation was 90 μm. Differences in loss caused by etch factor are relatively small.

4.3. Combined effects

Different loss mechanisms have been mostly examined separately in this thesis, however, in real applications losses in interconnects are always a combination of multiple factors. Figure 4.11 tries to fit every major factor contributing to interconnect loss to one figure in order to visualize how different factors relate to each other. Three different vertical axes are used to support values in three different units.

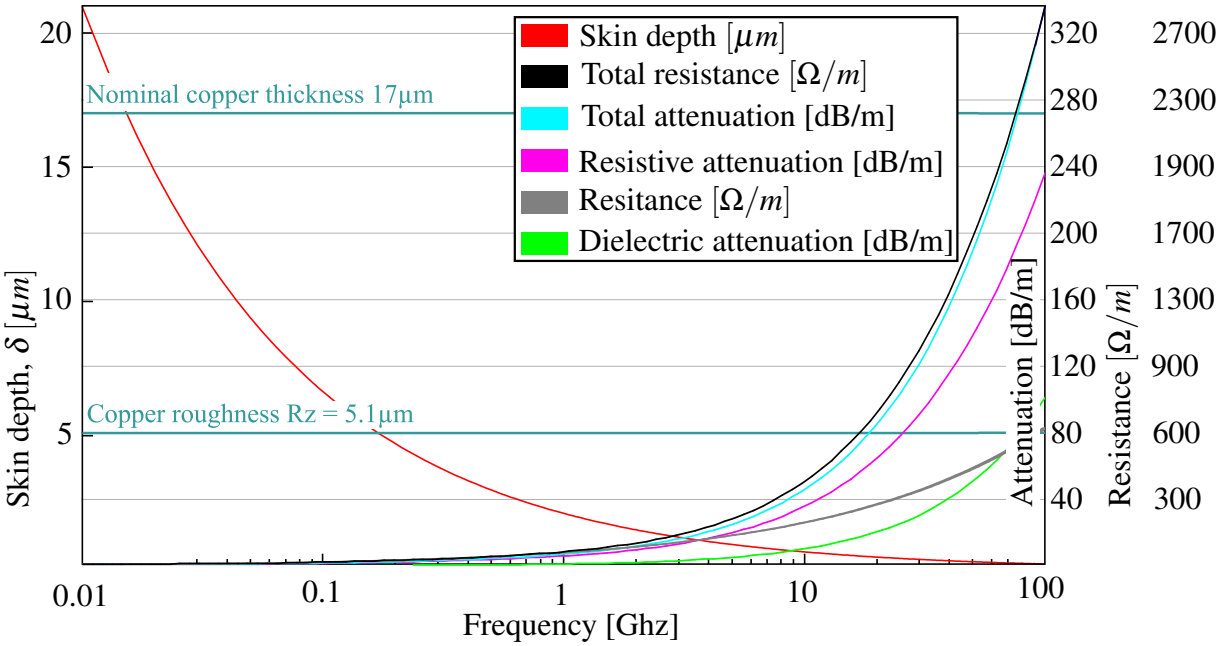


Figure 4.11. All major factors contributing to transmission line losses packed into one graph.

Red skin depth graph uses the leftmost Y-axis. Copper thickness and roughness, that have been used in the simulation have also been included in figure 4.11 for reference. Rightmost Y-axis has resistance per length as unit and it is used by gray and black resistance graphs. Gray graph is the apparent resistance of the interconnect with copper roughness not taken into account and black, total resistance graph represents the apparent series resistance with copper roughness effects taken into account. Green, purple, and turquoise graphs are attenuation graphs that summarize how varied factors translate to signal attenuation. Skin depth shrinks below copper thickness on relatively low frequencies and also below the surface roughness before frequency is even one gigahertz. Losses do however not start increasing instantly as skin depth goes below copper thickness but rather at much higher frequencies. Skin depth and resistance (without roughness) graphs would look very similar in shape only mirrored if they had comparably scaled Y-axes, which is to be expected. Resistance of a conductor can be calculated with

$$R = \rho \frac{l}{A} = \rho \frac{l}{wT} \tag{20}$$

where R is the resistance of the conductor, ρ is the resistivity of the conductor material, l is conductor length and A is the cross-sectional area of the conductor [4]. Conductor area is the product of conductor width w and conductor thickness T. On high frequencies, while skin depth is below conductor thickness $T = \delta$. By substituting resistivity of copper $1.58 \cdot 10^{-6} \Omega \cdot m$ and conductor area to the equation 20 conductor resistance per length can be calculated. For

$17\,\mu m$ thick, $115\,\mu m$ wide copper trace resistance per length is $0.08\Omega/cm$. On 1GHz skin depth is $2.1\,\mu m$ and resistance per length consequently $0.65\Omega/cm$. While resistance does increase substantially with frequency, it is still relatively low and given the fact that currents flowing in high-speed digital interconnects are small, power dissipated in the conductor resistance stays low. Moreover the energy of a signal is in the electromagnetic fields propagating in the dielectric material rather than in the conductor, which probably contributes to the fact that losses do not soar up notably when skin depth goes below conductor thickness or roughness.

4.4. Summary of loss and skew mitigation strategies

Various tricks to manage signal integrity problems caused by losses and fiber weave skew have been summarized in tables 4.5 and 4.6. Moreover, appendix 1 presents a fishbone diagram that summarizes different factors that may contribute to signal integrity problems on PCB.

Table 4.5 Summary of tricks that can be helpful when minimizing losses PCB.

Design choice	Effect
Low loss materials	Dielectric loss affects every interconnect on PCB and the lower the dielectric material's dissipation factor is the lower are also the losses on the PCB.
Smooth copper	Smooth copper attenuates signals less than rough copper, thus using smoother copper will make interconnects on the PCB less lossy i.e., better. Rz Roughness below $5.1\,\mu m$ is considered very low profile in the IPC 4562A standard, however copper smoother than this is available and beneficial in high-speed digital applications.
Wide PCB traces	Wider traces reduce conductor losses. Trace width is determined by Dk of the PCB substrate, dielectric thickness and required trace impedance. Lower Dk and thicker dielectric allow making traces wider for certain target impedance.
Short PCB traces	Attenuation increases with trace length, thus the shorter traces attenuate signals less than longer otherwise similar traces.
Uniform impedance	Impedance discontinuities cause reflections and increase the insertion loss of the interconnect. Uniform impedance enables the circuit board materials to perform their best.

Low etch factor	Etch factor closer to 0 means more square trace. More square traces allow more accurate impedance control. Low etch factor traces are also slightly less lossy than traces with higher etch factor. See figure 4.10.
RTF Copper	Reverse treat foil can provide smoother copper surfaces for a transmission line and the reference plane closest to it and thus reduce losses caused by copper roughness.

Table 4.6 Summary of tricks that can be helpful when minimizing fiber weave skew on PCB.

Design choice	Effect
Spread glass fabric	Glass and resin have different Dk values. Spread glass fabric as PCB substrate material shrinks the resin-only area in the substrate thus resulting in more even Dk and consequently more constant propagation speed and transmission line impedance.
ZigZag Routing	Routing differential traces in ZigZag pattern makes sure that both differential conductors see approximately the same amount of resin windows and glass bundles. Effectively minimizing the overall Dk differences between the two differential conductors and by that lowering the amount of differential skew.
Production panel tilting	Production panel tilting has the same goal as ZigZag routing, but this skew mitigation strategy can be applied after the PCB design has been finished.
Wide PCB traces	Wide PCB traces should average out the glass to resin variations of the substrate material.
Short PCB traces	Shorter traces allow less fiber weave skew to appear. Amount of fiber weave skew is, however not directly proportional to trace length.
Glass weave pitch as differential pair trace separation	When differential traces are routed on the same pitch as the glass weave blow and/or above the transmission line, both halves of the differential pair should be roughly over same kind of spot of the dielectric material.

5. DISCUSSION

The goal of this thesis was to explore how fiber weave effect and copper roughness affect interconnects on PCB among other factors and how to best simulate and mitigate their signal quality degrading effects. The focus was on high-speed digital signaling and how a PCB designer can make sure that the finished PCB performs adequately, with cost-effective materials and manufacturing processes. A practical design guidance document targeted for PCB designers will be created based on this thesis work. The design guidance will present key points of this thesis in a condensed manner. Multiple books, application notes, blog posts etc. have been written on different electronics product design phases. This thesis is not a replacement for any prior publication, but rather a summary of key signal integrity factors that affect PCB design with a closer look to fiber weave skew and copper roughness. While plenty of existing publications do provide very comprehensive data on some parts of the design cycle very little literature has been published from similar point of view as this thesis. There are plenty of factors and variables that have not been discussed in this thesis, moreover the matters covered in this thesis are by no means examined exhaustively. For example, connectors, cables, component packages, layer transitions etc. have not been considered to keep subject manageable and to keep content in this supporting the original research topic.

Fiber weave skew and copper roughness were the two key topics in this thesis. Rising digital data transmission speeds mean that interconnects on PCBs need to have more usable bandwidth than before. Skew budget gets also smaller as data transmission speeds increase. Increased bandwidth and reduced skew tolerance have made fiber weave effect and copper roughness relevant issues thus up to date overview of both issues was needed. A great deal of underlying theory needed to be covered before these two effects and involved tradeoffs could be discussed credibly. PCB design is a balancing act between multiple things and describing only a couple of factors while overlooking other affected variables would give a deceiving picture of the actual state of matters. Fiber weave skew and copper roughness are easy to understand on concept level: more uniform dielectric material equals more uniform transmission lines and rougher surface attenuates signals more than smooth surface. It is also evident that rough copper is easier to attach to dielectric material than very smooth copper. What makes these two issues tricky to manage is the fact that the root causes for both phenomena are hidden inside the PCB. Out of sight, out of mind is however not the way to go here.

Simulations for this thesis work were conducted exclusively in Siemens HyperLynx, which is a well-equipped and relatively easy to use simulation tool. The use of other simulation tools was considered but due to time constraints no other simulator was used to obtain simulation results. Performing equal simulations in different tools could reveal possible modelling differences or other variations between tools. All simulations were conducted in pre-layout simulation environment using generic driver and receiver models built into the simulation tool. The used simulation setup has a lot of abstraction compared to a fully-fledged 3D EM simulation extracted from a real PCB design. Nevertheless, the conducted simulations should serve their purpose in this thesis providing insight on what kind of behavior each parameter is expected

to cause. Differences between copper roughness models were also examined from models' end user's perspective. Cannonball model was deemed as the most useful model for general use as other models are harder to properly use with commonly available material data. Copper surface roughness units turned out to be way more complicated issue than one probably would initially have thought. This thesis does however do a reasonable job in explaining the most relevant surface roughness units for PCB design and thus should help with understanding and simulating copper roughness effects better. Overall, copper roughness was shown to be a rather complex issue with significant signal attenuating potential on multi-gigahertz frequencies. However signal attenuation caused by copper roughness can be mitigated to some extent with better materials and thought-out design choices such as wider traces and clever use of ED copper's two differently rough surfaces.

Lack of well-established simulation model for fiber weave effect makes it difficult to examine fiber weave skew through simulations. While fiber weave simulation models have been developed and verified to be representative of a certain real glass cloth, these models only represent the conditions they are developed and verified for. Developing and publishing an accurate general purpose FWE simulation model is a difficult task that is yet to be done. FWE can be relatively effectively mitigated with the strategies presented earlier in this thesis and thus not being able to accurately simulate it does not mean that it is impossible to design a working interconnect. Designer needs to keep in mind and account for all of the influencing factors, select materials and design the board in a way that is likely to meet and preferably exceed the performance demanded by the technology used to transmit data on the PCB. With an estimation of the total intra pair skew in a differential pair bit error and symbol error simulations can be conducted by specifying skew directly in simulations. Estimating FWE in simulation by specifying transmission line segments with different dielectric parameters is possible but for a simulation to be useful it should closely represent real world. How well this kind of model would represent real world is not a trivial thing to verify. However, such models have been defined and proven representative of real world [62].

Various skew mitigation strategies were presented in this thesis, all of which are suitable for different applications. Routing differential pairs on the same pitch as the glass weave may not be possible in some designs due to component package pitches, other space constraints or due to some other reasons. However, in the same design zigzag routing or production panel tilting may be possible. PCB designs can vary so widely that it is not possible to name one single skew mitigation strategy that would yield best possible results in every application. Zigzag routing will always consume some additional surface area and makes traces longer. More used area increases costs while longer traces increase losses, neither of which are desired side effects. In some circumstances it could be possible to optimize PCB shape for tilted orientation in the production panel in a way that would minimize wasted material yet still allow the design to make use of the advantages of the tilted orientation. Wasted material does not only add cost to the production process, but also creates unnecessary waste that needs to be processed in a responsible manner.

Plenty of references used compose this thesis were sponsored or published by some commercial party. With commercially financed publications it should be always considered whether a publication is objective or driven by commercial interests. Cited commercially financed references were from design tool vendors, PCB manufacturers and material suppliers all of which have different interests and point of views and thus their publications hopefully supplement each other. When technology development is rapid information printed in books always reflect a past state of the art from when the book was initially written. However even if signal speeds

increase and materials evolve the fundamental underlying principles stay the same.

How to implement state of the art technology with currently available tools and materials? A simple question that is very difficult to answer conclusively. The technical details provided in this thesis will in any case help to look for the correct things and simulate with higher confidence. This thesis will be most useful for new designers and anyone finding it difficult to make sense out of all different parameters, test methods etc. present in material datasheets and simulation software. The content of this thesis should also help to gain understanding on where some PCB manufacturing constraints originate from.

6. SUMMARY

This thesis has covered how interconnects on printed circuit boards are affected by several factors ranging from material features to design choices. Special attention has been paid on how copper roughness and inhomogeneity in the printed circuit board's dielectric material affect interconnect performance. Relevant theory and material concepts have been introduced prior going into the details of primary focus areas. The ultimate aim was to provide an analysis on what needs to be considered and how much different things affect high-speed digital design from manufacturing, materials and signal-integrity viewpoints.

Theory supporting high-speed digital transmission lines and key signal-integrity concepts were introduced first to supply basic knowledge. This was to allow also readers with scantier basic knowledge on the field of PCB design to grasp advanced concepts that have been presented in the thesis. The general structure of printed circuit boards and glass fiber based printed circuit board materials has been described in detail. Material features and their impacts for manufacturing and interconnect performance have been inspected. Diverse ways to indicate copper foil surface roughness have been described exhaustively to clear out any confusion that has existed between and within these surface roughness measures. A few common material test methods have also been described as proper material datasheets specify the test methods used to obtain values presented on the datasheet. Dissimilar test methods can output values that cannot be compared even if they describe the same property and are in same unit.

Finally, the actual effects of varied materials, design choices and manufacturing imperfections have been examined and explained through simulations and literature. Ways to overcome various signal integrity impairing phenomena have been proposed and demonstrated. While there are no new discoveries among the results, this thesis manages to gather relevant information from different fields and make it more practical thus filling a void that has existed in the design documentation space. Insertion loss simulations have mainly been used to inspect how much different frequencies are attenuated due to various factors. Five copper roughness models have been introduced and compared superficially without going into the mathematics behind the models. Copper roughness was found to have a significant signal attenuating effect, that can be mitigated to some degree with design choices. Major differences were shown to exist between simulation results obtained using different copper surface roughness models with same input parameters. Cannonball model was shown to output results that best reflect changes in the available input parameters. Dielectric loss was shown to be easier to predict than copper roughness, however fiber weave skew originating from the dielectric material's inhomogeneous internal structure was found to be currently one of the hardest signal integrity related phenomena on PCB to simulate.

Mitigation strategies for effects caused by copper roughness and fiber weave structures were presented. Using as wide traces as feasible is reduces both for fiber weave effect and copper roughness loss. Zigzag routing on the other hand can be useful for skew mitigation, but zigzagging traces are longer than straight PCB traces thus introducing more conductor and dielectric loss in the interconnect. Tilting a rectangular design in the production panel does not increase

losses as the conductor lengths stay the same but it wastes more material than same design in straight orientation. For a design to be cost effective and efficient need for some skew mitigation approach, smoother copper etc. needs to be evaluated and estimated on design-by-design basis based on data rates, signal rise times, interconnect lengths and other relevant factors. Accurate simulations and awareness of the plethora of signal integrity factors affecting PCBs make it possible to design PCBs that that can deliver good high-speed digital performance.

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APPENDICES

Appendix 1. Fishbone diagram about signal integrity on PCB

Appendix 1. Fishbone diagram about Signal integrity problems on PCB