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Optimization of CMOS at Deep Cryogenic Temperatures

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OPTIMIZATION OF CMOS AT DEEP CRYOGENIC TEMPERATURES

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OPTIMIZATION OF CMOS
AT DEEP CRYOGENIC TEMPERATURES

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ABSTRACT

OPTIMIZATION OF CMOS AT DEEP CRYOGENIC TEMPERATURES

by Prabjot Kaur Dhillon

Cryogenic CMOS is a sought-out technology because of its applications to fields like quantum computing and deep space exploration. Though slight advancements have been made within the field of cryogenic CMOS technology, there persists critical challenges that need to resolve to further advance the field. Hence, there is a need to solve challenges like understanding the undesirable effects due to the device physics at cryogenic temperatures such as high threshold voltage, kink-effects, abnormal subthreshold swing etc. and developing reliable circuit models because many rely on analytical modeling. The research models a NMOS ON-current and subthreshold slope at temperatures of 300K and 4K using Technology Computer-Aided Design (TCAD) by applying a single set of calibrated parameters. Additionally, detailing a proposed trap distribution model to reproduce abnormal subthreshold slope observed from 4K to 300K. The research also achieves to introduce an electron and hole mobility model for a wide temperature range since there has not been a unified model developed for silicon carriers from 4K to 300K. Lastly, the research aims to optimize MOSFETs at deep cryogenic temperatures by applying the calibrated parameters.

ACKNOWLEDGMENTS

Firstly, I would like to thank Professor Wong for his guidance and mentorship throughout my masters. Professor's Wong exceptional teaching environment had made me curious about quantum computing and electrical engineering like never before. Words cannot describe how much of an impact Professor Wong has made on my professional career and I am truly grateful and honored to have been apart his research endeavors. To my family who have been supportive throughout my masters. To my friends, Indraj Kaur, Sukhi Johal, Jennifer Lopez, Uyen Sou, and Susan Hopkins, this would have been much more difficult without their continual support and friendship. I am who I am today because of them, and I am extremely grateful of having them be part of my life.

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SS	Subthreshold Slope
DIBL	Drain Induced Barrier Lowering
TCAD	Technology Computer Aided Design
CMOS	Complemenetary Metal Oxide Semiconductor
SOI	Silicon on Insulator
FinFET	Fin Field-Effect Transistor
IV	Current vs. Voltage
SCE	Short Channel Effect
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor

1 INTRODUCTION

1.1 Desirability of Cryogenic CMOS Technology

With the ability to perform up to a million computations, quantum computers help in solving the world's most challenging and computationally extensive problems. Quantum computers can be applied to a variety of optimization problems that present day supercomputers are unable to achieve. These problems include companies wanting to balance risk of their investment portfolios, pharmaceutical companies modeling molecules to understand drug interactions, simulating chemical reactions to create efficient batteries for electrical vehicles, etc. [1]. The applications are endless, and the advantages are far more exceptional than present day supercomputers.

The computer architecture of a supercomputer and quantum computer vastly differ. Supercomputers evaluate combinations of problems successively, instead of in parallel. While quantum computers can create extensive multidimensional spaces for large problems [1]. Supercomputers store information in bits, where the bit is either zero or one. Quantum computers use quantum bits, or qubits. Qubits store data in a state of superposition, hence they can be zero and one at the same time. Because of this characteristic, qubits have the functionality of processing information in parallel. In 2019, Google's quantum computer, Sycamore, accomplished a mathematical calculation in less than four minutes, outperforming today's most powerful supercomputer by 158 million times [2]!

Due to the promising outlook, many companies such as IBM, Honeywell, PsiQuantum, Microsoft etc. are getting involved in the quantum computing field. The investment, development, and research being put into the field is essential for its advancement. The approach to building a quantum computer differs from company to company. Companies like PsiQuantum leverage photonics to generate qubits, claiming that it is the most efficient way to scale to a million qubits in order perform useful computation [2]. While companies like Google and IBM use superconducting qubits in their quantum computers. IBM currently has the largest quantum computer with 127 superconducting qubits (Fig. 1) [3]. Though different approaches may be beneficial in the advancement of the technology, the big question is how can the system efficiently scale up the number of qubits?

Fig. 1. IBM Q System One [3].

The key to efficiently scale quantum computers is to operate CMOS technology at cryogenic temperatures, about zero Kelvin. CMOS technology has always been desirable and

the driving force of the electronics business. This is due to the scaling trends which provide denser and faster integrated chips. The scaling trends suggests reducing the channel length to improve overall performance and density. Though the downfall is the total chip power consumption increases. Fig. 2 shows the trend of power supply, threshold voltage, gate oxide thickness against the channel length [4]. Performance improvements are substantially degraded below 1.5V because the threshold voltage decreases more slowly, causing inflexible device designs at increased electric fields [4].

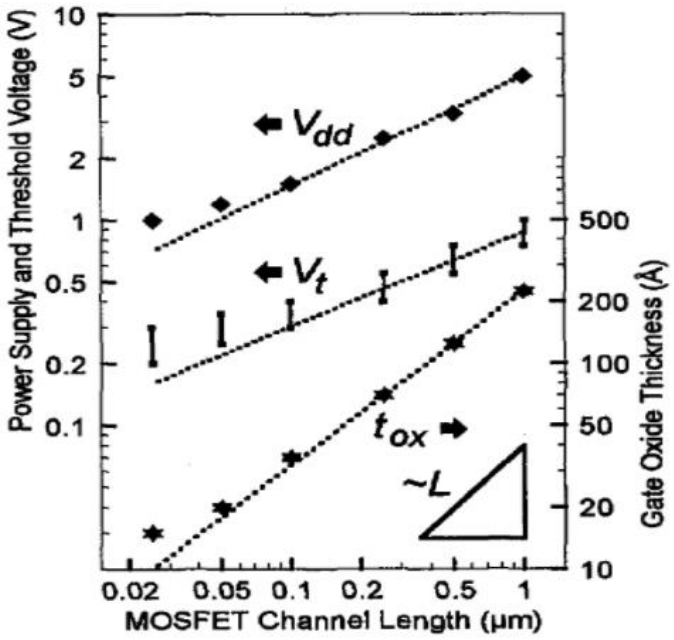

Fig. 2. Power Supply Voltage (V_{dd}), threshold voltage (V_t), and gate oxide thickness (t_{ox}), vs. MOSFET channel length [4].

However, by operating CMOS at cryogenic temperatures, there are numerous advantages that arise. These include improvements in the ON-state current, leakage current, subthreshold swing, and transconductance. Having such device characteristics become desirable to applications like deep space exploration, quantum computer, high-energy physics experiments, etc. Specifically with quantum computers, qubits at cryogenic temperatures

maintain minimal noise and are stable enough to perform useful computation.

1.2 Problem Statement

Though research has been performed concerning cryogenic CMOS, much of the development has been on older process nodes [5]. Older process technology is known to have limited performance compared to the present-day nanoscale CMOS process. There has not been much research carried out on the newer technology, though there have been a few achievements like quantum transport in 40-nm MOSFETs at deep cryogenic temperatures [6]. However, these slight advancements are not enough in the field of cryogenic CMOS technology, there remains crucial challenges that need to be uncovered to further advance the field. For instance, there are undesirable effects at the device level include high threshold voltage, hysteresis, kink effects, hot-carrier degradation, abnormal subthreshold swing, etc. It is essential that there be research carried out to further understand these effects and propose solutions to mitigate. Furthermore, when it comes to CMOS device characterization at deep cryogenic temperatures, there presents a need of physical and reliable circuit models.
By addressing these challenges will further enable the necessary development of cryo-CMOS technology needed to efficiently scale quantum computers.

1.3 Thesis Objectives

There are three primary objectives for this thesis. The first objective is to introduce an electron and hole mobility model for a wide temperature range since there has not been a unified model developed for silicon carriers from 4K to 300K. The second objective is modeling cryogenic NMOS ON-state current and subthreshold slope using Technology Computer-Aided Design (TCAD) based on a single set of parameters that are calibrated.

Finally, the third objective is to optimize the MOSFETs by applying the set of parameters and settings that are calibrated.

1.4 Thesis Organization

This thesis is organized in 6 chapters:

Chapter 1: States the primary motivation behind researching cryogenic CMOS technologies and the goal of this thesis.

Chapter 2: Background information and literature review.

Chapter 3: The calibration of parameters and modeling the ON-state current and subthreshold slope of a NMOS device.

Chapter 4: Mobility model for undoped silicon electron and hole for a wide temperature range.

Chapter 5: Optimization of MOSFET through the implementation of pre-calibrated parameters and settings.

Chapter 6: Conclusion to the thesis.

2 BACKGROUND OF CRYOGENIC CMOS

2.1 Introduction

This chapter will cover the background of the characteristics of CMOS devices at deep cryogenic temperatures. Firstly, the concepts of mobility, subthreshold slope, threshold voltage, and carrier freeze-out at cryogenic temperatures are discussed. Then, non-ideal characteristics foreseen in CMOS at cryogenic temperatures like the kink-effect and hysteresis are mentioned.

2.2 Physical Device Parameters at Cryogenic Temperatures

There are associated characteristics that are present in advanced semiconductor devices at cryogenic temperatures due to the device physics. First off, there is an overall increase in mobility, subthreshold slope, and threshold voltage. Furthermore, the phenomenon known as carrier freeze out is prevalent at cryogenic temperatures. The following sections will detail these physical device parameters.

2.2.1 Mobility

Scattering mechanisms in MOS devices determine the mobility of the carriers. The three major scattering mechanisms are coulomb scattering, surface roughness scattering, and phonon scattering. The total effective electron mobility because of scattering mechanisms can be obtained by employing Matthiessen's rule (Equation 1).

Equation 1: Matthiessen's rule (Version 1)

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{cb}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}$$

Coulomb scattering is the presence of electrostatic charges impacting the flow of channel carriers. The free carriers end up neutralizing some of the charges, which modifies their distribution in the region and screen external scattering mechanisms. The screening effect in turns decreases the coulomb scattering, especially at higher inversion charge concentrations. As T increases, coulomb scattering will decrease. Surface roughness scattering occurs when the vertical electric field pushes the carriers to the interface. As T increases, the carrier can have a higher energy hence being more resistant to the surface roughness scattering. Phonon scattering is due to lattice vibrations. This can be explained as collisions between the electrons and the vibrating lattice. As the temperature increases there is more phonon scattering, hence a higher mobility. Fig. 3 indicates the different scattering mechanisms and their effect on the mobility in relation to the temperature.

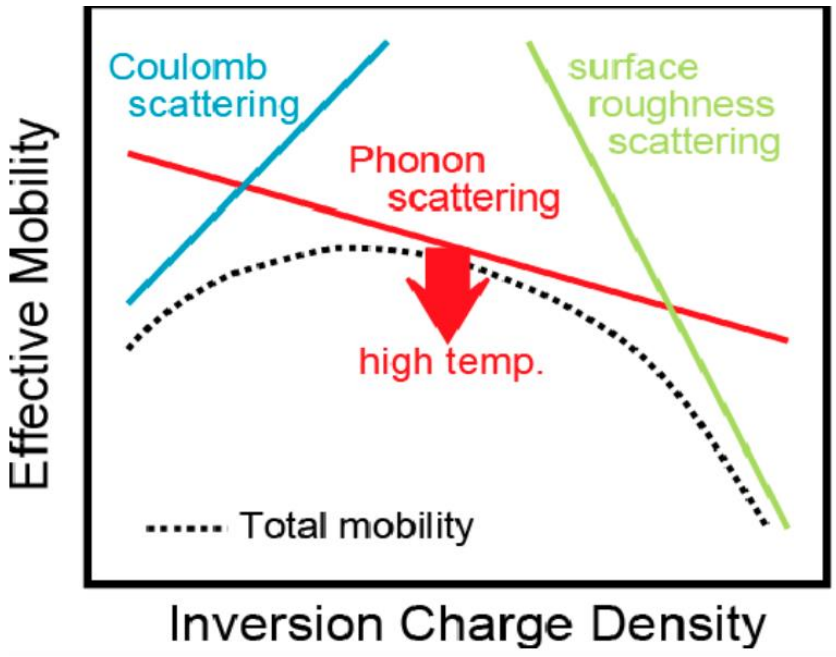

Fig. 3. Major scattering mechanisms in universal mobility curve on n-channel Si MOSFET [7].

For instance, one can observe that at higher electrical fields, coulomb scattering is less due to screening since a sheet of electrons is formed to protect from the electric fields from the impurity charges.

2.2.2 Subthreshold Slope

The subthreshold slope, SS, is defined as the gate voltage needed to increase the subthreshold current by one decade. Specifically, it is the measure of the rate at which charge diffuses from the channel region when the device is off. Ideally, a low subthreshold slope is desired. To calculate the subthreshold slope, Equation 2 is used.

Equation 2: Subthreshold slope

$$SS\ (T) = \ln(10) \times \frac{nkT}{q} \times (1 + \frac{C_{si}}{C_{ox}})$$

From Equation 2, one can infer that SS decreases as T, the temperature, decreases. n, the ideality factor, is also dependent on the temperature. At room temperature, where n=1, SS is ~ 60mV/decade. The SS at cryogenic temperatures such as 3K, is ~ 0.6mV/decade.

2.2.3 Threshold Voltage

The threshold voltage is the gate voltage that is necessary to create strong inversion. Equation 3 is used to calculate the threshold voltage, V_{TH}, of an NMOS.

Equation 3: Threshold voltage

$$V_{TH} = V_{FB} + 2\Phi_B + \gamma\sqrt{2\Phi_B}$$

In Equation 3, V_{FB} is the flat band voltage, Φ_B is the barrier voltage, and γ is the body effect coefficient. Since the freeze-out effect dominates at cryogenic temperatures, there are less free carriers present. Freeze-out also affects the lattice vibrations which makes the

mobility increase. The observed trend from experimental data is that as the temperature decreases, the threshold voltage will increase.

2.2.4 Carrier Freeze Out Effect

At room temperature dopants can fully ionize because there is enough thermal energy, however as the temperature begins to decrease the probability of carrier freeze out to take effect increases. For instance, if one looks at a PMOS device, as the temperature begins to decrease the fermi level will get closer to the valence band, hence the density of the mobile carriers will decrease in an exponential manner. All states within the valence band are neutrally charged because the carriers do not have enough energy to move into the conduction band from the valence band. Fig.4 shows how the carrier concentration is dependent on the temperature. Due to freeze out there is a continuous decrease of the carrier concentration with the decrease in temperature. The carrier concentrations even begin to decrease at higher temperatures and is much substantial for lower doping levels. This drop in carrier concentration is significant because the resistance will increase.

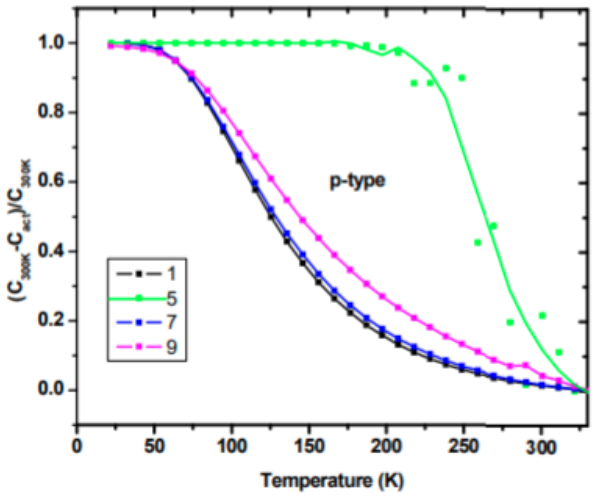

Fig. 4. P-type silicon material dependent on temperature, where carrier concentrations are (1) 2×10^{16} cm^{-3}, (5) 2×10^{12} cm^{-3} , (7) 2×10^{16} cm^{-3}, and (9) $3 \times 10^{16} cm^{-3}$ [8].

2.3 Kink Effect/Floating Body Effect

There is also a presence of the kink effect, also known as the floating body effect, at cryogenic temperatures. In Fig.5 one can see that once V_{DS} is large enough, there comes a point where the drain current experiences an abrupt increase, displaying a “kink” in the IV curve.

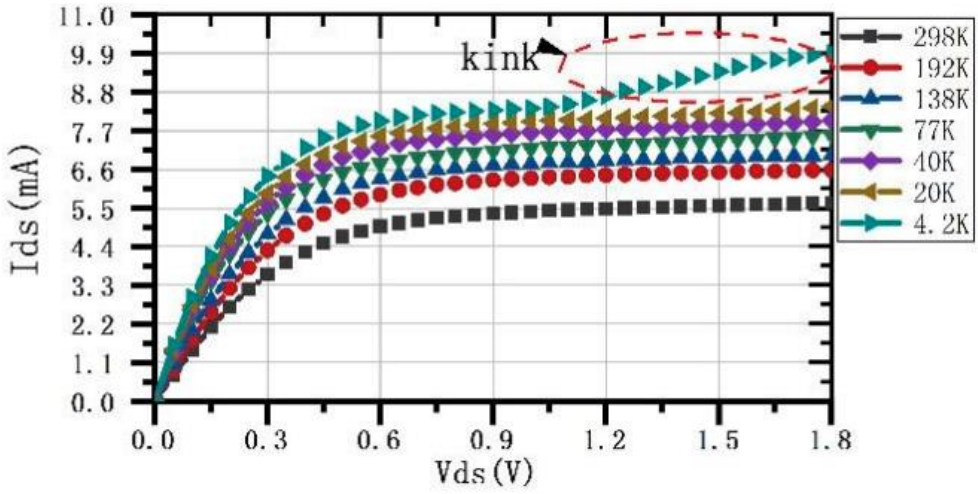

Fig. 5. $I_{DS} - V_{DS}$ of thin-oxide NMOS at different temperatures from 298K to 4.2K [9].

In partially depleted SOI MOSFETs, the kink effect occurs because of the majority carriers produced by impact ionization end up being stored in the body, hence increasing the body potential, and lowering the threshold voltage. This effect can also be observed in fully depleted SOI MOSFETs where a negative back gate voltage facilitates the accumulation of holes near the back of the interface causing the kink effect. This in turn leads to undesirable effects that cause off-state leakages degrading the device.

2.4 Hysteresis

Another abnormal behavior at deep cryogenic temperatures is hysteresis. Hysteresis is caused due to gradual ionization of traps between the gate oxide and the substrate [10]. This

is because at low temperatures, the ionization rate is much slower. When transitioning from the linear region to saturation region, more time is taken to form the depletion layer. Therefore, the current is much higher than ideal until the necessary amount of drain voltage is obtained [10]. Then the current decreases and saturates at a constant value. This effect can be seen in Fig. 6.

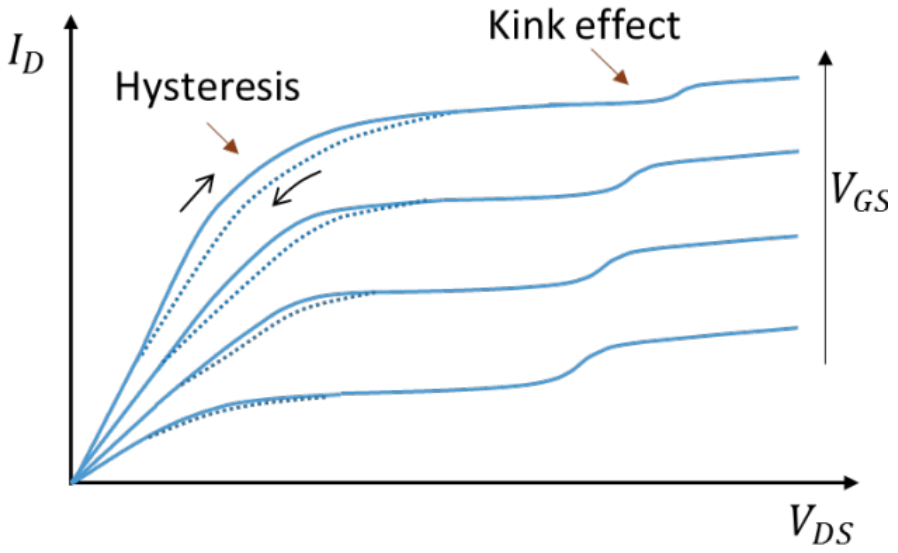

Fig. 6. Hysteresis of MOSFET at low temperatures [10].

3 MODELING OF ON-STATE CURRENT AND SUBTHRESHOLD SLOPE

3.1 Introduction

When it comes to researching and developing cryogenic electronics, most depend on analytical modeling [11] because TCAD lacks the maturity to model cryogenic CMOS effectively. This is due to the fact that there does not exist fine-tuned parameters at cryogenic temperatures [11], unidentified physics ("abnormal SS" present at cryogenic temperatures [12][13]), and convergence problems [14]. Because of the present convergence problems, most simulations performed in TCAD will go up to 77K. These simplified models do not apply well when trying to reach 15K [15]. Hence, to be able to model a reliable MOSFET at 4K is necessary to advance development in the field of cryo-CMOS.

According to the SS equation of a MOSFET, the SS is expected to scale with temperature, so at cryogenic temperature the SS should be steep. For instance, at 4K and n=1 the SS is about 0.8mV/dec, which in return enhances the I_{ON}/I_{OFF} trade off. Though experimentally, the observations show a different trend. This trend indicates that as the temperature decreases, the SS is 10mV/dec at 50K and 15mV/dec at 70K. The explanation of this abnormal SS trend can be supported by two popular theories. The most plausible theory is the existence of band tail states in the silicon [12][13]. The second theory is the existence of traps at the oxide/channel interface degrading the SS [16]. This theory is also encouraged since at cryogenic temperatures there is an increase in noise of 1/f. However, because of convergence issues present in TCAD, this theory has only been analyzed systematically and a very large interface trap density is needed to describe the decay. Hence, the research demonstrates the application of TCAD to model a nMOSFET ON-state current and SS with

appropriate parameter settings. The research even investigates the use of interfacial traps to model the abnormal SS.

3.2 TCAD Model and Simulation

TCAD is used to simulate the experiments because it is the preferred software to develop and optimize semiconductor processing technologies and devices. The device used for the simulation was a 0.35µm technology nMOSFET with W/L=10µm/10µm at temperatures of 300K and 5K. While the gate oxide thickness was, t_{ox}, 7.6nm and a drain bias of 0.1V was applied. [17] does not illustrate the fabrication process hence to achieve sufficient matching in [17], 0.35µm technology node is used since it is an older and widely used process. Fig.7 displays the device simulated in TCAD using SProcess [18]. SProcess models the fabrication process of semiconductor devices like etching, deposition, diffusion, implantation, etc. The device is accurate because one can see at the gate edge the oxide is thickened owing to Poly Reox and because of the source/drain lowered.

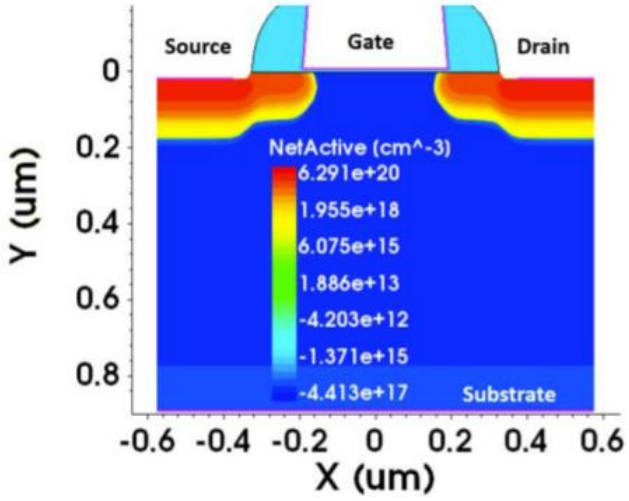

Fig. 7. Cross-section of the simulated 0.35µm nMOSFET [18].

To simulate the $I_D - V_G$ curves, SDevice is utilized. To achieve good convergence, certain settings were applied. The type of analysis applied was a transient simulation which included extrapolation and Backward-Euler. 80-bit precision is applied to ensure numerical stability. For precise trap modeling, the trap level discretization is raised to 1000. For the mobility calculations, the Philip Unified Mobility model and Lombardi Model for surface scattering were used. The parameters used for the Philip Unified Mobility come from [19]. Fermi-Dirac statistics is also employed. The incomplete ionization model is off because the doping is anticipated to completely ionize when in the ON-state. The velocity saturation model is also turned off since only $V_D = 0.1V$ is used.

Fig. 8 indicates that the ON-state current and SS fit respectably at 300K and 5K. There were 2 calibrations that were achieved during the simulation. The first one being Lombardi model's acoustic phonon scattering. Equation 4 is used for the acoustic phonon scattering portion.

Equation 4: Acoustic phonon scattering

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C\left(\frac{N + N_2}{N_0}\right)^{\lambda}}{F_\perp{}^{\frac{1}{3}}\left(\frac{T}{300K}\right)^{k}}$$

In Equation 4, N is the total doping concentration, T is the temperature, $F_\perp$ is the normal component of the electric field at interface, and the rest are fitting constraints. For most of the parameters, default values are used. However, to fit the 300K and 5K data well, parameter C is 340 $cm^{5/3}V^{-2/3}s^{-1}$ and parameter K is 0.45.

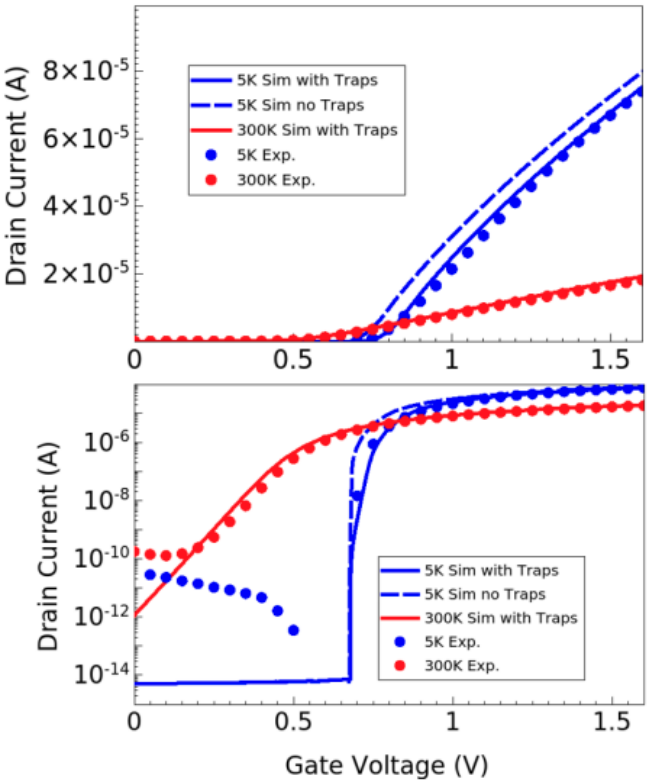

Fig. 8. Experimental and simulated $I_D - V_G$ curves in linear (top) and log (bottom) scales at temperatures of 300K and 5K [18].

From the results, it was found that the ON-state current fits well, though the simulated SS (~1mV/dec) and threshold voltage are too small at 5K (Fig. 8). Also, $6 \times 10^{13} \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ acceptor traps are assigned in a uniform fashion between $E_c - 5\mathrm{meV}$ and $E_c + 25\mathrm{meV}$ at the oxide/silicon interface [18]. The selection of the energy range and density of the trap is based on a manual fitting, this is described in more detail in the following section.

3.3 Modeling Abnormal SS Using Interface Traps

Though interface traps can be understood to model the SS at 5K, these traps can also model the SS at different temperatures. The research studies how the SS varies with oxide

thickness, gate length, and drain voltage. By using a transient simulation, the research was able to effectively account for the trap capturing and emission times. The capture rate is reliant on temperature due to thermal velocity (Equation 5).

Equation 5: Capture rate

$$c = \sigma v_{th,0} \sqrt{\frac{T}{300K}}\, n$$

In Equation 5, σ is the cross-section, $v_{th,0}$ is the thermal velocity at 300K, T is the temperature, and n is the carrier concentration.

3.3.1 Temperature Variation

To study the effects of interfacial traps on the SS, a device of W/L =1µm/5µm is constructed and two different oxide thicknesses were investigated, $\mathrm{t_{ox}} = 10\mathrm{nm}$ and $\mathrm{t_{ox}} = 2\mathrm{nm}$ [18]. A script was then written in svisual to simulate $\mathrm{I_D} - \mathrm{V_G}$ curves with $\mathrm{V_D} = 1\mathrm{mV}$. In order to fit the SS of different temperatures using interfacial traps, the highest temperature with abnormal SS is fitted first. Firstly, the fermi level locations at the start and end of the subthreshold region are classified and then a uniform trap is allocated between the two locations. The next temperature follows the same fitting protocol with the traps from the prior fit kept. These fits are completed up to 4K and in the end the shape is modified to achieve a smoother curve [18].

Fig.9 showcases $\mathrm{I_D} - \mathrm{V_G}$ curves with oxide thickness of 10nm with and without traps present. Fig.10 shows the optimized trap profile to replicate the abnormal SS at multiple temperatures. To extract the SS, the slope is taken from the $\mathrm{I_D} - \mathrm{V_G}$ curves when $\mathrm{I_D} =$

10^{-13}A and 10^{-10}A. Fig.11 shows this SS extraction and is plotted against the experimental values [12].

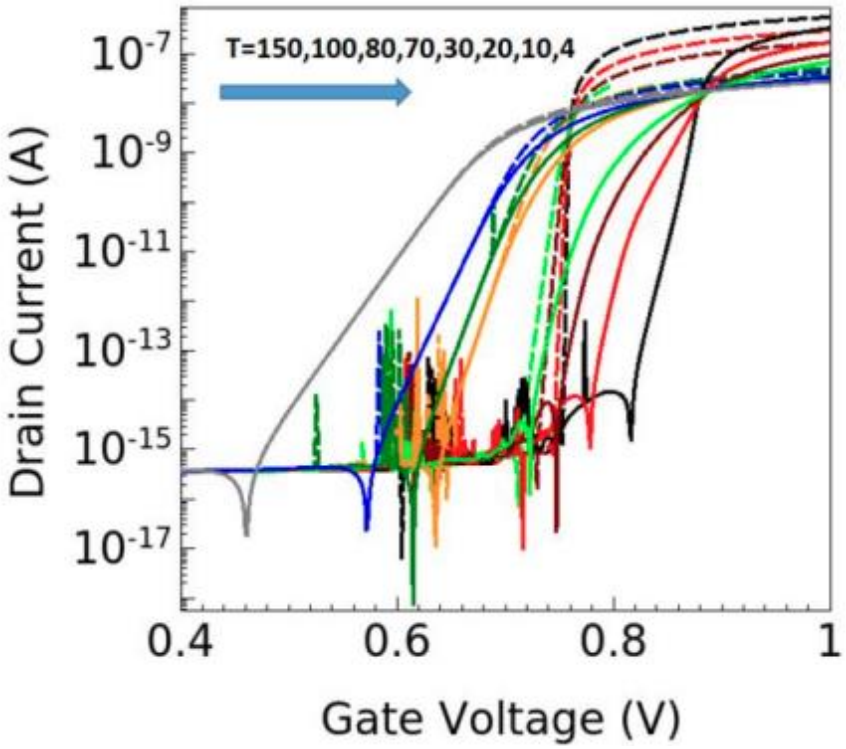

Fig. 9. $I_D - V_G$ at various temperatures with single set of traps (solid) and without traps (dash) [18].

The goal of these fits was to exhibit the prospect of fitting SS by using just one setting of trap distribution, since the only information from [12] was that they used 28nm technology while other device parameters like doping were unknown. What is observed is that the findings are like that of [12] at 300K. By using the trap profiles that were developed, the research was able replicate the SS curve (Fig. 10) [18].

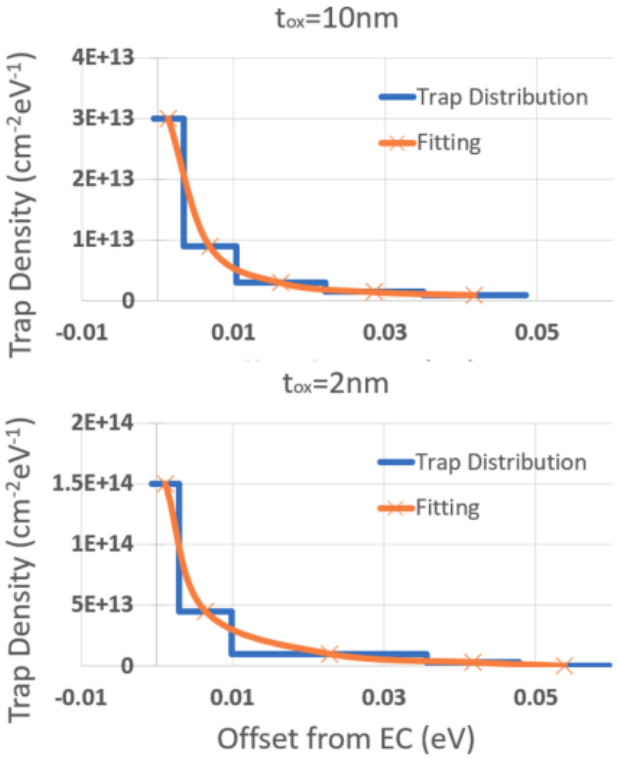

Fig. 10. Trap distributions that replicate the abnormal SS at all temperatures for 2 distinct oxide thicknesses [18].

3.3.2 Gate Insulator Variation

Acceptor traps effects on the $I_D - V_G$ curves are supported inversely on the gate oxide capacitance [18]. For technologies like FETs, to attain the same result more traps need to be placed. Hence to achieve this, the oxide thickness, t_{ox}, is 2nm and an additional optimal trap profile is defined in Fig.10 and the SS is plotted in Fig.11. The "Beckers" data is experimental data from [12]. Though the abnormal SS can fit, the total integrated charge is $1.14 \times 10^{12}\text{cm}^{-2}$ which turns out to be 5 times more than the first profile, verifying against the oxide capacitance which is 5 times higher as well [18].

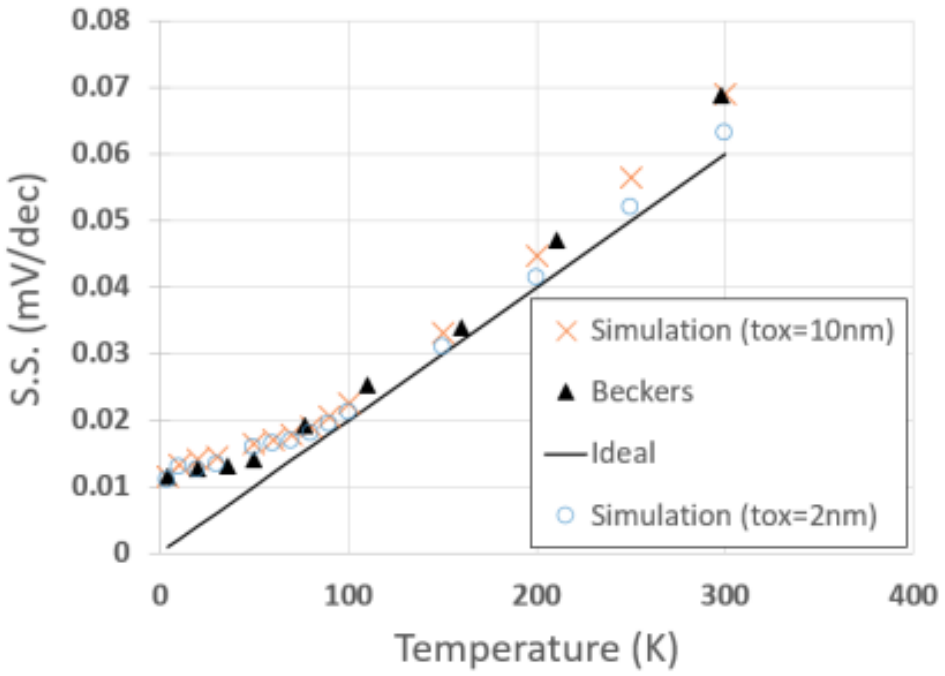

Fig. 11. S.S. as a function of temperature [18].

3.3.3 Drain Voltage Variation

Next, the influence of drain induced barrier lowering (DIBL) is studied when using interface traps to model abnormal SS. Device specifications include $L = 0.5\mu m$, $W = 0.5\mu m$, and $t_{ox} = 2nm$ and the trap profile from Fig.10 modeled with several drain voltages, V_D [18]. Fig.12 shows the extracted SS as a function of temperature. The SS resembles the general observation in the experiment and that the $I_D - V_G$ curves are similar at varying V_D.

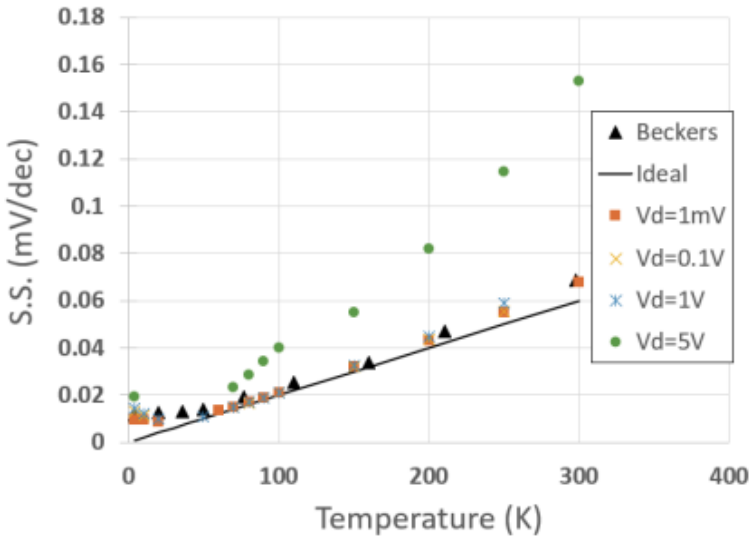

Fig. 12. SS vs. Temperature for varying V_D for L=0.5µm and $t_{ox} = 2nm$ [18].

A noteworthy observation made is that because of the abnormal SS, there is serious degradation in SS owing to the DIBL at high temperatures while at cryogenic temperatures the degradation is significantly less prevalent [18]. This observation is made from Fig. 12, 13, and 14.

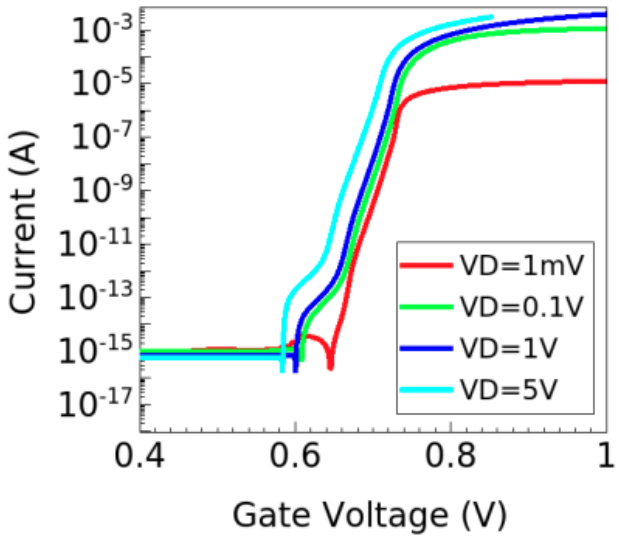

Fig. 13. $I_D - V_G$ at various V_D with interface trap distribution at 4K [18].

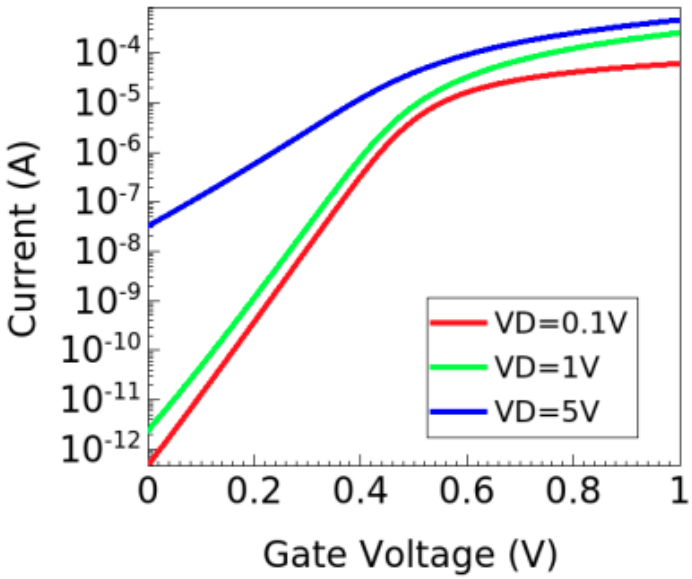

Fig. 14. $I_D - V_G$ at various V_D with interface trap distribution at 300K [18].

3.4 Conclusion

The research showcases the use of TCAD software to model the ON-state characteristics and SS of nMOSFET where a specific set of parameters and settings were applied at 300K and 5K. Moreover, the work validates its results to the experimental results. Most importantly, it was found that the oxide/channel interface acceptor traps close to the conduction band edge contribute to the abnormal SS from 300K to 4K, even with the presence of DIBL. Overall, the research opens the gateway to simulate and enhance cryo-electronics in TCAD.

4 ELECTRON AND HOLE MOBILITY MODEL

4.1 Introduction

In a quantum computer, CMOS must operate at deep cryogenic temperatures (4.2K and lower) to reduce noise and latency between the qubits and readout circuity. Viable semiconductor devices to achieve this include the bulk, SOI, and FinFET. To be able to create a qubit and CMOS integrated chip, entails that cryogenic CMOS be improved so that the produced heat is also reduced. Hence, to create reliable models and set of parameters are essential to facilitate the implementation of cryogenic CMOS.

Efforts have been made to study cryogenic CMOS modeling at the compact model stage. For instance, [20] studies from temperatures of 4.2K to 300K the linear region mobility of a device. References [21] and [22] developed compact CMOS models for 77K and 4.2K. Moreover, there have been developments in modeling cryogenic CMOS in TCAD. The studies include abnormal SS, incomplete ionization, high field saturation models. Challenges due arise with modeling electron mobility at cryogenic temperatures. This is due to the fact of the presence of negative differential velocity. According to reference [23], the Canali high field saturation model [24] has unusual findings below 20K. Part of the model can be improved using the Selberherr model [25], however the low and medium electric field portions below 77K are not modeled well. The model itself cannot capture the low field mobility and negative differential velocity. Thus, to have reliable TCAD simulations and to develop precise compact models, the need for a low field and high field mobility model is essential.

Experimental data of Si electron mobility for a wide temperature range is hard to come across from. The research intends to use the modified Farahmand model to model each of the experimental data in references [26] and [27]. Functions are developed to model the temperature reliant parameters in this model in order to predict the expected the mobilities at 4K.

4.2 Modeling and Calibration

To calculate the low field mobility in TCAD, the undoped bulk mobility model, μ_{bulk}, is summed with other mobility models by applying Matthiessen's rule (Equation 6). In Equation 6, μ_{low} is the total low electric field mobility, μ_{doped} is the impurity dependent mobility, and μ_{SC} is the surface scattering mobility. With the presented model, there is ability to include additional scattering mechanisms.

Equation 6: Matthiessen's rule (Version 2)

$$\frac{1}{\mu_{low}} = \frac{1}{\mu_{bulk}} + \frac{1}{\mu_{doped}} + \frac{1}{\mu_{SC}} + \cdots$$

Firstly, the experimental data are digitized from [26], this data includes hole <100> and electron <111> and electron <100> from [27]. Canali model is utilized to fit electron <111> data. Then, the Canali model is applied to the fit the electron <111> data (Equation 7). The parameters within Equation 7 that are temperature dependent include β, μ_{low}, and v_{sat}. They also consist of the following values: $\beta_{sat} = 1$, $T_0 = 130$, $b = 3$, $\beta_0 = 0.4$.

Equation 7: Canali model

$$\mu = \mu_{low}\left(1 + \left(\frac{\mu_{low}E}{v_{sat}}\right)^{\beta}\right)^{-\frac{1}{\beta}}$$

Table 1 includes all the derived equations that consist of parameters dependent on temperature. Fig. 15 displays the calibration results for electron mobility in transport direction of <111>.

Table 1
Temperature-dependent parameters of Farahmand model [28].

Equations and Parameters
$\mu = \frac{\mu_{low}+\mu_1\left(\frac{E}{E_0}\right)^{\alpha}+v_{sat}\frac{E^{\beta-1}}{E_1^{\beta}}}{1+\gamma\left(\frac{E}{E_0}\right)^{\alpha}+\left(\frac{E}{E_1}\right)^{\beta}}$
$\mu_{low} = A\,T^{-\gamma}$
A =2.36e7,2.36e7,1.35e8; γ = 1.7,1.7,2.2
$v_{sat} = v^*/\left(1+Ce^{\frac{T}{\Theta}}\right)$
v^* =2.4e7,2.4e7,2.3e7; C = 0.8,0.8,1.1; Θ =600,600,600
$\mu_1 = \left(1-\tanh\left((T-T_0)/T_1\right)\right)/(2k)$
T_0 =50,50,15; T_1 =65,65,100;k =2900,2900,3000
$\alpha = \alpha_{sat}(T/T_0)/(1+(T/T_0)^{a})^{1/a}+\alpha_0$
α_{sat} =2.5,2.54,2.54; T_0 =80,98,98; a =6,8,8; α_0 =1.05,1,1
$\beta = \beta_{sat}(T/T_0)/(1+(T/T_0)^{b})^{1/b}+\beta_0^{*}$
β_{sat} =2.8,2.5,2.5; T_0 =85,120,120; b =5,4,4; β_0 =1.8,2.2,2.2
$\gamma = \left(k\tanh\left((T-T_0)/T_1\right)+1\right)+\gamma_0$
k =0.6,0.59,1.64; T_0 =50,50,47.81; T_1 =50,4,19.5; γ_0 =1.7,1.7,1.47
$E_0 = E_{sat}\left(\tanh\left((T-T_3)/T_0\right)+1\right)\left(\tanh\left((T/T_1)^{p}\right)\right)\times(1-A\exp(-\lvert T-T_2\rvert/s))$
E_{sat} = 800,570,300; T_0 =33.3,60.3,83; T_1 =5,18,120; T_2 =125,123,160; T_3 =125,123,90; p = 2,1,0.8; A =2,1,-0.4; s =1.67,6,33.3
$E_1 = e_1 e^{\frac{e_2 T}{T_1}}\left(\tanh\left((T-T_0)/T_1\right)-1\right)+(I_1 T+I_2)\left(\tanh\left((T-T_0)/T_1\right)+1\right)$
e_1 =-1.725,-35,-28; e_2 =0.0441, 0.0158, 0.0157; I_1 =1.5,0.5,0.7; I_2 =340,475,240; T_0 =130,200,190; T_1 =1,1,1

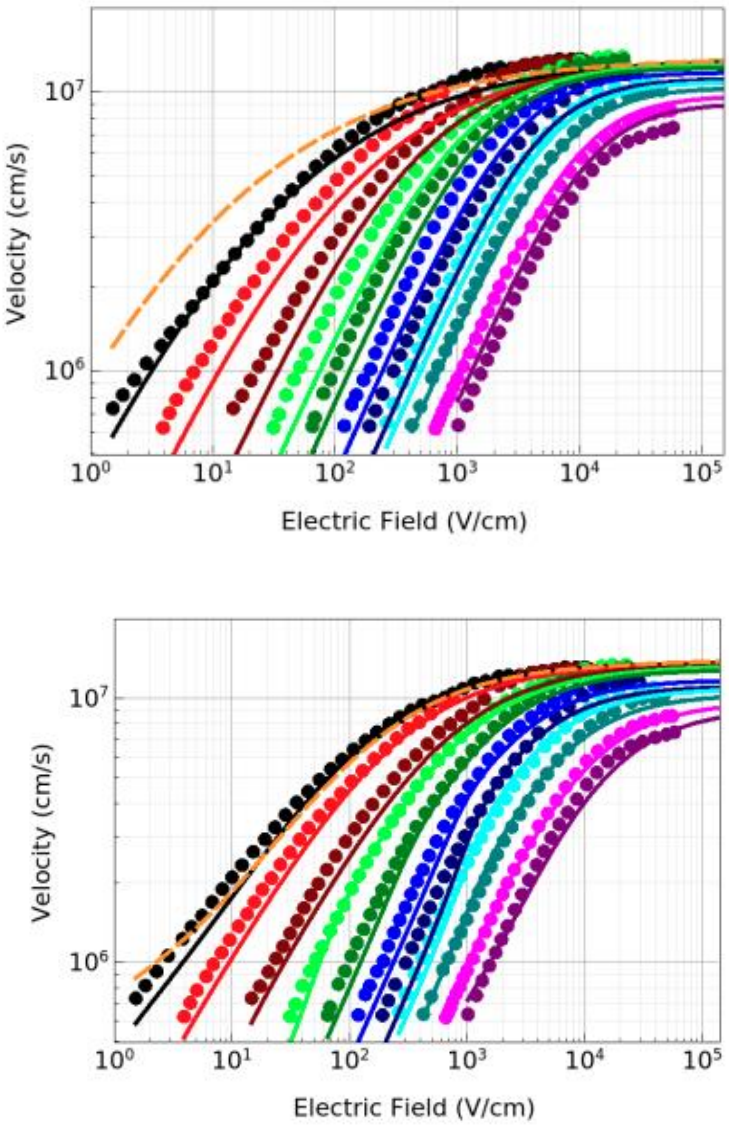

Fig. 15. The figure at top is Canali model and figure on bottom is the modified Farahmand. Electron velocity vs. electric field at 8K, 20K, 45K, 77K, 110K, 160K, 220K, 245K, 300K, 370K, and 430K. Continuous lines correspond to the model while dots correspond to the experiment. The orange dashed lines is the predicted 4K result [28].

The model itself covers a wide temperature range. μ_{low} and v_{sat} are calibrated using equations from [26], in which the parameters attain the temperature-dependent low field mobility and saturation velocity to match well with the experimental findings [28].

μ_{low} and v_{sat} are the same in <100> and <111> directions for the electron because they are isotropic in Si. At low temperature and medium electric field, the negative differential velocity appears in <100> direction. This is because the electrons moving at the transverse valleys increase in temperatures, gaining enough energy to enter the longitudinal valleys [26]. This effect cannot be seen in the <111> direction because of the lack of symmetry and intervalley scattering [28]. Since the Canali model cannot be used in this case, the modified Farahmand model is implemented (Equation 8) [29]. In Equation 8, μ_1, β, α, γ, E_1 , and E_0 are parameters that have been derived via equations and can be seen in Table 1.

Equation 8: Modified Farahmand model

$$\mu = \frac{\mu_{low} + \mu_1 \left(\frac{E}{E_0}\right)^{\alpha} + v_{sat} \frac{E^{\beta-1}}{E_1^{\beta}}}{1 + \gamma \left(\frac{E}{E_0}\right)^{\alpha} + \left(\frac{E}{E_1}\right)^{\beta}}$$

The calibrated model can effectively take in account the negative differential velocity (Fig. 16). <111> electron mobility is calibrated using the modified Farahmand model. This can be seen in Fig. 15. In comparison the fit using the Canali model, it seems that overall, it has a better fit especially in the high electric field area.

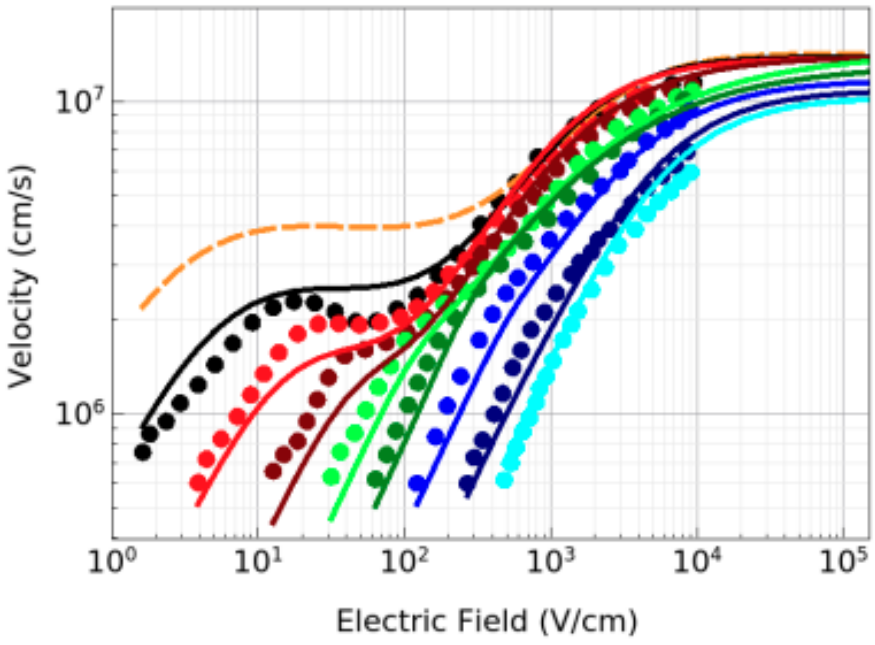

Fig. 16. Electron velocity <100> vs. electric field at 8K, 20K, 45K, 77K, 110K, 160K, 245K, and 300K. Continuous lines correspond to the model while dots correspond to the experiment. The orange dashed lines is the predicted 4K result using the modified Farahmand model [28].

The hole velocity in the <100> begins to have a leveled plateau at temperatures below 30K and at moderate electric field. By applying the same equations, the data can be fitted well and can be seen in Fig.17. Furthermore, for the hole, the v_{sat} parameters are developed so that they fit well with the experimental data [24] at high temperatures. At temperatures, below 24K, the observation made is that the hole mobility at low electric fields begins to differ from theory. An explanation for this occurrence would be because of impurities. Therefore, when fitting the 6K data and inferring the 4K curve, the research obtains $5\times10^5 cm^2/Vs$ and $7\times10^5 cm^2/Vs$ with impurities $<10^{12} cm^{-3}$ from experimental data [28].

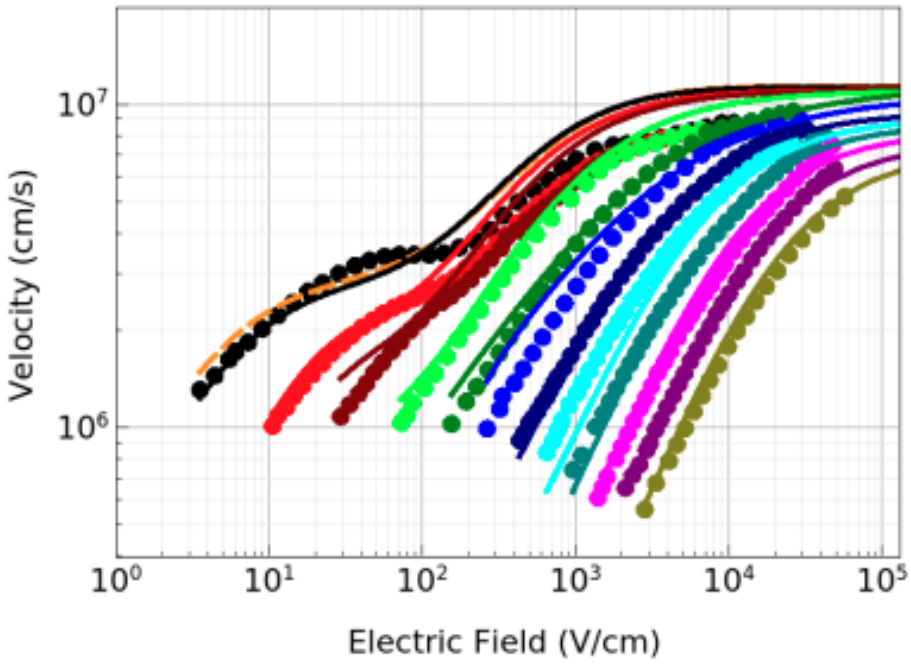

Fig. 17. Hole velocity <100> vs. electric field at 6K, 24K, 30K, 45K, 77K, 110K, 160K, 200K, 245K, 300K, 370K, and 430K. Continuous lines correspond to the model while dots correspond to the experiment. The orange dashed lines is the predicted 4K result using the modified Farahmand model [28].

4.3 Analysis

When developing and calibrating the model, schemes were applied to prevent overfitting. The most dominant model used to model negative differential velocity is the Farahmand model and it has been appropriate for TCAD implementation. The μ_{low} and v_{sat} parameters have defined values, though at times are calibrated to the experimental data. For the parameters which are temperature dependent, differentiable equations are developed. The 4K curves are then predicted which can be seen in Figs. 15-17. The parameter values are recorded in Table 2. The variation between the modified Farahmand model and the Canali model is < 20% for electric fields greater than 100V/cm [28].

Table 2
Parameters for both electrons and holes at 4K (Farahmand model) [28].

Type	μ_{low} #	v_{sat} *	μ_1	α	β	γ	E_0	E_1
e111	2.24	1.33	1408	1.17	1.93	2.06	0.72	4.12
e100	2.24	1.33	2333	1.10	2.28	2.11	4.72	76.6
h100	0.7	1.09	1664	1.10	2.28	0.87	4	60

The presented work will be of great importance when it comes to self-heating simulations. For device application like in quantum computing, the temperature range for the single device should not go beyond the 4K-40K limit. Hence, another set of parameters are defined for this use case. The same model is intended to have a good fit for the experimental data below 45K, including 45K. These parameters are shown in Table 3. The curve fit for <100> electron mobility can be seen in Fig.18, while the curve fit for <100> hole mobility can be seen in Fig.19.

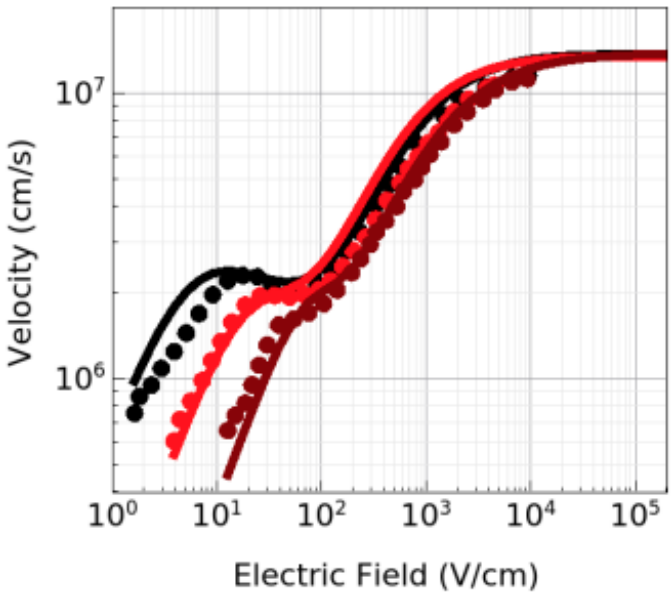

Fig. 18. Electron velocity <100> vs. electric field at 8K, 20K, and 45K using the parameters presented in Table 3. Continuous lines correspond to the model while dots correspond to the experiment [28].

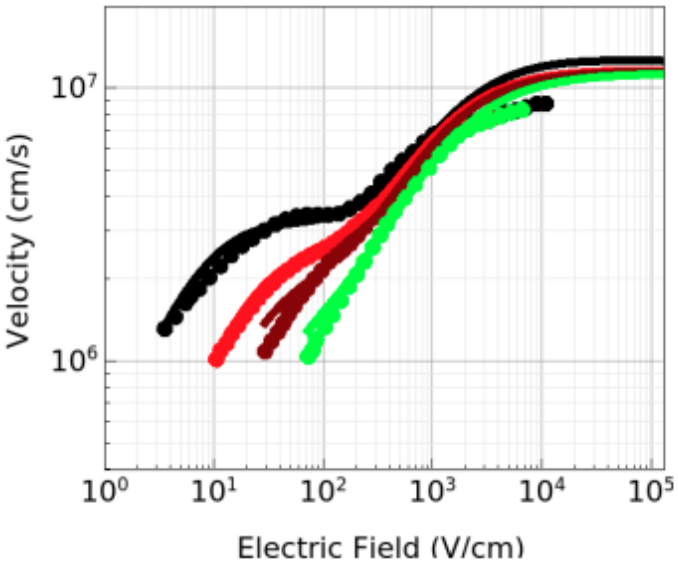

Fig. 19. Hole velocity <100> vs. electric field at 6K, 24K, 30K, and 45K using the parameters presented in Table 3. Continuous lines correspond to the model while dots correspond to the experiment [28].

Table 3
Temperature-dependent parameters of Farahmand model (6K-45K) [28].

Equations and Parameters
$\mu = \frac{\mu_{low}+\mu_1\left(\frac{E}{E_0}\right)^{\alpha}+v_{sat}\frac{E^{\beta-1}}{E_1^{\beta}}}{1+\gamma\left(\frac{E}{E_0}\right)^{\alpha}+\left(\frac{E}{E_1}\right)^{\beta}}$
$\mu_{low} = A\,T^{-\gamma}$
A =2.36e7,2.36e7,1.35e8; γ = 1.7,1.7,2.2
$v_{sat} = v^*/\left(1+Ce^{\frac{T}{\Theta}}\right)$
v^* =2.4e7,2.4e7,2.3e7; C = 0.8,0.8,1.1; Θ =600,600,600
$\mu_1 = \left(1-\tanh\left((T-T_0)/T_1\right)\right)/(2k)$
T_0 =50,50,15; T_1 =65,65,100;k =2900,2900,3000
$\alpha = \alpha_{sat}(T/T_0)/(1+(T/T_0)^{a})^{1/a}+\alpha_0$
α_{sat} =2.5,**3**,**1.4**; T_0 =80,**110**,**170**; a =6,**10**,**15**;
α_0 =1.05,**1.21**,**1.14**
$\beta = \beta_{sat}(T/T_0)/(1+(T/T_0)^{b})^{1/b}+\beta_0^*$
β_{sat} =2.8,**5.5**,**1.1**; T_0 =85,**230**,**140**; b =5,**2**,**1.1**;
β_0 =1.8,2.36,2.25
$\gamma = \left(k\tanh\left((T-T_0)/T_1\right)+1\right)+\gamma_0$
k =0.6,0.59,**2**; T_0 =50,50,**80**; T_1 =50,4,**58.8**; γ_0 =1.7,**1.84**,**1.5**
$E_0 = E_{sat}\left(\tanh\left((T-T_3)/T_0\right)+1\right)\left(\tanh\left((T/T_1)^{p}\right)\right)\times$ $\left(1-A\exp\left(-\lvert T-T_2\rvert/s\right)\right)$
E_{sat} = 800, **560**, **535. 6**; T_0 =33.3,**64**,**57.7**; T_1 =5,**32**,**73.2**; T_2 =125,**123**,160; T_3 =125,**110**,**105.3**; p = 2,1, **0. 585**; A =2,1,0; s =1.67,**18**,**100**
$E_1 = e_1 e^{\frac{e_2 T}{T_1}}\left(\tanh\left((T-T_0)/T_1\right)-1\right)+$ $\left(I_1 T+I_2\right)\left(\tanh\left((T-T_0)/T_1\right)+1\right)$ e_1 =-1.725,**-20**,**-46.5**; e_2 =0.0441, **0.033**, **0.017**; I_1 =*1.5,0.5,0.7*;I_2 =*340,475,240*;T_0 =*130*,***155***,*190*;T_1 =*1,1,1*

The overall process applied to fit the parameters will be discussed next. According to Equation 8, μ_{low} begins to dominate because of the small electric field. As the electric field slowly increases, the second term in the numerator of Equation 8 will dominate to capture the negative differential velocity. This effect is reliant E_0, γ, and μ_1 and $\frac{\mu_1}{\gamma}$. Once it reaches high electric fields, the third term must lead, and this is dependent on E_1. To have the third term dominate, requires that β be larger than α. Manual fittings are accomplished for each of the temperatures by altering the parameters in Equation 8. Through this process, attention to detail was made to ensure smoothness in the fit. Overall, the fitting was assessed on three methods. The first being creating fits that can achieve the overall trend of the experimental data, such as the negative differential velocity. Then, making sure the parameter values for both electron and hole are reasonable in manner. Lastly, to attain an average fitting error to the experimental curves be less than 10%. Figures 18 and 19 retain an error of 3.8% and 1.4% [28].

4.4 Conclusion

The research sought to develop and calibrate a Si mobility model that is field-dependent and temperature-dependent for electron in transport directions of <100> and <111> as well as hole in transport direction of <100> [28]. The correlation between the carrier mobilities and the electric field is centered on the modified Farahmand model. The model achieves to capture the negative differential velocity and the functions are smooth enough to effectively predict the carrier mobility at 4K [28].

5 OPTIMIZATION OF MOSFETS

5.1 Introduction

There are fundamental benefits when scaling MOSFETS, though there are unwanted effects such as short channel effect (SCE), drain induced barrier lowering (DIBL), hot carrier degradation, etc. Though by operating at cryogenic temperatures, many of these unwanted effects are subsided and the performance is much better because of reduced on-resistance and higher switching rate, which entails the devices will have lower power dissipation. Chapter 5 of this thesis dives into the optimization of MOSFETs operating at cryogenic temperatures.

Reference [30] presents a theory to predict the threshold voltage of short-channel IGFET's. When the space between the source and drain begins to reduce, the electrostatic potential distribution under the gate increases in contrast to the long-channel theory. Reference [30] details a simple model that uses geometrical approximation in combination with charge conservation assessment. The resultant is a threshold voltage equation that is simple yet preserves intuition of the initial charge conservation. Fig.4 from reference [30] illustrates the effect of the substrate doping on the threshold voltage for a junction depth, r_j, 0.5μm. To improve the short channel-effect, a back-gate bias is applied. This experimental data will aid in modeling the device and once the simulated results match [30], the research will continue to optimize the modeled device at cryogenic temperatures with the appropriate parameters and settings.

5.2 TCAD Simulation

A pMOSFET device is simulated in TCAD which has an oxide thickness of 500Å, junction depth of 0.5µm, an applied backgate bias of 5V. A set variable for the SDE is gate length, *L*, from 0.5µm to 6µm in increments of 0.5µm. Multiple projects were created for each doping concentration: N_D=1e15cm^{-3}, 1e16cm^{-3}, 5e16cm^{-3}, and 1e17cm^{-3}. SDevice was then used to simulate the $I_D - V_G$ curves. A script was then written to extract the threshold voltage where it would probe the $I_D - V_G$ curve when $I_D = 1e-9$ A. Fig. 20 shows the cross-section of the simulated pMOSFET when N_D=1e16cm^{-3} and *L*= 6 µm.

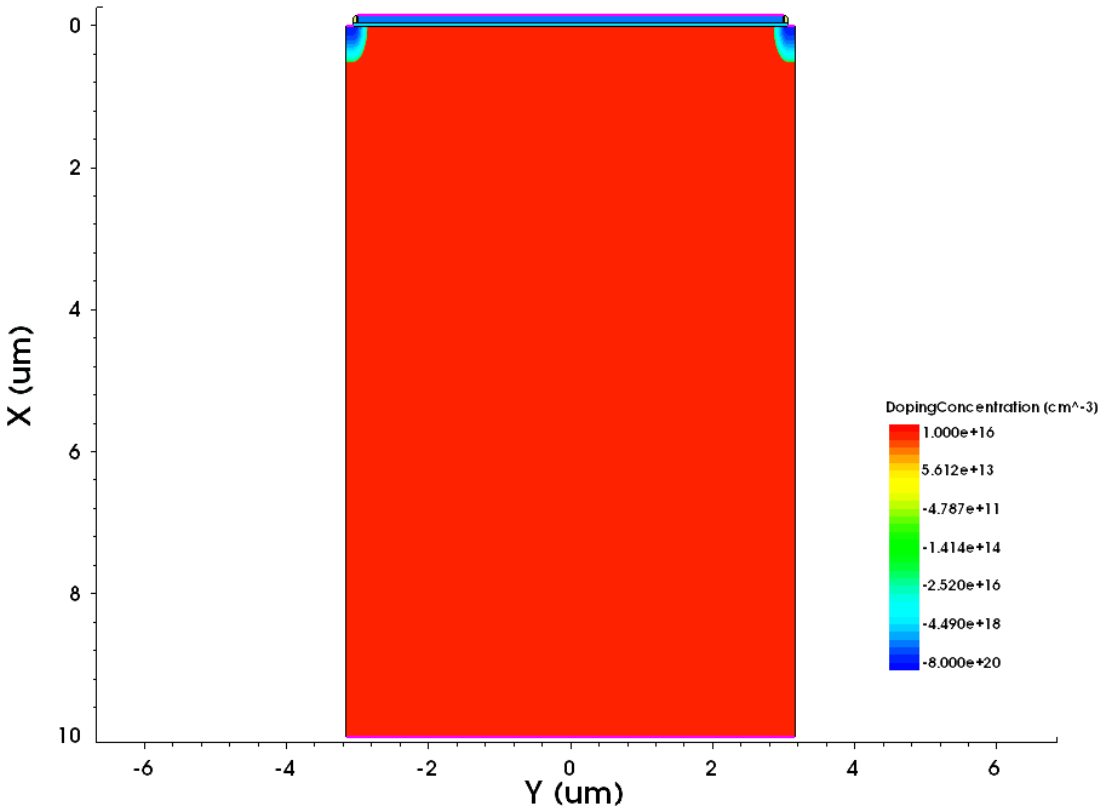

Fig. 20. Cross-section of the simulated pMOSFET.

Equation 9 is used to find the threshold voltage, V_T. This equation is applicable if and only if the channel length of the MOSFET is larger in comparison to the source and drain's junction depth. In Equation 9, V_{FB} is the flatband voltage, Φ_F is the surface potential, Q_B is the fixed charge due to the ionized impurity of the depletion area, and C_{OX} is the oxide intrinsic capacitance [30]. The bulk charge's purpose is to increase the threshold voltage. Though with short channel, the bulk charge does not make that great of an impact because some of the field lines deriving from the bulk charge are cancelled in the p^+ islands. Hence, in short-channel MOSFETS the threshold voltage is expected to be lower. The threshold voltage equation only takes in account the edge-effects of Q_B [30]. The flatband voltage, V_{FB}, is defined by the metal-semiconductor work function difference and the fixed charge in the oxide, hence it is constant beneath the channel (Equation 10).

Equation 9: Threshold voltage [30]

$$V_T = V_{FB} - 2\Phi_F - \frac{Q_B}{C_{OX}}$$

Equation 10: Flatband Voltage

$$V_{FB} = \Phi_M - \Phi_S = \Phi_M - \chi - \frac{E_G}{2q} + V_T \, ln\,(\frac{N_D}{n_i})$$

Fig.21 shows the simulated data from TCAD for various concentrations against the experimental data. For the channel length of 0.5µm and 1µm, $|V_T - V_{FB}|$ simulated is smaller than the experimental. This outcome can be because of the greater effect of charge sharing and drain induced barrier lowering (DIBL). For the doping concentration of 1e15 cm^{-3} , the threshold voltage could not be extracted because of the presence of too much short channel effect and channel length modulation.

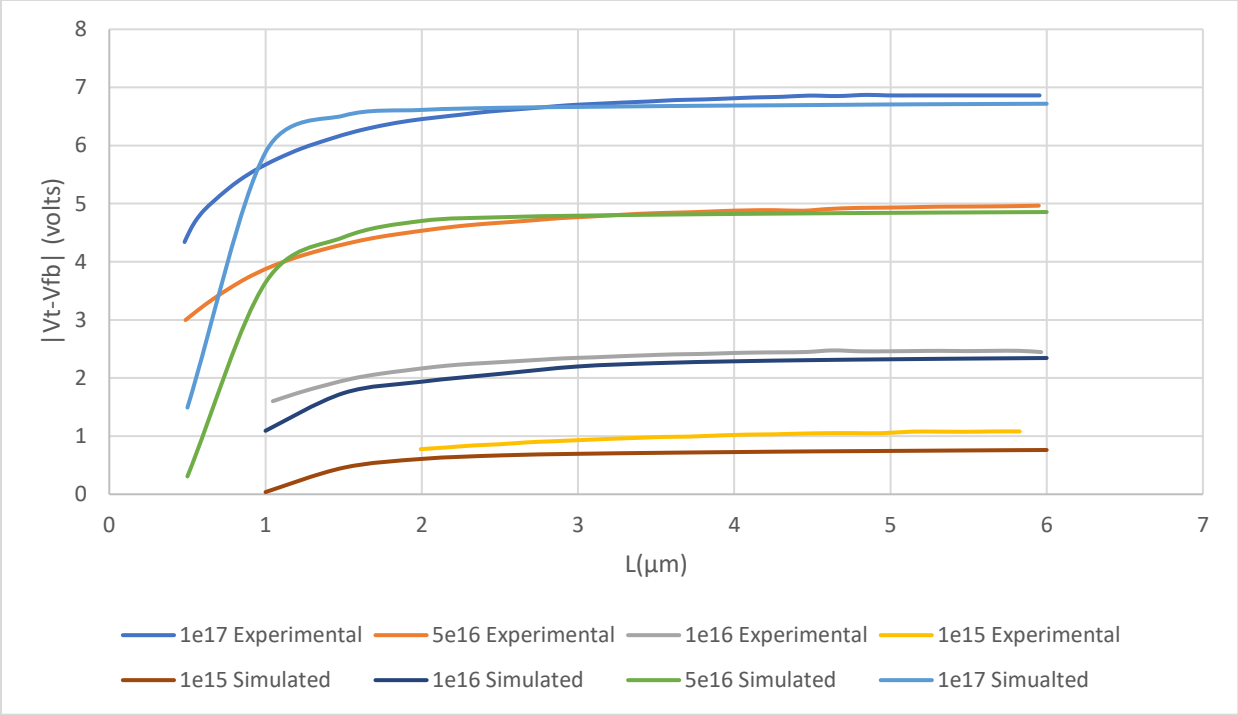

Fig. 21. $|V_T - V_{FB}|\ vs. L\ (channel\ length)$ with back gate bias of 5V. Experimental data from [30] is displayed in comparison to the simulated data.

Overall, the simulated results matched the experimental, hence the research continues to implement the parameters and settings needed to achieve convergence near 4K, which was mentioned in detail in Chapter 3 of this thesis. From the results, the threshold voltage is extracted for the various temperatures and channel lengths. The findings are evaluated and then optimization is performed on a NMOS with p-type well. The variables for this device include gate lengths of 0.2µm, 0.5µm, and 1µm in which the P-Well is 1e16cm^{-3}. A drain bias of 0.1V is applied as well as 1V and extract the threshold voltages from $I_D - V_G$ curves at various temperatures. This will be discussed in detail in the following section.

5.3 Results and Discussions

Fig.22 shows the threshold voltage, V_{th}, against various channel lengths for temperatures ranging from 50K – 300K where $V_D = -1V$ and $V_B = 0V$. Fig.23 shows the threshold voltage, V_{th}, against various channel lengths for temperatures ranging from 50K – 300K where $V_D = -1V$ and $V_B = 5V$. What can be inferred from Fig.22 and Fig.23 is that the short channel effect (SCE) is improved at lower temperatures. Improved SCE implies that overall device performance is improved as the gate length is reduced at cryogenic temperatures. The significance of this finding is that unwanted effects like SCE that were apparent as transistors were being scaled down to reduce the power dissipation, improve the resistance and capacitance, etc. is plausible if operated down to cryogenic temperatures.

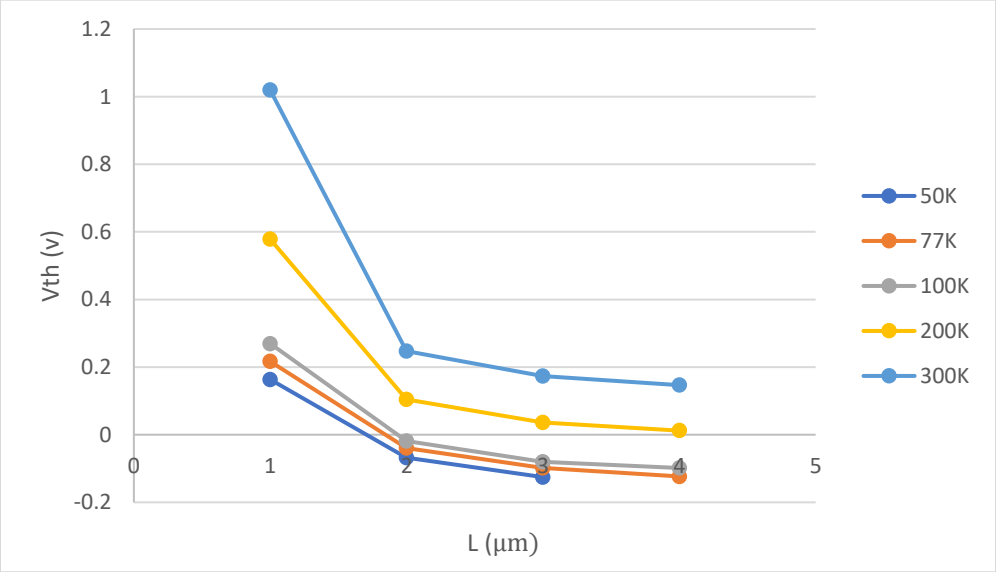

Fig. 22. V_{th} vs. L for 50K, 77K, 100K, 200K, and 300K. N_D=1 × $10^{15} cm^{-3}$, $V_D = -1V$, and $V_B = 0V$.

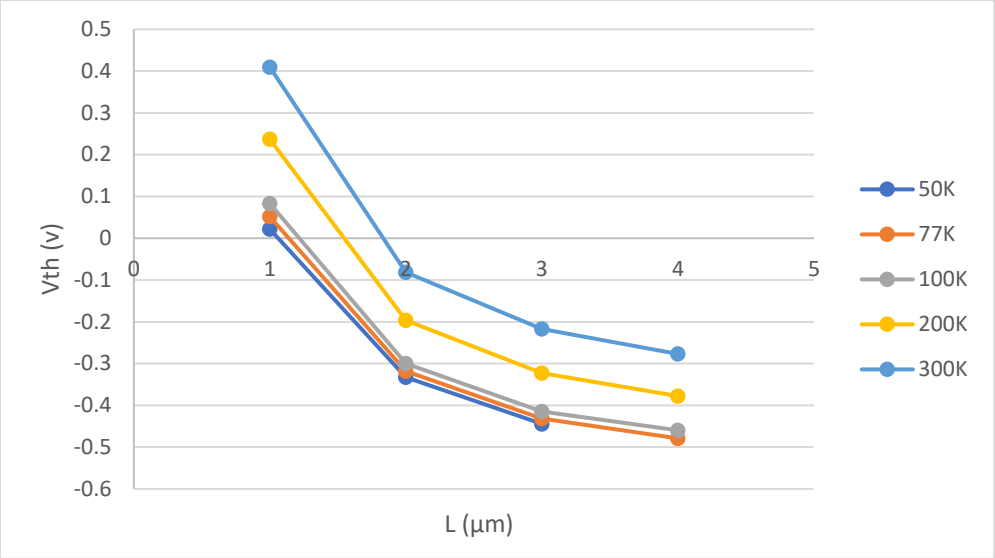

Fig. 23. V_{th} vs. L for 50K, 77K, 100K, 200K, and 300K. N_D=1 × $10^{15} cm^{-3}$, $V_D = -1V$, and $V_B = 5V$.

In Fig.24 and Fig.25 are the threshold voltage extractions for the NMOS device with P-type well. Fig.24 has an applied drain vias of 0.1V while Fig.25 has a drain bias of 1V. For gate length, L_g, of 0.2µm the extracted data was inconclusive because of the length being too short. To see how DIBL performs at lower temperatures, the difference of V_{th} between 0.1V and 1V is found and then plotted the difference for various temperatures for each gate length to get the DIBL (Fig.26). From Fig.26, the gate length of near 1µm, DIBL does slightly reduce at lower temperatures, while a gate length of 0.5µm DIBL is surely improved at lower temperatures. This is the case because there is less subthreshold slope degradation because of less punch-through and drain control.

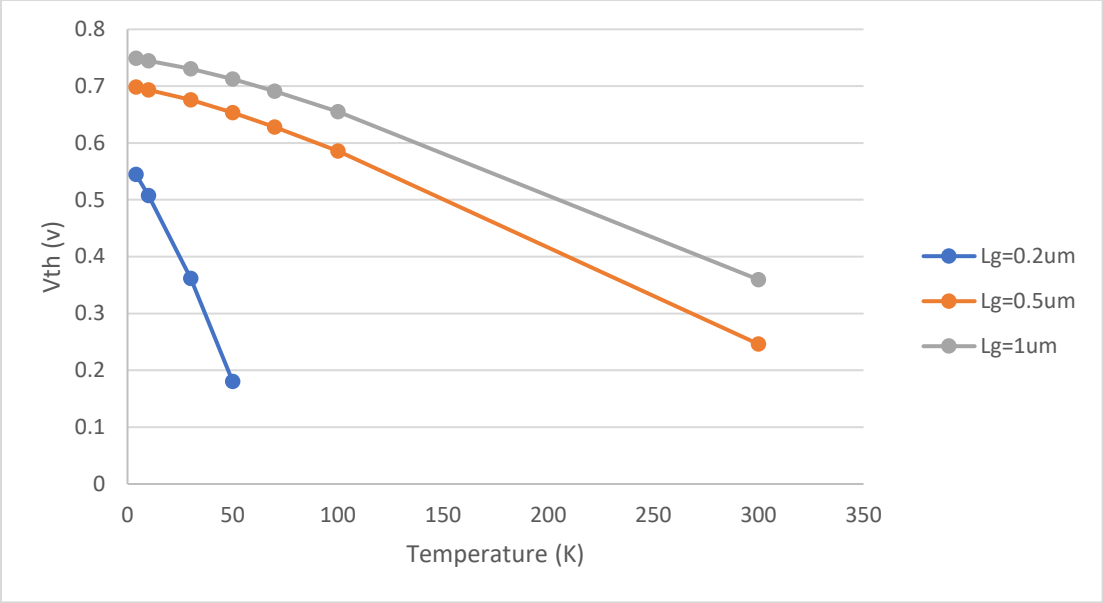

Fig. 24. $V_{th}\ vs. Temperature\ for\ various\ gate\ lengths\ and\ V_D = 0.1V.$

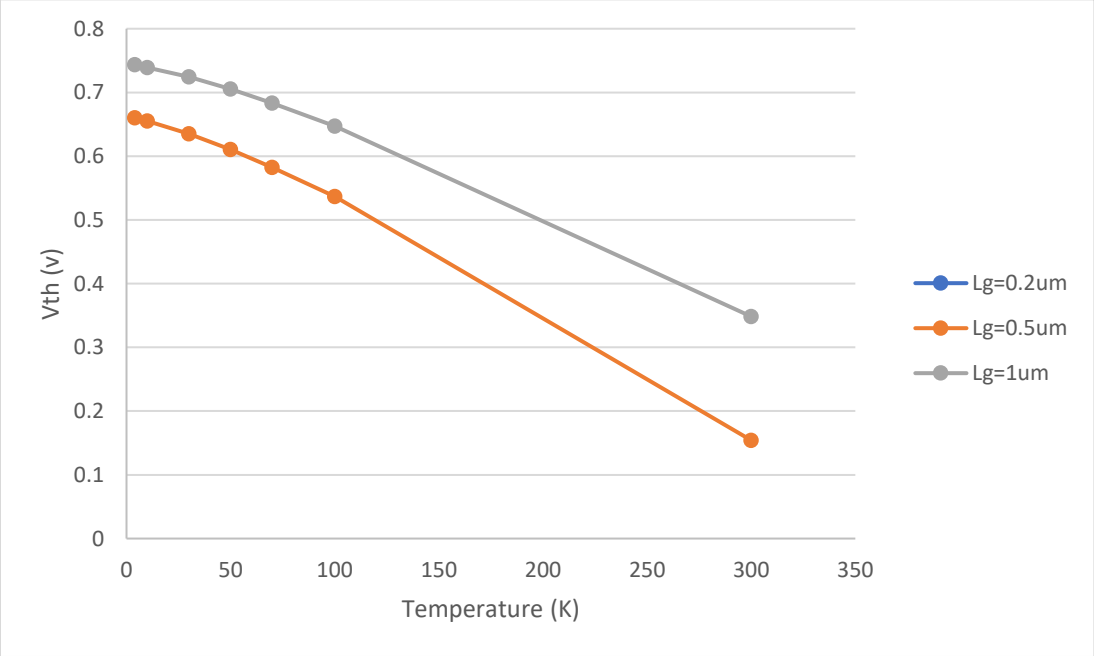

Fig. 25. $V_{th}\ vs. Temperature\ for\ various\ gate\ lengths\ and\ V_D = 1V.$

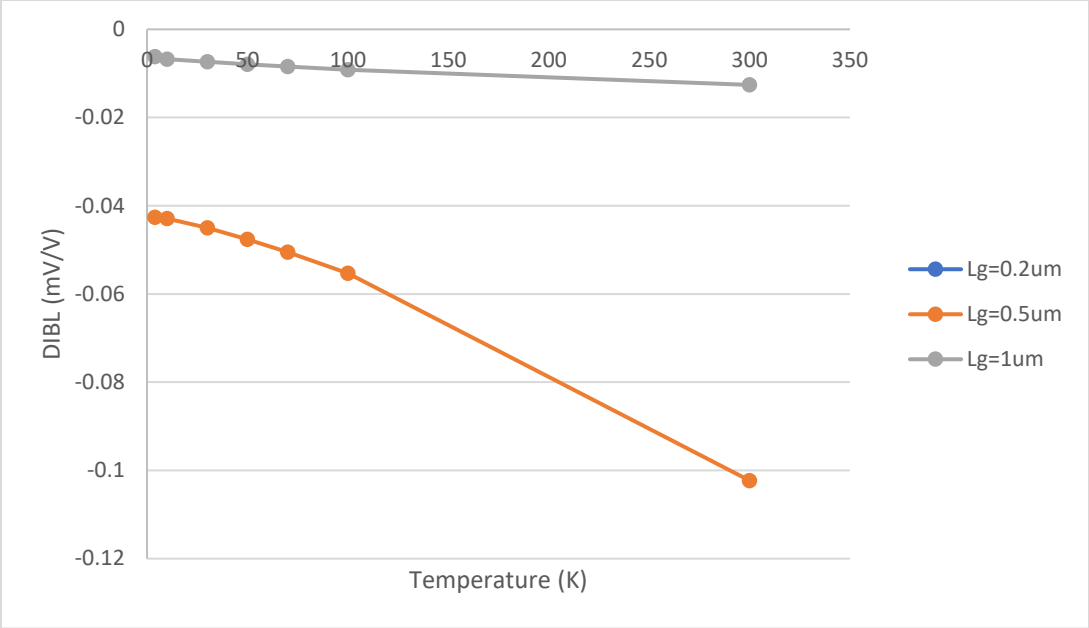

Fig. 26. DIBL vs. Temperature for various gate lengths, L_g.

5.4 Conclusion

This chapter intended to apply the calibrated parameters and settings from Chapter 3 for cryogenic temperatures for devices in TCAD. Specifically, the optimization of pMOSFET and NMOS with P-Well. The findings indicate the devices end up having improved short channel effect (SCE) and drain induced barrier lowering (DIBL) when operating at cryogenic temperatures.

6 CONCLUSION

In closing, the research conducted was the first to calibrate a set of parameter and settings to be applied at temperatures of 300K and 5K using TCAD to simulate and model the ON-state characteristics and SS of NMOS, which was also validated against the experiment. In particular, the results indicated that by placing oxide/channel interface acceptor traps close to the conduction band (~ 30meV), can model the abnormal SS that can be seen from 300K – 4K. Furthermore, the research aims to develop and calibrate a unified field-dependent and temperature-dependent mobility model in Si for both electron and hole in specific transport directions. The model successfully captures the negative differential velocity, and the curve fittings are smooth which allows to correctly deduce the carriers at 4K. Finally, the research aims to optimize MOSFET devices by applying the parameters and settings model introduced in Chapter 3. The findings from these simulations imply improvement in SCE at cryogenic temperatures.

To further optimize cryogenic CMOS, there are plenty of undesirable effects at cryogenic temperatures that need to be evaluated. Moreover, deeper research can be done in understanding the interface traps at cryogenic temperatures. The implementation and review of the electron and hole mobility model would be essential to its application to TCAD simulations. This in turn would make the model more reliable and effective. Lastly, the optimization was only carried out on the MOSFET, future work would include the implementation on various devices such as SIO, FinFET, etc.

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