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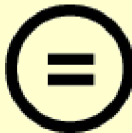

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Master's Thesis

Heterogeneously integrated DBR laser

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Department of Electrical Engineering

Ulsan National Institute of Science and Technology

2022

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Heterogeneously integrated DBR laser

A thesis/dissertation submitted to
Ulsan National Institute of Science and Technology
in partial fulfillment of the
requirements for the degree of
Master of Science

Jinhyun Cha

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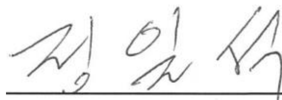

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Heterogeneously integrated DBR laser

Jinhyun Cha

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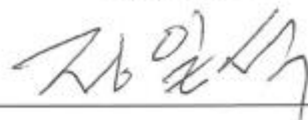

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Abstract

The importance of data is increasing day by day. The whole world is communicating using data as optical link. More and more people are using data. So, data traffic also increases rapidly. Therefore, there is a need to develop faster and more efficient lasers used for long-distance data communication. And this laser can be used in data centers for long-distance optical communication and can be applied to future technologies such as 5G mobile network, artificial intelligence, cloud computing and storage and Internet, which are services we will use.

What are the requirements that we need to satisfy? First, a laser having a wavelength band of 1310 nm or 1550 nm is required. Second, high power efficiency is required for sufficient output power for data transmission. For better long-distance communication, single mode and narrow linewidth are required. Finally, it must be integrated on silicon in order to use for the silicon photonic chip.

Through this study, we designed a structure that reduces optical loss and increases transition efficiency so that it can be used in high power lasers. By designing the taper structure through BPM and Lumerical commercial simulation, we proposed a structure to reduce scattering loss when transitioning from epitaxy to silicon waveguide, and to reduce optical loss by adjusting the thickness of each layer of epitaxy. In addition, when the light emitting device generates a lot of heat, the output power is reduced. In order to solve the problem, an experimental method for efficient heat dissipation was applied. By applying this, it will be possible to achieve a high-output device.

We have demonstrated the light emitting device. Our target is the laser, but fabricated device is not lasing, just operating like LED. The reasons were the problem of heat caused by resistance and the problem of epitaxy dislocation. We considered the problem and suggested a solution. Further work will allow us to make lasers with better properties than we currently have.

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List of Acronyms

AFM	**Atomic Force Microscopy**
ALD	**Atomic Layer Deposition**
BOX	**Buried Oxide**
BOE	**Buffered Oxide Etchant**
BCB	**Benzocyclobutene**
CVD	**Chemical Vapor Deposition**
CW	**Continuous Wave**
CMOS	**Complementary metal-oxide-semiconductor**
DBR	**Distributed Bragg Reflector**
DFB	**Distributed Feedback**
DIW	**Deionized Water**
DWB	**Direct wafer bonding**
DVS-BCB	**Divinylsiloxane-bis-benzocyclobutene**
IPA	**Isopropyl alcohol, Isopropanol**
LD	**Laser Diode**
LED	**Light Emitting Diode**
MQW	**Multiple Quantum Wells**
MOCVD	**Metal-Organic Chemical Vapor Deposition**
OM	**Optical microscope**
PD	**Photodiode**
PECVD	**Plasma Enhanced Chemical Vapor Deposition**
PIC	**Photonic integrated circuits**
QW	**Quantum Well**
RIE	**Reactive ion etching**
RT	**Room temperature**
SCH	**Separated Confinement Heterostructure**
SEM	**Scanning Electron Microscope**
SOI	**Silicon-On-Insulator**

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Chapter 1. Introduction

1.1 Motivation

Data has recently become the world's most important and valuable resource and has become a part of our lives. And, according to companies' market site as of 2022, 4 out of the 5 largest companies in the world are IT companies providing hardware and software [1]. As can be seen from this data, the IT industry using data is the most important industry closely related to our lives. This is because people easily use internet shopping, social network services, streaming, etc. using data-enabled smartphones and computers, and access and search for desired information from anywhere. Since all of this is done using data, the amount of data used increases exponentially. A new field in which research is being actively carried out, like the artificial intelligence (AI) and Internet of Things (IoT), is certain to further increase data usage in the future. Accordingly, there is a need for improvement of interconnects that efficiently process data transfer rates and transfer amounts.

Figure 1.1: Google servers in St.Ghigslain, Belgium

Hybrid in-plane laser is used to send and receive signals at a distance of 1 km or more. It is mainly used for optical connection within the data center shown in Fig.1.1, and it is also used for long-distance communication and 5G/6G backbone. Not only the data processing needs to be fast, but also the ability to send accurate signals over long distances is also required.

In addition, for compatibility with Si-based devices used for photonic integrated circuits (PICs), an optical device must be fabricated on a silicon substrate and process conditions that do not weaken the characteristics of the passive device are required. This is called a complementary metal-oxide-

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semiconductor (CMOS)-compatible process, which means that it can be processed on SOI wafers using standard CMOS-processing tools and recipes (like dry etching and deposition).

1.2 Silicon photonics

Silicon (Si) is the most used semiconductor material for electronic applications due to its abundant reserves, low prices, high yields and high-volume manufacturing of electronic systems. It is widely used in the recently developed optical device field, for example, a CMOS image sensor, a photodetector, and the like. Therefore, Silicon (Si) is the most used semiconductor material for electronic applications. Due to its abundant reserves, low prices, high yields and high-volume manufacturing of electronic systems. Fig.1.2 below shows the packaging of the Si photonics chip. There are various components on silicon photonics platform like ultra-low loss waveguide in passive, Si/III-V optical amplifiers, Lasers, modulators and detectors in active section [2].

Figure 1.2: IBM's first on-package silicon photonic chips [13].

According to Yole's report, a market research company shown in Fig.1.3, data center and other new applications will bring a billion-dollar market for silicon photonics technology by 2026 [4]. Si photonics is single-mode so it has merit from the increased use of single mode fiber (SMF) in mega data centers. Si photonics is seen as a realization method for chip-level optical interconnect.

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2020-2026 silicon photonics die forecast by application

(Source: Silicon Photonics 2021 report, Yole Développement, 2021)

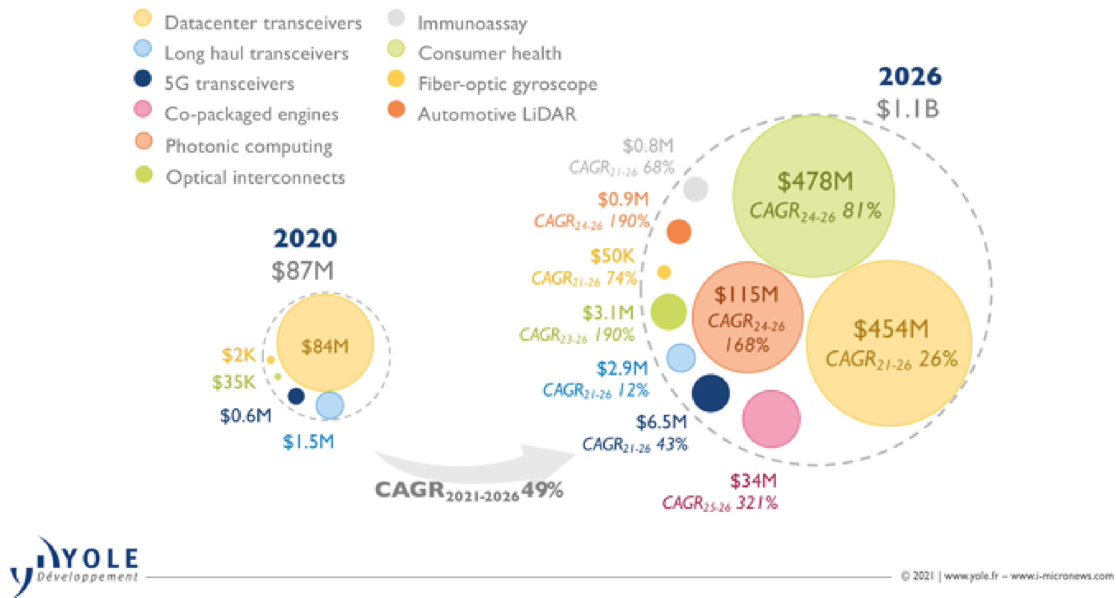

Figure 1.3: Schematics of silicon photonic 2020-2026 forecast by application [4].

Several approaches in which silicon photonics are used as a light source are shown in Fig.1.4 [5]. It will be briefly described here. The first approach is to couple the laser from the fiber shown in Fig. 1.4(a) to the silicon chip. This off-chip light source has the advantages of excellent temperature stability and easy replacement of the laser, but has disadvantages such as a very large coupling loss between the laser source and the chip and high packaging price [3].

The second approach is to couple the prefabricated compound semiconductor laser shown in Fig.1.4(b) to the silicon chip through bump bonding. Although it has a relatively high coupling efficiency compared to the first method, very precise alignment (<micro-meter) is required in the bonding process for that purpose [5].

The third method is the on-chip method shown in Fig.1.4(c). This is a method of attaching a hybrid laser directly on Si using a standard CMOS-compatible process (lithographic and etching). This eliminates the high precision alignment step of the second method and realizes alignment through a lithographic step. Wada et al. first demonstrated a III-V Fabry-Perot laser, fabricated on a SOI wafer via direct wafer bonding [6]. This shows an evanescent laser in which an optical mode is formed in the III-V layer and it is transferred to a silicon waveguide. This is called heterogeneously (or hybrid) integrated laser.

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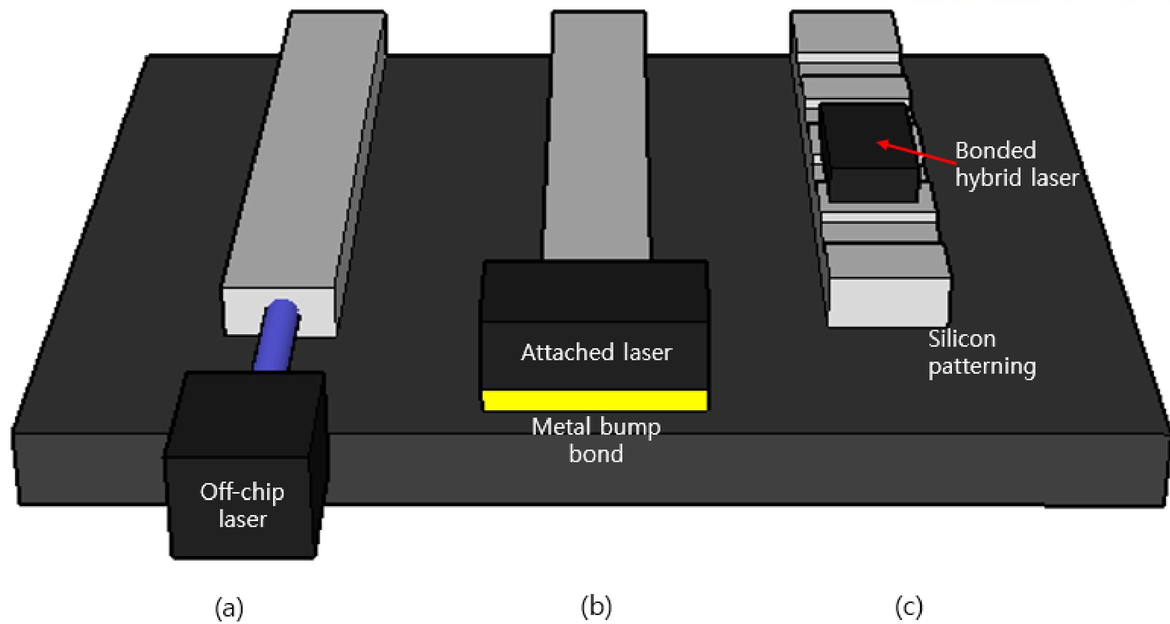

Figure 1.4: **Three Methods to supply laser light to a photonic integrated circuit on the silicon.** (a) coupling off-chip lasers to Si waveguide. (b) Coupling method by attaching pre-fabricated laser to PIC using metal (or soler bump). (c) heterogeneously integrated III-V materials onto silicon to form a hybrid laser (on-chip laser).

1.2.1 Laser for silicon photonics

As above, Si is used in many devices, but there is a limit to its use as a light source. The limitation lies in the fundamental problem of the energy band structure of Si. Optical transition must obey the law of conservation of energy and momentum, but it is not satisfied in the case of Si. Direct bandgap means that the wave vector of the highest point of the valence band and the lowest point of the conduction band is the same; that is, they share the same crystal momentum. As shown in the left side of Fig.1.5, radiative recombination for stimulated emission occurs rapidly, and electron-hole pairs are efficiently recombined. Therefore, materials with direct bandgap are essential to make light emitting devices (like III-V compound semiconductors, gallium arsenide (GaAs) and indium phosphide (InP) for example).

Indirect bandgap means that the wave vectors of two points are different. As can be seen from the right side of Fig.1.5, Si is a material with a different indirect band gap, that is, the highest point of the conduction band and the lowest point of the wave vector of the valence band. Free electrons exist in the X valley of the conduction band, which does not match the wave vector of the free hole in the valence band. Therefore, if the radiative recombination leading to the emission of the photon is to occur, a third particle (phonon) that can lead to an additional momentum (wave vector) change must be involved. Therefore, the process appears at a very slow rate [7]. The major carrier transition processes for non-

radiative recombination such as Si are Auger recombination and free-carrier absorption. Auger recombination is when electrons (or holes) absorb energy from electron hole recombination and are excited to a higher energy level. Free-carrier absorption is a process in which free electrons in the conduction band absorb photons and jump to higher energy levels [7]. In high-level carrier injection device or heavily doped layers, free-carrier loss is orders of magnitudes higher than the material gain [8].

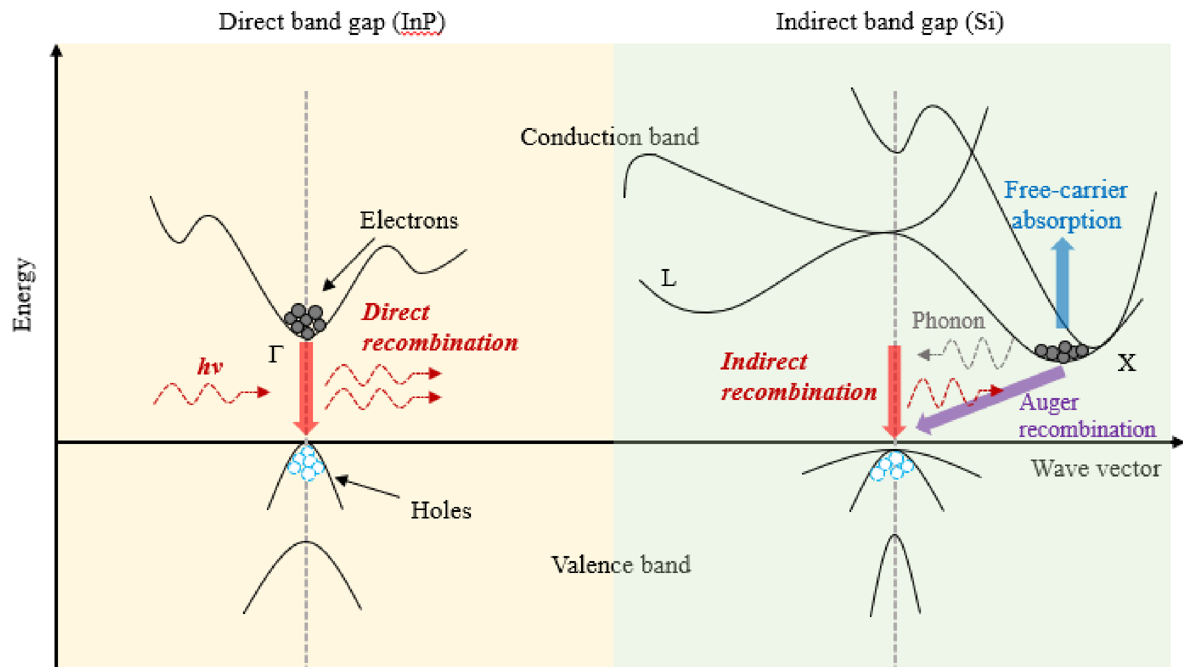

Figure 1.5: Simplified energy band diagrams and major carrier transition processes in direct and indirect materials. In a direct band gap structure (left, such as InP), electron-hole pair (EHP) recombination almost results in direct recombination and then emits the photon. In an indirect band gap structure (right, such as Si), non-radiative transition such as Auger recombination and free-carrier absorption occurs, and indirect recombination exists simultaneously, resulting in little photon emission.

Since non-radiative transitions have very low lifetimes and occur at a relatively fast rate, the internal quantum efficiency of light emission in Si is very poor [7].

Various studies on hybrid photonics laser have been conducted due to various advantages of using Si substrate.

Epitaxial lasers growth on Si

It is a laser made by growing other materials on a Si substrate. There is a method of growing Germanium-based materials and a method of growing III-V materials. Germanium (Ge) is an indirect bandgap material, but the bandgap can be engineered using strain resulting from doping and thermal expansion coefficient mismatch between Si and Ge [9].

Direct growth of III-V direct bandgap materials is difficult. The reason is that when compared to Si, GaAs and InP have mismatch of lattice constants of 4.1% and 8.1%, respectively. And the thermal expansion coefficient mismatch was also 120.4% and 76.9%, respectively [7]. This mismatch causes dislocation, and the dislocation acts as a non-radiative recombination center, and the efficiency is low.

Solder bump hybrid lasers

This method is shown in Fig.1.3(b). This is a method of bonding a fully pre-fabricated laser chip on a Si substrate using solder bumps (or metal) [5]. It has been studied as a good approach because it is made of a direct bandgap material, guarantees laser efficiency, and solves problems caused by lattice mismatch. However, as mentioned earlier, this method requires precise alignment for good coupling efficiency. And it is not CMOS-compatible because a separate process is required.

Wafer bonded hybrid lasers

As shown in Fig.1.3(c), this method attaches III-V active material to the SOI platform and makes a laser. The bonding method will be described in detail later. III-V epitaxy is grown on its own substrate, ensuring quality for dislocation and good optical properties. The unpatterned III-V wafer is bonded to the patterned SOI wafer and the thick III-V substrate is removed through selective wet etch, leaving only the active region. Lasers can be fabricated using CMOS-compatible processing, and alignment problems can also have high precision through a lithography step [5]. The light generated in the III-V active region is transmitted to the silicon waveguide by evanescent coupling, and the confinement factor for high power can also be engineered by modifying the waveguide width. Depending on the cavity and patterning method on SOI wafers, there are Fabry-Perot cavity [10] and distributed feedback (DFB) lasers [11], and distributed bragg reflector (DBR) laser [12]. It is divided into in-plane and vertical-cavity according to the direction in which light is output.

1.3 Recent progress of hybrid in-plane lasers

The laser used in the data center is generally placed on-board on the Si phonics chip. Laser basically has the effect of decreasing the output power as the number of thermally excited carriers increases when the temperature is high. Therefore, research on technology to improve cooling is also in progress.

In order to reach high data rates, the 3-dB frequency bandwidth of lasers needs to be increased. However, bandwidth cannot be increased simply by increasing the driving current. A figure of merit to characterize such an ultralow threshold and ultrahigh speed laser is the modulation current efficiency factor (MCEF), defined as [14]:

$$MCEF \equiv \frac{f_{3dB}}{\sqrt{I-I_{th}}} \tag{1.1}$$

where f_{3dB} is 3-dB frequency of a small-signal response spectrum, I is the driving current and I_{th} is threshold current of laser. A diode laser with high MCEF can achieve operating speed at low current and has high energy efficiency and less self-heating characteristics.

Communication lasers are generally in the 1310 nm or 1550 nm wavelength because natural dispersion minimum of optical fiber. As shown in Market research, the size of the device used in the data center is very large, so research in this area is being actively conducted. Such heterogeneously integrated lasers include standard Fabry-Perot cavity, and DFB, DBR lasers, and photonic crystal (PhC)-based lasers.

Laser for using long-distance communication is required narrow linewidth. The linewidth is the FWHM (Full-Width-Half-Maximum) of signal. The linewidth and confinement factor is defined as:

$$\Delta f_{spon} = \frac{\Gamma R'_{sp}}{4\pi N_p}\ , \tag{1.2}$$

$$\Gamma = \frac{\iint_{region} E(x,y)E(x,y)^* dxdy}{\iint E(x,y)E(x,y)^* dxdy} \tag{1.3}$$

where N_p is photon density, Γ is the confinement factor in active layer and R'_{sp} is the single-mode spontaneous emission rate from total band-to-band spontaneous emission rate [16]. Confinement factor, gamma, obtain the integration of the E-field intensity of the desired region over the integration of the entire E-field intensity. Nowadays, many studies are conducted to reduce the active volume through direct growth methods, etc. and to increase the confinement factor [45, 46].

To achieve the narrow linewidth, we should decrease confinement factor or R'_{sp}. However, in order to obtain a lot of gain for high power laser, the confinement factor overlapping QW must be high. Therefore, the confinement factor cannot be reduced. Therefore, R'_{sp} must be reduced for narrow linewidth. R'_{sp} is the inversely proportional to the cavity length. Therefore, a laser for long-distance communication is used with a long cavity, that is, a laser with a large active volume.

Major progress of hybrid in-plane lasers came from the University of California in Santa Barbara (UCSB) group. According to a paper [12] reported by A. W. Fang in 2008, the performance of a silicon evanescent laser using a distributed bragg reflector has a threshold current of 65 mA and an output

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power of 11 mW. And the data rate of this device is up to 4Gb/s in case of direct modulation. They also designed a very shallow etch depth waveguide to minimize scattering loss and increase modal volume. And by using additional grating to the basic DBR, an Extended-DBR (E-DBR) structure was created to achieve a Lorentzian linewidth of 1kHz for an ultralow noise laser. And it demonstrated a strong output power of 37mW [15,16]. Also, for the E-DBR grating used in [17], a narrower Lorentzian linewidth of 320 Hz and an output power of 24 mW were achieved by using a Si_3N_4 material with a lower propagation loss than a silicon waveguide as a waveguide.

1.4 Thesis contribution and organization

1.4.1 Thesis contribution

The main goal of my research is to propose the high-power laser. To achieve our goal, we need to increase the efficiency of transition from III-V to Si waveguide. Also, we design a structure that minimizes transition loss by finding an appropriate adiabatic taper structure for III-V epitaxy and Si waveguide and optical loss by adjusting thickness of epitaxy layers.

- As a method to increase transition efficiency, there is a method to optimize the epitaxy layer. In the case of an in-plane laser, if the distance between Si and III-V active layer is far, the efficiency is lowered. So, we will find the appropriate thickness.
- In addition, if there is no taper structure in epitaxy, the efficiency decreases sharply. Therefore, by designing an appropriate taper structure, a structure that can take maximum efficiency is designed.
- For single mode operation, the width of the waveguide inside the cavity and the width of the waveguide outside of the cavity are optimized so that it can be used for long-distance communication lasers.

In addition, a heterogeneously integrated laser using a DBR mirror will be made and measured directly, and the results will be reviewed.

1.4.2 Thesis organization

In this thesis, we present the results of simulations for an efficiency-enhancing hybrid DBR laser. And through the simulation, we will directly manufacture and measure the laser. The main contents of this thesis includes:

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Chapter 1, Introduction, describe research motivation and introduce optical interconnect. In addition, the market economy and research progress of silicon photonics that have been conducted and have a high potential for development were reviewed.

Chapter 2, Theory and design principle, describes the theory required for in-plane lasers. In addition, simulation results and device design principles to increase the efficiency of heterogeneously integrated lasers will be described.

Chapter 3, Wafer bonding of III-V to SOI, describes the method of wafer bonding, which is the most important step in making a heterogeneously integrated laser. Starting with pure direct wafer bonding, the process sequence and results of adhesive bonding that can be used even if the epitaxy surface quality is poor will be presented.

Chapter 4, Fabrication and discussion of device, includes process results for heterogeneous lasers. Images for each process and device fabrication will be described in detail. Problems encountered during the process and solutions will also be described. Then, characterization results and considerations are included.

Chapter 5, Conclusion, will summarize the main results of this paper and suggest improvements, future progress, or corrections based on the results of the fabricated device.

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Chapter 2. Design principle

Semiconductor laser theory is very complex because it is necessary to understand all optical, electrical and thermal phenomena to explain laser operation [18,19]. These phenomena interact and couple with each other, and for a perfect design, quantum mechanical phenomena of the III-V active region must also be considered. The simulation also requires rigorous standards because the results vary greatly depending on minor setting values such as boundary conditions and simulation regions.

In this chapter, we will examine the basic theories of heterogeneously integrated laser operation, simulations of the structures of III-V epitaxy and Si waveguides that increase the efficiency proposed above, and how much expectations can be obtained from the fabricated devices. The key things of simulation in this chapter are to optimize the thickness of n-contact layer of epitaxy and taper structure of Si and III-V epitaxy. We are going to develop III-V and Si taper design from grating design starting with general hybrid laser structure.

2.1 General structure of the hybrid III-V/Si laser

The hybrid evanescent III-V/Si laser consists of III-V epitaxial layer stack bonded on Si rib waveguide patterned on a silicon-on-insulator (SOI) wafer. The general cross-sectional image of such the laser including optical mode is shown in Fig. 2.1.

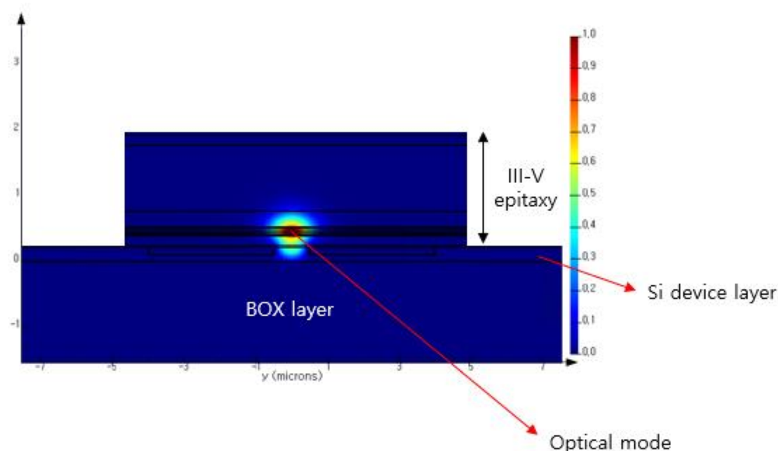

Figure 2.1: The concept of the heterogeneously integrated III-V/Si waveguide laser

The III-V epitaxy, consisting a mesa and an n-type contact layer is electrically pumped to form the population inversion in the active region comprising multiple quantum wells (MQWs). The reason why

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population inversion is necessary in lasers can be explained by looking at the band-to-band transition as shown in the Fig.2.2 below.

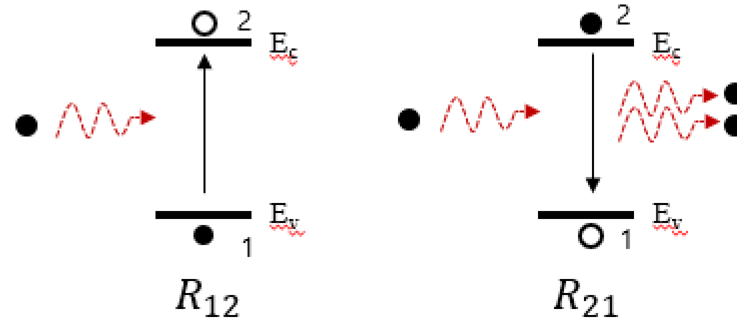

Figure 2.2: Band-to-Band radiative transition: stimulated absorption, stimulated emission.

First, in case of photon emission, photons with energy corresponding to Ec-Ev enter and elevate electrons in the valence band to the conduction band. This process is called stimulated absorption, and as a result, the incoming photons disappear and a new free-carrier is generated. After that, when another photon enters, it stimulates the free-carrier in the conduction band to recombine the carrier through the downward transition. This process is called stimulated emission, and as a result, two photons corresponding to Ec-Ev are emitted and contribute to light. Therefore, the more electrons in the high energy state, the stronger the lasing. Therefore, population inversion is important, and electrically pumped laser is achieved through current injection [18].

All these structures, including the III-V region and the SOI region, represent a hybrid waveguide. Design a more efficient structure through the contents to be developed later.

2.2 Epitaxy design

The overall structure of Epitaxy was inspired by [20] reported from UCSB. The role of each layer, from the super lattice, which is a layer close to the SOI (silicon-on-insulator) substrate, to the p-contact layer, is briefly described.

Super lattice layer

In case of the evanescent in-plane laser, the quantum well layer is only about 300 nm away from the III-V and SOI wafer bonding interface, so the conditions that may occur at the bonding surface are likely to adversely affect QW. To protect the QW, two pairs of lattice-matched InP/InGaAsP layers were installed as the first layer.

N-contact layer

A commonly used n-type InP doped with $1x10^{18}/cm^3$ was used as a contact layer. As described in Section 2.1, the evanescent laser requires a contact layer because it generates population inversion through electrical pumping.

Quantum Well and Barrier

As mentioned earlier, as the temperature rises in the laser operation, the free-carrier is thermally excited, leaving the quantum well and operating with current leakage. To prevent this, InAlGaAs material with high conduction band offset was selected [21]. Seven quantum wells were used to increase the confinement factor. The composition used the conditions provided by the company for the stability of epitaxy growth. The gain peak wavelength was selected to be 1300 nm. This intentional shift of the photoluminescence (PL) peak was designed at 1300 nm to compensate for the 'red-shift' of the peak wavelength as the temperature rises.

Electron blocking layer

To prevent electrons from escaping from the active region, an electron blocking layer (EBL) with a bandgap larger than the barrier layer was installed. Due to this layer, current leakage due to free carrier escape is reduced.

Separated confinement heterostructure (SCH) layer

In order to increase the quantum confinement factor, many optical modes should be located in the III-V region. The optical mode is attracted to the material with a high refractive index, $n_{Si} = 3.47$, $n_{InP} = 3.17$, where n is the refractive index of the material, so it is attracted towards Si. Therefore, a material with a high index should be present in the epitaxy region. Therefore, a composition corresponding to a wavelength of 0.9 μm was used for the bandgap [20].

P-type cladding layer

The p-type contact layer generally uses highly p-doped InGaAs. However, the material causes optical loss due to free-carrier absorption. Therefore, it is necessary to put a p-type cladding layer so that the optical mode does not overlap the p-type contact layer as much as possible.

P-type contact layer

A commonly used highly p-doped InGaAs was used. The doping concentration is $1x10^{19}/cm^3$.

2.2.1 Optimization of thickness of n contact layer

Hybrid laser has a hybrid (gain) section with III-V and Si waveguide to obtain optical gain and a waveguide section with only Si waveguide for output. In the gain section, the optical mode is concentrated in III-V, so when moving to the waveguide section, a design to increase transition efficiency using a taper structure should be considered. In this section, the SCH and cladding layers that affect the optical mode profile are fixed and the degree of mode transition according to the thickness of the n contact layer is investigated. For the simulation, beam propagation method (BPM) was used.

Simulation settings

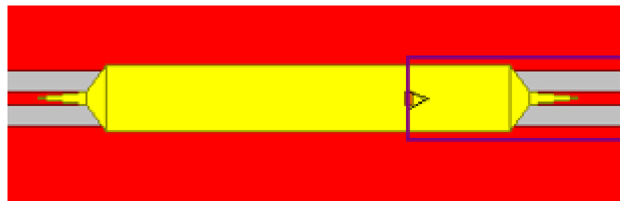

Figure 2.3: Structure of hybrid laser in BPM simulation. Epitaxy, yellow color, has a taper structure as described below. Si waveguide has also taper structure. It is marked with a red structure.

- Si waveguide is tapered from 2um to 0.6um over 50um, as will be explained later.
- Epitaxy layer has taper structure from 10um to 2um over 30um, then, 2um to 0.2um over 70um as shown in Fig.2.3.
- P cladding layer and p contact layer is 1um, 150nm, respectively.

The above conditions were set as fixed conditions, and the transition efficiency was obtained by changing the thickness of the n-contact layer to 150 nm, 130 nm, and 110 nm. The graph shown in Fig.2.4 is the result. The green graph is the extent to which the optical mode overlaps with the active layer, and the blue graph is the extent to overlap the Si waveguide. The leftmost graph is the case where the n contact layer is 110 nm. At this time, the area where III-V taper is finished is the part where the green graph is zero. The thinner the N contact layer, the better the efficiency, but for the convenience of the process, an appropriate thickness of 130 nm was selected.

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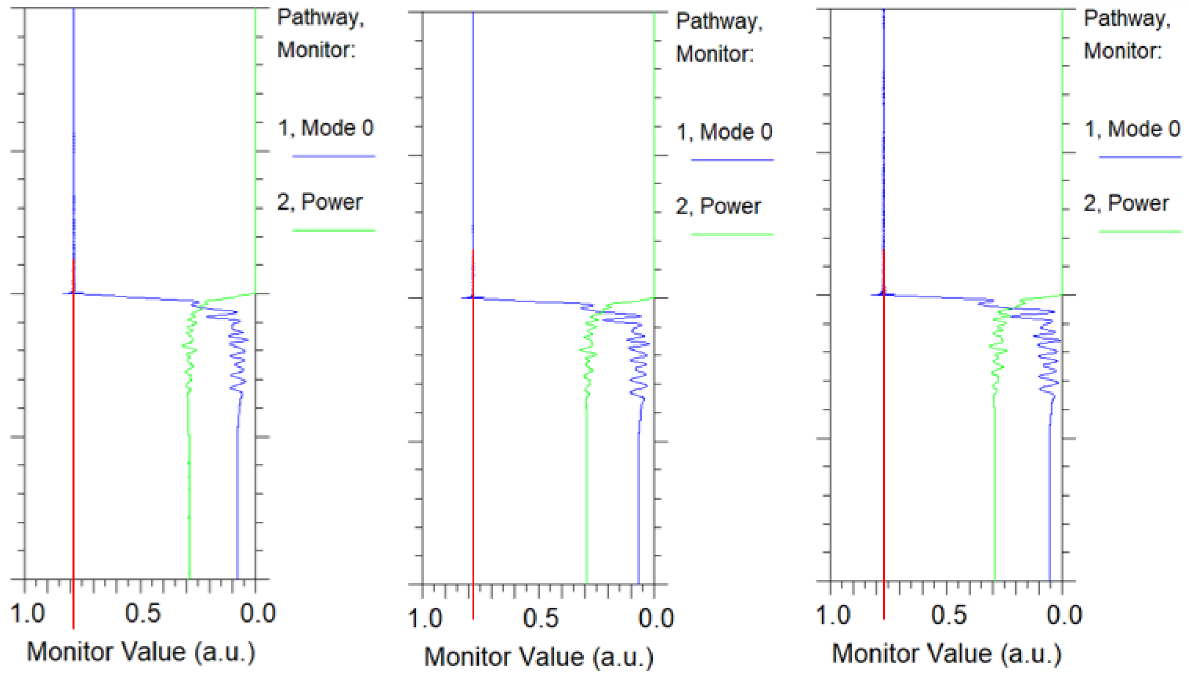

Figure 2.4: From the left, the graph for the n contact layer thicknesses of 110 nm, 130 nm, and 150 nm. The transition rates from III-V epitaxy to Si waveguide through the taper structure are 79%, 77.5%, and 76%, respectively.

2.2.2 Calculate the optical loss related to p-side layer

As mentioned earlier, the degree of overlap in the p contact layer with large optical loss decreases according to the p cladding thickness. The optical loss and absorption coefficient (α) are obtained by the following equations:

$$\alpha = \frac{4\pi k}{\lambda} \tag{2.2}$$

$$optical\ loss = \alpha * \Gamma \tag{2.2}$$

In Equation 2.1, k is the imaginary part involved in loss among the refractive indexes, λ is the wavelength, and Γ in Equation 2.2 is the optical mode confinement factor shown in Equation 1.3. That is, the confinement factor refers to how much the entire optical mode overlaps the area of interest.

The cross-sectional structure of the evanescent laser is shown in Fig. 2.5. InAlGaAs for the SCH layer, InP for the p cladding layer, and InGaAs for the p contact layer were used. Fig.2.6 shows the confinement factors when InP is 1 μm and 1.25 μm. The reason y1 and y2 are from -2 to 2 is because the width of the p contact metal is 4um and the area through which the current path passes acts as a loss. The results on the upper left and lower left are the confinement factors of InP and InGaAs, respectively, when InP is 1um. The results in the upper right and lower right corners are the confinement factors of InP and InGaAs when InP is 1.25um.

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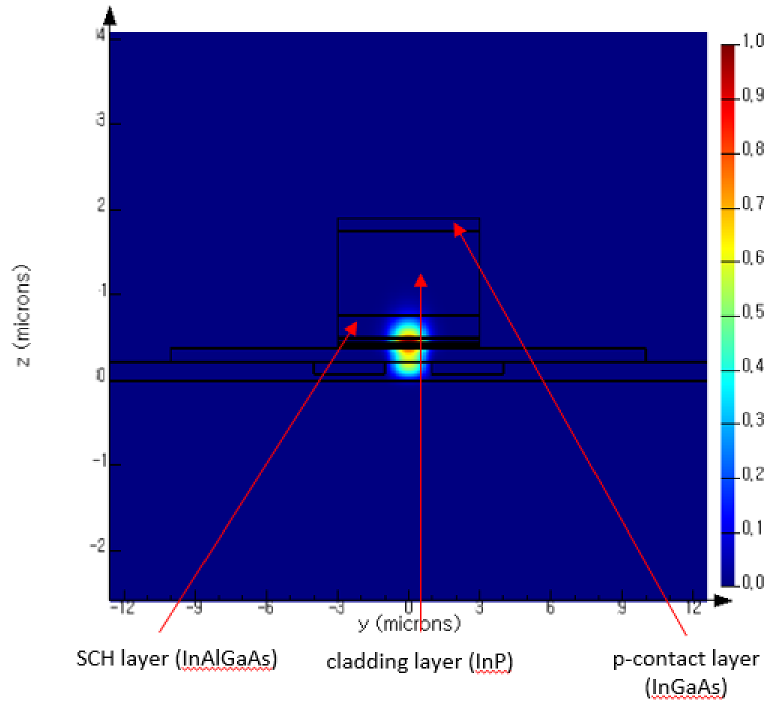

Figure 2.5: Cross-sectional structure of hybrid laser. InAlGaAs, InP, and InGaAs were used for the SCH, p cladding, and p contact layers, respectively. Confinement factor of active layer is about 10%.

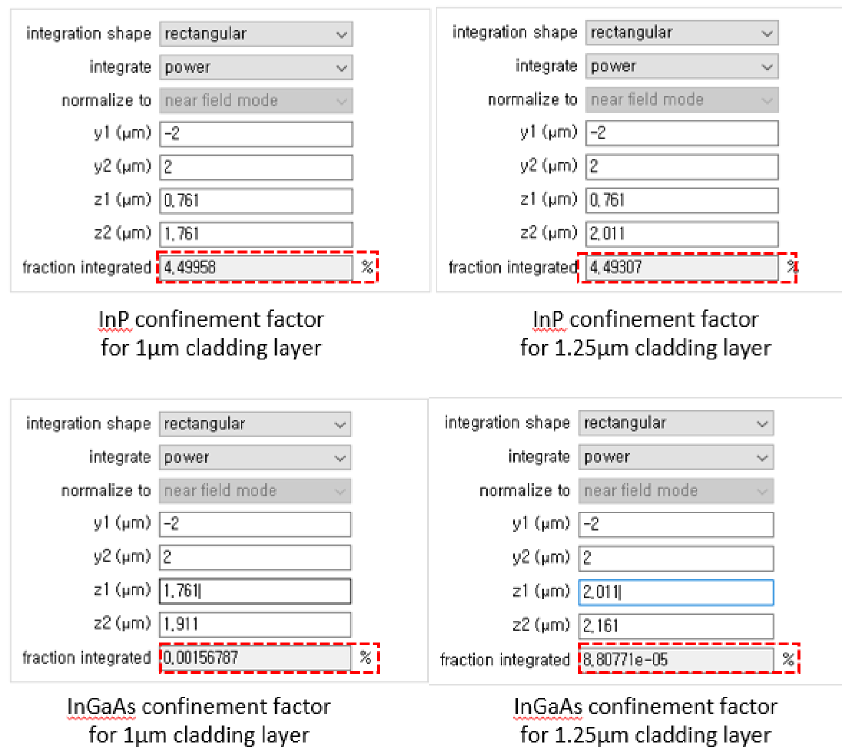

Figure 2.6: Confinement factor of InP and InGaAs when InP is 1um and 1.25um.

The imaginary of refractive index of InP and InGaAs are 0.0048 and 0.106 at 1310 nm wavelength, respectively. When the absorption coefficient is calculated using Equation 2.1, 460 cm^{-1} for InP and 10168 cm^{-1} for InGaAs are obtained. The meaning of this value is that the optical mode overlapping with InGaAs acts as a loss, and it is disadvantageous to a high-power laser because it cannot be obtained as a gain. Therefore, a higher gain can be obtained by minimizing the overlap with InGaAs.

The result of calculating the optical loss through Equation 2.2 is as follows:

- Optical loss of InP when cladding layer is 1um: 20.7182cm^{-1}
- Optical loss of InGaAs when cladding layer is 1um: 0.1593cm^{-1}
- Optical loss of InP when cladding layer is 1.25um: 20.6882cm^{-1}
- Optical loss of InGaAs when cladding layer is 1.25um: 0.009cm^{-1}

Although there is a certain difference, the 1um cladding layer is selected because it does not significantly affect the operation of the actual laser. There is an epitaxy image in Fig.2.7 below.

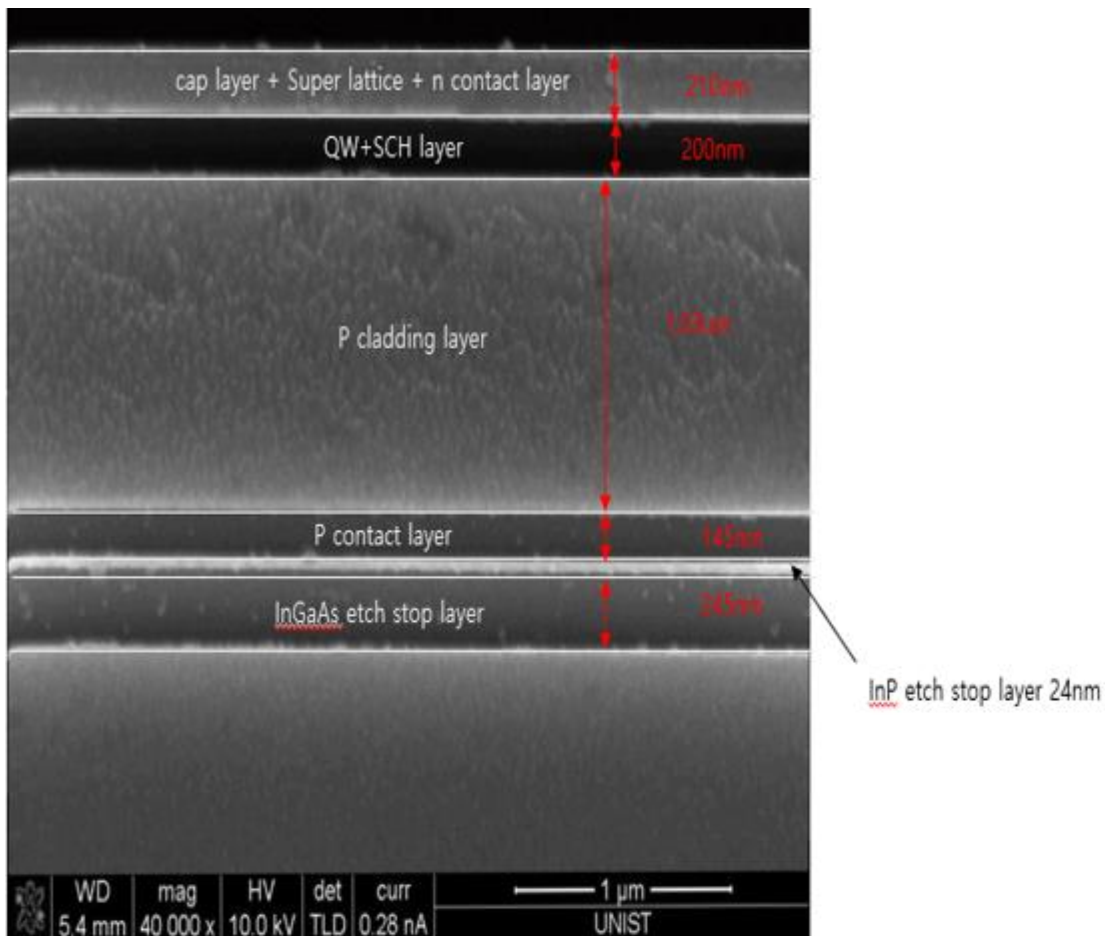

Figure 2.7: SEM image for epitaxy structure produced by PAM-XIAMEN company.

The epitaxy was manufactured by PAX-XIAMEN in China, and each layer was grown by metal-organic chemical vapor deposition (MOCVD). Epitaxy's target wavelength is 1300nm. The reason is that when the laser operates, the internal temperature rises, and the wavelength shifts to a longer

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wavelength under the influence of temperature. If you look at the photoluminescence (PL) data received from the manufacturer, it can be seen that there is no significant difference at 1293 nm.

Issue found in fabricated epitaxy

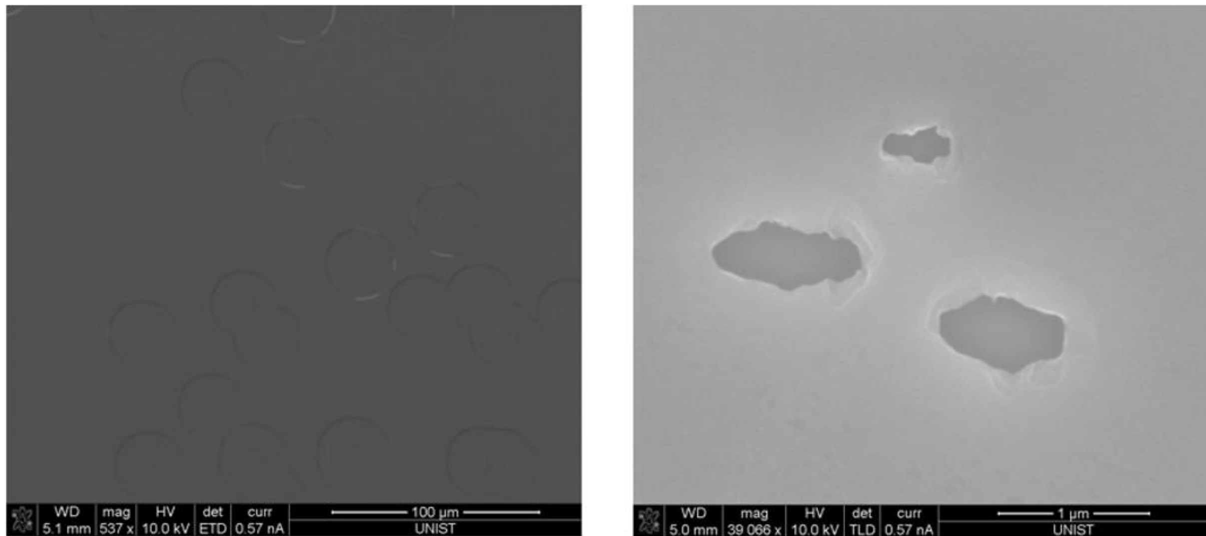

Figure 2.8: SEM images for surface of fabricated epitaxy. There are many holes that appear to be dislocations.

As a result of observing the surface through SEM, there were many dislocations. The impact of this will be covered in the discussion.

2.3 Taper structure design

When the optical mode transitions from III-V to Si, the scattering loss is greatly affected if the index changes rapidly. So, in order to change the index slowly, a taper structure with decreasing width is used. Also, for single-mode operation, the waveguide also applies taper. In this section, we will check multi-mode excitations when the waveguide is wide and find the appropriate width for single-mode excitation.

The effect of scattering loss is shown in Fig.2.9. Fig.2.9(a), (b) shows the structure without and with taper in epitaxy, respectively. If you compare the two graphs, you can see that the transition efficiency is very different. When epitaxy is terminated, the index changes abruptly and the scattering loss is very large [23].

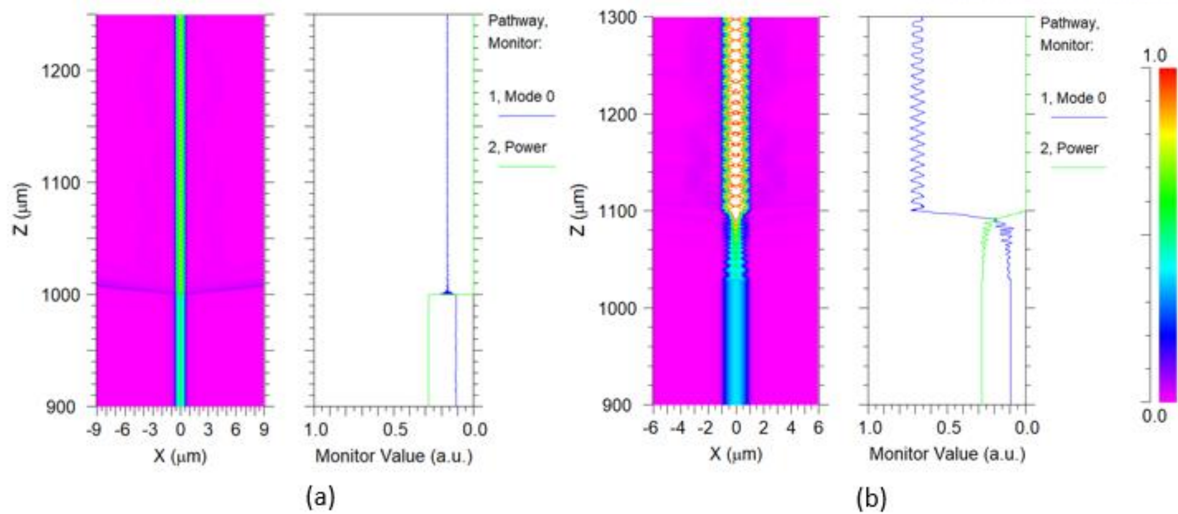

Figure 2.9: (a) Simulation of structure without taper in epitaxy. (b) When the taper structure is applied only to epitaxy. In this case, the silicon width is 2um.

Fig.2.9(b) shows that the Si waveguide has no taper and width of 2um. Looking at the graph, ripple occurred heavily, which is evidence of multi-mode excitations. For single-mode excitation, the width should be reduced.

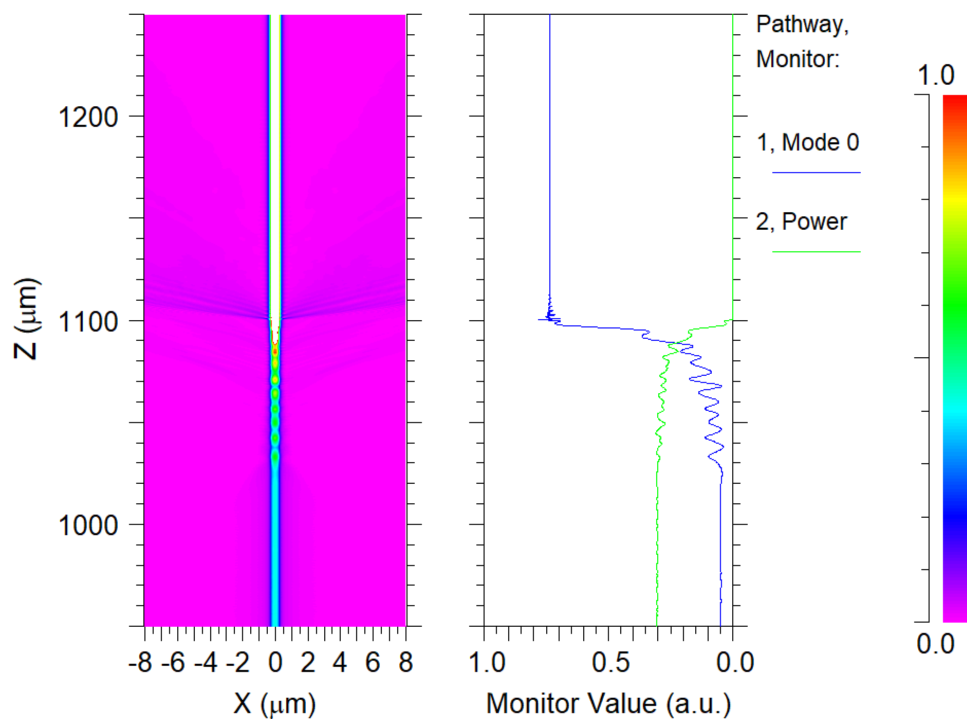

Figure 2.10: Simulation in case Si waveguide width is 0.6um.

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Fig. 2.10 is the simulation result when the waveguide width is 0.6um. Comparing with the graph in Fig.2.9(b), the taper structure of epitaxy is the same. However, only the width of the Si waveguide was changed from 2um to 0.6um. If we look at the result of the graph, we can see that the ripple has disappeared. Therefore, it can be seen that 0.6um is required for single-mode excitation. However, for high transverse confinement in the gain section, the width of Si in the gain section should be wide.

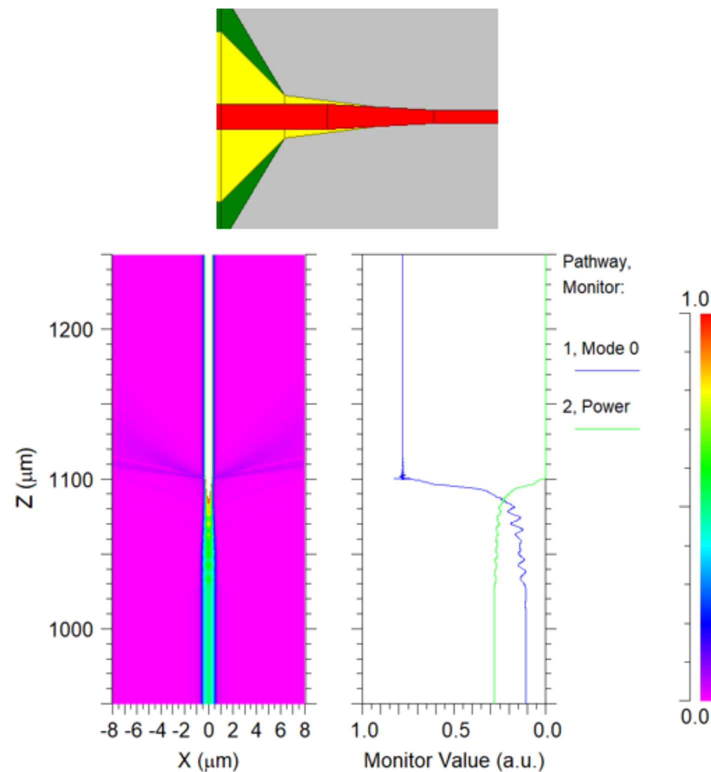

Figure 2.11: Simulation in case Si waveguide width has taper from 2um to 0.6um over 50um.

Fig.2.11 is the simulation result of the structure in which the waveguide is taper from 2um to 0.6um. The structure shown in red above is a waveguide. Looking at the results below, it can be seen that the efficiency is higher than Fig.2.10. Therefore, a structure with higher transverse mode confinement and higher efficiency was designed [23].

2.4 Thermal design

The most important process when making a hybrid laser is bonding. As will be explained in detail in Chapter 3, the efficiency of dissipation of heat generated by QW varies according to the bonding method. In this thesis, I proceeded with 3 bonding methods, and calculated the heat generated using the heat simulation result. Simulation used heat in lumerical. Heat power was calculated with reference to [22]. Thermal conductivity of Si, BCB, Al_2O_3 are 148W/m/K, 28W/m/K and 0.293W/m/K, respectively.

Direct wafer bonding case

Figure 2.12: Simulation result for direct wafer bonding. Thermal resistance is 0.13℃/mW.

Direct wafer bonding is a structure without an intermediate layer between III-V and Si. In this case, since it is in direct contact with Si, which has high thermal conductivity, the generated heat is easily discharged downward. Thermal resistance represents the temperature change when the heat power of 1 mW is increased. The smaller the change, the better the characteristic. Thus, direct wafer bonding case, thermal resistance is 0.13°C/mW.

BCB bonding case

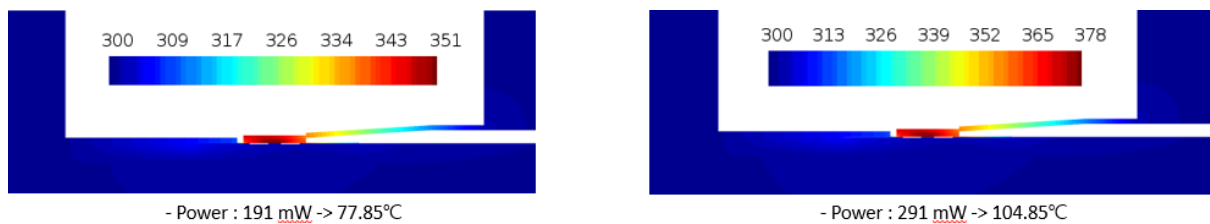

Figure 2.13: Simulation result for BCB bonding. Thermal resistance is 0.27℃/mW.

BCB bonding has BCB polymer as adhesive layer between SOI and epitaxy. Due to the low thermal conductivity of BCB, heat generated in the active region cannot be transferred to Si. Therefore, the heat cannot escape, so the internal temperature is very high, and the thermal resistance value is also high.

Al_2O_3 bonding case

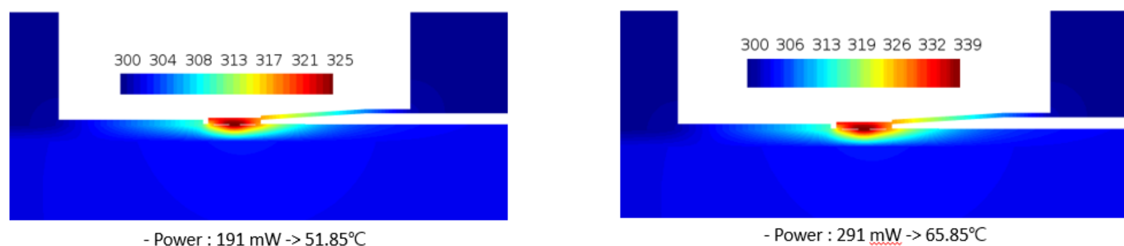

Figure 2.14: Simulation result for Al_2O_3 bonding. Thermal resistance is 0.14℃/mW.

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Al_2O_3 bonding has Al_2O_3 layer between SOI and epitaxy. Compared to BCB, it has higher thermal conductivity, so the heat generated from QW is transferred to Si and the heat dissipation efficiency is good. It has the advantage of high bonding strength and is widely used.

2.5 Mirror design

DBR laser has a back mirror and a front mirror. By changing the width or height, the effective index is changed, and the reflectance is determined by the difference in the index. In our case, side wall etching (changing width) was performed to finely control the index. 1138 pairs were superimposed on the back mirror to achieve 81% reflectance. By superimposing 378 pairs on the front mirror, 50% reflectance was obtained.

2.6 Summary

We designed from structure of epitaxy to mirror. The taper structure was designed for high power laser and the epitaxy thickness was adjusted for high efficiency. The efficiency was highest when the N contact layer was 110 nm, but 130 nm was adopted for the convenience of the process. And the optical loss of the p contact layers was quantitatively obtained and the effect was judged. And in order to be less affected by heat, the thermal resistance of Al_2O_3 bonding was obtained and the bonding method was determined.

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Chapter 3. Wafer Bonding of III-V to SOI

3.1 Introduction

As I mentioned in chapter 1, Since silicon has an indirect bandgap, recombination is impossible without intervention of phonon. Therefore, it is very difficult and inefficient to make a light-emitting device with a silicon platform. So, heterogeneously integration using III-V and Si is one of the solutions for using the silicon platform. However, the requirements for CMOS compatibility, such as thermal budget, contamination, planarization, etc., are challenges to be addressed. Direct epitaxial growth on Si is a very good approach, but growing directly on Si has unresolved problems. While the lattice constant of crystal Si is 5.431 Å, the lattice constant of InP is 5.869 Å and has a mismatch of 7.46%, so when InP is grown on Si, a defect due to mismatch occurs.

Wafer bonding is one of the most important steps to create heterogeneously integrated devices [24]. Several methods have been studied. It can be divided into whether there is an intermediate (Adhesive) layer or not. Direct wafer bonding (DWB) has no intermediate layer and is attached by electro-static and molecular force. However, since there is no intermediate layer, the surface roughness of the die samples is critical. The roughness of the surface is difficult to control as it is affected when the epitaxy layer is grown or the cap layer is removed. Intermediate bonding is a process of attaching III-V and SOI between samples by increasing adhesion using polymer or glass. To fabricate heterogeneous integration devices, direct bonding or adhesive bonding is very suitable.

The idea of wafer bonding is to place the patterned SOI wafer/die on a clean III-V Epitaxy wafer/die that has not been processed or has only the cap layer removed. And it is a process of permanently bonding two wafers/die using a mechanical bonding tool that applies temperature and pressure. Wafer bonding can be done at low temperatures, making it CMOS-compatible. After bonding, substrate of III-V epitaxy is removed leaving the III-V layer including n, p contact QW etc. In other words, it can be thought of as transferring the main epitaxy layer on Si. Therefore, the quality of the material is guaranteed because it is III-V grown on a unique lattice-matched substrate to overcome the problem of defects caused by lattice mismatch, which is a disadvantage of direct epitaxial growth. In the case of optics, the advantage of this method is that III-V and Si are in close contact and light is easily coupled from one layer to another, so that a light emitting device using a Si substrate can also be fabricated.

Wafer bonding is a key technology in manufacturing future laser devices. And, as mentioned earlier, this is the most important process. This is because, depending on the quality of bonding, the area to be used as a laser device and the characteristics of the device are also determined. Although direct wafer bonding has the best properties, it could not be applied to large parts of this work because the surface of III-V epitaxy is the most important issue. Adhesive bonding method was mainly carried out in two

ways. First, the ultra-thin BCB layer was used, and the Al_2O_3 method was used. In fact, Al_2O_3 bonding can be viewed from the perspective of direct wafer bonding, but in this paper, it is classified as an adhesive layer from the viewpoint of an adhesion layer. The entire bonding procedure will be described in the next section.

3.2 Direct wafer bonding

As described in Section 3.1, direct wafer bonding is a bonding method that proceeds without an adhesion layer. Two wafers with a flat, mirror-polished and absolutely clean surface are bonded by molecular force.

3.2.1 Bonding mechanism

Before mechanical bonding, the prepared III-V sample is manually flipped and brought into contact with the SOI sample. Then, gentle and smooth pressure is applied to stick the two samples together enough so that the III-V sample can't be moved on the SOI sample. This process is called "manual" bonding. This step is carried out at room temperature and in normal atmosphere, where bonding is achieved by relatively weak Van der Waals force [25]. The bonding strength is dramatically increased by annealing in the bonding machine. In this step, covalent bonds with strong bonding strength are formed in the sample, which was weakly attached by the Van der Waals force.

The surface chemistry of the samples directly influences the direct wafer bonding. According to the chemical group of the surface, it is classified into two types: hydrophilic and hydrophobic [25].

In case of hydrophilic surfaces, they are covered with thermal oxides. This surface is terminated by polar hydroxyl groups OH-, and therefore adheres well to polar water molecules. As I mentioned earlier, these water molecules act as a bridge connecting the surfaces of two samples by the Van der Waals force of a few monolayers of water at room temperature. When this sample is heated at a high temperature, strong covalent bonds in the form of Si-O-Si are formed. In this paper, hydrophilic bonding is used.

Hydrophobic surfaces, another case, were obtained by removing native oxide on the surfaces of both samples. The removal method is generally HF, BOE (buffered oxide etchant). Hydrophobic surfaces devoid of native oxide have no water molecular layer. Therefore, initially, hydrogen (with a small amount of fluorine) acts as a bridge and is attached by weak Van der Waals force. In high temperature, as hydrogen and or fluorine are desorbed, crystal-to-crystal (Si-Si) bonding is formed. Hydrophobic

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bonding is more sensitive to surface micro-roughness than hydrophilic bonding because there are no water molecules between the intermediates.

In the case of Si wafer, gas bubble or void occurs at the interface when annealing below 800℃. Therefore, annealing should be performed at 800°C or higher. However, 800°C exceeds the limits of CMOS-compatible processing. And it is impossible to make heterogeneously integrated devices due to mismatch of thermal expansion coefficients [26]. During cooling, the strain created by the different coefficient unbonded area occurs.

To overcome the above limitations, oxygen plasma-assisted bonding, which can perform bonding at low temperatures, is mainly used [25-27].

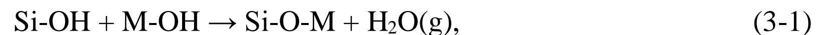
3.2.2 Plasma-assisted direct wafer bonding

Previously, it was said that the anneling temperature for bonding should exceed 800℃. In case of hydrophilic, however, oxygen plasma treatment to activate hydrophilic enables bonding at annealing temperature below 500℃.

The oxygen plasma treatment has several effects on bonding. This forms a thin oxide layer on the surface. That layer is more hydrophilic than native oxide. The oxide region helps to accelerate the formation of covalent bonds at low temperatures.

The last step creates a high density of polar -OH hydroxyl groups on the surfaces of both samples by immersion in deionized (DI) water.

The reaction between Si and III-V can be described by the following equation.



$$\text{Si-OH} + \text{M-OH} \rightarrow \text{Si-O-M} + H_2O(g), \quad (3\text{-}1)$$

$$\text{Si} + 2H_2O \rightarrow SiO_2 + 2H_2(g), \quad (3\text{-}2)$$

where M are the elements of the III-V compound semiconductor. The first equation shows the process by which the -OH hydroxyl group between silicon and the compound semiconductor is transformed into a covalent bond. The byproduct of this reaction is water and exists in the gaseous state. In the second equation, water reacts with Si to form additional SiO2 at the interface, where H2 gas is a byproduct gas.

For oxygen plasma treatment, a reactive ion etching (RIE) process is generally used. At this time, RF power should be kept as low as possible to avoid physical etching.

In plasma bonding, the annealing temperature is rapidly lowered. According to the experimental results, bonding was usually done at around 300℃. Oxygen plasma-assisted direct wafer bonding has made CMOS-compatible.

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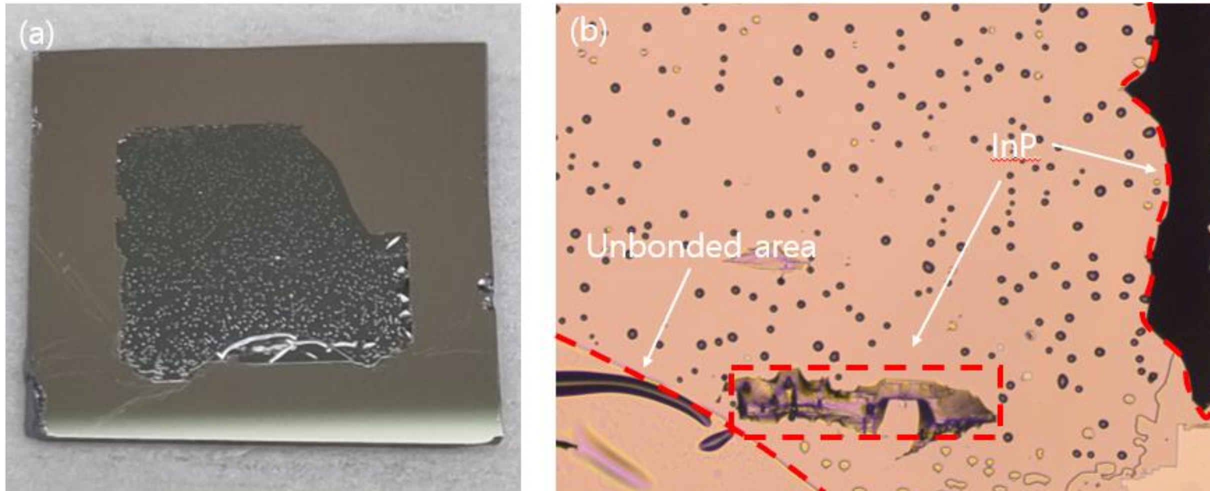

Figure 3.1: Sample images of SOI and III-V bonding without forming vertical outgassing channels (VOCs). (a) Many appear to be voids, and unbonded areas and boundaries are observed. (b) optical microscope (OM) image. The black dots are voids caused by byproduct gases, and the unremoved portion of the substrate and the unbonded area are visible.

One problem with bonding at low temperatures is the byproduct gas shown in equations (3-1) and (3-2). This byproduct gas is generated at the bonding interface, thereby generating voids. Fig. 3.1 is a figure of the sample without the formation of a channel for the byproduct gas to escape. This sample is a sample subjected to heat treatment at 300° C. for 2 hours. In Fig. 3.1, It can be observed that numerous voids were formed on the surface due to byproduct gas and bonding was not performed properly. In Fig. 3.1(b), it shows the little amount of the remained InP substrate as black lines and black area. At high temperature, these gases diffuse out through the micro-roughness of the surface or are efficiently absorbed by the porous SiO_2 [29,30]. However, at low temperature, diffusion is insufficient and a large number of voids are formed by byproduct gas. A method for degassing is to form vertical outgassing channels (VOCs). This procedure was discovered by the J.E. Bower group at the University of California-Santa Babara [28].

The schematic illustration of how to remove the byproduct gases through the VOCs is described in Fig. 3.2(a). VOCs make a way for gases to enter the BOX layer, diffuse through the porous oxide layer and escape, and finally there are no gases at bonding interface. The spacing and size of VOCs affects the void density. When spacing is reduced and size is increased, fewer voids are formed. In our experiments, a 7 μm x 7 μm square pattern with a spacing of 70 μm led to void-free bonding. Figure 3.2(b) shows a sample in which a 7um x 7um square pattern is periodically formed at an interval of 70um.

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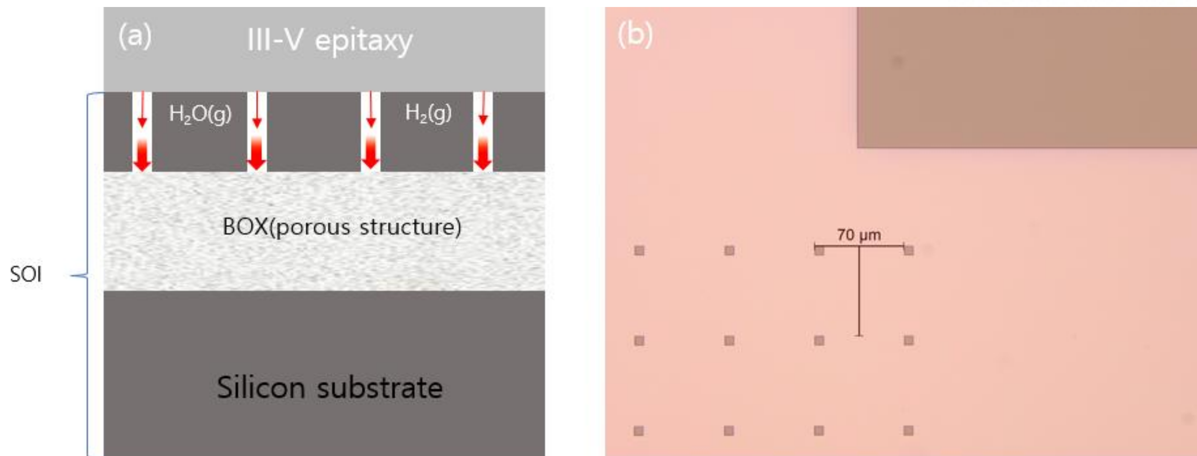

Figure 3.2: (a) Schematic illustration of the principle that byproduct gases are eliminated through outgassing chaeenls. (b) A micrograph showing VOCs with a spacing of 70um in a 7um x 7um square pattern.

3.2.3 Bonding procedure and surface roughness issue

The biggest drawback of direct bonding is that the surface must be absolutely flat, clean, and contamination-free. This means rigorous cleaning procedures and surface preparations are essential. Any surface roughness or particle contamination can lead to unbonded regions, voids, and/or reduce bonding strength and ultimately failure.

Fig.3.3 shows the process flow of direct wafer bonding. The first step in the cleaning procedure is the solvent cleaning step for both samples using the ultrasonic tube. First, soak in acetone to remove resist or large particles. III-V compound semiconductor is usually covered with (one or more) cap layers. By selective wet etching, this cap layer is removed and large particles or contamination would be lifted off.

One of the commonly used rigorous cleaning methods for SOI sample is the RCA-1 (sometimes called "standard clean-1, SC-1) solution which is heated to 70-80°C. That solution consists of the ratio $1NH_4OH{:}1H_2O_2{:}5H_2O$. NH_4OH slightly etches the surface of the wafer, forming undercuts under the particles and lifting the particles off the surface. However, in my case, the damage on the surface had a bad effect, so bonding was not done properly. As an alternative, a solution of piranha (3 H_2SO_4:1 H_2O_2) was used [31,32]. Here's the idea: The goal of RCA-1 cleaning is to remove organic matter and particles from the surface. If there are particles of 1 μm on the surface during the DWB process, it creates an unbonded area of 1 cm [25]. Therefore, the key idea is to remove organic matter and particles from the surface with piranha solution that does less damage to the silicon surface. Therefore, it is necessary to do the best to remove the removable particles on the surface. And by applying plasma to the two samples,

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a lot of hydroxyl groups were created on the surface. Finally, immerse in water to make more -OH arms, heat it to leave only the monolayer, and then perform manual bonding at room temperature. After that, put it in the machine and proceed with bonding at 300°C for 2 hours to complete the sample. After that, if the substrate InP is removed by putting it in HCl, the post-bonding process is completed.

One of the most important things is particle contamination, especially direct wafer bonding case, so, special care is required to handle the sample during the bonding process, and it takes a lot of effort to succeed.

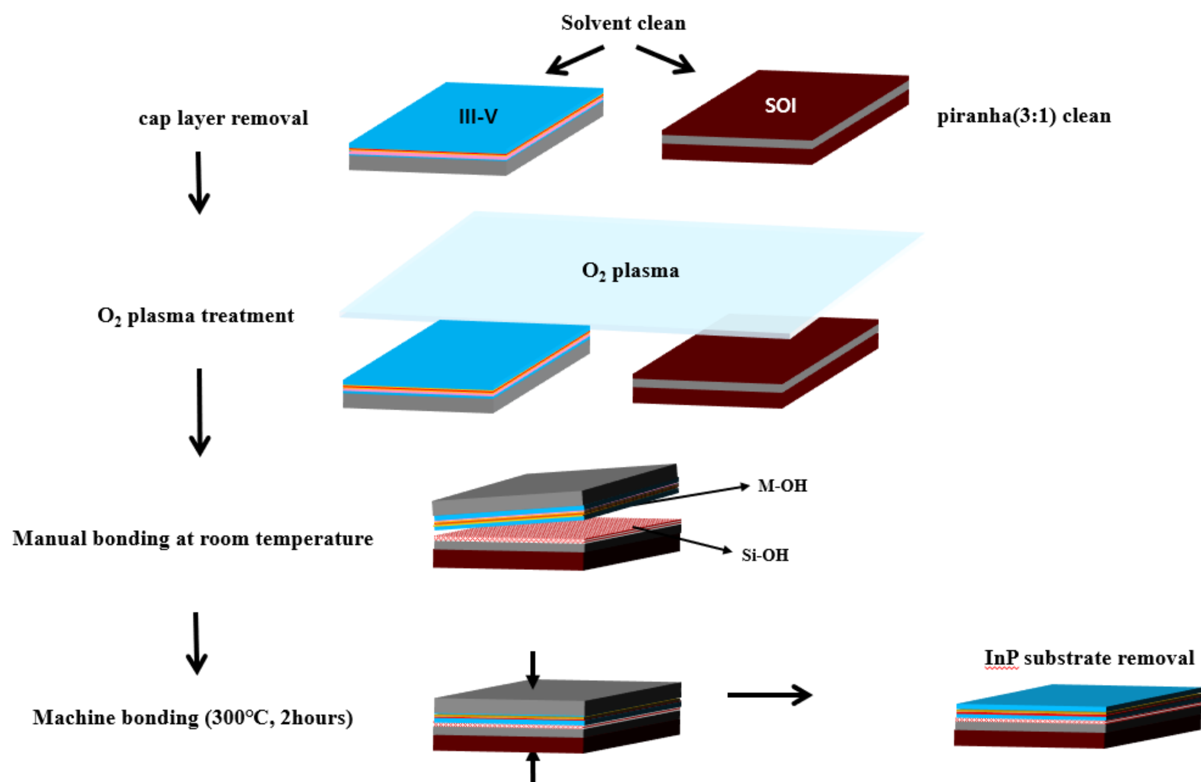

Figure 3.3: Process flow of direct wafer bonding. After the application of O_2 plasma, the bonding strength becomes stronger when immersed in DIW to further activate hydroxyl groups.

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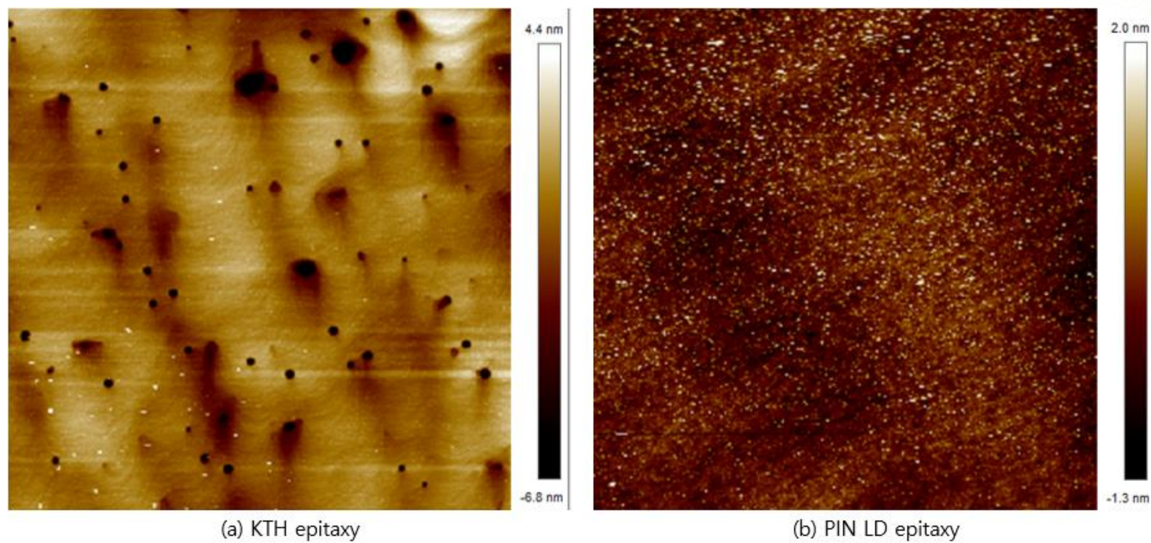

Figure 3.4: AMF images of the surfaces of (a) KTH and (b) PIN epitaxy wafers. KTH epitaxy has rough surface morphology and particles that cannot be removed. (b) PIN epitaxy has better surface morphology and a clean and smooth surface.

However, no matter how clean the surface is, if the surface is not mirror-polished, flat, and smooth, direct bonding is difficult to achieve. As reported, the root mean squared (RMS) value should be less than 1 nm [24,29].

Fig 3.4 are pictures of our epitaxy surfaces observed by atomic force microscopy (AFM). Figure 3.4(a) is the surface of the KTH epitaxy, and Figure 3.4(b) is the surface of the PIN LD epitaxy. The morphology of the KTH epitaxy is quite curved and the surface is quite rough. Furthermore, a lot of particles are found on the surface of the epitaxy. These particles are embedded in the epitaxy when it was grown from the company, and cannot be removed. Therefore, KTH epitaxy does not have the necessary surface roughness for the direct wafer bonding method, so bonding by that method is impossible. The PIN epitaxy has significantly better surface morphology and fewer particles that cannot be removed and the surface is smoother.

3.2.4 Result of Direct wafer bonding

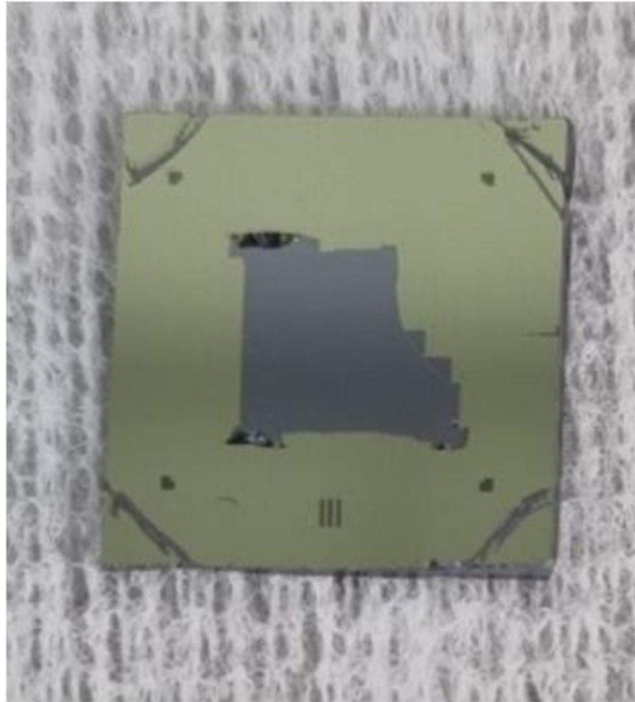

Figure 3.5: Photograph of bonding result of III-V (PIN epitaxy) to SOI direct wafer bonding. The area shown in dark gray in the center is the well-bonded area. It can be seen that the substrate remains on both sides due to the difference in etching speed, and the boundary part with weak bonding strength is separated.

PIN epitaxy was performed to satisfy the conditions of the direct wafer bonding method corresponding to surface roughness and clean surface, and III-V was bonded to the SOI substrate made of VOCs as shown in Fig. 3.5. However, it can be confirmed that the surface is clean as voids caused by byproduct gases are absorbed into the porous BOX layer by VOCs. Areas with weak bonding strength fell off. and the HCl as etchant of (1 0 0) InP is anisotropic and it can't etch the exposed (0 1 -1) planes [36, 37]. As a result, ridges of unetched InP were formed on the two opposite edges of the bonded epitaxy.

3.3 Adhesive wafer bonding

Direct wafer bonding is attached by Van der Waals force, covalent bonding without an intermediate layer to increase adhesion. However, the aforementioned drawbacks (surface roughness issues) exist and can be done, so the conditions for Epitaxy are difficult. Therefore, this chapter introduces adhesive wafer bonding using an intermediate layer (polymer, glass) that can increase adhesion.

Compared to direct wafer bonding, these methods are less sensitive to surface roughness issues and have strong bonding strength. As explained in Part 3.1 above, Al_2O_3 bonding is similar to direct wafer bonding in terms of forming bonds between -OH hydroxyl groups, but the content is explained in adhesive wafer bonding from the point of view that there is an intermediate layer.

3.3.1 Properties of BCB polymer

Polymer is the most commonly used material for adhesive bonding [34]. Among them, the polymer we used is BCB. Divinylsiloxane-bis-benzocyclobutene (DVS-BCB, or BCB for short) polymer was selected since the fabrication of hybrid integrated laser satisfying CMOS-compatible processing is needed low temperature bonding and high resistance to chemicals used in post-processing. The advantages of BCB as an adhesive polymer are: low curing temperature, low dielectric constant, excellent chemical resistance, etc.

The BCB polymer used for bonding is a non-photosensitive polymer (3022-35) purchased from DOW Chemical Company. The adhesion promoter is used for AP3000. The degree of curing of BCB and its phase depends on time and temperature as shown in Fig. 3.6. As time and temperature increase, the liquid polymer between the two wafers changes to a solid state and bonds. Generally, curing is carried out at 250°C for about 1 hour.

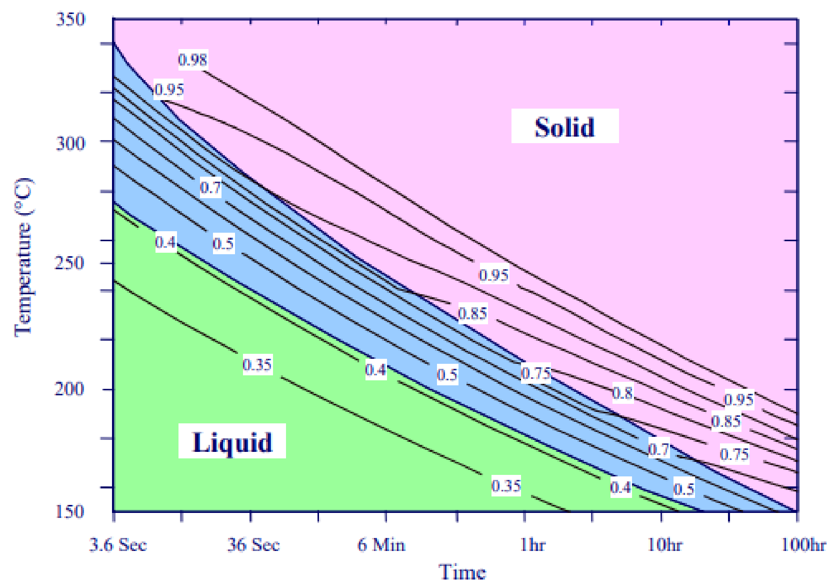

Figure 3.6: BCB cure as a function of temperature and time. Adapted from [35]

3.3.2 BCB bonding procedure and result

The process of BCB bonding is shown in Fig.3.7. First, solvent clean that removes organic matter and resist from the surface, cap layer removal, and piranha clean are the same. After that, a thin layer of SiO_2 (~30nm) is deposited to increase the adhesion between III-V and BCB. Then, plasma treatment is performed and thin (~30nm) spin-coating of adhesion promoter AP3000 and BCB is applied. Then, soft bake and manual bonding. And bonding is finished by removing the substrate after machine bonding. BCB bonding differs from direct wafer bonding in that VOCs are not required because direct bonding is not performed. And by entering the intermediate layer, it is less affected by the surface roughness issue. However, due to the characteristics of BCB and SiO2, which have low thermal conductivity, heat cannot easily escape to the substrate, so it is not effective for high-power devices.

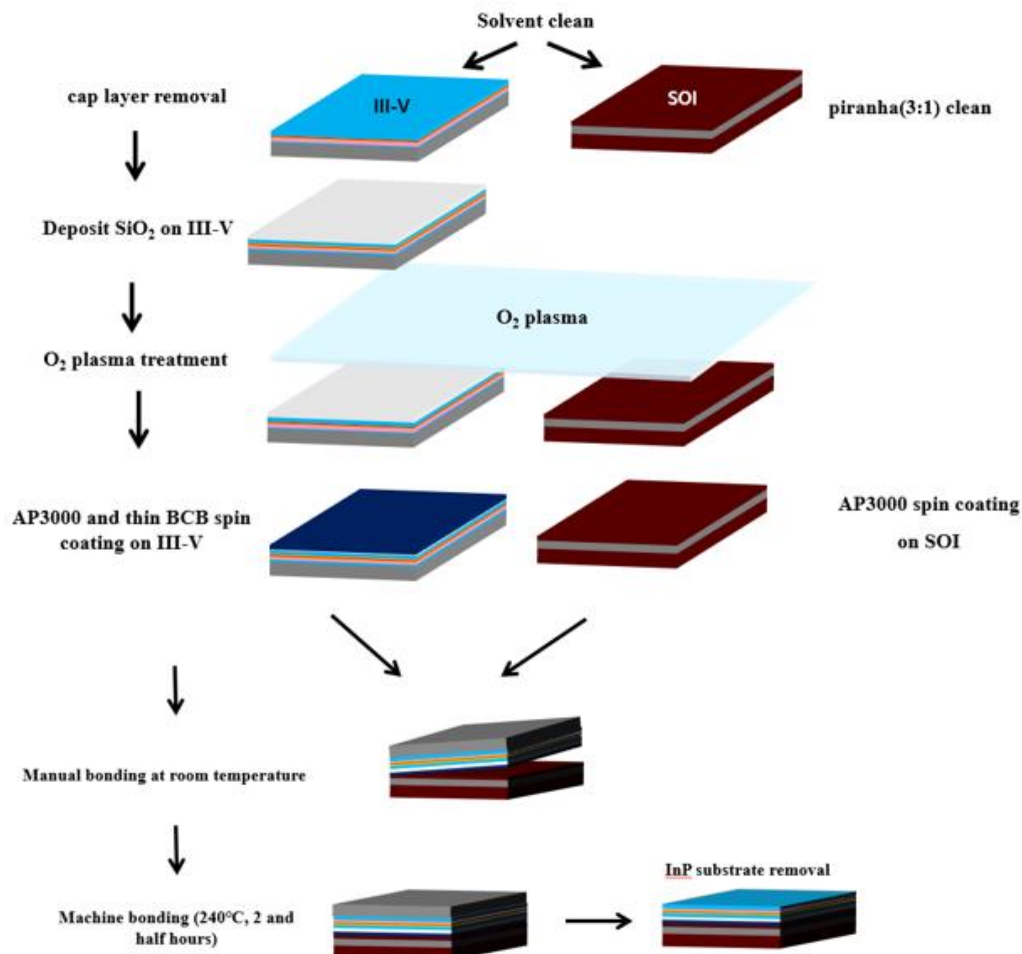

Figure 3.7: Process flow of BCB bonding of III-V onto SOI.

Fig.3.8 shows the results of BCB bonding. The KTH epitaxy shown in Fig.3.4(a) has poor surface roughness and contains many immovable particles. However, even if the roughness of the surface is not good due to the characteristics of BCB bonding, the overall bonding quality is good as shown in Fig.3.8(a). It can be seen that a larger area was bonded than Fig. 3.5 using PIN epitaxy with a cleaner surface. Fig.3.8(b) and Fig.3.8(c) are the edge and center part of the sample by taking optical microscopy (OM), respectively. As can be seen in (b) and (c), the surface of the epitaxy has an immovable wavy pattern created during epitaxy growth. However, since the bonding strength is strong, it can be confirmed that a large area is bonded.

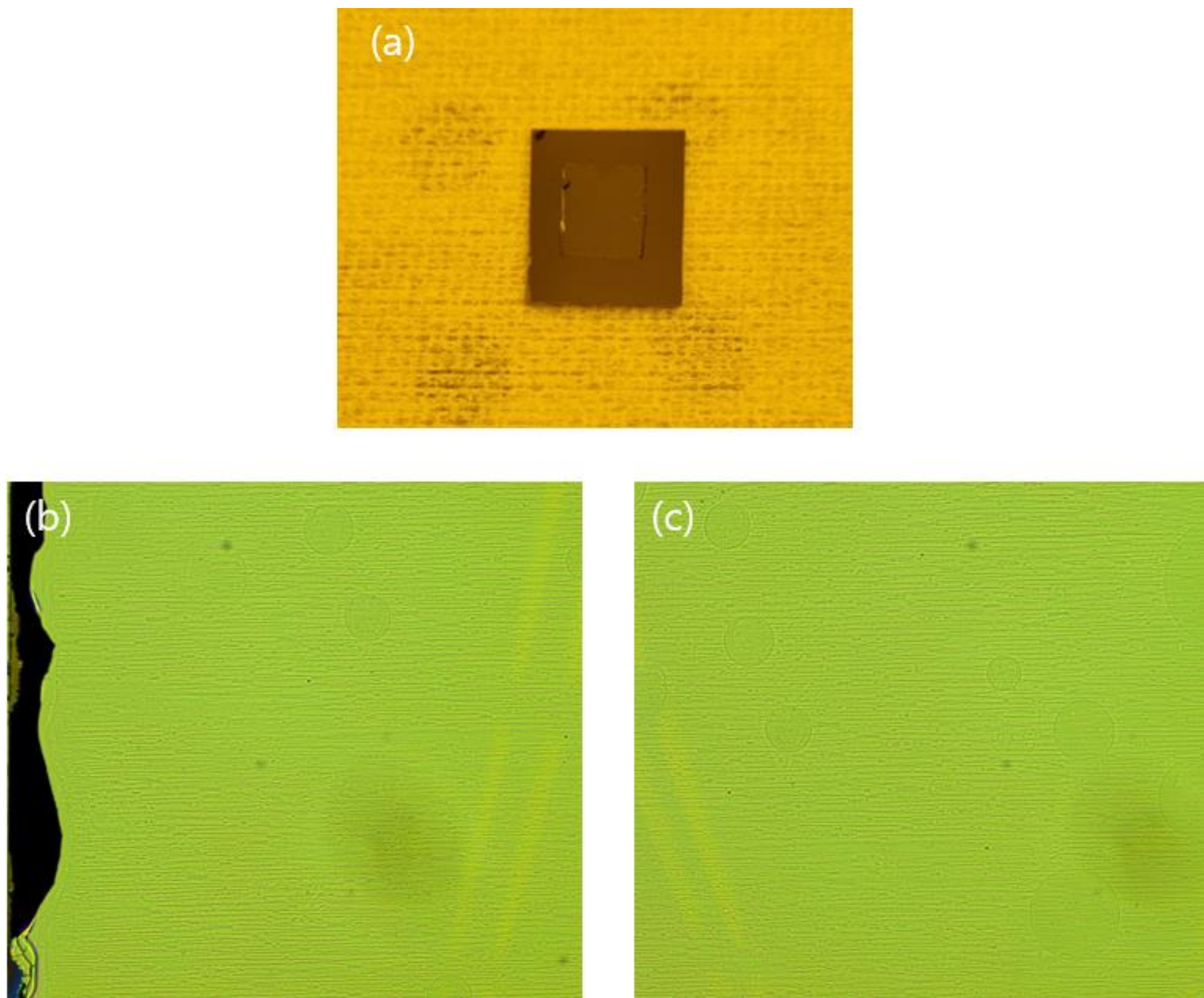

Figure 3.8: Result of BCB bonding. (a) Photograph of KTH epitaxy on SOI substrate after substrate removal. Fig.(b) and (c) are the Edge and center of the KTH epitaxy images by taking OM, respectively. The surface of the epitaxy has an immovable wavy pattern during epitaxy growth.

3.3.3 Adhesive Al_2O_3 wafer bonding procedure and result

The key idea to achieving high bonding strength is to deposit material with high -OH hydroxyl group density as an intermediate layer. Al_2O_3 is an excellent material for an intermediate layer. It has a high hydroxyl group density of around 18OH/nm^2(110 surfaces) [39]. Al_2O_3 is deposited with high accuracy using atomic layer deposition (ALD). ALD has excellent step coverage and helps in achieving thickness control at the sub-nm scale and does not add any surface roughness. Fig.3.9 shows the process flow of Al_2O_3 bonding. The overall flow is the same as that of DWB, but the procedure for depositing an Al_2O_3 intermediate layer on both sides to maximize hydroxyl groups was added. The thickness of Al_2O_3 was thinned to 4 nm so that heat could easily escape to Si [38-40]. Through this, the bonding strength can be further improved, and by using Al_2O_3, which has better thermal conductivity than BCB, it has better properties in terms of extracting heat to Si. So, it is advantageous for high power devices.

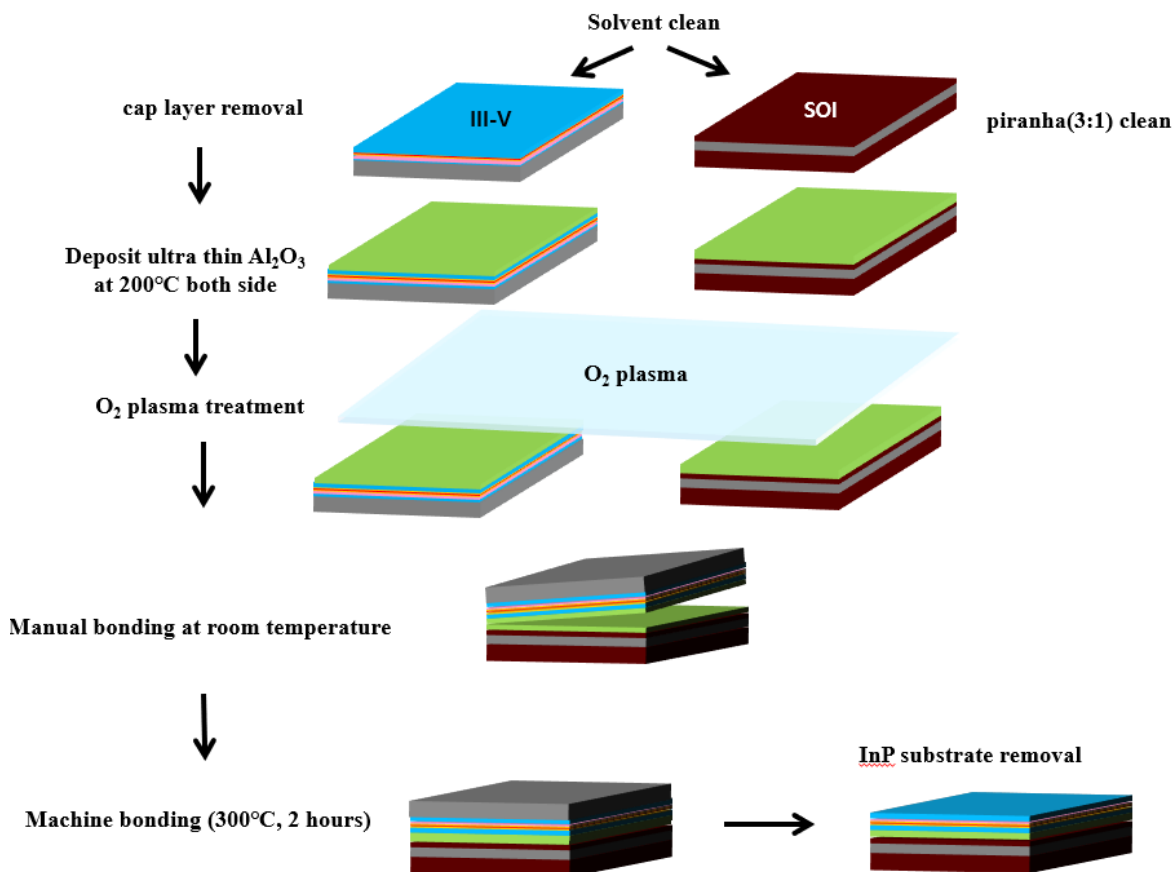

Figure 3.9: Process flow of Al_2O_3 bonding.

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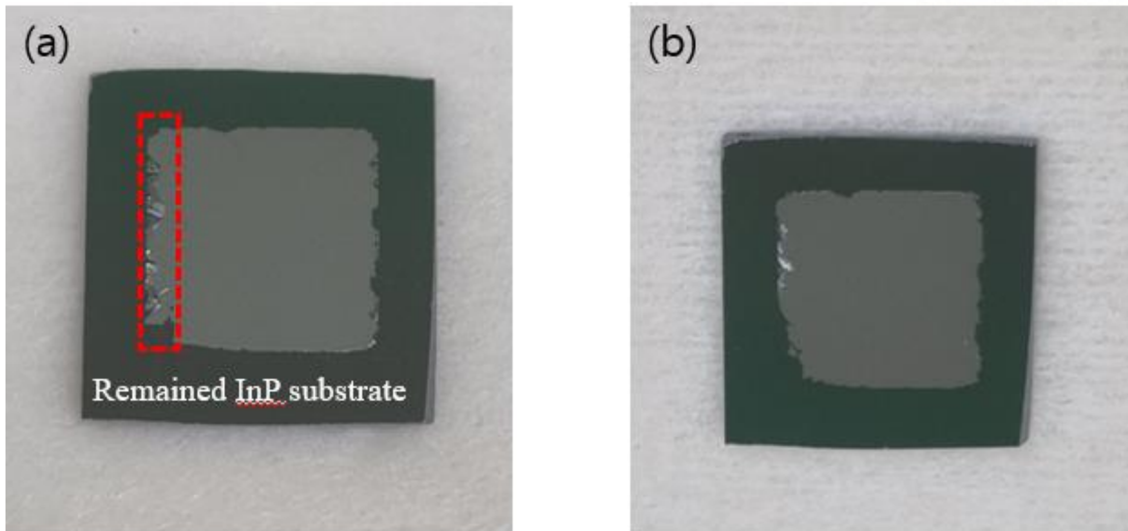

Figure 3.10: Photographs of the result of Al_2O_3-assisted bonding. (a) The unremoved InP substrate is shown in the red rectangle. (b) Picture after removing the remaining InP substrate.

Fig.3.10 shows the result of Al_2O_3 bonding. Similar to BCB bonding, it can be seen that bonding strength is also excellent as most of the area remains. Of course, there is no polymer that can compensate for surface roughness, so it is still sensitive to roughness issues, but it is not necessary to choose as rigorous as direct wafer bonding. The remaining InP substrate as called ridge is shown in Fig.3.10(a) appears due to the difference in etching rate depending on the InP substrate [36, 37]. Only that part can be removed by immersing it in hydrochloric acid or removing it with a tweezer to make it as shown in Fig.3.10(b).

3.4 Summary

In this chapter, the principles and results of bonding were reviewed. Bonding is the most important fabrication technology for creating heterogeneously integrated laser devices. By applying plasma-assisted bonding, a CMOS-compatible process became possible. Since bonding results vary greatly depending on the state of epitaxy, carefully examine the surface morphology and particles in advance and select an appropriate bonding method according to the characteristics of the device.

We discussed two methods for wafer bonding: the direct and adhesive bonding.

In the hydrophilic direct bonding case, molecular bonds are formed between -OH hydroxyl groups on the oxidized surfaces when they touch each other. During machine bonding, the molecular bond changes to a covalent bond at high temperatures, causing the two wafers/die to become permanently

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attached. When water treatment is applied, more -OH arms are formed on the wafer surface, and the bonding strength is increased.

Adhesive bonding is a method to improve bonding strength by presenting a substance that increases adhesion between two wafers as an intermediate layer. It is applied in the liquid state to level the surface and fill any voids. And it hardens through the curing process to permanently bond the surface. Generally, BCB polymer is widely used. It is widely used because it is not sensitive to surface morphology by filling voids on the surface, and has strong bonding strength and ease of use. However, this bonding method is not suitable for high power lasers, where thermal conductivity is not good and heat dissipation efficiency is important. And although Al_2O_3 bonding is classified as direct wafer bonding by many, it is classified as adhesive bonding according to the presence of an intermediate layer. In this case, when plasma is applied by depositing Al_2O_3, more hydroxyl groups are generated and the bonding strength is strengthened and a high yield can be obtained. In addition, the thermal conductivity is far superior to that of BCB, so it is excellent in terms of heat dissipation.

Subsequent samples were produced by adhesive Al_2O_3 bonding, and NILT nano imprinter or SB6L bonder was used for mechanical bonding. The condition according to the machine will be summarized again in the following chapter.

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Chapter 4. Fabrication of hybrid DBR laser

4.1 Introduction

The purpose of this work is to fabricate a device using the designed factors. Fabrication of device in a UCRF clean room is the most important task, and it takes the longest time during the master's program. This chapter will explain in detail the process steps required to fabricate a hybrid in-plane laser. For the simplification of manufacturing, I tried to make a laser with a structure without a taper.

4.1.1 CMOS compatibility

Silicon has been the main material for semiconductor electronic devices for the past 50 years. Mass production using CMOS (Complementary Metal-Oxide-Semiconductor) processing of Si-based electronic products has been continuously developed. SOI (Silicon-On-Insulator) platforms have gained a lot of popularity thanks to the reduction of operating voltage and reduction of parasitic capacitance.

The transparency of silicon in the infra-red wavelength range makes it a material for optical communication, and its high index contrast allows it to guide light well, making it useful as a passive and active device. Use of CMOS processing means It means that Si photonic devices can be mass-produced at low cost using the process infrastructure already developed for Si process.

4.2 Process flow

Fig.4.1 shows the overall structure of the hybrid laser. As explained in Chapter 2, although the scattering loss increases, a structure in which epitaxy is terminated at both ends of the mirror is adopted abruptly for single mode operation. The part with the mirror within silicon waveguide is indicated by a black dash line. The area marked in orange and yellow is the III-V gain section, the dark gray is the Si device layer, and the light gray is the BOX layer. Yellow is the metal for ohmic contact, the top and bottom are n-ohmic metal, and the middle is p-ohmic metal. The parts overlapping the two regions of the p(n) metal pad and the n(p) ohmic metal were separated using Photo-BCB (cyclotene 4022-35). For an efficient heat dissipation structure, the metal pad is thickly deposited.

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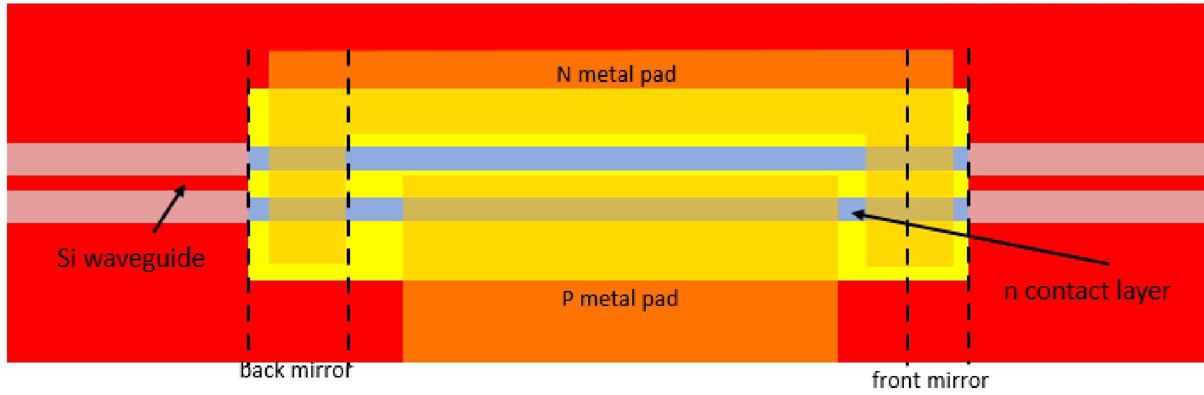
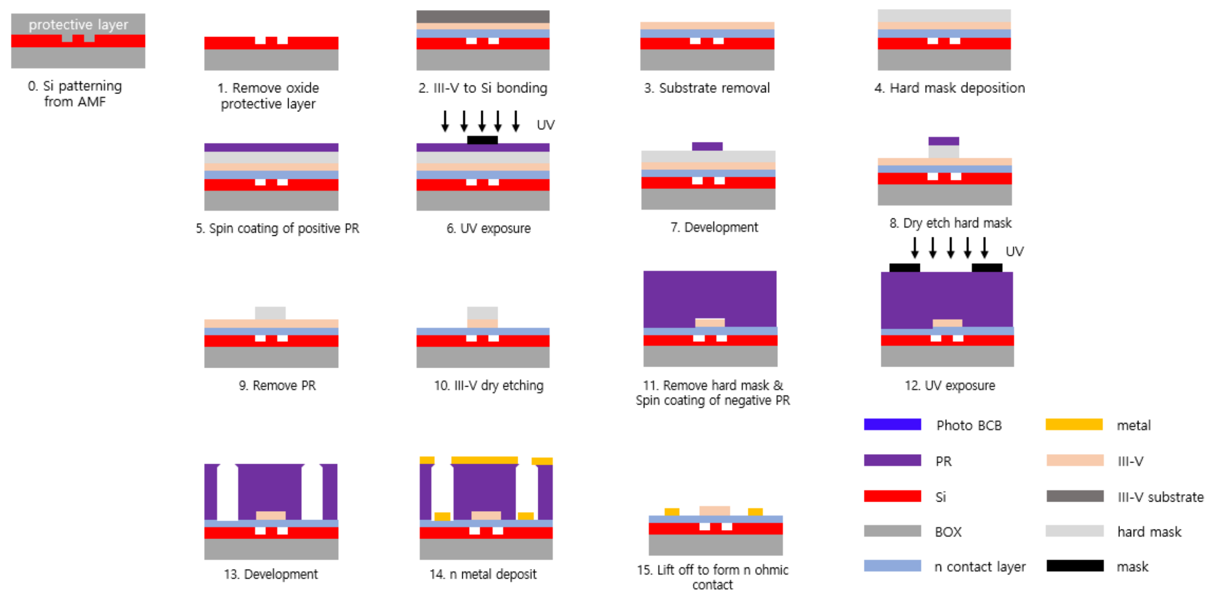


Figure 4.1: Schematic of hybrid in-plane laser

Schematic of process flow



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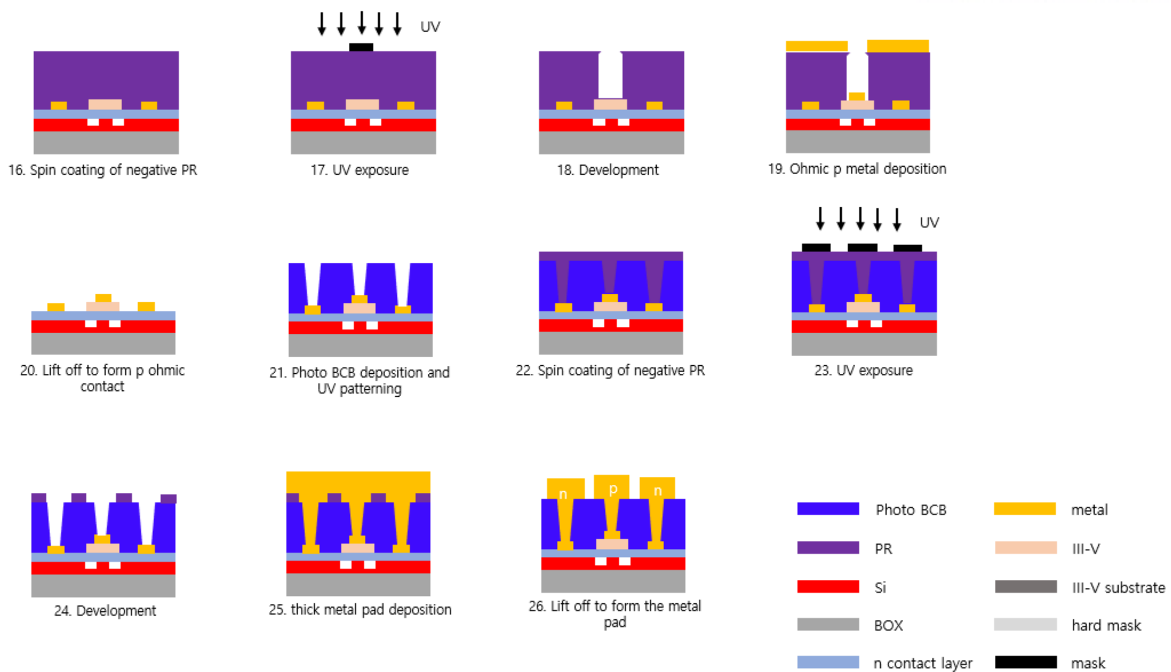

Figure 4.2: process flow of hybrid in-plane laser.

Sample preparation

Fig.4.2 shows the processes required to make a hybrid laser. Because of the limited quantity and high price of III-V wafers, all devices are chip-size. If you purchase a wafer, cover it with photoresist (PR) as a protective layer to protect particles from rising on the wafer surface during cleaving. The cleaving uses a tungsten tip to make small scratches near the edge of the wafer. Do not scratch directly on the bonding surface. This is because that small scratch has a bad influence on bonding. So all samples have scratches on the back. In addition, if there is a scratch on the back side of the area where the device will be inserted, it may cause problems with the device characteristics.

The III-V die sample is 7mm x 7mm, which is suitable for handling while saving material. In the case of SOI wafer, it is designed in Chapter 2, and since the chip was received from the AMF foundary, separate cleaving is not performed. The size of the SOI chip is approximately 1cm x 1cm by filling the space allotted to us. Both SOI and III-V chips undergo solvent cleaning to remove PR as protective layer and particles. After that, O2 plasma is floated to remove the residual resist. The chip received from AMF is deposited 150nm of SiO2 as a protective layer as shown in Fig.4.3. The protective layer is removed by immersing it in Buffered Oxide Etchant (BOE) for about 30 seconds (etch rate: ~10nm/s). This is up to step 1 of Fig.4.2.

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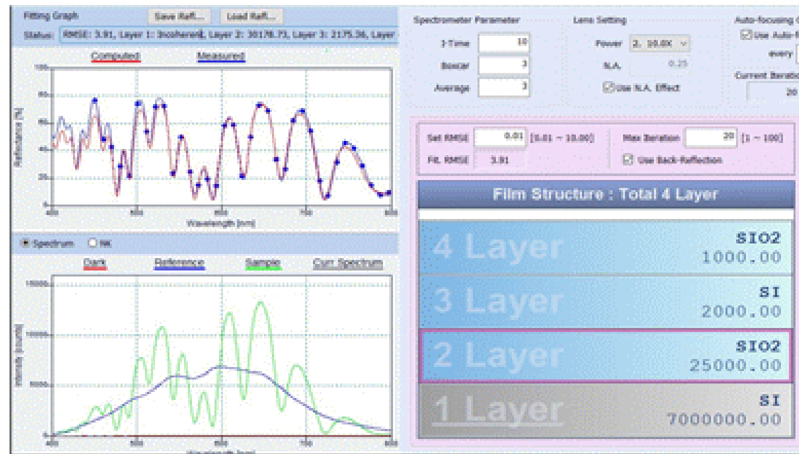

RMSE: 3.91, Layer 1: Incoherent, Layer 2: 30178.73, Layer 3: 2175.36, Layer 4: 1496.28

Figure 4.3: Filmtek results. 1 Layer, shown in the lower right, 2 Layer, 3 layer and 4 layer represents the thickness of the Si substrate, BOX, Si device, protective layer, respectively. The unit is Å.

Wafer bonding

In chapter 3, the conceptual part of wafer bonding is explained in detail, and the process steps and conditions are explained in this part. Soak in piranha solution (3 H_2SO_4:1 H_2O_2 (30%)) for 2 minutes to remove organic and metallurgic contamination in SOI samples [31,32]. Then, it is immersed in hydrofluoric acid to remove the unwanted oxide layer generated during the reaction. The cap layer of InP has two layers, InP and InGaAsP, respectively. Soak in HCl (37%), $1H_2SO_4$:$8H_2O_2$:$8H_2O$ solution for 5 seconds and 17 seconds to perform selective wet etching. Since we do Al_2O_3 adhesive bonding, we deposit Al_2O_3 on both samples by 4 nm using atomic layer deposition (ALD) equipment [40, 41]. After that, it maximizes the hydroxyl -OH groups on the surface through plasma and water treatment and leaves only the monolayer of water molecules through dehydration. Then, manually invert the prepared III-V sample and attach it to the SOI (refer to the manual bonding part in Figure 3.9). Then apply smooth pressure to hold both samples and to immobilize them while moving them to the bonding machine. The mechanical bonding was performed using SB6L bonder, and 290℃ and pressure of 1500mbar was applied for 2 hours. If the bonding was successful, there will be no debonding during substrate removal by immersion in HCl (37%). Since the thickness of the substrate is 600um, it will be stopped by the InGaAs etch stop layer after about 75 minutes. This etch stop layer is not removed at this stage, but is removed later in order to use it as a protective layer in a later process. This step is up to step 3 in Fig. 4.2. In Fig.4.4, there is a picture of the substrate removed after bonding. As mentioned above, the SOI patterning below has been produced by the AMF foundary.

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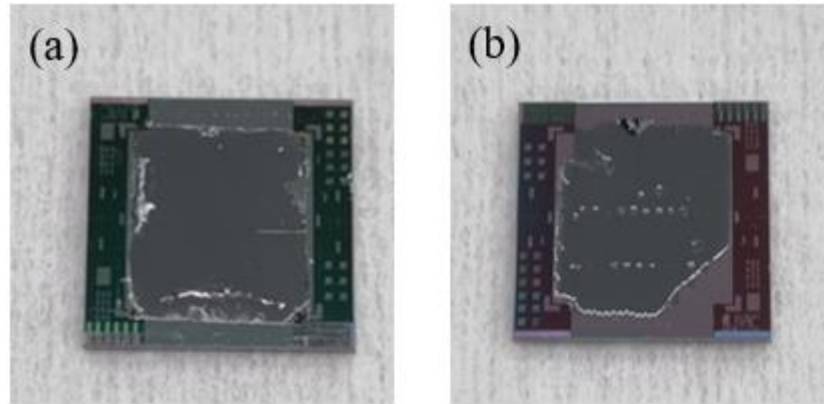

Figure 4.4: Result of adhesive Al_2O_3 bonding, a photograph of the unetched ridge removed. In both samples, the unbonded part appeared to float or disappeared.

Hard mask patterning to form mesa structure

The contents of Steps 4 to 9 are as shown in Fig.4.2. When InP dry etching proceeds at 180℃, if a resist mask is used, it is very difficult to remove the resist because it burns. Therefore, it was decided to use a SiO_2 hard mask with a fast deposition rate. 300 nm of SiO_2 was deposited using plasma-enhance chemical vapor deposition (PECVD) equipment. And after applying PR (Az 5214E), lithographic patterning was done through UV exposure and development. Then, dry etch the hard mask using Metal-RIE equipment and remove the PR on it.

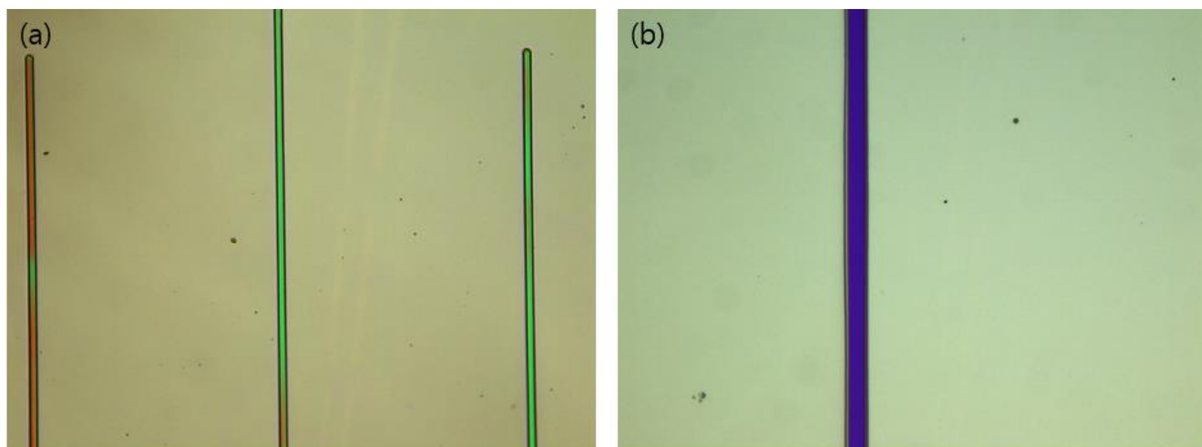

Figure 4.5: (a) OM image corresponding to step 8 in Figure 4.2. Resist remains and the color on the ridge appears green or pink. (b) OM image corresponding to step 9. It can be seen that the resist has been removed by looking at the blue color.

III-V etching

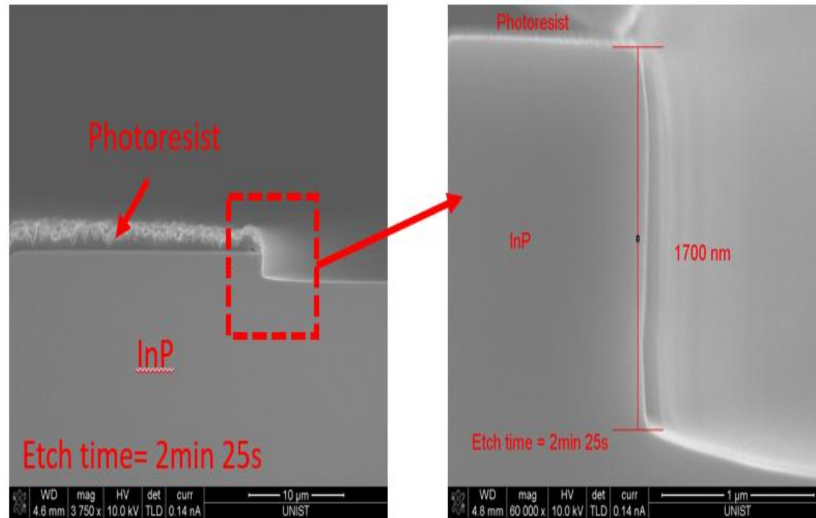

Figure 4.6: SEM image for finding etch rate for InP. We can find that the etch rate is approximately 11 nm/s.

The dry etching condition was found through Dummy InP. Etched using Metal-ICP RIE equipment, gas flow and coil power will be written down in the process flow step of the Appendix.

To preserve the thin N-contact layer, dry etching was performed up to the middle of the SCH layer, and the remaining quaternary materials were selectively wet-etched using citric acid [42]. After this process is finished, the protective layer, SiO2, is removed. In Fig.4.7, there is the result after etching the III-V layer.

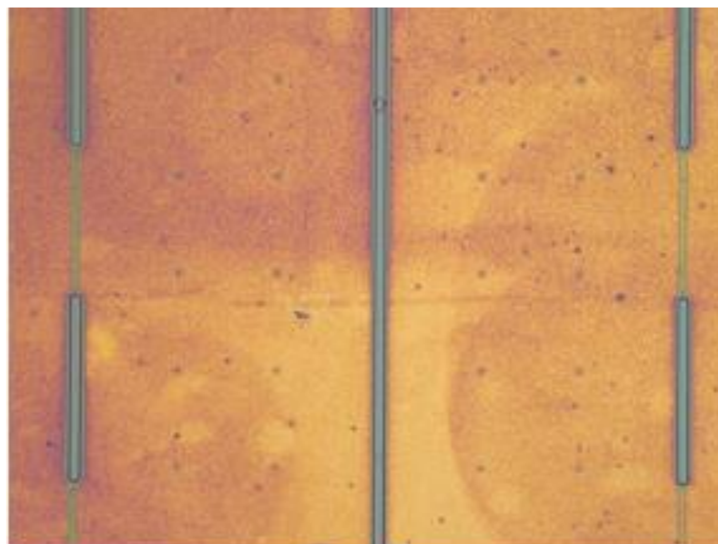

Figure 4.7: OM image after III-V etching. Until middle of SCH layer or QW layer, dry etch is carried out. After that, selective wet etching is carried out before N-contact layer.

N ohmic metal deposition

To deposit metal only in the desired area, a process called lift-off must be used. In order to properly perform lift-off, an undercut structure is required, and when this is properly formed, the metal is formed as desired without breaking. This corresponds to steps 13 to 15 in Fig.4.2. First, Az nLoF 2035, a negative resist, was selected as a resist for undercutting. In case of using the standard recipe, it was judged appropriate because the thickness of the resist was sufficiently high as 3.5um. In general, the thickness of resist must be three times higher than that of metal to proceed properly. For the metal composition, Ni/Ge/Au capable of ohmic contact with the n InP contact layer was used. After the metal is deposited, immerse in acetone and wait for about 15 minutes to remove the resist and you can see that the metal remains only in the desired area. After that, the rapid thermal annealer (RTA) process is performed for the alloy of the metal. The temperature is increased from 200°C to 420°C for 60 seconds and then heat-treated for 15 seconds. To prevent oxidation at high temperatures, the annealing is done in nitrogen atmosphere. Fig.4.8 (a) is a picture after metal deposition and lift-off process. Metal is bright yellow. Fig.4.8(b) is a picture after heat treatment is performed to form a metal alloy, and it can be seen that the color has changed compared to (a).

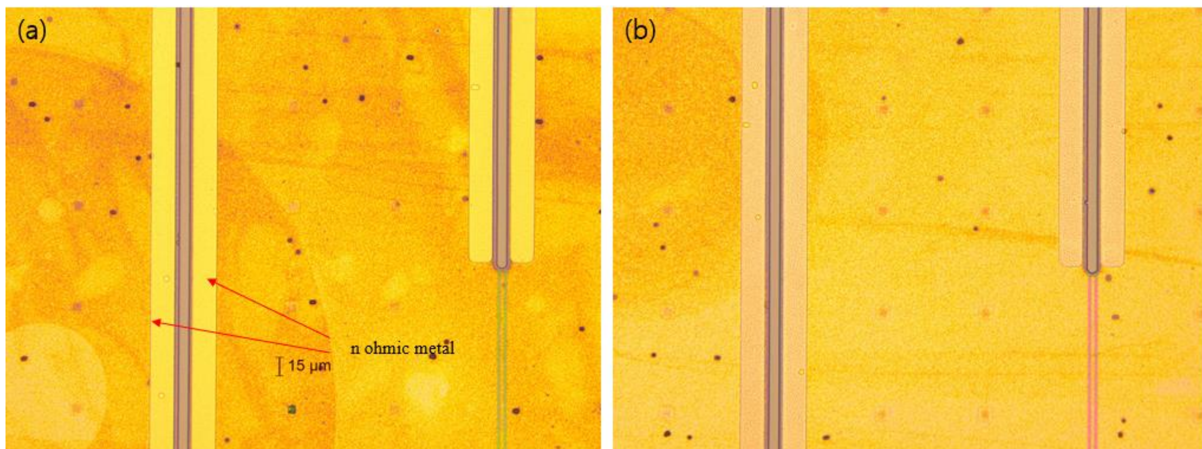

Figure 4.8: OM images after forming n-type ohmic metal through lift-off. (a) before annealing. (b) after annealing.

P ohmic metal deposition

It has the same steps as the previous n-ohmic metal deposition. It is the process from steps 16 to 20 in Figure 4.2. The difference from N-conact is the composition of the metal. Since the material of the P contact layer is InGaAs, Ti/Pt/Au that can make ohmic contact with the material was deposited. Another difference is that an annealing process is not required.

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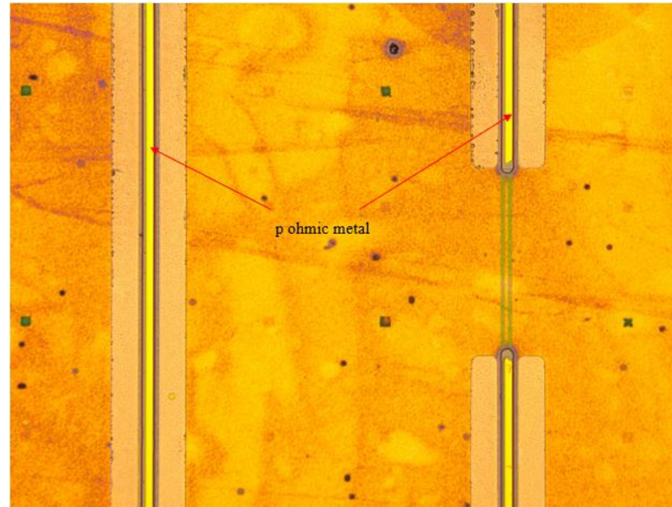

Figure 4.9: OM imges after lift-off for p metal.

Planarization

Photo BCB (cyclotene 4022-35 bought from DOW chemical) was used to connect Ohmic metal and thick contact pad. An important point in this part is that the metal deposited with the contact pad does not break and goes well along the slope of the photo BCB. So, it is better to have a gentle slope of the photo BCB. Fig.4.10(a) is a picture of 300nm metal deposition after photo BCB patterning. As you can see here, the metal continues along the curved surface without breaking.

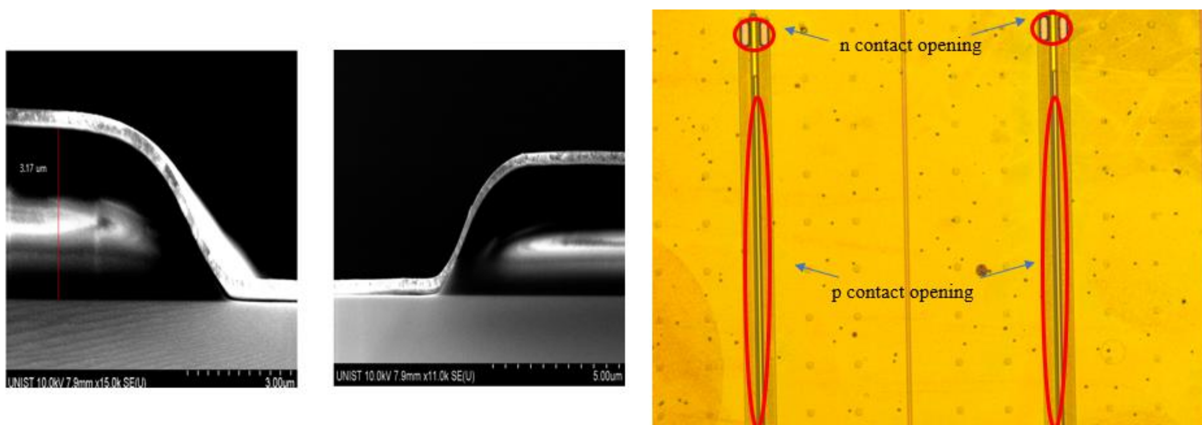

Figure 4.10: (a) Photo BCB test image. It can be confirmed that the metal deposited on the top has an appropriate slope and continues along the slope without breaking. (b) is an OM image patterning a real sample using photo BCB. The area marked in red is the opened area.

We can see that the part marked in red is opened in Fig.4.10(b). The area and the contact pad are connected so that current can be supplied.

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Contact Pad Formation

It is the last part of the process of making a hybrid laser. The process sequence itself is the same as when depositing n and p ohmic metal. Here, Ti to increase adhesion and Au, which is connected to the tip to supply current, were deposited. If you look at Figure 4.11(a), you can see that patterning was done using negative resist. In Figure 4.11(b), Ti/Au was deposited and a contact pad was formed through the lift-off process. Through this, the production of hybrid laser device was completed.

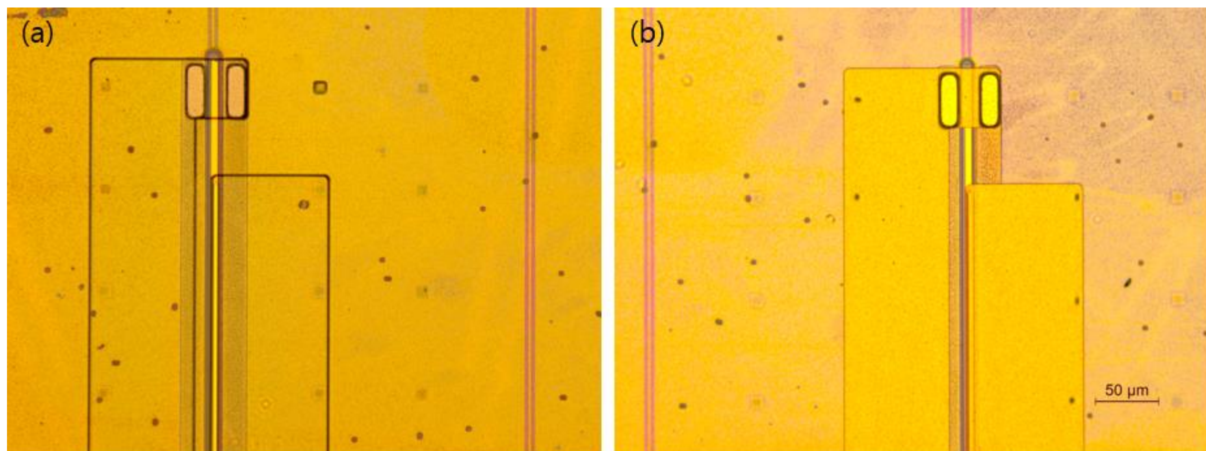

Figure 4.11: (a) OM image patterning the part where the contact pad will rise using negative resist. (b) OM image in which the metal is deposited and the metal is left only in the desired part using the lift-off process.

Chapter 5. Characterization and discussion

The fabricated laser sample is made with Al_2O_3 bonding, and optical power and voltage are measured according to current through the measurement set-up in our lab. Through this, the characteristic evaluation and discussion of the laser will proceed.

5.1 Characterization

5.1.1 Measurement set-up

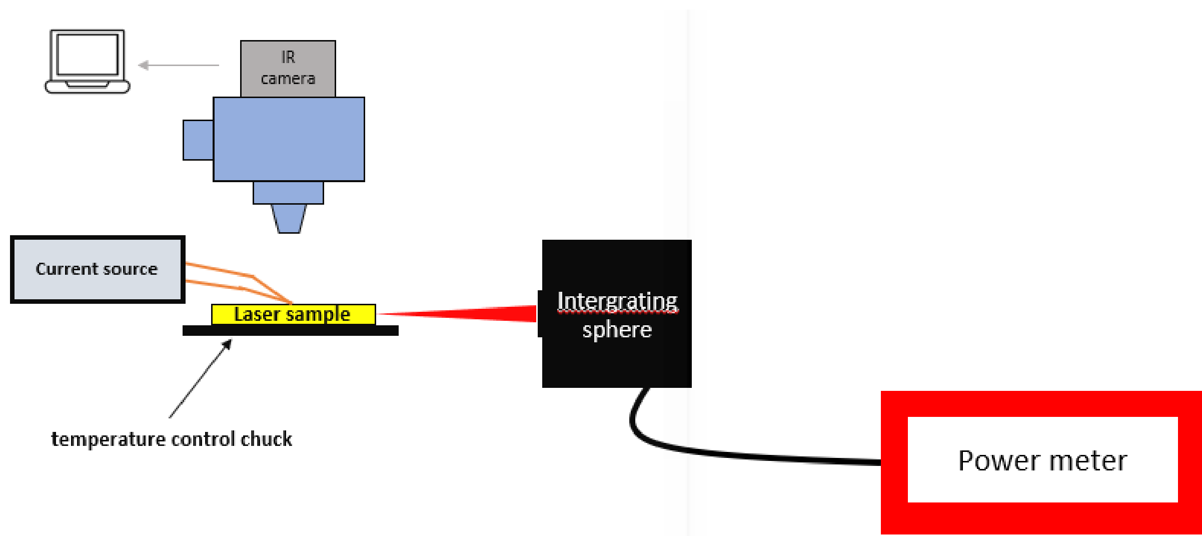

Figure. 5.1: Schematic of measurement set-up.

This is the schematic of the set-up used for measurement. We can find the desired under the IR camera and contact the probe to the corresponding n and p metal pad. It operates by flowing current fromt the current source to laser. When the light from the laser is injected into the integrating sphere. The light absorbed by the integrating sphere is read by a power meter. So, I-L (current-output power) curve can be obtained. Obtain the I-V (current-voltage) curve using the software supported by the current source.

5.1.2 Measurement results

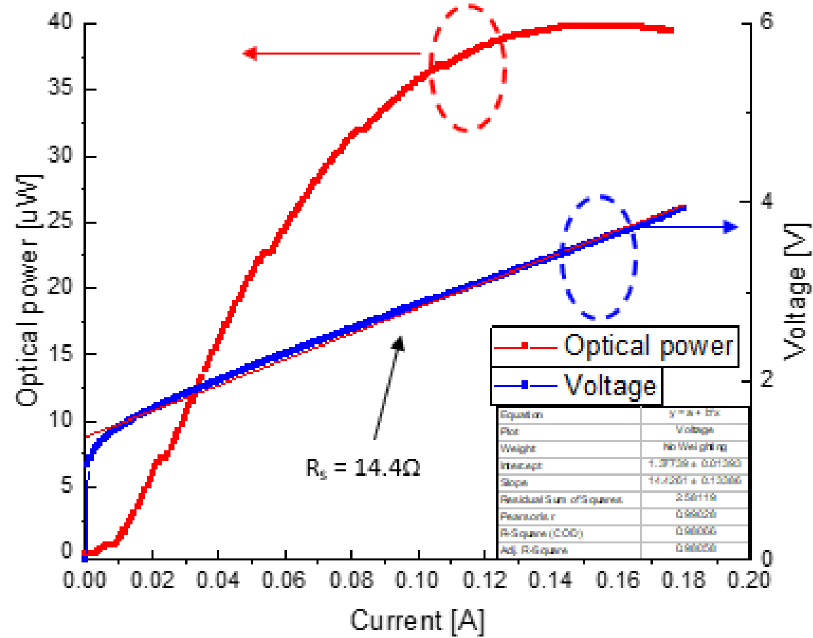

Figure 5.2: L-I-V (power – current – voltage) curve of 600um cavity.

Fig.5.2 shows the LIV curve of a laser sample with a 600um cavity. In general, threshold current (I_{th}) in which the power rapidly increases due to stimulated emission appears in the I-L cureve. However, no threshold current is observed in our laser sample. Therefore, it can be seen that lasing is not performed. And a high differential resistance (Rs) value was measured. This effect on Rs will be described later.

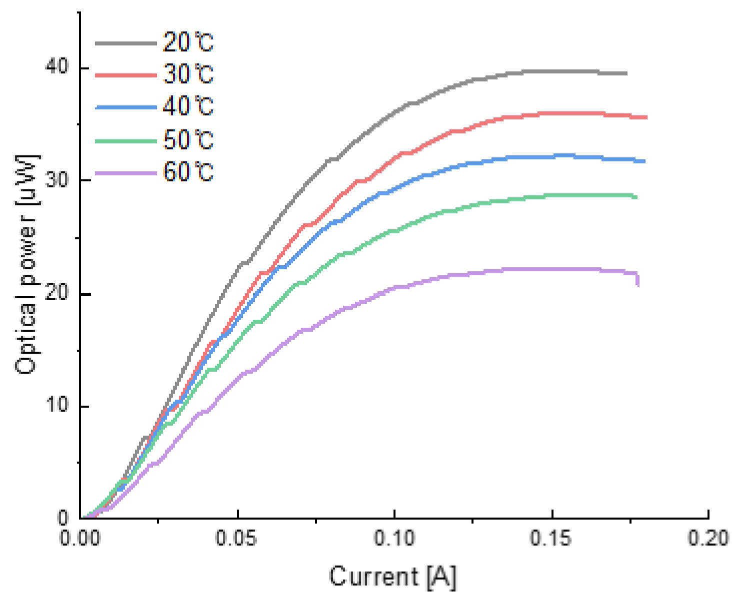

Figure 5.3: Result of optical power according to temperature.

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Fig.5.3 is a graph measuring the optical power while increasing the temperature from 20°C to 60°C. When the temperature increases, the electron-hole pairs that need to recombine in the QW gain energy by heat and exit the QW. The free carriers cannot recombine after that and are drawn to the contact by the potential difference. Therefore, as the temperature increases, the optical power decreases.

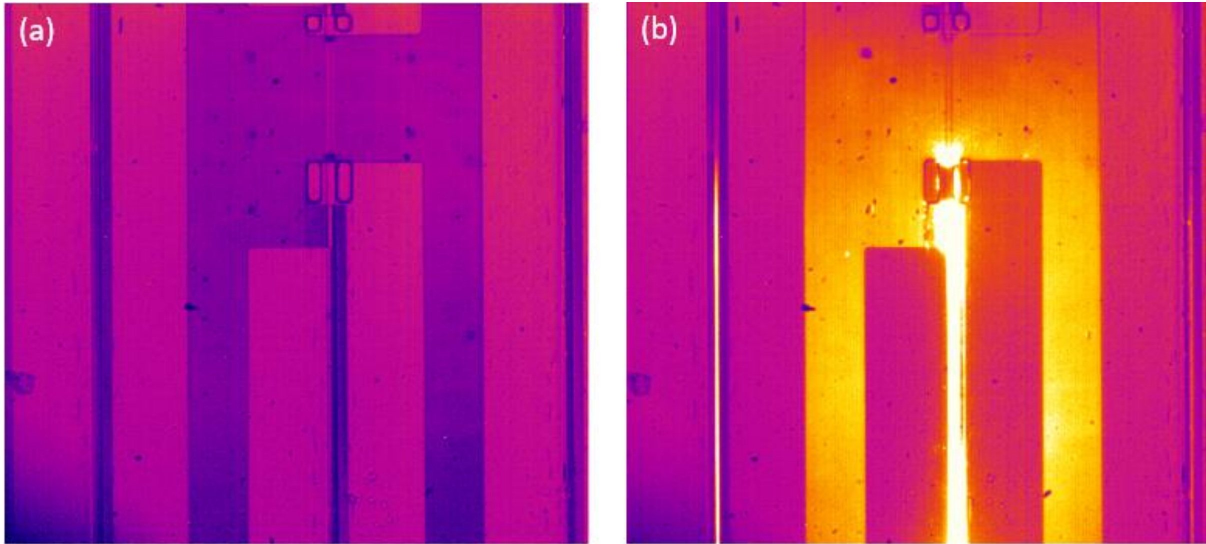

Figure 5.4: 600um cavity sample photograph observed with IR camera. (a) before applying current. (b) after applying 50mA current. There is no specular pattern.

Fig.5.4 is the photographs of 600um cavity laser. It can be confirmed that the light is generated when the current flows. However, it can be confirmed that it is not coherence light through the fact that the specular pattern normally observed in laser is not visible. Through this, it was judged that lasing was not performed according to the conclusion from the I-L curve.

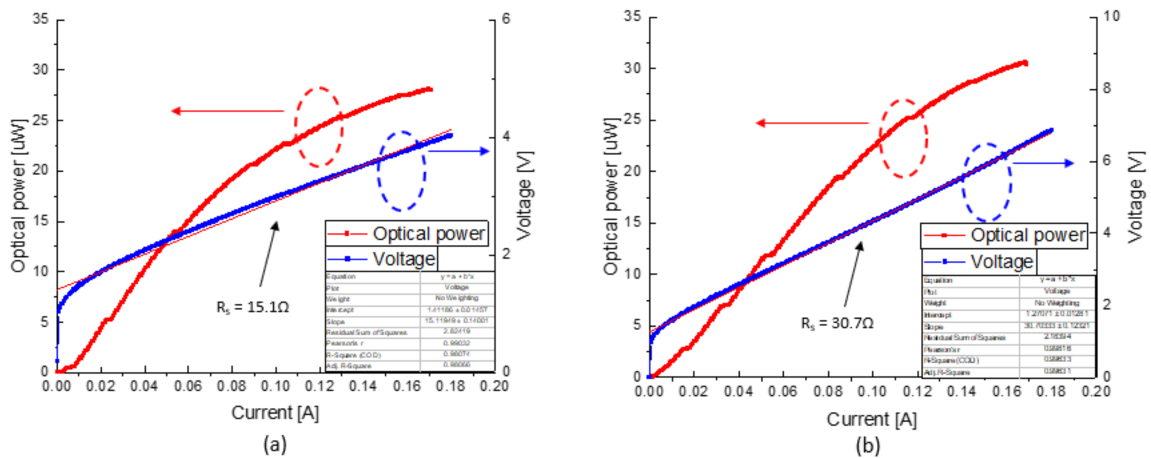

Figure 5.5: (a) This graph is the L-I-V curve corresponding to 1000um cavity. (b) This graph is an L-I-V curve corresponding to a 2000um cavity.

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No threshold current is observed about 1000um and 2000um cavity as shown in Fig.5.5. It can be seen that these cavities are not raised equally. Differential resistance is measured 15.1Ω and 30.7Ω, respectively.

5.2 Discussion

5.2.1 Comparison of I-V curve

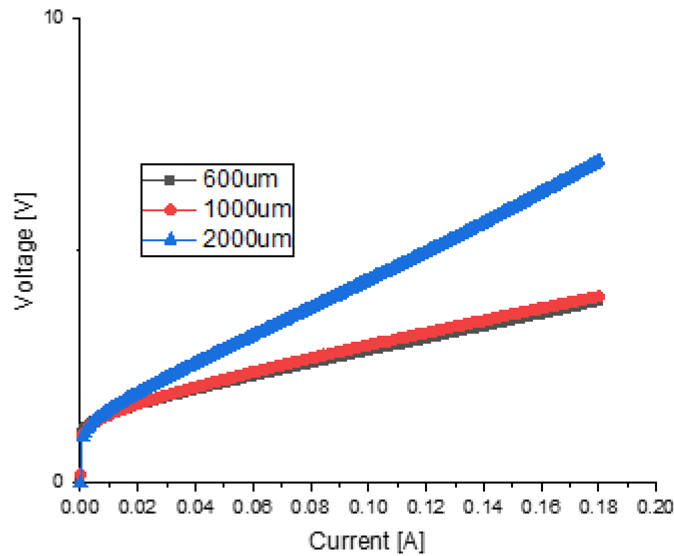

Figure 5.6: Graph showing the I-V curve of three cavities. It can be seen that the resistance increases as the cavity increases.

Fig.5.6, which compare to the IV curve for three cavities, shows differential resistance is larger for longer cavity sample. As a result of examining the reason, it was found that N-contact greatly affects resistance.

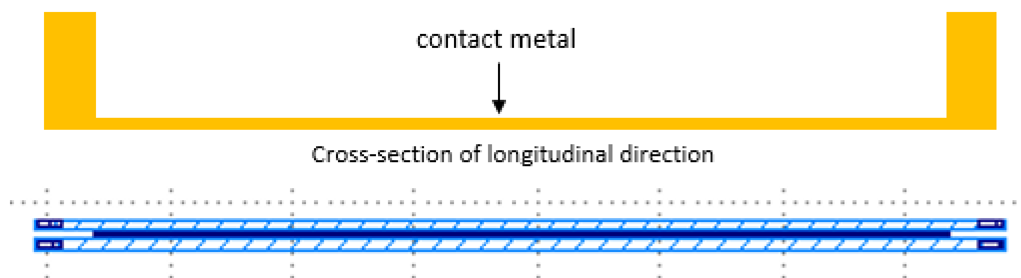

Figure 5.7: (Above) Schematic with N contact formed. The bottom is n ohmic metal, and the part that rises on both sides is an N contact pad. (below) layout file for N ohmic contact and contact opening.

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As shown in Fig. 5.7, the gap between N contacts increases as the length of the cavity increases due to small opening region. This means that the longer the cavity, the longer the current path for electrons. The resistance is obtained from Equation 5.1 below.

$$R = \rho \frac{L}{2A} \quad (5.1)$$

ρ is the resistivity, L is cavity length and A is area of ohmic metal. Because current flows from both sides so, current path for electrons is half the length. Therefore, the factor of 1/2 is caused. The results are summarized in a table below.

Cavity	Calculation	Measurement
600um	12Ω	14Ω
1000um	19Ω	15Ω
2000um	38Ω	30Ω

Table 5.1: Calculated and measured results of differential resistance.

It can be seen that current path for electrons increases with cavity longer. Resistance also increases with cavity longer. I searched other group's researches [16, 43]. The differential resistance of their works is below 10Ω.

Through the resistance calculated above, the heat power generated by Joule heating can be calculated. The result was derived from Equation (5-2).

$$P = I^2 R \quad (5.2)$$

The original heat power is calculated by subtracting the optical power from the electrical power. Equation (5.2) is related to electrical power, but the optical power of this sample is about several tens of uW, so it can be ignored. Therefore, electrical power is assumed to be heat power and calculated.

Cavity	Power generated by Joule heating
600um	176mW
1000um	292mW
2000um	585mW

Table 5.2: Calculated results of heat power from differential resistance.

Using the heat power obtained above, the temperature increasing by resistance can be obtained. The further increased temperature is obtained as Heat power*Thermal resistance.

Cavity	Further increased temperature
600um	24℃
1000um	40℃
2000um	81℃

Table 5.3: Calculated results of increased temperature by resistance.

Since that is an additionally increased temperature, the actual temperature is obtained by adding the room temperature to it. In general, an in-plane laser which has a large cavity does not work beyond 60°C. Therefore, from this result obtained in Table 5.3, it can be inferred that one of the reasons for not lasing is heat. In addition, we can conclude that the longer cavity creates higher resistance and generates more heat.

5.2.2 Comparison of I-L curve

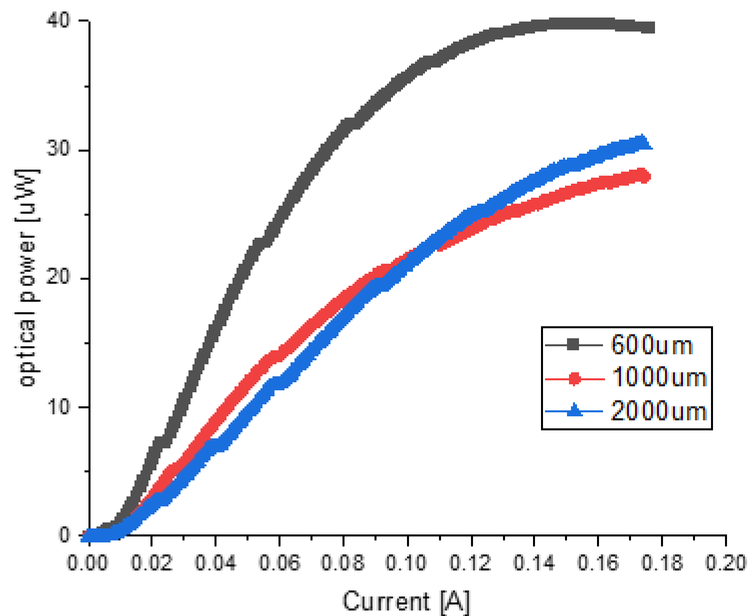

Figure 5.8: Graph showing the I-L curve of three cavities. The longer the cavity length, the lower the optical power.

Looking at the Fig.5.8 results for the three cavities, it can be seen that the optical power of the 600um cavity is the highest. The reason is that the heat generated by the resistance obtained above is the lowest, and as a result, it can be inferred that the optical power of 600um is the highest.

5.2.3 Impact of dislocation

Fig.5.9 shows the surfaces of fabricated epitaxy. If you look at the surface, there are a lot of dislocations or etch-pits. When removing the cap layer, dip into HCl or H_2SO_4 to proceed with selective wet etching. At that time, the etch-pits by the solution combine with the dislocation and a hole as shown in Fig.5.9

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is generated. According to [44], threading dislocations have a strong influence on radiative efficiency. The screw and mixed dislocations should act as the dominant non-radiative centers. It can be confirmed that significant amount of dislocation acts as a non-radiative center, and as a result, lasing does not occur.

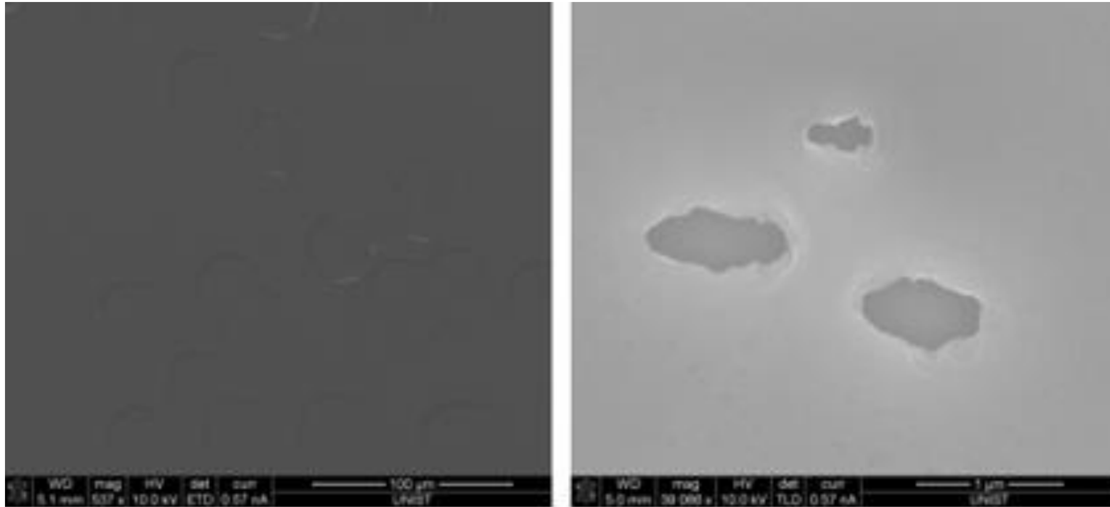

Figure 5.9: Significant amount of dislocation has been observed on fabricated epitaxy.

In the next section, we will discuss solutions to the problems presented above, dislocation as non-radiative center and heat generated by resistance.

5.3 Solution

New N-contact design

The large resistance problem presented above exists for the following reasons:

- Due to current path for electrons
- Due to very thin N-ohmic contact metal

Among them, the method to solve the current path problem is shown in Fig.5.10. Fig.5.10 (a) shows the current structure. It has a very long current path for electrons, so a lot of heat is generated by the resistance. Considering the structure of Fig.5.10 (b), the current path is reduced by more than 1/4 compared to (a). Therefore, it can be expected that the resistance by the current path will drop to 1/4 or less. Fig.5.10 (c) is a structure that covers all of the N-ohmic metal with the contact pad. In this case, it can be expected that there will be only resistance due to the contact between the metal and the substrate because there is no current path for electrons. Through these structures, the differential resistance can be reduced and the power generated by the resistance also can be reduced. As a result, it is possible to reduce the burden on the laser by reducing the further increased temperature.

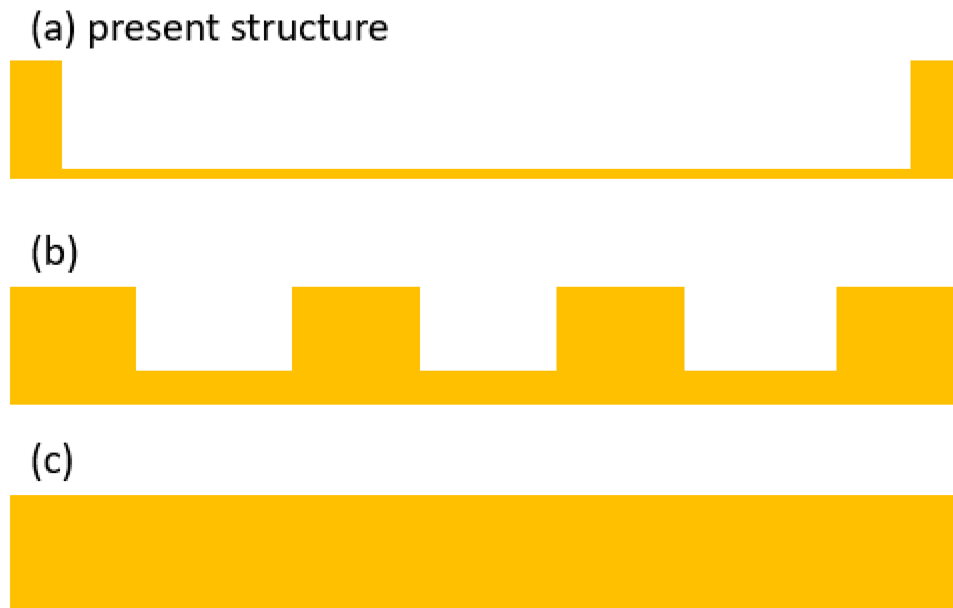

Figure 5.10: structure of N-metal appearance. (a) present design. (b) Design that reduces current path by more than 1/4. (c) Design that covers all N-ohmic contacts with contact pad.

In addition, the thickness of the N-ohmic contact is now 20nm. If you increase it to 100nm, the second effect can also be reduced to more than 1/5. These two methods will solve the heat problem.

Improvement of epitaxy

The most common solution can be obtained from the reason dislocation occurs. Epitaxy consists of stacks of various materials. Dislocation occurs when the lattice mismatch between the materials overlaps and grows. Therefore, if InP as the buffer layer, which is the same material as the substrate, is grown by 1~2um to compensate for lattice mismatch, we can be sure that dislocation will occur less.

In general, the doping level of the p contact layer is 1e19 like ours. However, the degree of dislocation is also different depending on the material to be doped. Therefore, optimizing the p-contact layer using a widely used material is one way to reduce dislocation.

5.4 Summary

We measured the produced laser and analyzed the results. The laser did not do stimulated emission, and the reason was quantitatively analyzed. The first reason is the increased heat due to the large differential resistance. The second reason is the large number of dislocations distributed on the surface.

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As a solution to the first problem, it is suggested to reduce the current path for electrons and to deposit the ohmic contact metal thickly. As a solution to the second problem, stacking a buffer layer and optimization of p-doping of InGaAs are presented.

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Chapter 6. Conclusion

6.1 Summary

In this thesis, In-plane hybrid laser which has large active volume is used for optical connection in data center and long-distance communication. A study was conducted to improve the efficiency of the laser used here to transmit data faster and longer distances. To increase its efficiency, we established the full design procedures for hybrid DBR lasers corresponding to the following:

- To increase the transition efficiency and decrease optical loss, we adjusted the thickness of the appropriate n contact layer and the thickness of the p cladding layer through designing of epitaxy
- To operate single-mode, we designed the narrow width of waveguide and taper structure
- Thermal design for efficient heat dissipation.
- Design the reflectance of DBR mirrors using the transfer matrix method.

In addition, we established the full processing condition including bonding method with good heat dissipation efficiency and bonding strength for hybrid DBR laser in UCRF. this could also be used to make advanced lasers.

Although the fabricated sample did not work as a laser, LED with power of several tens of uW was demonstrated. And the reason for not lasing was considered and the solution was suggested. By reducing the current path for electrons and increasing the Au thickness of the N-ohmic metal, the resistance can be lowered and heat generation due to the resistance can be reduced. In addition, it is possible to reduce the amount of dislocation acting as a non-radiative center through growth of the buffer layer and optimization of p-contact InGaAs.

6.2 Further work

Recently, research on Si_3N_4 waveguides with lower propagation loss than Si is being conducted. You can try making a laser on a waveguide made of Si_3N_4. In addition, in this paper, a very large scattering loss occurred because the taper structure was not applied to the epitaxy and waveguide. If it is made by realizing a very narrow line width through E-beam lithography, it will be possible to make the expected high-power laser. Finally, lasing will be possible enough if you remove the above-mentioned factors.

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Life is like a maze. Depending on the moment's direction selection, the arrival time may be earlier or significantly delayed. However, if you carefully assess your current location and judge rationally, you can eventually escape. Don’t fret, and don’t be so happy and sad. In the end we will laugh. The same is true for research and for everything to come. If you don't get discouraged and work hard until the end, you'll get the results you want. May everyone around me eventually reaches happiness.

Jinhyun Cha

UNIST

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