Master's Thesis

A 6.78MHz Adaptive-ZVS Class-D PA with Dynamic Dead-Time for Wireless Power Transfer system

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Approved by

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Abstract

In this thesis, a class-D power amplifier (PA) with adaptive zero-voltage switching (A-ZVS) technique for Low power 6.78 MHz resonant wireless power transfer (R-WPT) system is proposed. In R-WPT operation, the loading impedance of a PA can be varied by the process tolerance of the LC resonant components and WPT environments, such as the resonant topology, coupling coefficient and loading condition of the receiver. The proposed A-ZVS feedback loop of PA calibrates the equivalent resonant capacitance using PWM-controlled switched capacitor in real-time to achieve ZVS by adjusting the loading impedance to be slightly inductive. Furthermore, the proposed PA adjust the dead-time according to variation of WPT environments. The proposed PA was fully integrated except for one switched capacitor used as the tuning element and fabricated in a TSMC 0.18um BCD process. The measurement results demonstrated robust ZVS operation with a peak system efficiency of 52.7% and an enhanced maximum transmitting power of 107%.

Key Words—R-WPT system, Class-D power amplifier, Adaptive zero-voltage-switching(A-ZVS), Dynamic dead-time control, PWM-controlled switched capacitor

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I. Introduction

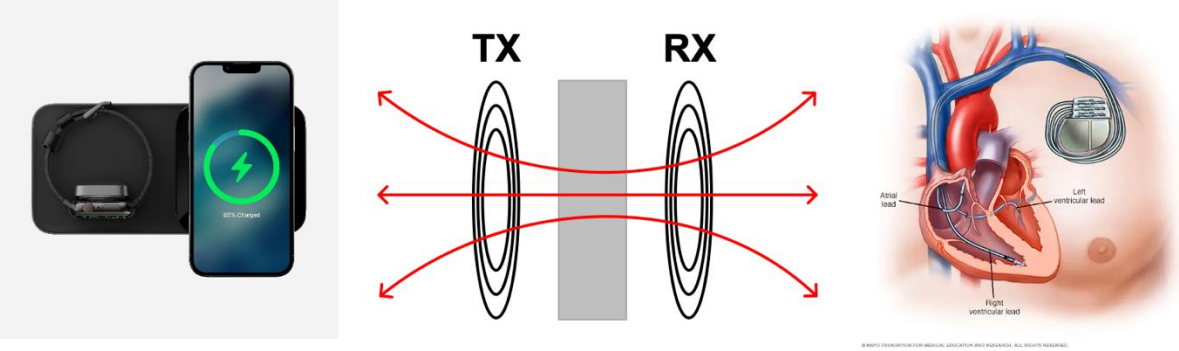


Fig.1 Utilization of wireless power transfer technology

The utilization of wireless power transfer (WPT) technology is increasing exponentially. WPT is applied to various applications such as portable devices and implantable medical devices (IMD) [1]-[4], fig.1. In a low power resonant wireless power transfer (R-WPT) system for portable devices or implantable medical devices, series-parallel (SP) compensation topology and multi-MHz resonance frequency are used to reduce the value of LC components and achieve high efficiency.

Class-D and Class-E configuration have been widely used as the power amplifier (PA) of the Multi-MHz R-WPT system. Class-E can achieve high efficiency by satisfying both zero-voltage-switching (ZVS) and zero-voltage derivative switching conditions through optimized output filter design in specific loading conditions. However, since the optimal condition is sensitive to variation of coupling and loading condition, it is difficult to maintain the optimal condition in a situation where it is difficult to fix the WPT environment. On the other hand, class-D PA has the advantage of being able to perform well under relatively wide coupling and loading conditions, and having less voltage and current stress on the power switch than class-E PA [5].

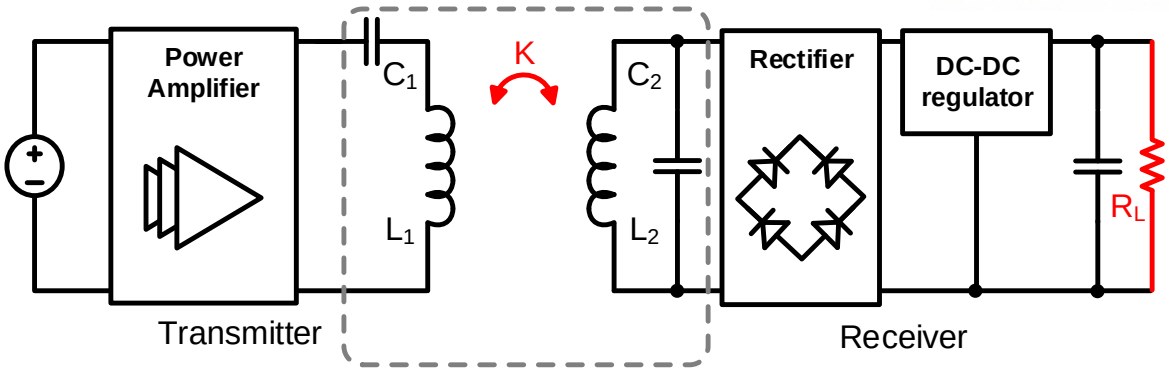


Fig.2. Design consideration of wireless power transfer system

Class-D PA consists of two power switches and a switch driving signal, fig.3. It is a structure in which two switches are turned on and off to push-pull the floating V_X node. For class-D PA to perform ZVS operation, the VX node must be charged/discharged during the dead time so that the V_{DS} is zero at the turn-on time of the switches. When PA drives a slightly inductive load, ZVS is achieved, and the waveform at that condition is shown on the right. There are three other conditions that are not tuned, fig.4. They are classified according to the relationship between switching frequency and resonance frequency. In resonance condition, hard-switching occurs and body-diode connection occurs in inductive condition. However, in capacitive condition, both hard-switching and body-diode-connection occur. They all contribute to reduced efficiency of PA.

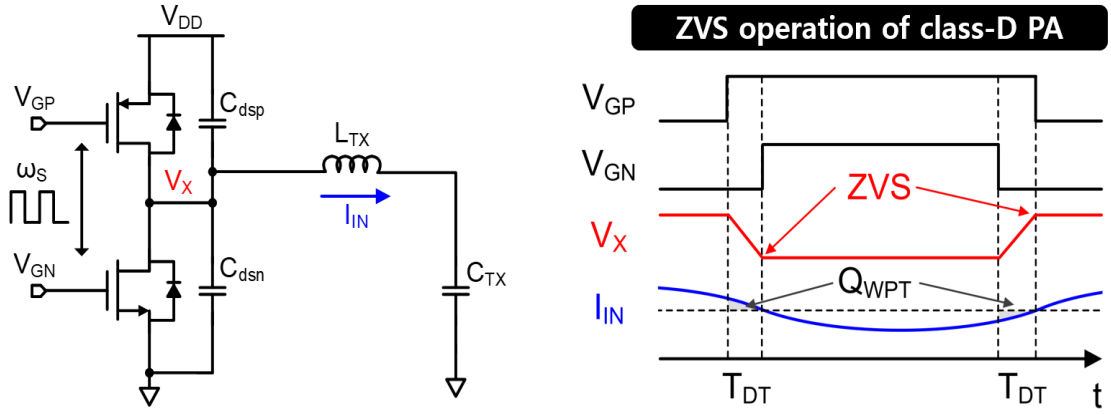


Fig.3. Zero-Voltage-Switching condition of class-D PA

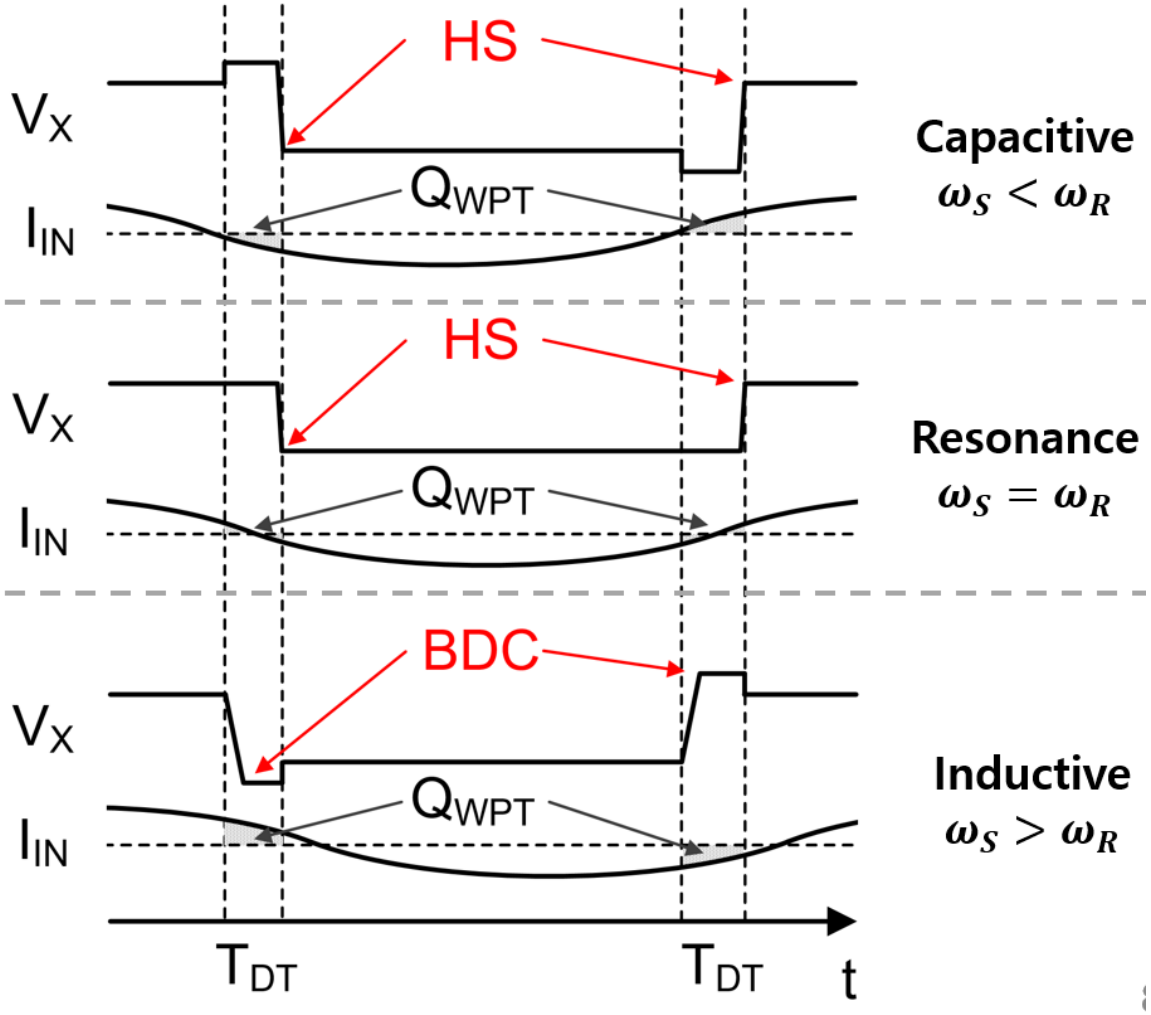


Fig.4. Untuning condition of class-D PA

Since the R-WPT system of multi-MHz is designed to have a high Q-factor to overcome low magnetic coupling, deviation of resonant frequency of LC tank can weaken the generated magnetic field and drastically reduce the amount of power that can be transmitted. Unfortunately, value of inductance and resonant capacitance of the coil may be changed by process variation and transmitter (TX) coil inductance may be affected by ferromagnetic elements used to protect the electronic device from a magnetic flux in the receiver (RX). Furthermore, as shown in fig.5, SP topology which is frequently used in low-power applications, has the characteristic that the inductance of TX coil is detuned as the coupling coefficient (K) increases.

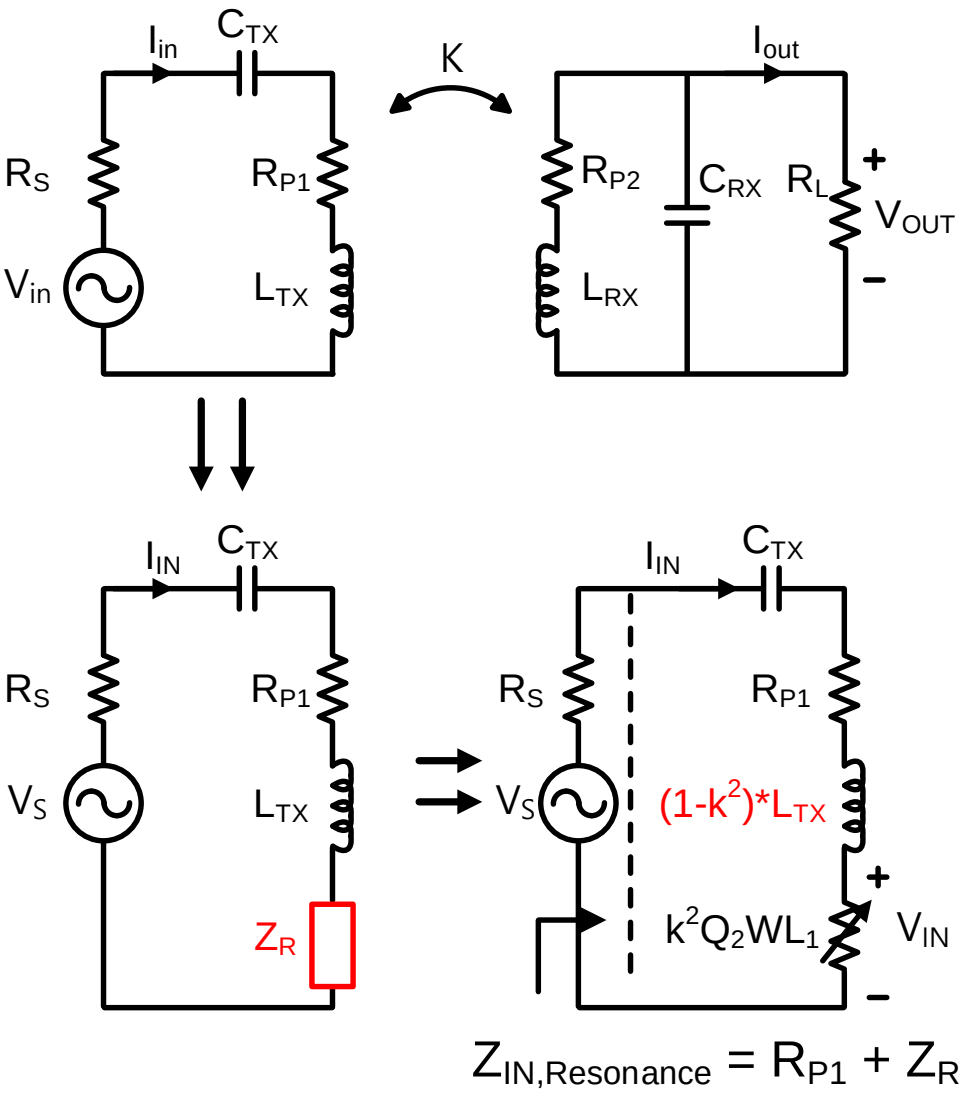


Fig.5 Equivalent modeling of series-parallel topology with reflected impedance

Due to this detuning phenomenon, the resonant frequency of the TX LC tank is shifted to higher frequency than the designed value and the PA operated in a capacitive region, resulting in switching loss due to hard-switching. The hard-switching behavior of PA with multi-MHz switching frequency causes high-frequency ringing in the power loop by the parasitic inductance of print-circuit-board (PCB) and output capacitance of the power switch, fig.6. This ringing generates electromagnetic interface (EMI) and increases the power loss that occurs in power switch [6], [7].

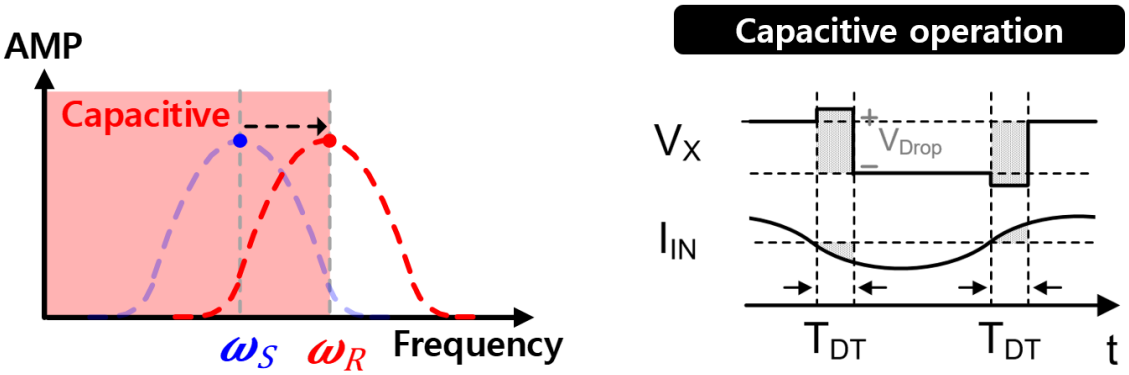


Fig.6. Capacitive load of class-D PA

The problem of resonant frequency deviation can be solved by tracking excitation frequency according to the resonant frequency of LC tank [8], [9], but it is difficult to apply because the frequency available by band allocation restrictions is limited. Therefore, to increase the efficiency of the R-WPT system and increase the amount of transmitting power, the ZVS of PA must be achieved and the resonant frequency calibration of the TX LC tank must be performed according to coupling and loading conditions.

To increase the power conversion efficiency (PCE) of PA by removing the switching loss proportional to the output capacitance of PA and the operating frequency of multi-MHz, techniques for achieving ZVS were presented in [10]-[14]. In [10], capacitors were added in parallel to the series-resonant LC tank of the receiver so that the equivalent loading condition viewed from PA was inductive, and ZVS condition was achieved by adjusting dead-time using DLLs. However, ZVS may not be achieved as variation of coupling and loading condition, because it is applicable only to a specific RX capable of shifting the resonant frequency of the RX LC tank from excitation frequency and standard delay cells vulnerable to PVT variation are used inside the DLL.

In [11]-[12], a series-connected auxiliary tank with a cut-off frequency much lower than TX LC tank was added in parallel to the output node of PA so that equivalent loading condition viewed from the PA was inductive. Then the dead-time was set by calculating the amount of charge to achieve the ZVS and current flowing through the auxiliary LC tank. This method requires a large external LC component and the current flows continuously in the auxiliary LC tank, resulting in additional conduction loss.

In [13]-[14], to improve additional conduction loss, the auxiliary LC tank was operated discretely only at dead-time, reducing the value of LC components, and eliminating constant current consumption. However, the ZVS technique using auxiliary LC tank cannot resolve the resonance frequency deviation and component tolerance of the TX LC tank, requiring additional resonance point calibration technique.

To compensate for environmental effects such as loading condition or adjunct ferromagnetic elements and LC component tolerance, equivalent capacitance of TX LC tank tuning method is widely used. In [16], the voltage-controlled capacitor (Varactor), and in [17]-[21], the resonant capacitance tuning technique using the switched capacitor was presented. Among them, [17]-[18] tune the capacitance required for resonant point calibration using a selectable capacitor array, which increases the system volume and cost because it requires many capacitors and HV switches to increase the tunable resolution and tunable range. In [18]-[21], a pulse width modulation (PWM) technique was used to calibrate the duty ratio to which the switched-capacitor is connected. The equivalent capacitance of switched capacitor can be adjusted by calibrating the duty ratio of a PWM signal, so it can be implemented in a smaller area than a method using capacitor array. However, in [18]-[20], the ramp signal and the variable feedback voltage are compared using comparator to generate a PWM signal, and in the multi-MHz operating frequency, the effect of the circuit delay occurring in comparator cannot be ignored, thus reducing the controllable duty range, and affecting the phase and operation timing. Also, in class-D PA, the power loss and ringing phenomenon due to hard-switching can still occur because ZVS is not achieved at the resistance load where the resonant point of TX LC tank is fully compensated. In [21], ZVS was achieved with slightly inductive tuning, but feedback loop was composed with several external devices such as DSP and two HV switches.

In this thesis, class-D PA for 6.78MHz R-WPT system was presented, which performs resonant point tuning of TX LC tank and ZVS calibration of PA at the same time. The duty ratio of the PWM controlled switched capacitor was adjusted to satisfy the ZVS condition of PA through the fully integrated feedback operation to eliminate the switching loss of PA and suppress the ringing phenomenon. The PWM controller performed duty ratio control using Delay-line without a comparator so that it could operate stable even at multi-MHz. Dynamic dead-time control was presented that adjust dead-time in response to variation of coupling and loading condition so that the ZVS feedback loop has increased its operating region and guarantees stability for WPT environments.

Through the proposed techniques, it was possible to increase the transmittable power in supply voltage of PA and improve the PCE of the PA. All calibration circuits and tuning switch of switched capacitor are implemented in the on-chip and only one external capacitor is used. Therefore, the form-factor and power consumption were reduced.

Chapter 2

II. Design consideration

Fig. 7(a) and fig.7(b) respectively show the wireless power loop of the transmitter using the most used series-series (SS), series-parallel (SP) resonant topology and voltage source in the WPT system. Assuming that the excitation frequency and resonance frequency are matched, and ideal resonant cancellation occurs, TX coil's parasitic series resistance, R_{P1}, equivalent reflected impedance, Z_R remain in the wireless power loop. At this time, Z_R differs according to the resonant topology of RX. Which contains the capacitive component of $-jk^2wL_{TX,}$ resulting in the detuning effect of TX inductance. For this reason, the PA operates in a capacitive region.

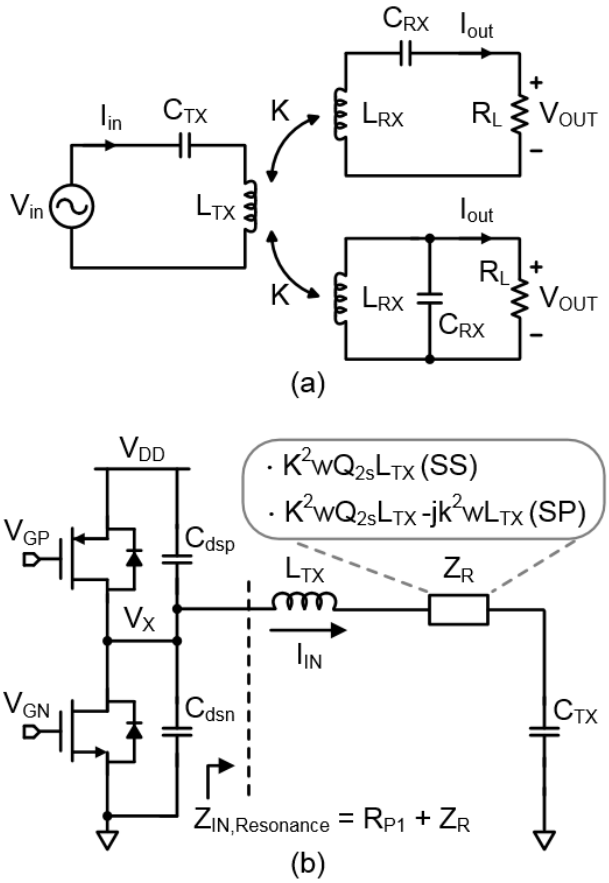


Fig. 7. (a) series-series (SS) and series-parallel (SP) resonant topology, (b) equivalent reflected impedance according to resonant topology

Class-D PA has a dead-time in which both switches are turned off between the operations of the switch to prevent the high and low side switch from being turned on at the same time. In the case of an

inductive power transfer (IPT) system using an excitation frequency higher than the resonance frequency of an LC tank, a current flowing through the inductor during this dead-time is charged or discharged by a parasitic capacitor of a V_X node, thereby performing a soft-switching operation. On the other hand, in the case of the RWPT system using the resonance frequency, the sum of the inductor currents during the dead-time is 0, or in the worst case, the PA operates in the capacitive loading condition and is opposite to the direction of the inductor current flowing during the dead-time. In this case, during the dead-time, the internal diode of the power switch is turned on to cause a body-diode conduction loss, and when the dead-time is over, a switching loss occurs due to hard-switching (1), (2).

$$P_{Diode} = \int_{t}^{t+T_{DT}} i_{in}(t) \cdot V_{Drop}\, dt \qquad (1)$$

$$P_{SW} = \frac{1}{2} C_o V_{DD}^2 f \qquad (2)$$

T_{DT} is the dead time, C_O is the total output capacitance of the output node of PA, and f is the excitation frequency of PA. Considering these power losses, the power conversion efficiency (PCE) of the class-D PA is summarized as follows (3).

$$\eta_{PA} = \frac{P_O}{P_{Diode}+P_{SW}+P_{COND}+P_O} \qquad (3)$$

P_{COND} is the conduction loss caused by the on-resistance of the power switch and the parasitic resistance of the TX coil, and the P_O is the power transferred to the coupled reflected load. Therefore, to improve the PCE of the PA, power loss must be minimized through ZVS. The amount of charge to achieve the ZVS condition of PA is $Q_{ZVS} = (C_{dsp}+C_{dsn})\cdot V_{DD}$, which is proportional to output capacitance and supply voltage. The previously reported auxiliary LC tank presented in figure 8 moved the Q_{ZVS} to achieve ZVS using current, I_{ZVS}, flowing through L_{ZVS} during dead-time, T_{DT}. In [11], [12], the LC component value and dead-time interval of the auxiliary LC tank to achieve ZVS are presented, assuming the perfect resonant condition of the wireless power loop. However, in the practical case, since resonant point deviation occurs due to environmental effects or component tolerance, ZVS may not be achieved according to coupling and loading condition of the wireless power loop as shown in figure 9.

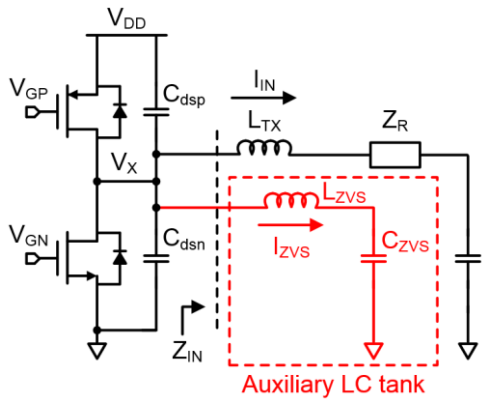


Fig. 8. Auxiliary LC tank

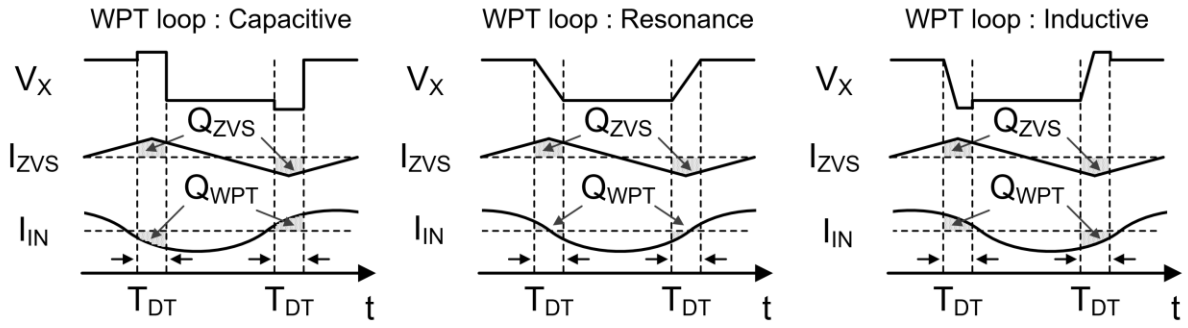


Fig. 9. Timing diagram of ZVS compensation from auxiliary LC tank when WPT loop is (a) capacitive, (b) resonance, (c) inductive.

Fig. 10 is a PWM-controlled switched capacitor used for wireless power loop resonant point tuning. ZVS turn-on of the tuning switch is essential for capacitance tuning using PWM-controlled switched capacitors. Since the R-WPT system uses a high Q-factor, the high AC voltage amplified by the Q-factor is applied to the resonant capacitor, C_{TX}. When the tuning switch of the switched capacitor is opened, the amplified AC voltage is applied to the drain-source voltage, V_{SW} of the tuning switch through a capacitive coupling. If the tuning switch does not operate in the ZVS turn-on operation, the charge stacked through the capacitive coupling flows out to the ground to generate power loss, and a sudden change in voltage at both ends of the redundant capacitor may occur, causing harmonic distortion.

The proposed paper used the following strategy for the switched capacitor's ZVS turn-on, fig. 11. In an ideal resonance condition, the driving signal, V_X, and inductor current, I_{IN}, of the PA are in-phase, and the capacitor voltage, V_C, is 90 ° lagged. Based on this, V_C synchronizes with the rising edge of V_X, which becomes the negative maximum, and turns on the driving signal, V_{PWM}, of the tuning switch for a predetermined period. During the T_{ON} when the tuning switch is closed, the fractional capacitor and the C_{Frac} are connected in parallel to the C_{TX}. Thereafter, when the tuning switch is opened, the C_{Frac} is

disconnected and the V_{SW} follows the V_C slope through a capacitive coupling. When the V_{SW} falls below 0 V and the internal diode is turned on, the switched capacitor is connected in parallel again and the V_{SW} remains at the negative diode turn-on voltage. Then, when the tuning switch is turned on in the next cycle, only the voltage drops as much as the diode-voltage drop occurs, this voltage drop is sufficiently small compared to the VC voltage amplified by the high Q-factor, and thus can be ignored.

Since the LC resonant tank acts as a bandpass filter and the driving signal applied from the PA becomes a sinusoidal wave, the equivalent capacitance value of the PWM-controlled switched capacitor can be calculated from fundamental elements. When the current flowing through Inductor, L_{TX}, I_{IN}, and $I_O\sin(wt)$ are used, the current flowing through C_{TX}, and the fundamental element of I_{CTX} can be calculated as follows.

$$I_{CTX\_fund} = \frac{2}{T}\int_0^T I_{CTX} \cdot \sin(wt)\, dt \tag{4}$$

$$I_{CTX\_fund} = \frac{I_O}{T}\{T + 2(\beta - 1)t_{on} + \frac{(1-\beta)T}{2\pi}\sin(2wt_{on})\} \tag{5}$$

T is the period of excitation frequency and β is $C_{TX}/(C_{TX}+C_{Frac})$. In addition, the fundamental element of voltage applied to C_{TX} from (5) can be calculated as follows.

$$V_{CTX\_fund} = \frac{1}{jwC_{TX}} \cdot I_{CTX\_func} \tag{6}$$

Since the current applied to the total equivalent capacitor, C_{Eq}, is equal to I_{IN}, C_{Eq} is obtained from (5) and (6) as follows.

$$V_{CTX\_fund} = \frac{1}{jwC_{Eq}} \cdot I_{In} \tag{7}$$

$$C_{Eq} = \frac{TC_{TX}}{\{T-(1-\beta)(2t_{on}-\frac{T}{2\pi}\sin(2wt_{on})\}} \tag{8}$$

As can be seen from (8), C_{Eq} is adjustable through T_{ON}.

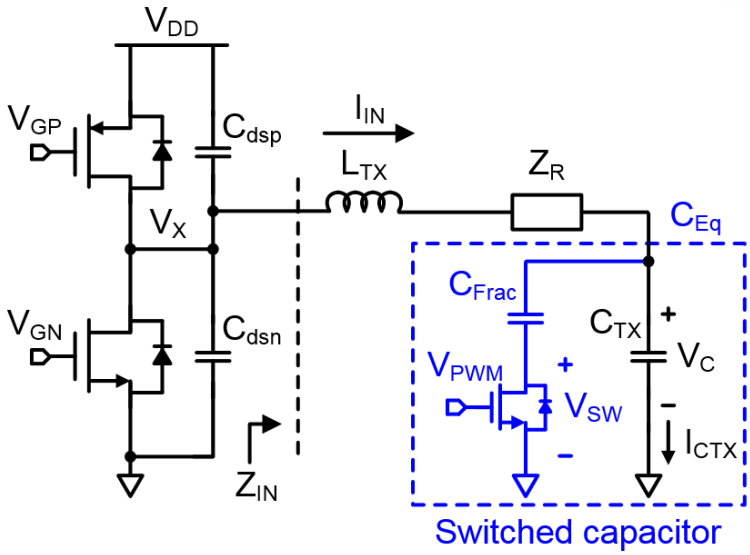


Fig. 10. PWM-controlled switched capacitor

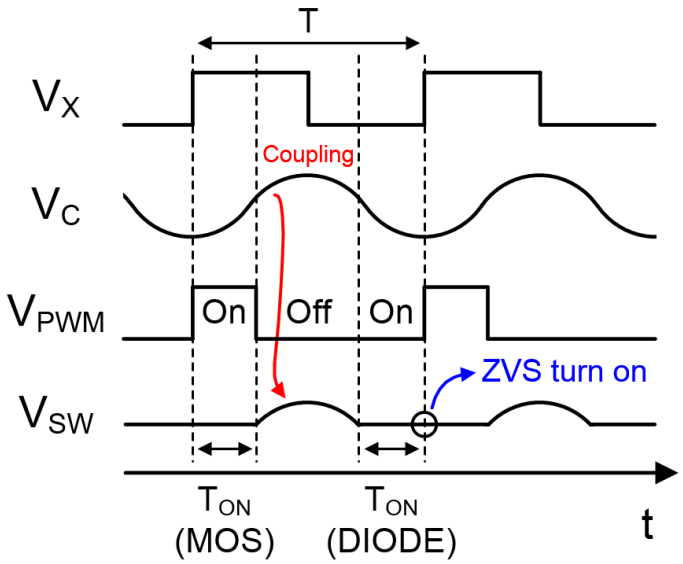


Fig. 11. Tuning switch control strategy and its timing diagram

Feedback operation through accurate resonance detection is required for fine capacitance tuning. Commonly used methods for resonance detection are tracking to maximize the value of the inductor current or capacitor voltage of the LC tank [16] or comparing the driving signal of the PA with the phase of the LC tank [18], and zero-crossing detection [21]. However, since the current or voltage is changed by the loading and coupling condition, in [15], output voltage information of rectifier was received through in-band communication and capacitance tuning was performed to maximize the output voltage. This method requires communication with RX and requires an external power consuming data processor. In [18], an external detection coil coupled to the inductor was additionally used, and after the current phase of the detection coil was 90° lagged compared to the inductor current, the capacitance value was

tuned so that the driving signal was different by 90°. In [21], DSP was used for detection and operation. As such, external devices used for capacitance tuning increase the complexity of the system.

Previous approaches [18]-[20] used PWM-controlled switched capacitor only as resonant point tuning, but the proposed PA can achieve real-time zero-voltage switching regardless of environmental effects and component tolerance by tuning the equivalent capacitance so that the loading condition of PA is a slightly inductive region. In addition, unlike [21], a capacitance tuning loop was implemented without the use of an external device through a fully integrated feedback loop. Detailed circuit implementation and operating principle are presented in section III.

Chapter 3

III. Circuit implementation

The overall architecture of the proposed PA is shown in fig. 12. The PA consists of main power stage and the proposed two control loops that conduct dynamic dead-time (DDT) control and adaptive zero-voltage switching (A-ZVS) feedback control with PWM-switched capacitor.

The proposed A-ZVS feedback loop continuously calibrates the total equivalent capacitance through a duty ratio change of the PWM-controlled switched-capacitor, C_{SW}, parallelly connected to the resonant capacitor, C_{TX}, to achieve ZVS. Equivalent capacitance is proportional to the tuning switch, driving signal of M_{SW}, and duty ratio of V_{PWM} as shown in equation (8), and the duty ratio of V_{PWM} is determined by the input V_{CAL} of the voltage-controlled delay line (VCDL) obtained through feedback. The feedback loop operates so that the V_{HOLD} sampled by V_X becomes zero to achieve ZVS. In addition, since the equivalent capacitance is calibrated through feedback, it is possible to respond to environmental changes such as loading and coupling conditions at the same time as achieving ZVS.

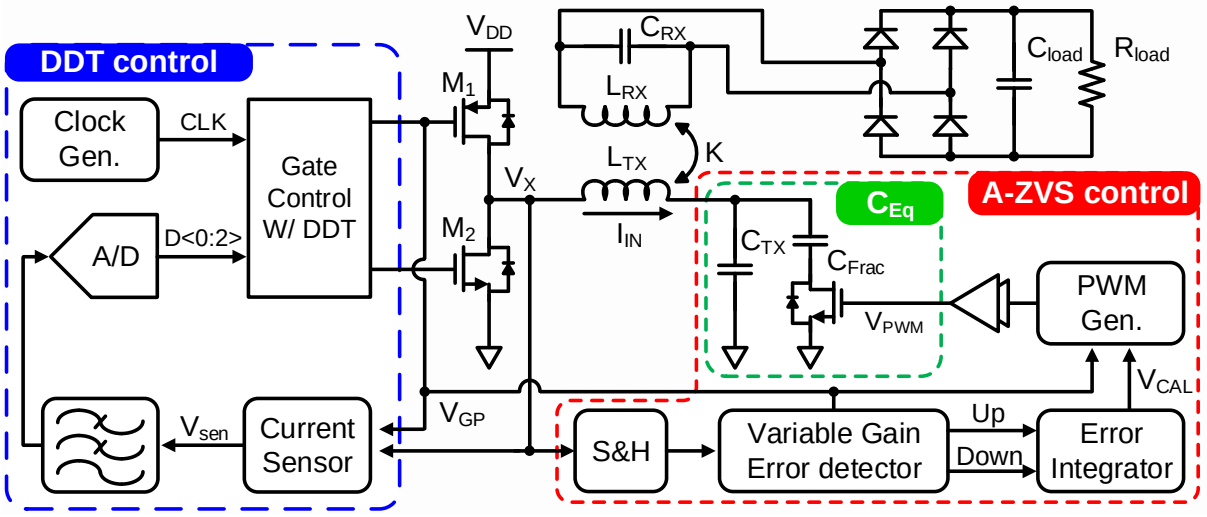


Fig. 12. Overall System Architecture of the proposed class-D PA

The proposed PWM generator in figure 13 presents a structure in which a delay-based operation is performed to solve the circuit delay issue of the existing comparator-based structure. This thesis removes ramp generator [22] and comparator [23]-[25] and generates V_{PWM} using voltage-controlled delay line (VCDL) and SR latch which proportion to voltage, V_{CAL}, to obtain an accurate switch timing and increasing controllable duty range. The timing diagram is shown in fig.14.

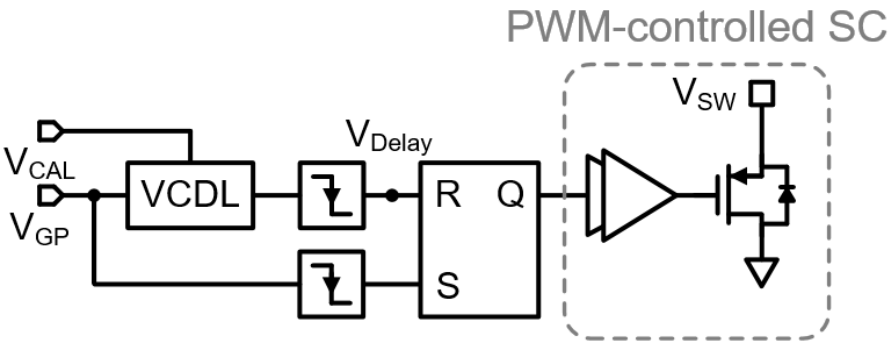


Fig. 13. Circuit implementation of PWM generator

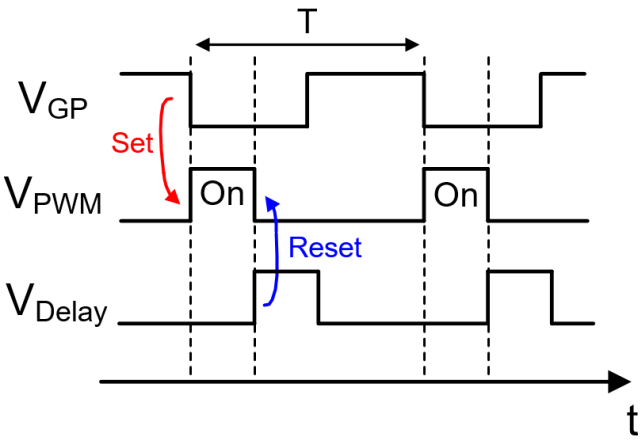


Fig. 14. Timing diagram of PWM generator

The A-ZVS compensation is executed through the current I_{IN} of the wireless power loop during dead-time when the high-side switch, M_1, and low-side switch, M_2, are all switched off. However, according to the WPT environment, the impedance reflected in the TX changes, and the amplitude of the I_{IN} flowing in the primary power loop also changes. Variation in I_{IN} affect ZVS compensation executed through I_{IN}. Therefore, the proposed PA constructed a dynamic dead-time (DDT) control loop that changes dead-time to reduce the effect of variation in I_{IN} on A-ZVS loop. Since the amount of charge to achieve ZVS is fixed to $Q_{ZVS} = I_{ZVS}*T_{DT}$, the DDT control loop in fig.12 changed the dead-time to be inversely proportional to the change in amplitude of I_{IN}, minimizing the effect on the change in I_{IN}. Through DDT control loop, the stability of ZVS compensation for environment variation was strengthened.

The proposed PA was fabricated in a TSMC 180nm BCD process. All control loops including power transistors were designed using CMOS components and tuning switch, M_{SW}, was designed using HV laterally diffused MOSFER (LDMOS) with a drain-source voltage limit of 65V to withstand voltage stress applied by capacitive coupling.

A. ZVS control circuitry

For calibration of V_{CAL} required for V_{PWM} duty control of PWM generator, ZVS feedback control loop is composed of sample and hold (S&H) circuit, Variable gain error detector, integrator, PWM

generator and switched capacitor. The loop is as shown as fig.15.

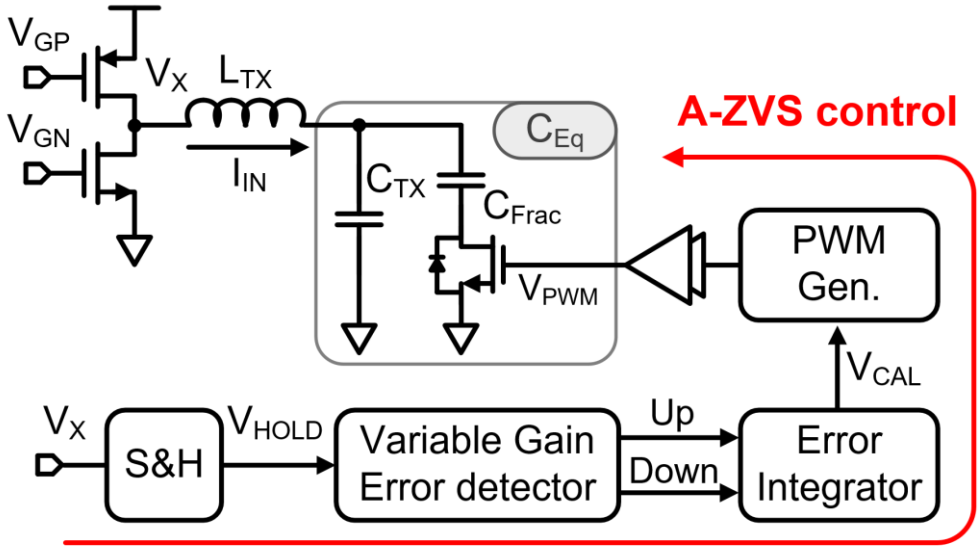


Fig. 15. A-ZVS control loop of the proposed class-D PA

The sample and hold (S/H) circuit samples the V_X node voltage at the moment of M_2 turns on. In this case, the RC delay interferes with accurate sampling and is reflected as an error in the ZVS feedback loop operating so that the V_{HOLD} is finally zero. Therefore, to minimize the RC delay, it is possible to obtain accurate V_{HOLD} by placing cut-off frequency at the GHz.

Fig.16 shows the charge pump as error integrator. The variable gain error detector and charge pump calibrate the V_{CAL} that determines the duty ratio of the V_{PWM} so that the V_{HOLD} becomes zero. The process of calibration of V_{CAL} is as follows. First, the charging/discharging of VCAL is determined by comparing V_{HOLD}, which is a voltage value sampled by the (S/H) circuit, with 0V. When V_{HOLD} is higher than ground, which means that greater equivalent capacitance is needed to achieve ZVS, and Dynamic On-time Generator (DOTG) drives the PMOS, causing the PWN generator to output a wider width V_{PWM} by charging C_q. On the contrary, when the V_{HOLD} is lower than 0V, it means that lower equivalent capacitance is required, and thus DOTG (down) drives the NMOS to disable C_q and output a narrower width V_{PWM}.

DOTG presents a structure that dynamically changes the calibration speed of V_{CAL} by generating a UP (DOWN) signal with an on-time proportional to V_{HOLD}. The DOTG generates a UP (DOWN) signal in synchronization with the CLK. Thereafter, a variable on-time proportional to the V_{HOLD} value is generated through VCDL. The higher the input value, the longer the pulse with on-time, and the lower the pulse with the shorter on-time. Therefore, DOTG has the advantage of decreasing the settling time by increasing the calibration speed by taking a large amount of change in V_{CAL} when V_{HOLD} is close to VDD, and on the contrary, when V_{HOLD} is close to GND, the resolution of calibration can be increased by reducing the amount of change in V_{CAL}.

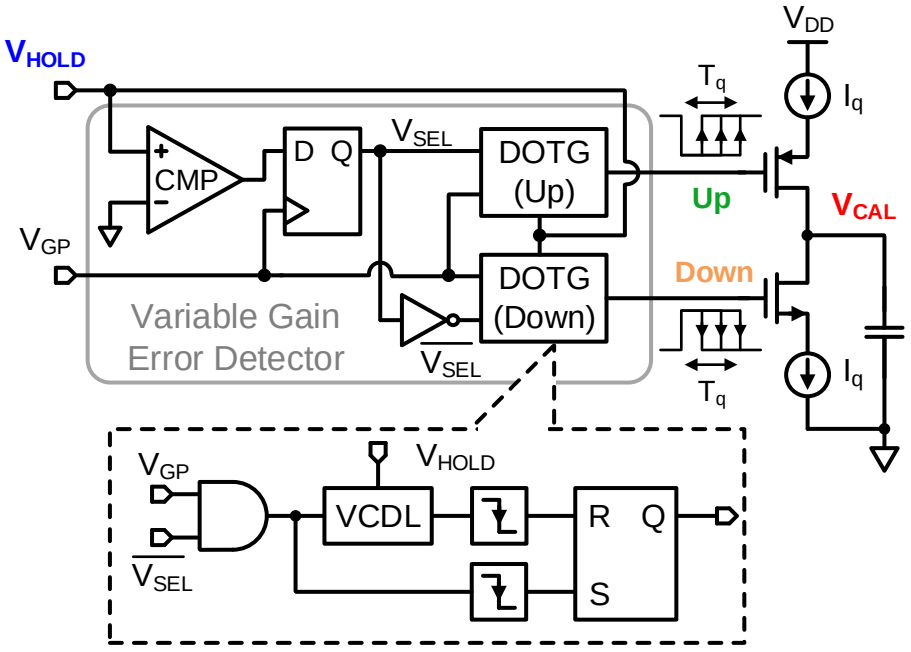


Fig. 16. Circuit implementation of variable gain error detector and error integrator

Fig.17 shows the structure [28] of the VCDL used to generate the on-time of the DOTG and PWM generator. The structure consists of a voltage to current (VTC) that converts an input voltage into a current and a current stacked inverter chain structure that adjusts a current supplied to the inverter chain to generate a delay. The delay generated in the inverter chain is the sum of the RC delay of the inverters as shown in equation (9), and the effective resistance of the inverters, R_n, is inversely proportional to the I_{FB} supplied by VTC.

$$Delay(In \rightarrow Out) \propto \sum_{n=1}^{k} R_n C_n \propto \sum_{n=1}^{K} {C_n}/{I_n} \quad (9)$$

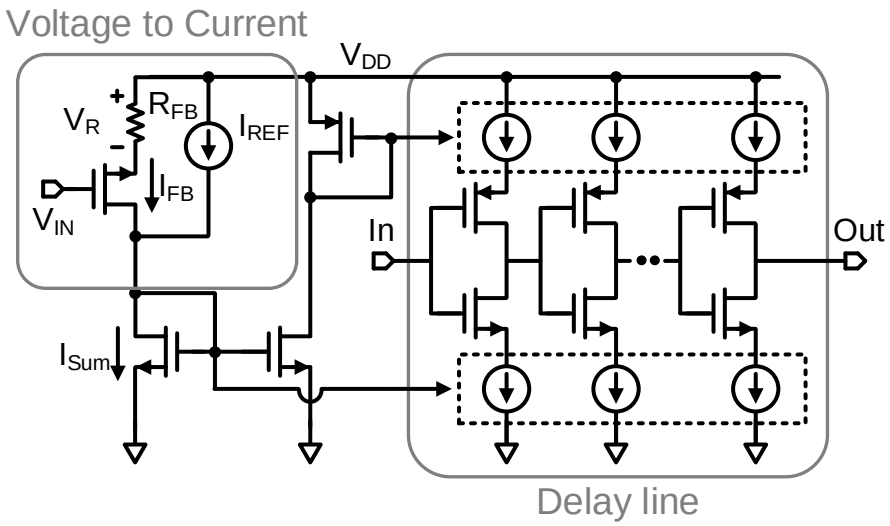


Fig. 17. Circuit implementation of voltage-controlled delay line

The on-time of the V_{PWM} is determined by the V_{CAL} calibrated by the A-ZVS feedback loop, and the on-time is generated through the previously used VCDL. The V_{PWM} generated through the ZVS

feedback loop adjusts the equivalent capacity so that the PA can achieve the A-ZVS.

B. DDT control circuitry

Figure 18. shows the Dynamic Dead-Time (DDT) control loop. The loop consists of the current sensor, LPF, 3bit ADC, and Gate driver with Dead-Time Selector (DTS).

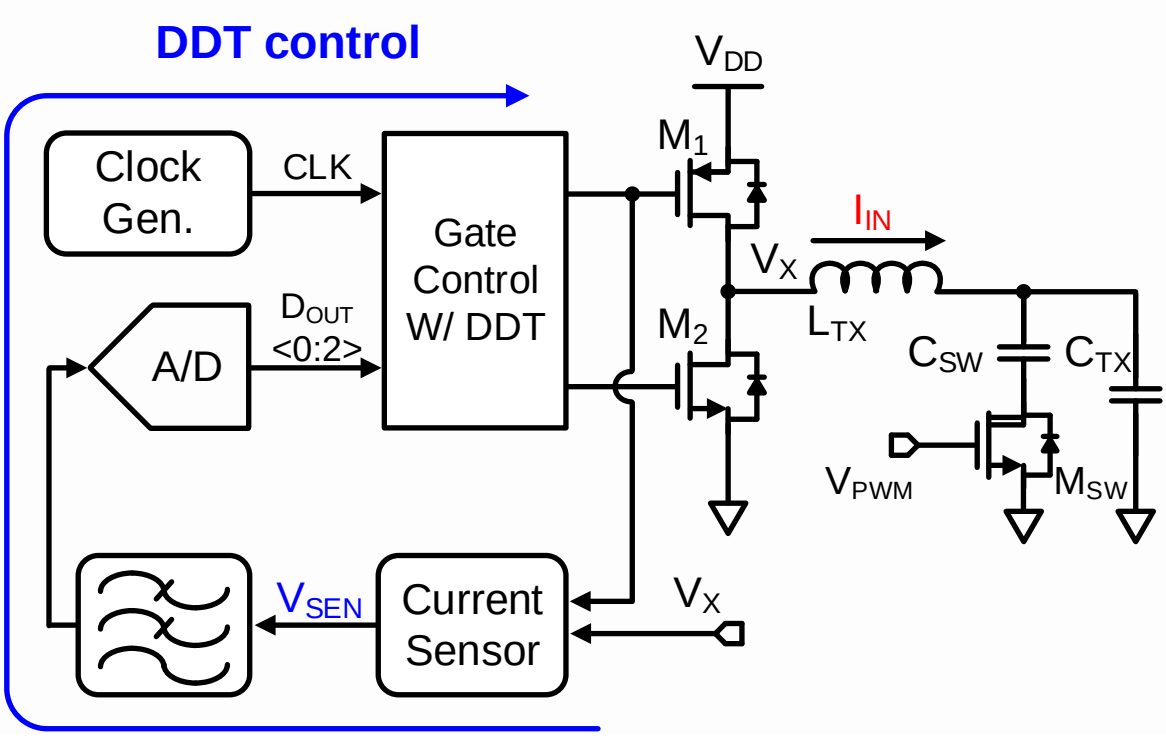


Fig. 18. DDT control loop of proposed PA

Fig.19 shows the circuit implementation of the current sensor. The current sensor obtains a current replica proportional to the size ratio of the MOSFETs with a power switch, M_1, in the power amplifier and a replica MOSFET, M_{R1}, scaled down 1/2000. For accurate current sensing, enforce V_{X1} and V_{X2} nodes as feedback loops via Error Amp so that the two MOSFETs, M_1 and M_{R1} have the same drain-source voltage values. The GBW of loop gain including Error amp was set to 920KHz, which is lower than the switching frequency of 6.78MHz, so that the V_{X2} node forms an average value of V_{X1}. When the V_{GP} is GND, the I_L is supplied through the M_1 and the V_X value is supplied to the V_{X1} through the M_{S1}. Two current biases of $M_{3\text{-}6}$ that make up the feedback loop, in Fig.10, I_{X1} and I_{X2} are also supplied by V_{X1} and V_{X2}, respectively. Also, to supply current bias when V_{GP} is V_{DD}, M_{S2} operating when V_{GP} is high was added. Replicated current, I_S is entered as Rsen and generates Vsen, except reference current I_{X2}. The equation of the sensed voltage is as follows.

$$V_{SEN} = R_{SEN} * I_{SEN} = R_{SEN} * \frac{I_L}{N} \quad (9)$$

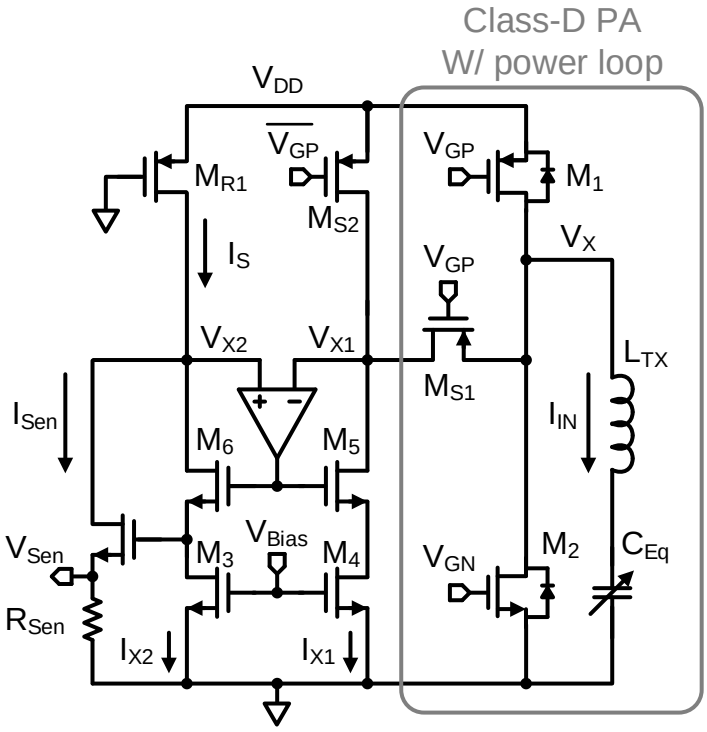


Fig. 19. Circuit implementation of current sensor

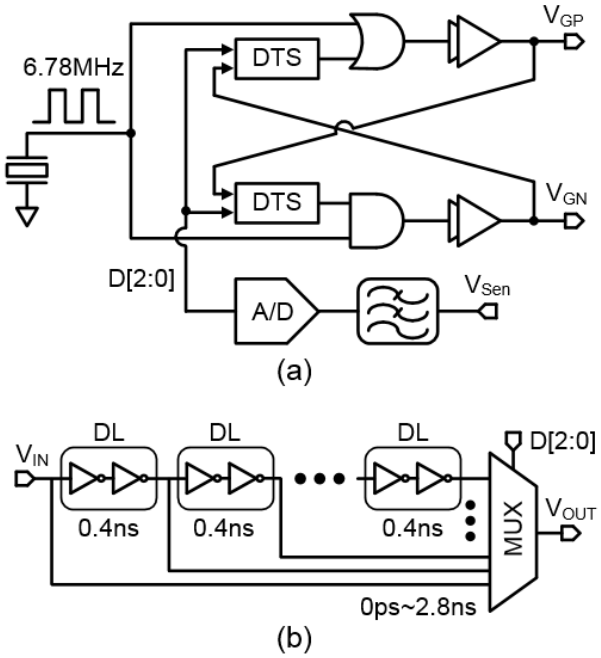
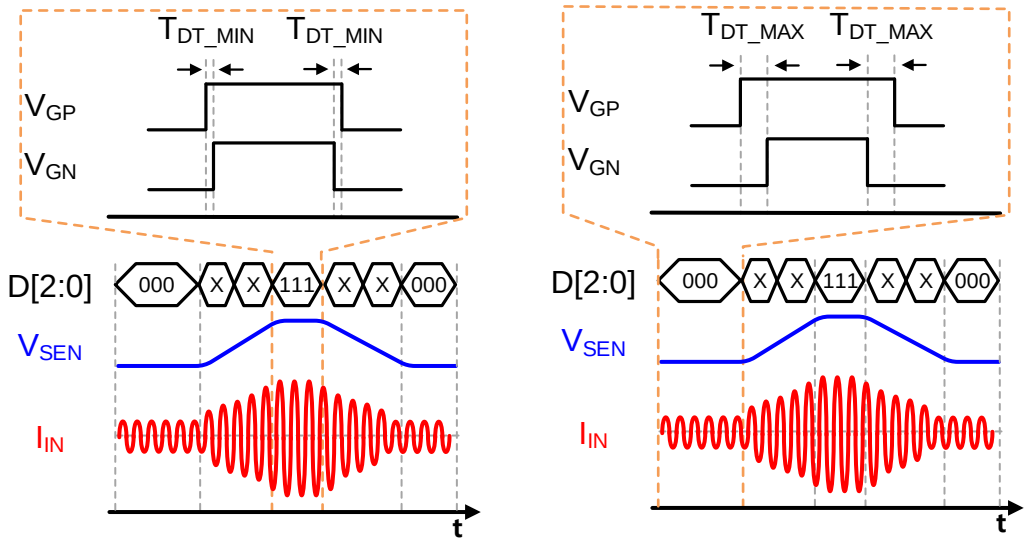


Fig. 20. Circuit implementation of (a) dynamic dead-time controlled gate driver
(b) dead-time selector (DTS)

V_{SEN} passes through an LPF with a cutoff frequency of 50KHz to eliminate high frequency noise, and passes through a 3-bit flash ADC to become digital data that determines the dead-time of PA.

Fig.20(a) shows the circuit implementation of the gate driver with Dead-Time selector (DTS). The

gate driver is designed to have dead-time to prevent shot-through, in which high-side and low-side switches are turned on at the same time. It operates under a clock signal of 6.78 MHz, with dead-time generating from 1 ns generated by the gate driver and 0 to 2.8ns variably generated by the amplitude of I_{IN} in power loop in the DTS, from 1 ns to 3.8 ns. As shown in Fig.20(b), DTS consists of eight units of Delay Cell (DL) and 8 to 1 MUX. 3 bits output from ADC select delay from DTS. As shown in Fig.21, when the inductor current, I_{IN}, is the largest, the input signal is directly output without going through the delay cell. Conversely, when the inductor current is the smallest, I_{IN}, the signal that has passed through the eight delay cells becomes output.



(a) (b)

Fig. 21. Operation waveform of DDT loop

Chapter 4

IV. Performance Behavior

A. Design parameter determination

Since the magnetic material and conductor sheet affect the magnetic flux of the TX coil, the inductance of the TX coil is very sensitive to the TX–RX distance variation [19]. As shown in Fig. 23, the inductance of the TX coil L_{TX} was measured according to the distance between the TX and RX. As the distance approaches, detuning occurs from 2.85uH to 2.4uH. As mentioned earlier, detuning effect not only causes hard-switching, but also increases the reactance of PA. Therefore, in proposed work, it was possible to compensate for the change in TX inductance while setting C_{SW} to 120pF.

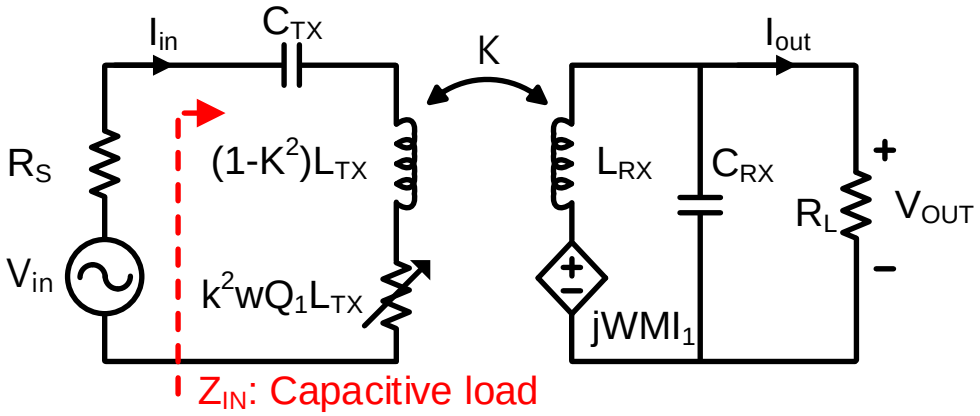


Fig. 22. Equivalent circuit of WPT system with SP topology

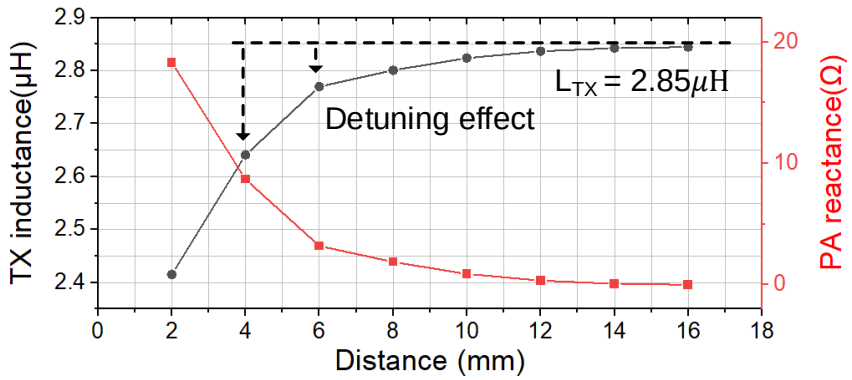


Fig. 23. Measured inductance detuning effect

B. Stability analysis

To verify that the A-ZVS feedback loop operates stably, we present a small-signal analysis for loop stability verification. Figure. 2s4 is a small-signal model of the A-ZVS loop.

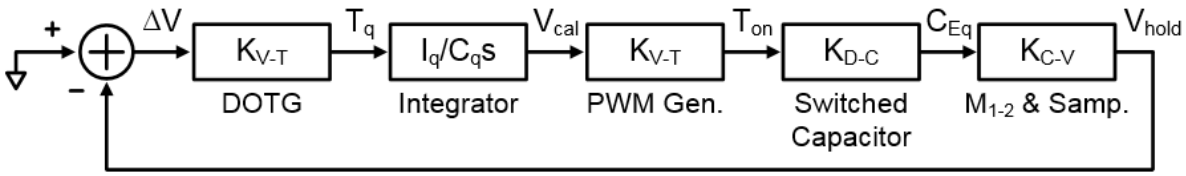


Fig. 24. Small-signal model of the ZVS calibration loop

Variable gain error detector, PWM generator was modeled with voltage to time block because delay occurs according to input voltage. The DC gain of these blocks is expressed as $K_{V\text{-}T}$. The switched capacitor was modeled as a time to capacitance block because the equivalent capacitance value changes according to the duty of the input signal (pulse). DC gain of this block is described as $K_{T\text{-}C}$. The Power MOSFET & sampling circuit was modeled the change in Vx node according to the change in equivalent capacitance with a capacitor to voltage block. In addition, the pole of the sampling circuit was ignored because the speed of the sample&hold circuit was much faster than the carrier frequency of 6.78MHz. The DC gain of this block is expressed as $K_{C\text{-}V}$. Variable gain error detector, PWM generator, switched capacitor, and power MOSFET & sampling circuit, except Integrator, have only frequency-independent DC gain in the frequency band desired to operate. Therefore, the transfer function of the A-ZVS control loop has 1 pole at origin and can be expressed as follows.

$$H(s) = K_{V-T1} \cdot K_{V-T2} \cdot K_{D-C} \cdot K_{C-V} \cdot \frac{I_q}{C_P s} \quad (10)$$

DC gain in loop gain is not affected by frequency, but has a variable DC gain depending on the operation point. Moreover, unlike other transfer functions, $K_{C\text{-}V}$ has environment dependency because it uses the inductor current, I_{IN} of the wireless power loop as the compensation current for A-ZVS loop. I_{IN} is inversely proportional to reflected resistance, $Z_R=k^2wQ_2L_{TX}$, and is affected by coupling coefficient and load resistance values.

The A-ZVS feedback loop synchronizes with the carrier frequency of 6.78 MHz and performs voltage sampling of the V_X node. For the feedback loop to operate stable and robust, the gain-band width (GBW) of the loop gain must be set lower than 6.78 MHz as in the figure.27. Therefore, in this paper, the maximum GBW of loop gain is designed to be 1/5 or less than carrier frequency even at the operating point where the variable DC gain of each transfer function is maximized.

To obtain the maximum DC gain, DC gains for the input of each block were extracted. Voltage controlled delay-line (VCDL) used as DOTG and PWM generator and PWM-controlled switched capacitor used for capacitance tuning have different gains depending on the input values as shown in Figure.25. As shown in figure 25, the simulation results of blocks modeled by voltage to time show that KV-T has a value of 0.1-19 ns/V. For the maximum GBW calculation, 19ns/V, the largest value, is used as the gain of PWM generator, and the gain of DOTG block operating at the steady state time of 0.7V is used as 0.1ns/V. In addition, Fig.26 shows the result of the PWM controlled switched capacitor block. This block has a maximum DC gain value of 1.92 pF/ns.

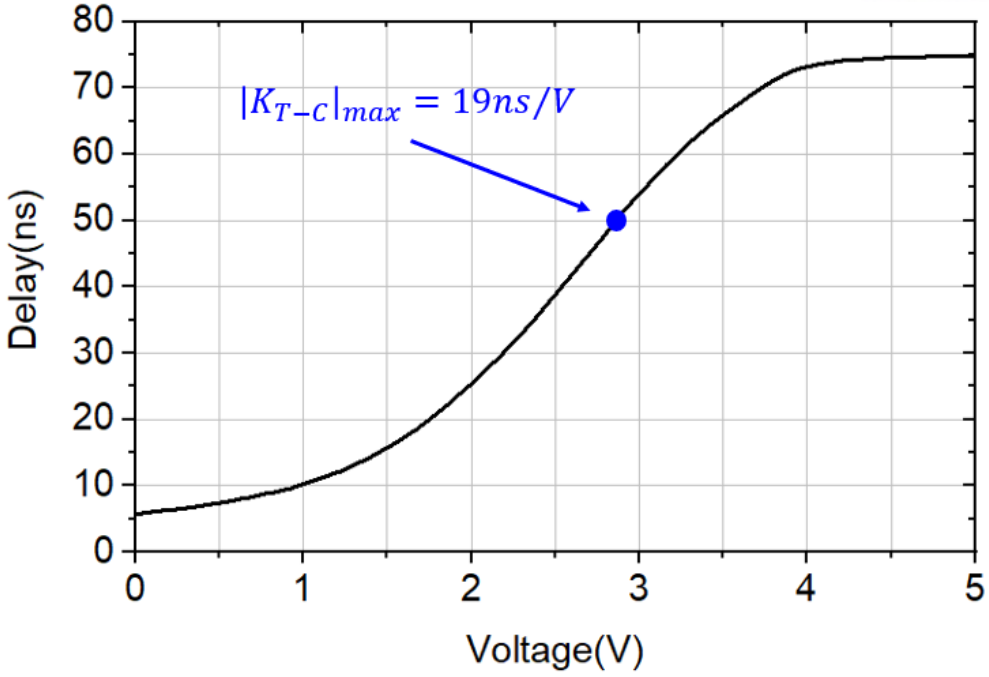


Fig. 25. Simulation results of the voltage-controlled delay line

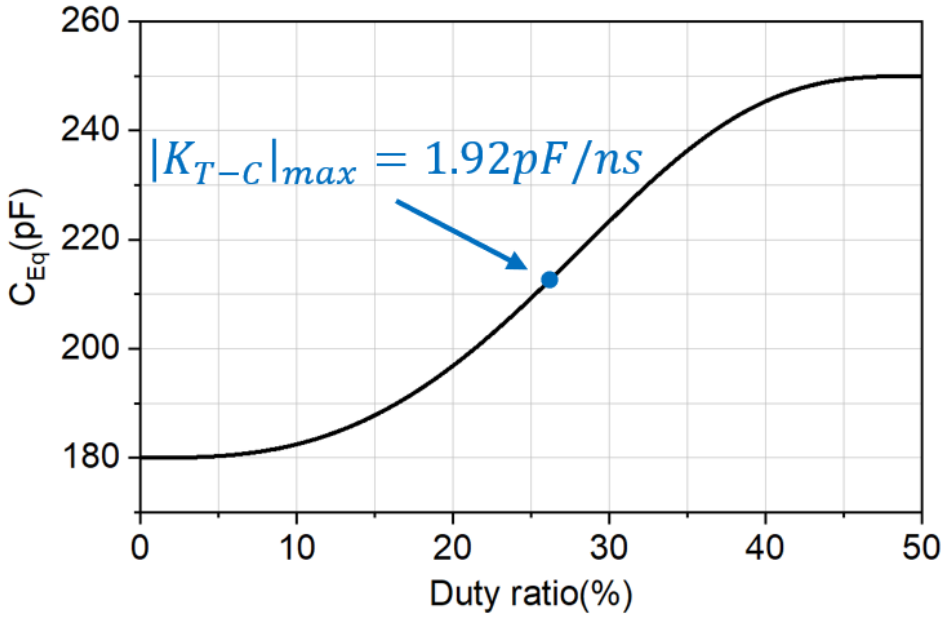


Fig. 26. Simulation results of equivalent capacitance

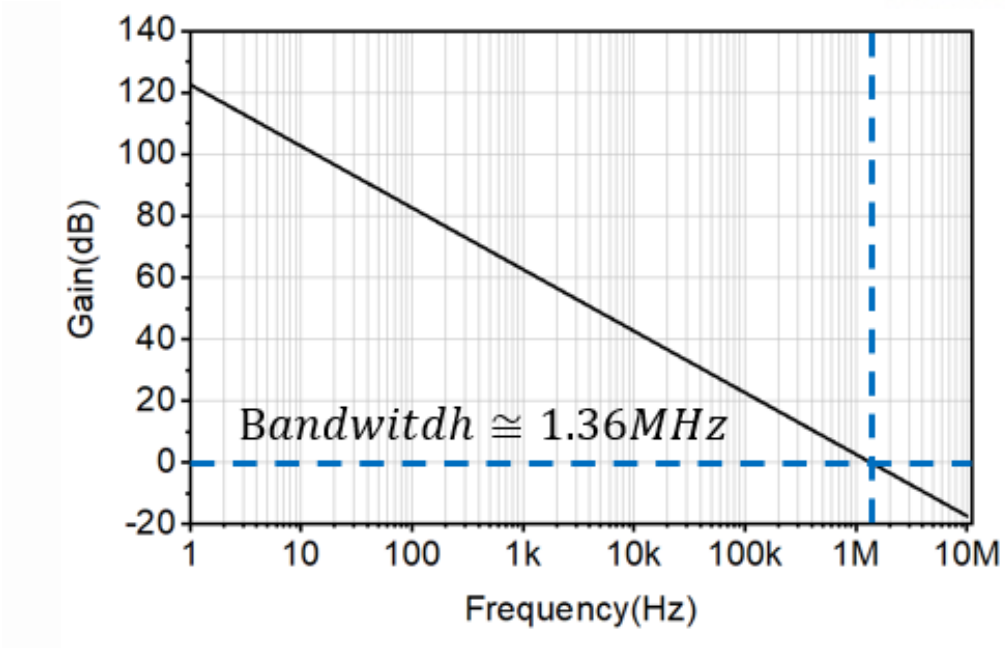


Fig. 27. Bode plot of ZVS feedback loop

Through the DC gain and boundary conditions (<1/5 GBW) of each transfer function of the A-ZVS feedback loop, we present the range of coupling and loading conditions in which the feedback can operate stably. Through equation (10) and $K_{C\text{-}V}$ with environment-dependency (according to K and R_L), the boundary condition of $K_{C\text{-}V}$ with loop gain maximum GBW of 1/5*6.78 MHz was expressed as the red line in the figure.28. Since the current, I_{IN}, of the primary power loop decreases as K and R_L increase, $K_{C\text{-}V}$ also decreases. In other words, in coupling or loading condition higher than the red line, the $K_{C\text{-}V}$ value is reduced, and the GBW of the feedback loop is set lower than the boundary condition. Therefore, the A-ZVS loop works more stable and robust in strongly coupled or light loading conditions than red line.

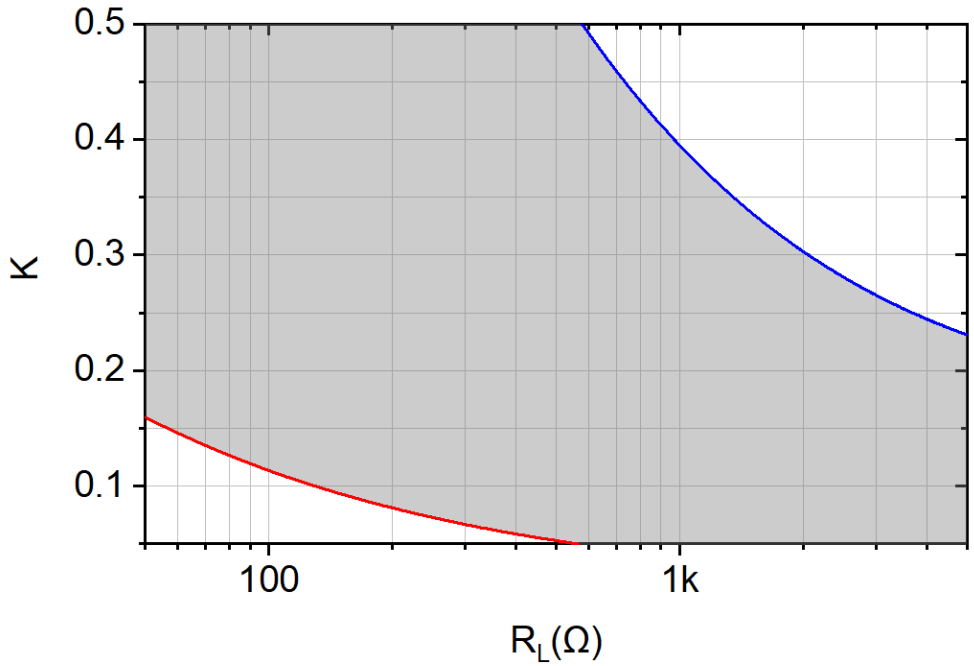


Fig. 28. Compensation region of the ZVS calibration loop

However, the amplitude, I_{IN} of the inductor current decreases as it is inversely proportional to reflected resistance, $Z_R=k^2wQ_2L_{TX}$ as the operating region moves to strong coupled or light loading condition. Therefore, a decrease in current means a decrease in ZVS compensation ability, and A-ZVS loop generates a PWM signal with a wider width for achieving ZVS. PWM signal increased the equivalent capacitor value and increased the ZVS compensation ability with phase shifted inductor current, I_{IN}, but increased input impedance as it moved away from the resonance point, and the amplitude of the current decreased. Accordingly, there is a maximum charge value that may be compensated in a specific condition K and R_L. The conditions for achieving ZVS are as shown in equation (11). At this time, the compensable charge is expressed as the blue line in the figure.28 by connecting conditions (K, R_L) in which the values of both sides are equal in equation (11). Therefore, in the region formed between the two lines, the A-ZVS loop operates stable and robust.

$$\int_{t_0}^{t_0+DT} I_O \sin\left(\omega t + \tan^{-1}\left(\frac{Im}{Re}\right)\right) * dt > Q_{ZVS} \quad (11)$$

However, since DDT control loop affects A-ZVS loop, stability including this effect should also be considered. In figure 28, the red line has the largest inductor current of all conditions that can be compensated with the lowest reflected impedance. This line is the points with the lowest dead-time due to the DDT control loop, and the point where the dead-time changes is formed in an area higher than the corresponding line. Therefore, from the perspective of frequency response, DDT control loop does not affect the robustness of A-ZVS loop.

Figure 29 shows the calibration of the ZVS feedback loop and the operation waveform of the DDT loop during the load transient. In the simulation, the load varies from 0.1KΩ to 1KΩ. As the load changes, the inductor current of PA changes, and as a result, the V_{CAL} and dead-time required for ZVS calibration change. In heavy to light load transient situations, increased I_L causes excessive ZVS compensation. For this reason, the voltage of the V_{HOLD} node drops to the diode turn-on voltage of the power N-MOSFET, and the body-diode turns on for a while, causing a decrease in efficiency. The A-ZVS feedback loop performs calibration while decreasing V_{CAL}. At the same time, DDT loop reduces dead-time in proportion to the increase in I_L, since the direction of the I_L can be changed and compensated in the reverse direction during too long T_{DT}, such as [10]. Conversely, in the light to heavy load transient, the voltage of the V_{HOLD} node increases due to insufficient ZVS compensation as I_L decreases. The A-ZVS feedback loop performs calibration while increasing the V_{CAL}. DDT loop increases dead-time, and the compensation ability insufficient due to the reduced I_{IN} is supplemented by the increase in T_{DT}, and according to the change, the wave form in which V_{HOLD} descends can be seen. In addition, when the equivalent capacitance increases for compensation for ZVS in conditions that low I_{IN}, the operating point moves to the inductive region, which is prevented, and the PA is locked to the near-resonance point. Therefore, proposed architecture enhances the robustness of A-ZVS through DDT loop and attenuate environment dependency.

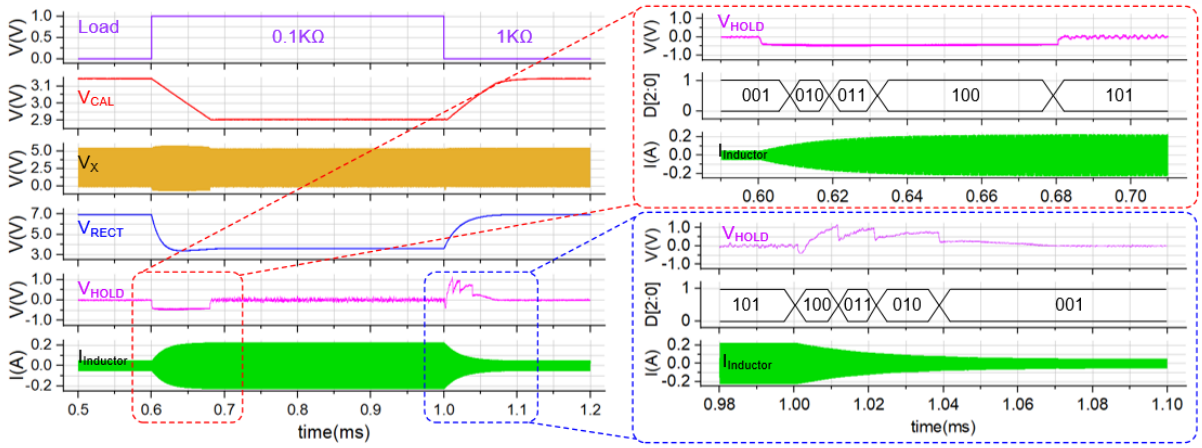


Fig. 29. Simulation behaviors of the ZVS feedback loop and DDT loop at during load transients.

Fig. 30 shows the simulated waveforms of the VX node under PVT variations. The simulation results show that the A-ZVS feedback loop performs calibration without any problems even with changes in process and temperature. Therefore, we prove the robustness of proposed techniques for PVT variation.

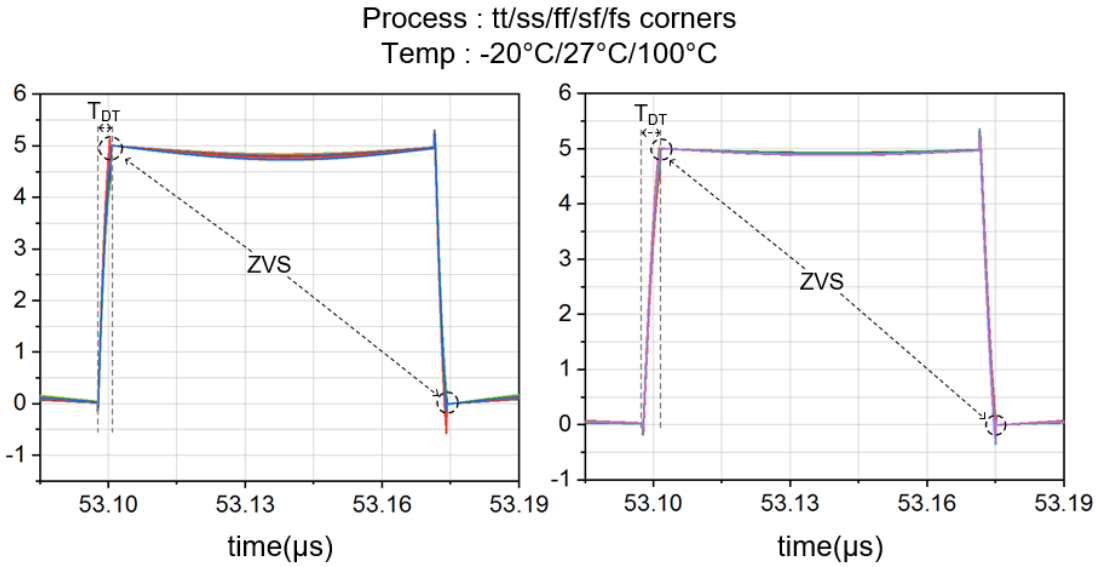


Fig. 30. Simulated waveforms of compensated V_X node under PVT variations:
(a) K = 0.2, R_L = 200 (b) K = 0.3, R_L = 500

Chapter 5

V.Measurements

The proposed fully integrated A-ZVS class-D PA with DDT loop is fabricated using the TSMC 0.18-um BCD process. Fig.31 shows a micrograph of the chip with dimensions of 1.71mm X 1.24mm, including the pads, and an active area of 0.9mmX0.65mm. Fig.32 shows the measurement setup, which consists of the PA chip in print circuit board, coil pair, rectifier with external components. On the TX coil side, a resonant capacitance, C_{TX}, is 180pF and a switched capacitance, C_{SW}, is 120pF. The value of C_{SW} was chosen to compensate TX inductance detuning. Fig. 33 shows the measured waveform of proposed PA with A-ZVS feedback loop and DDT loop. A-ZVS feedback operation is shown from startup to steady state under a coil distance (D) of 6mm and a load resistance (R_L) of 100Ω in RX. When A-ZVS loop is disabled, hard-switching and body diode connection occur due to resonant point deviation. After calibration begins, the pulse-width of the VPWM increases according to the voltage level of VCAL until ZVS is achieved. Fig.34 show the measured end-to end system efficiency η_{Total} and the transmitting power enhancement ΔP_{TX} by the A-ZVS technique with R_L = 100Ω under variations in distance between coils from 4 mm to 13 mm. The output power level with A-ZVS technique applied is also shown at each distance. A peak η_{Total} of 52.7 % and a peak ΔP_{TX} of 107 % were achieved at D = 7mm and D = 11mm, respectively.

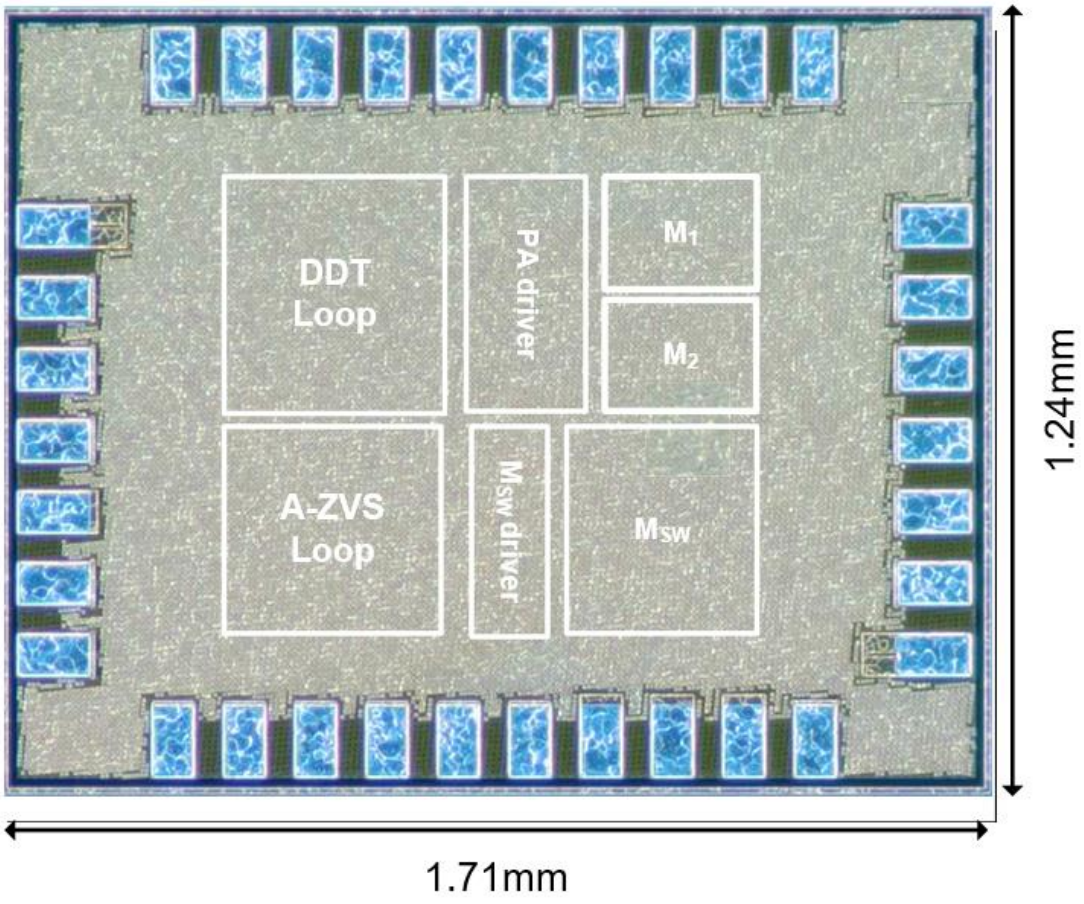


Fig. 31. Die micrograph of the transmitter chip

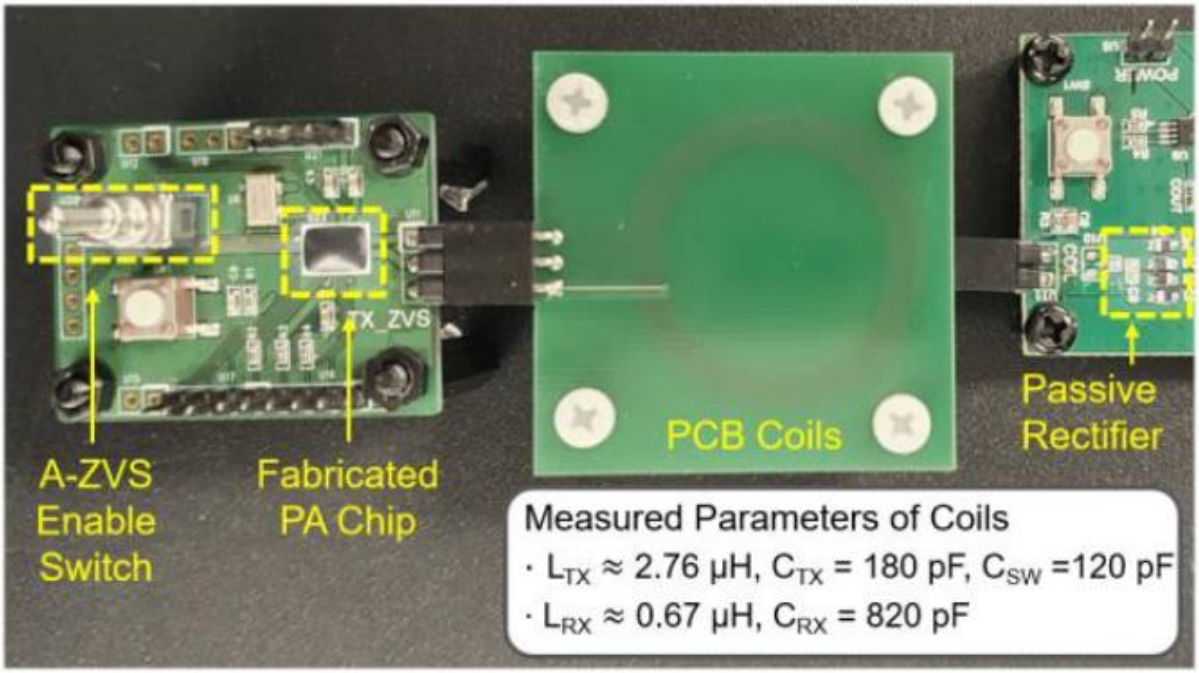


Fig. 32. Measurement setup

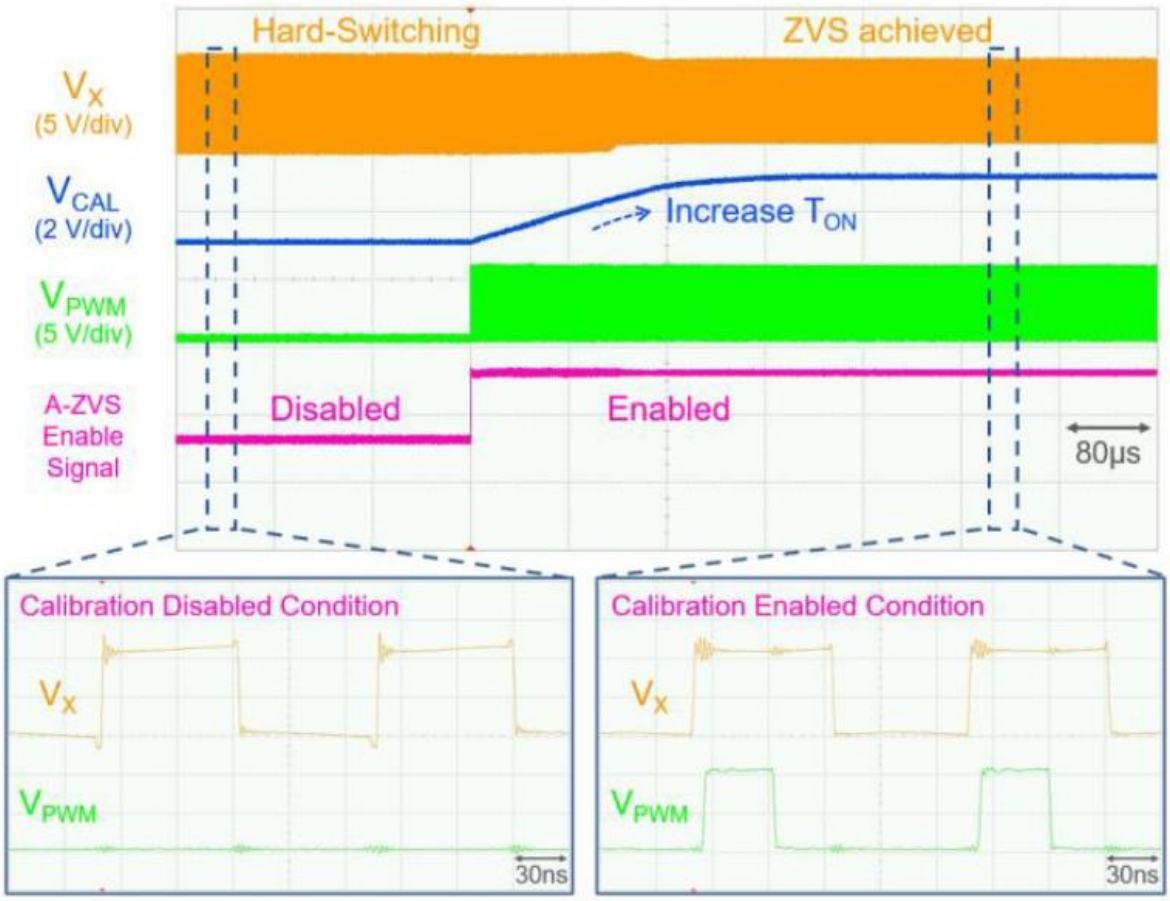


Fig. 33. Measurement waveforms of A-ZVS calibration

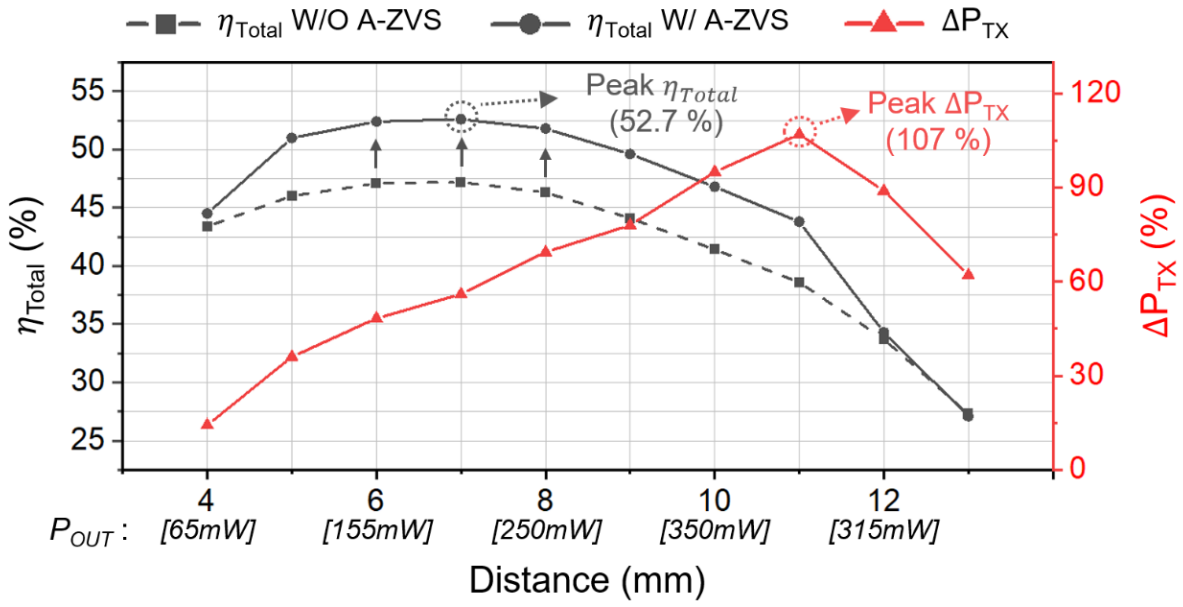


Fig. 34. Measured system efficiency and enhanced transmitting power

TABLE I
COMPARISON WITH STATE-OF-THE-ART POWER AMPLIFIERS

	JSSC [10]	TPEL [21]	TIE [5]	TCAS-I [6]	**This work**
Year	2019	2020	2020	2021	**2021**
Technology	BCD 0.35 μm	Off-chip	Off-chip	HV CMOS 0.35 μm	**BCD 0.18 μm**
Frequency (MHz)	0.075-2.6	0.1	13.56	6.78	**6.78**
ZVS Compensation	Fixed ZVS	Adaptive ZVS	Fixed ZVS	Fixed ZVS	**Adaptive ZVS**
Impedance compensation (Detuning compensation, Environmental change compensation)	Yes	Yes	No	No	**Yes**
Compensation element	Capacitor In RX	Switched capacitor	Auxiliary LC tank	Auxiliary LC tank	**Switched capacitor**
Compensation Site	TX & RX	TX	TX	TX	**TX**
Input range (V)	4.2	100	7.5–45	15	**4.2**
Off-chip controller	No	DSP	MCU	No	**No**
Dead-time control	Yes **(coupling & loading variation)**	No	No	No	**Yes (coupling & loading variation)**
PCE (%)	N/A	N/A	N/A	57.3%	**52.7%**

Chapter 6

VI. Conclusion

In this thesis, Adaptive-ZVS class-D PA with DDT loop is proposed to enhance the power conversion efficiency and transmittable power of 6.78MHz WPT system. Compared to previous work, A-ZVS loop can be achieved regardless of the variation of WPT environment by calibrating the loading impedance of PA. The on-chip calibration loop adjusts the duty ration of PWM signal to control the equivalent capacitance of the switched capacitor. The DDT control loop attenuate the WPT environmental dependence of the ZVS loop. To reduce design effort over multi-MHz operation, a delay line based PWM generator replaces the conventional comparator based PWM generator. The cost and volume of the PA can be considerably reduced by proposed technique. The simulation and measurement results verified robust ZVS operation under PVT variations and variable WPT environments.

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