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A NEW REDUCED SWITCH ZVS-PWM THREE-PHASE INVERTER

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A NEW REDUCED SWITCH ZVS-PWM THREE-PHASE INVERTER

(Thesis format: Monograph)

by

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Department of Electrical and Computer Engineering
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A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Engineering Science

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The University of Western Ontario
London, Ontario, Canada

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Abstract

Dc-ac inverters convert a dc input voltage into a desired ac output voltage and are widely used in many industrial applications, including utility grid interfaces, motor drives, and wind energy systems. Because of their widespread use, there has been considerable interest to try to make them more efficient to conserve energy. One way of doing so is to reduce the losses that are generated by the switching of the inverter devices as they help convert the dc input voltage into an ac output. As a result, there has been considerable research into implementing inverters with so-called soft-switching - zero-voltage and zero-current switching techniques that make either the voltage across a switch or the current through it zero at the time of a switching transition (from on to off or off to on). Since the power dissipated in a switch is related to the amount of overlap of voltage and current during a switching transition, making either the switch voltage or switch current zero at this time can result in a significant reduction in switching losses.

A new, reduced switch, zero-voltage switching (ZVS), three-phase dc-ac inverter is proposed in this thesis. The proposed inverter does not have the drawbacks that other previously proposed ZVS-PWM inverters have such as cost, increased conduction losses, the appearance of distortion in the output waveforms, and the lack of bidirectional operation capability. In the thesis, an extensive literature review of previously proposed soft-switched inverters is performed. The new inverter is then presented and its operation is explained in detail. The steady-state operation of the new inverter is analyzed and the

results of the analysis are used to determine the converter's steady-state characteristics. Based on these characteristics, a procedure for the design of the inverter is developed and then demonstrated with an example. Finally, the feasibility of the proposed converter and the validity of the analysis are confirmed with simulation results obtained from PSIM, a widely used, commercially available software simulation package for power electronics.

Acknowledgements

I would like to acknowledge my great debt to my advisors, Dr. Gerry Moschopoulos and Dr. Amirnaser Yazdani for providing me the invaluable opportunity to study in ECE, UWO, and for their guidance, encouragement and support during my studies. Their profound knowledge, creative thinking and consistent encouragement have been the source of inspiration through the course of this work.

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Last, but not the least, I would like to thank my wife, Sharmin Akhtar, for her continuous support during my study period at UWO. I am grateful for her love, patience and trust that acted as a driving force for the completion of the work.

Table of Contents

List of Figures

Nomenclature

AC	Alternative Current
DC	Direct Current
UPS	Uninterruptable Power Supply
EMI	Electromagnetic Interference
EV	Electric Vehicle
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
ZVT	Zero Voltage Transition
ZCT	Zero Current Transition

Chapter 1

Introduction

1.1. Research Background

In recent years, three-phase power inverters (dc-ac converters) have been widely used in many applications such as motor drives, active filters, uninterruptible power supplies (UPSs), and utility interfaces. A circuit diagram of a three-phase inverter is shown in Figure 1.1. To minimize low output harmonic distortion, acoustic noise, and size of the circuit components, high frequency switching operation is required for inverters. For this reason, inverters are normally designed with the highest achievable switching frequency in power supplies and utility applications. In motor drive applications, such as electric vehicle (EV) traction drives, higher switching frequencies can reduce the acoustic noises as well as torque and speed ripples.

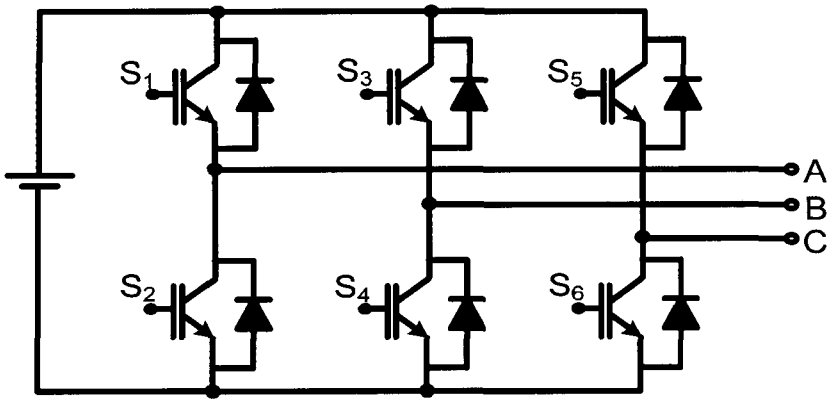


Figure 1.1. The schematic of a three-phase inverter

However, high-switching frequency operation of three-phase PWM inverters can cause some difficulties due to the high switching losses of the power devices that reduce inverter efficiency and affect power density. This phenomenon widely depends on the semiconductor device technology, which is reviewed below.

1.2. Power Semiconductor Devices

Power semiconductor devices perform the on-off action that is the basic operation of static power converters. In the evolution of power electronic inverters, the power devices that have been used have included the mercury arc rectifier, the thyristor, the bipolar junction transistor (BJT), the metal oxide field effect transistor (MOSFET), and the insulated gate bipolar transistor (IGBT) [1]-[5]. Inverters were first able to operate with higher switching frequencies with the introduction of the BJT. The BJT is a bipolar device that can operate with low conduction losses, but its switching speed is still low (although it is much higher than that of a thyristor), which prevents its use in applications requiring high switching frequencies.

The power MOSFET, which was first introduced commercially in the late 1970s, can operate with much higher frequencies than the BJT, and attractive for many applications such as computer power supplies and automotive electronics. The current rating and the conduction losses of a power MOSFET are determined by the drain-source resistance ($R_{ds,\ on}$) of the device. The resistance can be reduced by making the channel length small, especially in the case of devices with blocking voltages below 100 volts. Its on-resistance, however, increases significantly with an increase in the blocking voltage, and thus it has

not been possible economically manufacture high voltage power MOSFETs with high current ratings.

The IGBT (insulated gate bipolar transistor) device was first introduced in late 1980s to combine the advantages both from MOSFET and BJT. These devices have the low-conduction-loss feature of the BJT [6], but can operate at higher switching frequencies as they have the gate features of MOSFETs. As a result, IGBT devices have become the most popular choice for industrial drive applications [7]-[10], which range from few KW up to several MW and usually require a voltage rating higher than 500 volts.

1.3. Hard-Switching Inverters

The traditional three-phase inverter operates in hard-switching mode, which means the power devices (IGBT or MOSFET) are driven "hard" directly by the gate driver during the switching transient. As a result, a power device turning on has the whole bus voltage (typically in the range of 350-600 V) across it as it changes state. During a switching interval (less than 0.5 microseconds), there is a finite time when the power device begins to conduct as the voltage across the device begins to fall at the same time as current begins to flow through it. The simultaneous presence of voltage across the transistor and current through it (overlap between voltage and current) means that power is being dissipated within the device during the switching transition time.

A similar event phenomenon occurs when a transistor turns off with the full current flowing through it. As the switching frequency is increased, the faster rise and fall times generate more high frequency energy that is radiated and conducted out of the unit as

unacceptable electromagnetic interference (EMI) and radio frequency interference (RFI), which further decrease the system efficiency. If the rise and fall times are intentionally slowed to reduce the electromagnetic interference (EMI) and radio frequency interference (RFI), the power losses in the transistor increase proportionally, increasing the thermal stress put on the device, thus reducing its lifespan. In this way, older hard switching topologies are a compromise between electrical efficiency reduction and EMI "noise" trade-offs.

1.4. Losses in Power Semiconductor Devices

Generally, semiconductor losses can be grouped into the following three categories [11]:

I. Switching losses
   a) Turn-on losses
   b) Turn-off losses

II. Conduction losses
   a) On-state losses
   b) Dynamic saturation losses

III. Off-state Losses

Off-state losses are generally a very small portion of the total losses and are considered negligible. The relative magnitudes of the switching and conduction losses, however, are greatly dependent on the type of load, the turn-on and turn-off snubbers (switch protection) used, and the characteristics of the transistor itself. Once a topology and the appropriate switching devices are selected, there is little that can be done to reduce

conduction losses. Switching losses, however, can be reduced if the overlap between voltage and current during switching transitions is reduced. Most efforts to improve the efficiency of inverters have focused, therefore, on doing just that.

1.5. Soft-Switching Inverters

The overlap between voltage and current prior to switching transitions has to be reduced to achieve an efficiency improvement and lower EMI noise. The purpose of soft-switching techniques is to decrease or eliminate the simultaneous presence of voltage and current through the power device. The soft-switching operation of the three-phase inverter is typically done by some form of resonant technique that uses some auxiliary circuit consisting of resonant components and auxiliary switch(es) to trigger the resonance. There are some basic expectations for a three-phase soft-switching inverter, including the following:

a) The overall system efficiency should be increased.
b) All the main switches including the auxiliary switches and all the diodes should be soft-switched to reduce overall switching losses.
c) The auxiliary circuit should be simple and cost effective.

In recent years, various soft-switching techniques have been developed. The categories of soft-switching inverter techniques are shown in Figure 1.2. There are two major methods in the Passive Approach category - lossy snubbers and lossless snubbers [12]-[21]. Lossy snubbers use a resistor-capacitor-diode (RCD) combination as shown in Figure 1.3(a) to improve the turn-off performance of a switch, and a resistor-inductance-diode (RLD)

combination as shown in Figure 1.3(b) to improve the turn-off performance of a switch. A combination of both snubbers can be used to improve the switching performance for both types of switching transitions.

At turn-off, the switching device current is diverted to the snubber capacitor, thus slowing down the rate of increase of the voltage. This, in turn, reduces the overlap between the rising voltage and the falling current. At turn-on, the snubber inductor slows down the increase of the current, thus reducing the overlap between the falling voltage and the rising current. The RCD snubber dissipates the energy stored in the snubber capacitor in the snubber resistor when the switch turns on, while the RLD dissipates the energy stored in the snubber inductor when the switch turns off.

In lossless snubbers the snubbered energy circulates in the snubber circuit and no energy is dissipated in a resistor. Figure 1.4 shows an example of a passive lossless snubber for inverters. Although passive snubbers help reduce switching losses, they are not effective in reducing switching losses in converters operating with switching frequencies in the range of tens of kHz, and active snubber approaches are typically used in these cases.

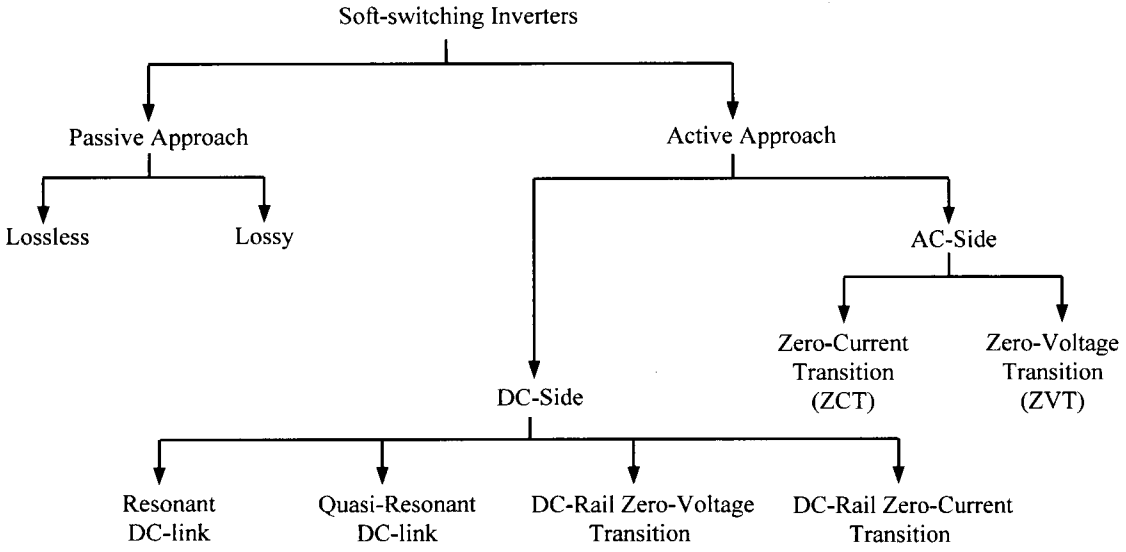
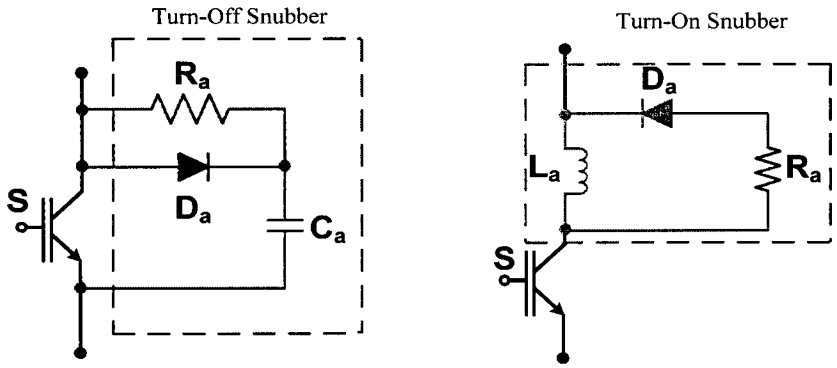


Figure 1.2. Classification of soft-switching inverter techniques



(a) Turn-Off Snubber (b) Turn-On Snubber

Figure 1.3. Passive RCD and RDL snubbers

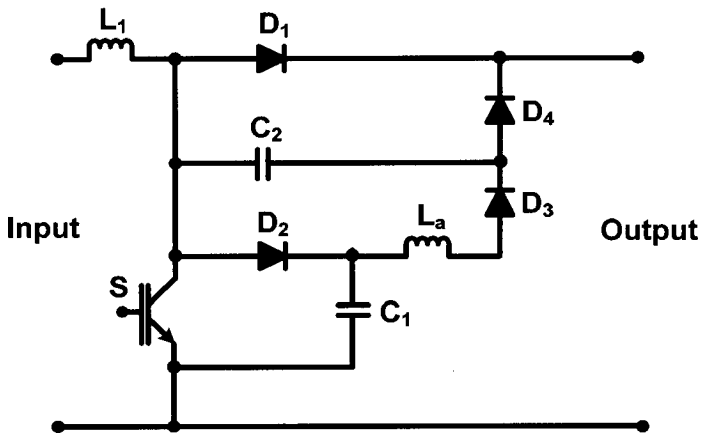


Figure 1.4. Passive lossless snubber

1.6. Review of Three-Phase Active Soft-Switching Inverters

Active snubbers (or active auxiliary circuits) are snubbers that contain an active switching device in their circuit. Various types of active snubbers are reviewed in the section.

1.6.1 DC-Side Soft-Switching Inverters

The fundamental philosophy of the DC-side soft-switching inverter is to use auxiliary circuitry to create a zero-voltage duration of the DC bus at desired switching instants [22]-[24]. This allows the appropriate devices in the three-phase legs to be switched under zero-voltage conditions. A typical configuration of DC-side soft-switching inverters is shown in Figure 1.5. DC-side soft-switching topologies can be classified into the following groups: resonant DC-link inverters [22], [23], [25]-[37], quasi-resonant DC-

link inverters [38]-[42], DC-rail ZVT inverters [43]-[45] and DC-rail zero-current-switching inverters [46].

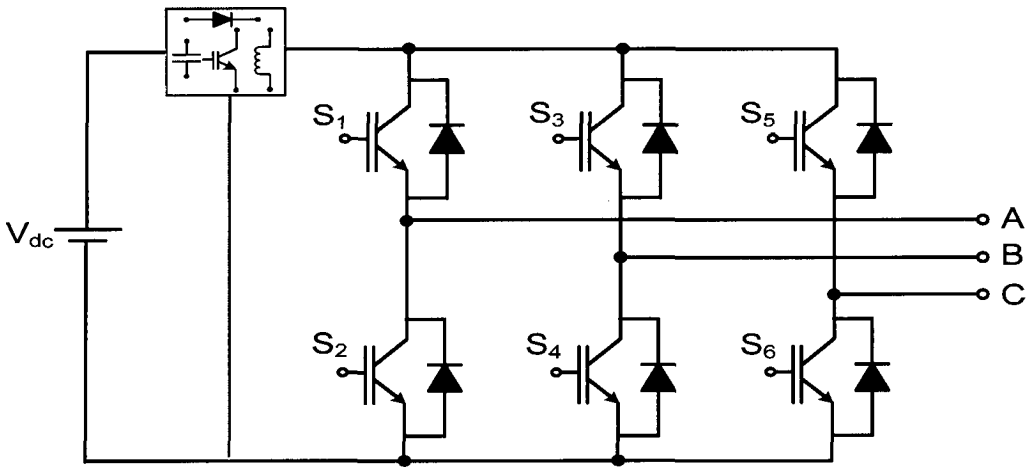


Figure 1.5. Typical configuration of DC-side soft-switching inverter

1.6.1.1. Resonant DC-link (RDCL) Inverters

A six-switch resonant DC-link voltage source inverter (RDCL) topology, for realizing zero-voltage-switching (ZVS) has been proposed by Divan [22]. In this inverter, shown in Figure 1.6, the DC-bus is made to oscillate at a high frequency so that the bus voltage goes through periodic zero crossings. This allows the inverter switching devices to turn on with zero-voltage-switching (ZVS). This topology has several advantages, including the following [47]:

- Elimination of switching losses and snubbers
- Minimum number of power devices

- High switching frequency is achievable
- Excellent transient response
- Low acoustic noise
- Multi-quadrant operation
- Maximization of power density
- Simple power structure

However, this topology imposes considerable peak voltage stress (> 2.5 times the DC-bus voltage V_{dc}) across the devices.

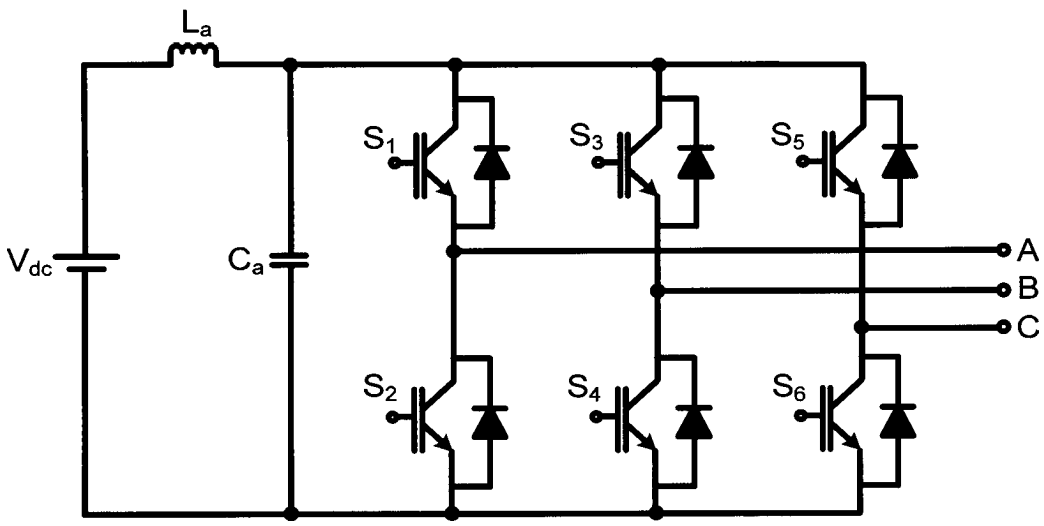


Figure 1.6. The six-switch resonant DC-link inverter [22]

An alternate topology for realizing zero-voltage-switching in high power converters is the actively clamped DC-link (ACRDL) inverter [23], [33]-[35] shown in Figure 1.7. In this topology, the presence of a clamp switch (S_a) restricts the voltage stresses to nearly 1.3-

1.4 times DC-bus voltage (V_{dc}), but, like the resonant DC-link inverter shown in Figure 1.6, RDCL inverters have to use discrete pulse modulation (DPM) instead of using PWM control, which normally causes undesirable sub-harmonic oscillations [25].

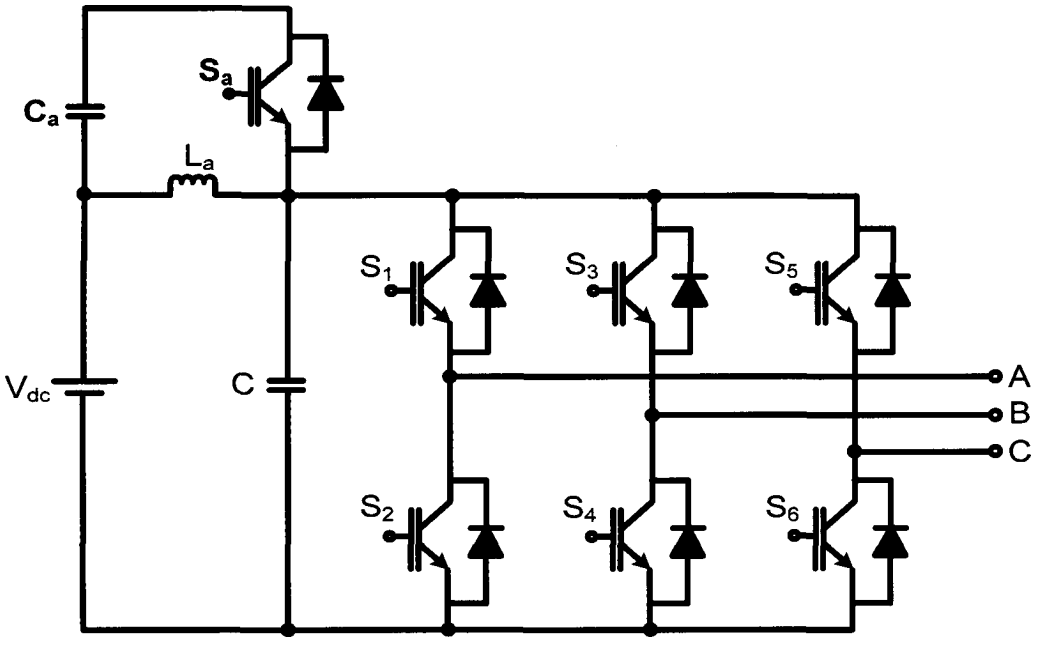


Figure 1.7. Actively clamped resonant DC-link inverter [23]

An improved topology has been made to eliminate the problems associated with discrete pulse modulation (DPM) strategies and resonant DC-link inverter topologies. This is the synchronized resonant DC-link (SRDCL) that has been proposed in [36], [37] and is shown in Figure 1.8. The control strategy that is used for this topology is a hybrid of PWM and DPM. Although this topology offers improved performance for single-phase applications over RDCL type converters [36], it has difficulties eliminating the sub-harmonics of its output voltages when used in three-phase applications unless the

equivalent switching frequency is reduced considerably [37]. Some PWM have been implemented in RDCL inverters [26], but the range of allowable PWM is very limited, and the converter has difficulty maintaining the appropriate DC bus resonance required for ZVS operation when operating under heavy load conditions [48].

Many improved topologies have been proposed to overcome the drawbacks of RDCL inverters, either using one auxiliary switch [27]-[29] or two auxiliary switches [30]-[31]. These improved topologies still suffer from the switch overvoltage problem. The topology proposed in [28] is complicated and bulky. In the DC-voltage-notch inverter proposed in [29] and [47], the auxiliary switch has a hard turn-on and off that somewhat offsets the expected savings in the losses in the main switches. Another improved topology is proposed in [30], but it needs an initializing circuit to control the initial inductor current, which makes the topology complex. The topology proposed in [31] has the weakness that the auxiliary switch has a hard turn-off (with high current), which results in high losses in the auxiliary circuit.

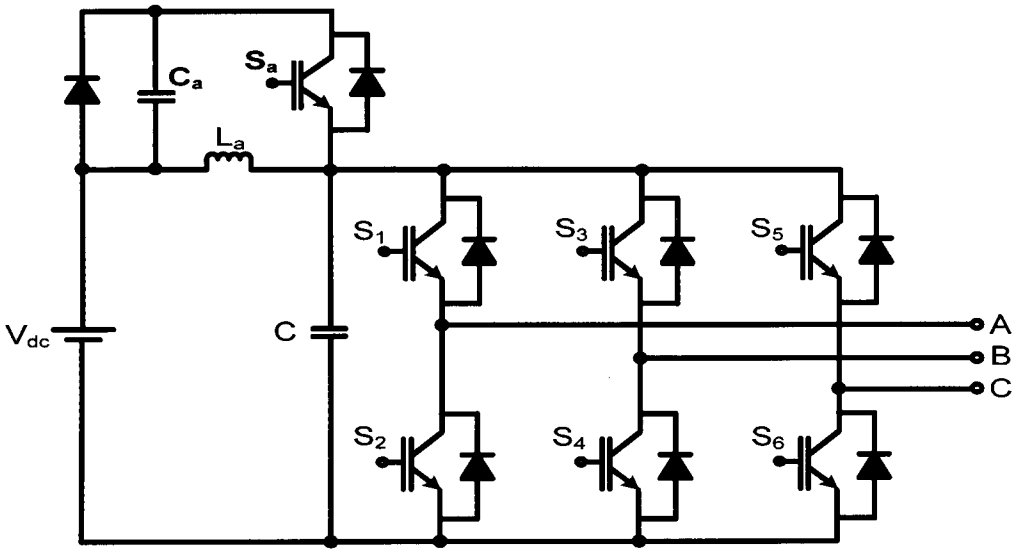


Figure 1.8. Synchronized resonant DC-link inverter [36]

1.6.1.2. Quasi-Resonant DC-link (QRDCL) Inverters

Aiming to correct the drawbacks of RDCL inverters, many quasi-resonant DC-link (QRDCL) inverter topologies (also known as parallel resonant DC-link (PRDCL) inverters) have been proposed [38]. Their main objective is to avoid the high peak voltage stress of the inverter switches and to allow the inverter to operate with PWM control. Unlike RDCL inverters, the main auxiliary switch (DC-rail switch) in QRDCL inverters is placed in series with the DC-link, and a controlled resonant branch is placed in parallel with the main bridge circuit. A typical configuration of a QRDCL inverter is shown in Figure 1.9.

Under normal operating conditions, the DC-rail switch passes the input power directly to the main bridge. During switching transitions, the DC-rail switch separates the main bridge from the input power, and the resonant branch helps to achieve soft-switching conditions in a resonant manner. However, the main drawback of this topology is the fact that the DC-rail switch must be placed in series with the DC-bus, so it has to conduct the full load current of the inverter; this increases conduction losses. Also, the DC-rail switch must be turned off under hard-switching conditions with high current, which also increase switching losses. Other drawbacks include the fact that the PWM scheme needs to synchronize the switching actions of the main switches (ultimately resulting in increased ripple in the output).

The auxiliary circuits in QRDCL inverters are complicated compare to those in RDCL inverters. The PRDCL inverter topology proposed in [38] has four auxiliary switches that are turned off with high current. The QRDCL inverter proposed in [41], uses two auxiliary switches, but the method used to control these switches and synchronize their operation is very difficult and complex. The QRDCL inverter topology proposed in [49] has a good soft-switching scheme, but it is difficult to get soft-switching operation for wide operation range.

The parallel resonant DC link (PRDCL) inverters proposed in [50]-[52] have lower output voltages than traditionally hard switching inverters using the same control strategies, and the switches or resonant components in the DC link cause high losses [50]. In [53], a novel resonant pole three-phase inverter that permits the zero-voltage switching of the main switches and the zero-current switching of auxiliary switches is proposed. It has a

small power auxiliary circuit, low switching power losses, and low peak voltage stresses due to resonant voltage and is the best PRDCL type inverter.

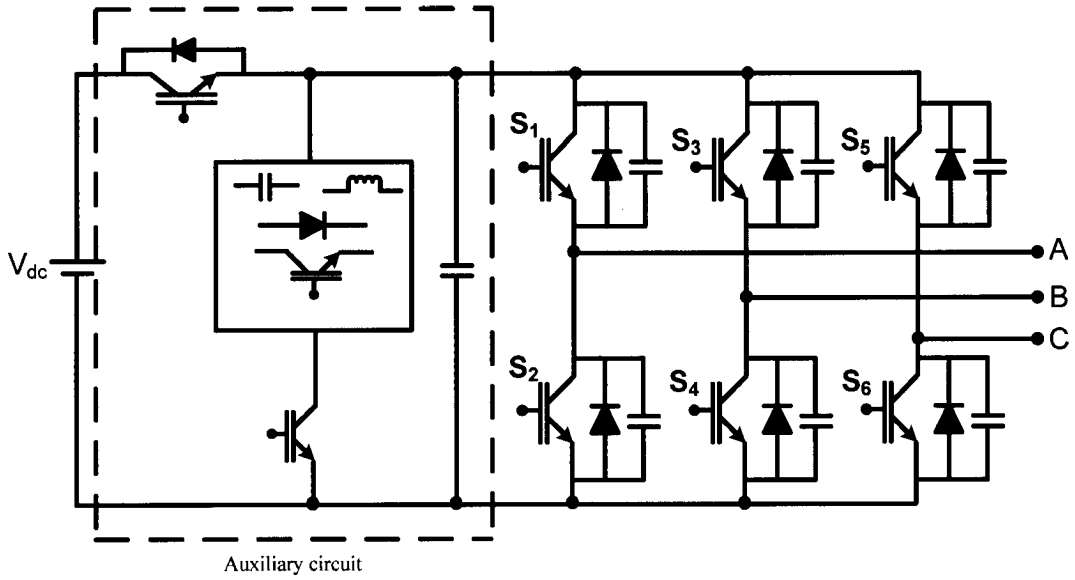


Figure 1.9. Typical configuration of quasi-resonant DC-link inverter

1.6.1.3. DC-Rail ZVT Inverters

Three-phase DC-rail zero-voltage-transition (ZVT) inverters were first introduced in [43], and an example inverter is shown in Figure 1.10. Like QRDCL inverters, DC-rail ZVT inverters have an auxiliary switch (DC-rail switch) that is placed in series with the main DC-bus, which causes high conduction losses. The DC-rail switch is turned off at high current, which also causes high switching losses. Moreover, the implementation of the auxiliary switch is complicated. A modification of this DC-rail ZVT inverter topology in which the DC-rail switch is changed into diode so that the converter becomes a boost

rectifier is proposed in [44]. Because of this diode, bidirectional power flow is impossible and thus boost topology cannot be used for inverters. Recently, a DC-rail parallel resonant ZVT inverter topology has been proposed for three phase AC motor drives in [45], but its auxiliary circuit consists of three switches, which makes the topology too expensive for practical implementation.

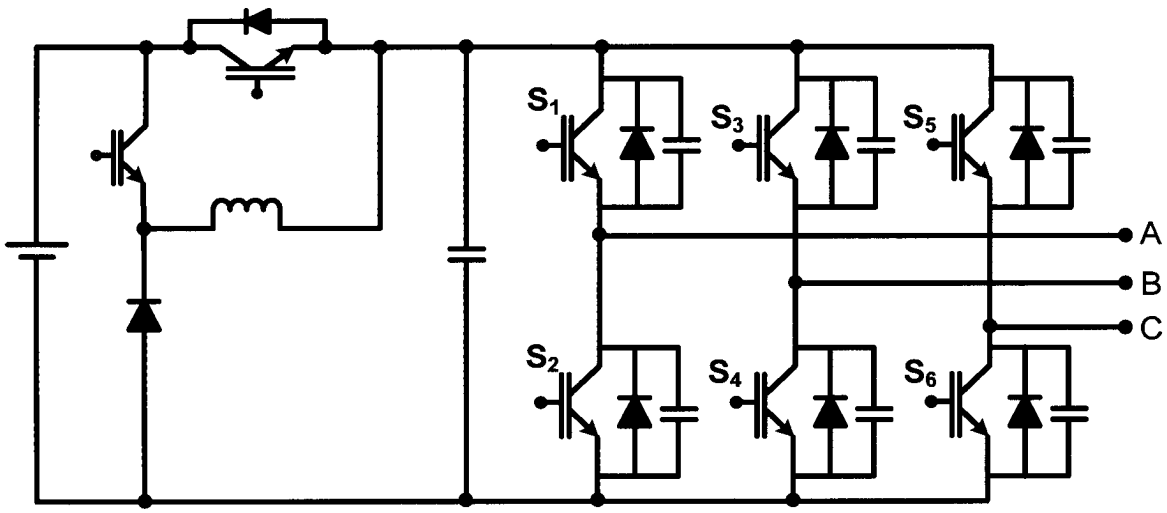


Figure 1.10. DC-rail ZVT inverter [43]

1.6.1.4. DC-Rail Zero-Current-Switching Inverters

The DC-rail zero-current-switching inverter proposed in [46] and shown in Figure 1.11 uses two auxiliary switches to reduce the main switch turn-off losses. The auxiliary switches help make the current through a main inverter switch to zero during a turn-off switching transition. Conduction losses, however, increase as the auxiliary switches are

placed in series with the main DC-bus. Moreover, this topology requires the synchronous turn-off of the main switches, which creates additional switching events, and increases the ripple of the output current.

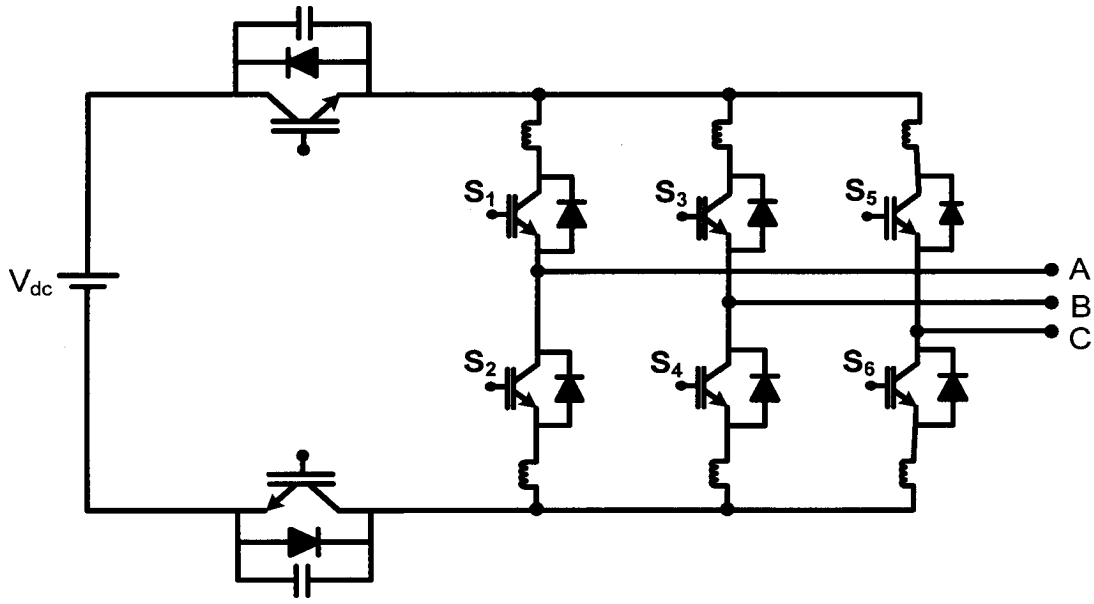


Figure 1.11. DC-rail zero-current switching inverter [46]

1.6.2 AC-Side Soft-Switching Inverters

AC-side resonant inverters do not have the drawbacks of DC-link resonant inverters. Many AC-side soft-switching inverters have been proposed, and they are either ZVT or ZCT (zero-current-transition) topologies. Both types of AC-side soft-switching inverters put the auxiliary circuit in shunt with the main power-processing bridge circuit so that the auxiliary circuit does not need to carry the full load current. This is one major advantage of AC-side inverters over DC-side inverters, which often put the auxiliary circuitry in

series with the main power flow path. A typical configuration of an AC-side soft-switching inverter is shown in Figure 1.12.

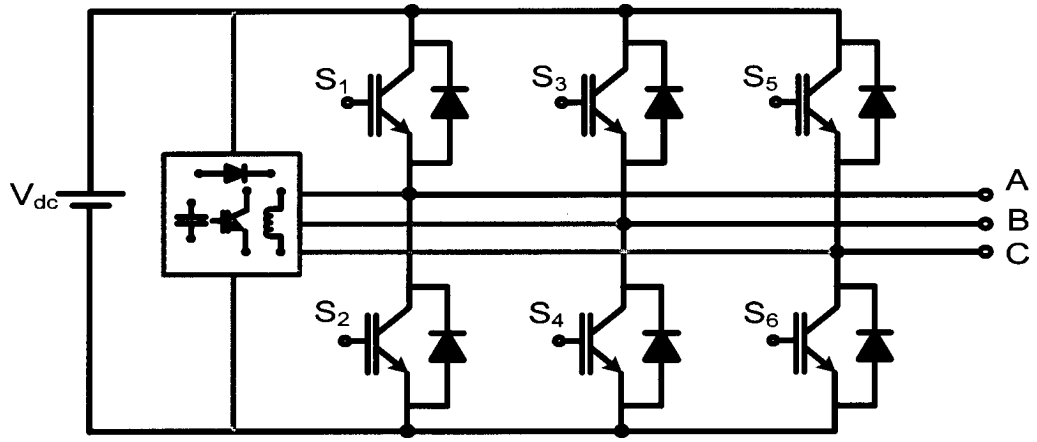


Figure 1.12. Typical configuration of AC-side soft-switching inverter

1.6.2.1 AC-Side ZVT Inverters

The auxiliary resonant commuted pole (ARCP) inverter was the first topology of this kind to be proposed [54], [55]. A circuit diagram of the ARCP inverter is shown in Figure 1.13. In this topology, each auxiliary circuit is composed of a resonant inductor and two switches that form a bidirectional switch configuration. The ARCP inverter can operate with zero-voltage turn-ons for the main switches and zero-current turn-offs for the auxiliary switches. The auxiliary turn-off loss is partially reduced with the help of snubber capacitors that are usually paralleled with each main switch. The ARCP inverter, however, has many drawbacks, including the following [56]:

- The need to determine exactly when to turn on an auxiliary switch necessitates additional sensing and precise switch timing, which reduces the overall system reliability [60]-[61]. Zero-voltage switching will be lost and extra loss will be incurred if these measures are not taken [62].
- Measures taken to protect the auxiliary devices against overvoltage due to the reverse recovery energy stored in the resonant inductance result in extra loss and circuit complexity [63], [64].
- The potential variation of the DC-link capacitor center tap further reduces system reliability - this is especially true when a half-bridge inverter is feeding a heavy low-frequency load [65]. For a single or three-phase system where the net current flowing into the center tap during a switching cycle may add up to zero in theory [55], the stabilization of the center-tap potential may be lost when asymmetrical operation conditions arise between the plus and minus semi-cycle of the ac load current in each phase.

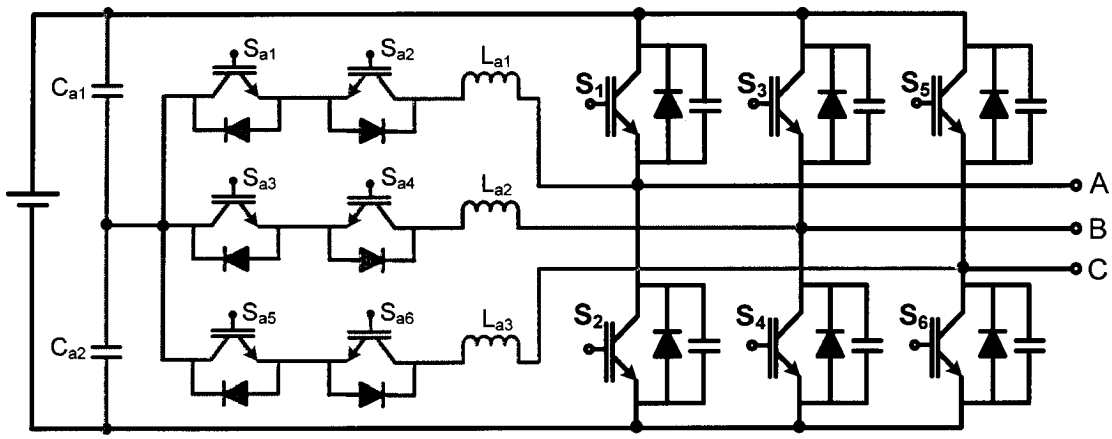


Figure 1.13. The ARCP inverter [54], [55]

The topology proposed in [57]-[59], can realize zero-voltage turn-ons for the main switches and zero-current turn-offs for the auxiliary switches without using any split DC capacitor bank in the DC-bus, but a main switch will be exposed to high peak voltage when it is turned off when the inverter operates with non-peak load current levels [56].

The topology proposed in [56], shown in Figure 1.14, uses coupled inductors to correct the drawbacks found in ARCP inverters, but these inductors are bulky and difficult to design, and ways must be found to properly reset them, which makes the converter more complex. An approach proposed in [64] uses only three auxiliary switches - only one auxiliary switch per phase leg as shown in Figure 1.15 - and allows the auxiliary switches to conduct resonant current in both directions (unlike the ARCP inverter in Figure 1.13). The turn-off of an auxiliary switch, however, must be precisely timed relative to the operation of the rest of the converter or else inverter switch may lose the ability to turn on with ZVS. This results in the need for additional current detection circuitry (even though the rest of the inverter is sensorless), which makes this topology impractical of many industrial applications. A similar drawback exists for the topology proposed in [66], which also uses three auxiliary switches to help the main inverter switches operate with ZVS. The topology proposed in [67], which is shown in Figure 1.16, has an auxiliary circuit that uses only one auxiliary switch in the entire converter, but the auxiliary circuit has high conduction losses that partially offsets the benefits of the simplified circuit.

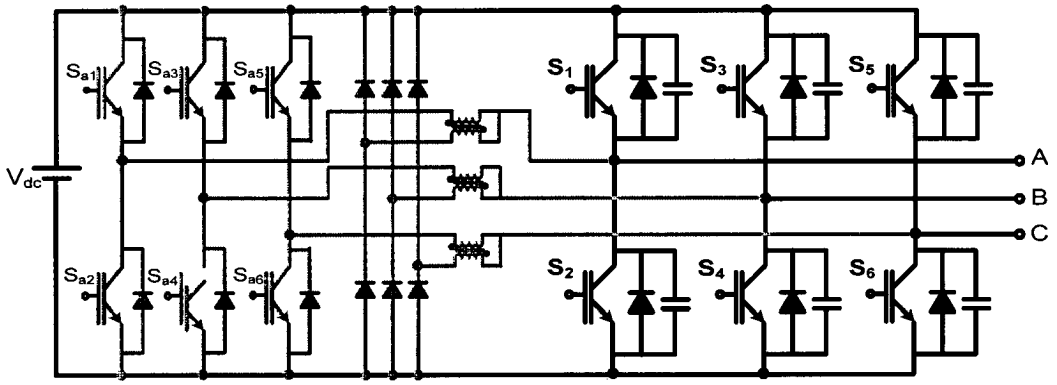


Figure 1.14. The ZVT inverter with coupled inductor feedback [56]

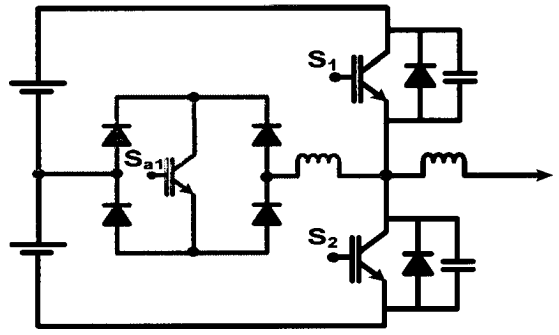


Figure 1.15. The ARCP inverter using one auxiliary switch per phase leg [64]

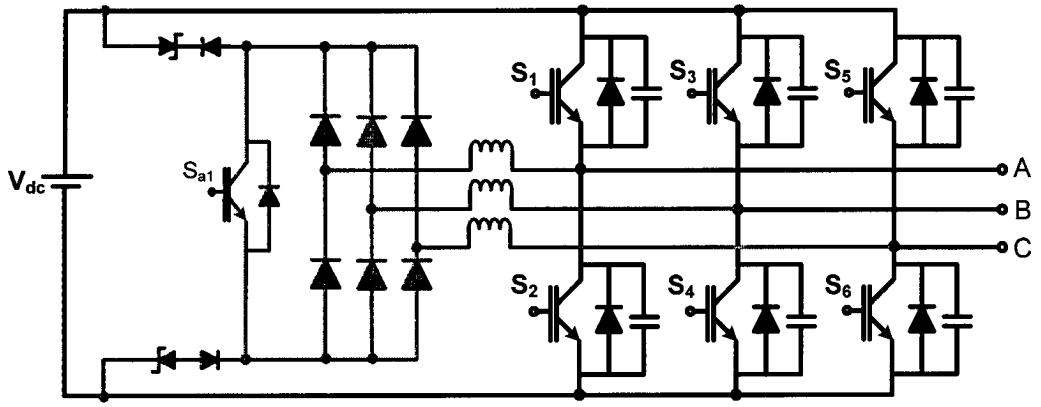


Figure 1.16. The ZVT inverter using one auxiliary switch [67]

Previously proposed ac-side ZVT inverters all have at least one drawback that limits their effectiveness. An ac-side ZVT inverter with two auxiliary switches (Figure 1.17) is proposed in [68], but the auxiliary switches cannot be turned off softly. Another topology proposed in [69] needs large and bulky inductors to operate properly, which are very difficult to design. Another topology proposed in [70] is also complicated and difficult to design. The topology proposed in [71], uses only one auxiliary switch for the soft-switching of all the switches, but cannot work in bidirectional way as an inverter/rectifier, as is the case for many ZVS inverters, which limits the applications where it can be used.

An inverter that allows its main power switches to operate with *zero-voltage-zero-current* switching (ZVZCS) for turn-on and turn-off transitions is proposed in [72], but it uses a third auxiliary switch in series with the main DC-bus, which increases conduction losses. The ZVZCS inverter proposed in [73] does not have this problem, but its implementation is complex and expensive. The same is true for the inverter proposed in [74], which avoids the use of a split-capacitor DC bus. The ZVZCS topology proposed in [75] is simpler, but requires the use of a sophisticated space-vector PWM control technique and cannot be operated bidirectionally.

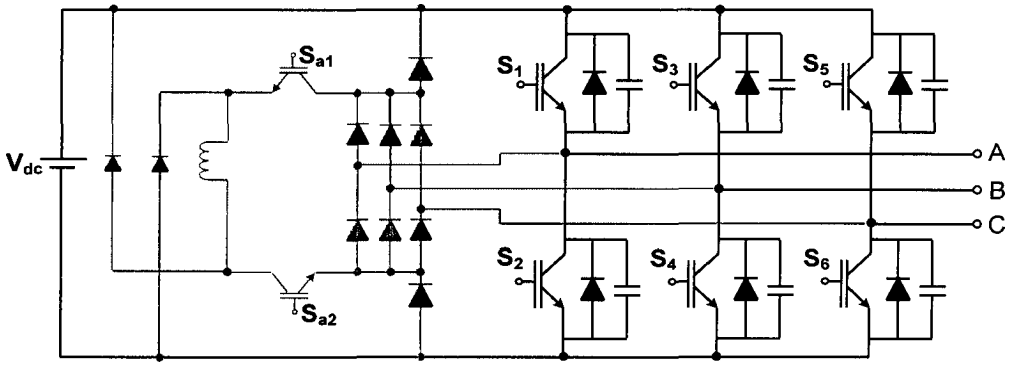


Figure 1.17. The ZVT inverter using two auxiliary switches [68]

1.6.2.2 AC-Side ZCT Inverters

Generally, zero-current-transition (ZCT) inverters have auxiliary circuits with L-C resonant tanks [76]-[79], as shown in Figure 1.18. By controlling the timing of the auxiliary switches, ZCT converters can realize zero-current turn-off and near zero-current turn-on. The ZCT inverter proposed in [76] allows the main inverter switches to turn off softly, but the auxiliary switches are not turned off softly. The improved ZCT inverter proposed in [78] achieves a soft turn-off for the main diodes and a zero-current turn-off for the auxiliary switches, but main switches turn-on exposed to at least the full DC-link voltage (which can result in significant turn-on losses), and some topologies require at least six auxiliary switches, which is not cost effective. The topology proposed in [80] tries to correct these drawbacks, but its main switches still have considerable turn-on losses, and these losses are more significant in the topology proposed in [81]. The topology proposed in [82] also has issues with losses related to the inverter switches.

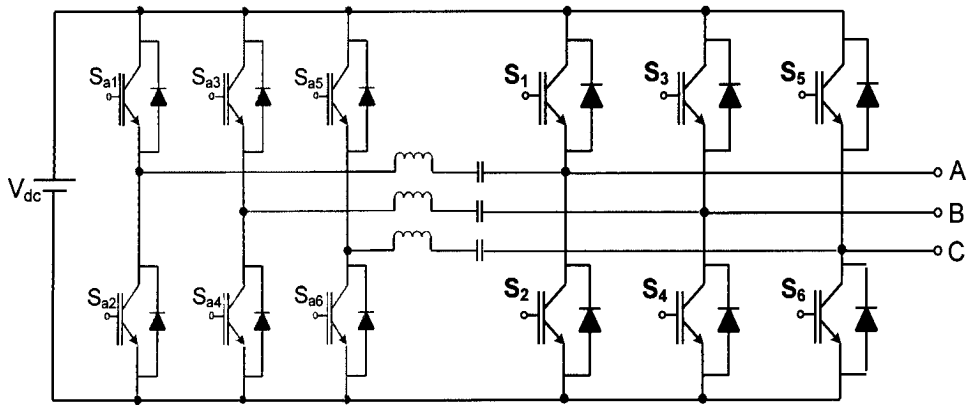


Figure 1.18. The six-switch ZCT inverter

1.7 Choice of ZVT or ZCT

Zero-voltage-switching topologies can eliminate turn-on losses by forcing the voltage across a main power switch to zero before turning on. They can also reduce turn-off losses with the assistance of snubber capacitors, but large snubber capacitances are needed to reduce the turn-off losses to a satisfactory level. Moreover, if for any reason a zero-voltage turn-on is not achieved, the energy stored in the snubber capacitors is dumped directly into the switch, causing excessive turn-on loss. Zero-current-switching topologies can force the current flowing through an inverter switching device to zero prior to its turn-off, and can thus significantly reduce turn-off losses, but are not as effective as ZVS topologies in reducing turn-on losses.

The choice between ZCT and ZVT depends on the semiconductor device technology that is used. In case of minority carrier devices like the IGBT, the best choice would be ZCS. An IGBT has lower capacitive turn-on losses than a MOSFET. An IGBT has a fixed voltage drop across its collector and emitter that is nearly independent of the current it conducts. The nearly fixed voltage drop of the IGBT along with its higher voltage rating and power density (as discussed in Section 1.2.) makes it the device of choice in high power applications where switches must conduct greater currents and conduction losses must be reduced. The main disadvantage of an IGBT is that it is a minority carrier device and thus charge cannot be quickly removed from it when it is about to be turned off. It, therefore, turns off very slowly and with a considerable "current tail" that creates switching losses. These losses can be reduced if ZCS techniques are used to make the

current flowing through an IGBT zero, before it is turned off. Doing so eliminates the current-tail that creates the turn-off losses.

A MOSFET acts as an equivalent drain-source resistance ($R_{ds,on}$) when it conducts current. In high power applications, where the power devices conduct greater current, the choice of MOSFET as a power switch will result in increased conduction losses. However, in low power applications (lower current ratings), a MOSFET is generally a better choice than an IGBT if the converter needs to operate with high switching frequencies. In this case, ZVS techniques are used to improve efficiency.

1.8 Objectives of Research

The main objectives of this work may be summarized as follows:

- To propose a new three-phase inverter for low power applications (< 5 kW) that has the following features:
  - It should require fewer devices than previously proposed inverters. As can be seen from the diagrams of several of the previously proposed inverters that have been reviewed in this chapter, many soft-switching inverters have very sophisticated and expensive auxiliary circuits.
  - It should be able to operate with high switching frequency. High switching frequency operation can reduce the size and weight of the inverter and make the inverter produce three-phase output voltage waveforms that are closer to being ideally sinusoidal than those achievable by low switching frequency operation.

- Its main power switches should operate with ZVS. ZVS is the standard, preferred option over ZCS in high frequency, low power applications.

- If auxiliary circuits are used to help the inverter's main power switches operate with ZVS, then the switches in these circuits should operate softly, if possible, and not be subjected to excessive voltage and current stresses. Moreover, the operation of the auxiliary circuit should not interfere with the inverter's ability to produce sinusoidal output voltages.

- It should be able to operate as an inverter (dc-ac converter) and as a rectifier (ac-dc converter). In other words, it should be able to operate in applications where there is a need for the bidirectional flow of power. Such applications include application where there is battery storage (the same converter can be used to charge the battery or to allow the battery to supply power to the mains) or in small wind energy systems. This is something many previously proposed soft-switching inverters cannot do, since the mechanism used to ensure that the main power switches operate with soft-switching restricts the inverter's ability to process power bidirectionally.

- It should be able to operate with PWM control. A number of previously proposed inverters need to operate with non-standard, non-PWM, variable switching frequency control methods that require the intricate timing of the switching transitions so that the inverter switches can be turned on or off softly. These

methods are very sophisticated and do not allow the inverter to produce the same quality of output voltage as PWM methods can.

- To analyze the steady-state operation of the new inverter so that its steady-state operating characteristics can be determined and its operation understood.
- To develop a design procedure that will allow for the proper selection of components to be implemented in the inverter.
- To confirm the feasibility of the proposed inverter by computer simulation.

1.9 Organization of Thesis

The thesis is organized as follows:

In Chapter 2, the new inverter is introduced. A PWM scheme that the proposed converter can use to ensure that three-phase sinusoidal output voltages can be produced is discussed along with its operation. The various modes of operation that the inverter goes through during a single switching cycle are explained and are analyzed mathematically, and the inverter's features are stated.

In Chapter 3, the results of the analysis performed in Chapter 2 are used to determine the steady-state characteristics of the new inverter and the effect that certain individual parameters have on its performance. A design procedure for the selection of key inverter components is established, and then demonstrated with an example.

In Chapter 4, computer simulation results that demonstrate the feasibility of the proposed inverter and the validity of the steady-state analysis are presented. PSIM, a recognized commercially available power electronics simulation software package, is used to perform the simulations.

In Chapter 5, the contents of the thesis are summarized, the main conclusions and contributions of the thesis are stated, and suggestions for future work are made.

Chapter 2

Proposed Three-Phase Reduced Switch ZVS-PWM Inverter

2.1 Introduction

In this chapter, a new ZVS-PWM three-phase inverter is proposed and its operation is discussed. A PWM method that can be implemented in the inverter is discussed, and the various modes of operation that the inverter goes through during a single switching cycle are explained and are analyzed mathematically. The results of the analysis are used in the next chapter to help determine the converter's steady-state characteristics so that its properties can be understood. Finally, the inverter's features are discussed.

2.2 Operating Principles

The new three-phase reduced switch ZVS-PWM inverter is shown in Figure 2.1. It is based on the reduced switch inverter that was examined in [83]-[88]. The inverter consists of four main switches Q_1, Q_3, Q_4, and Q_6 and four capacitors that are each connected across a main switch C_1, C_3, C_4 and C_6. Each of the two inverter legs that contain a pair of switches has an auxiliary circuit connected to it. Q_{a1} and Q_{a2} are auxiliary switches, C_{s1} and C_{s2} are clamping capacitors and L_{s1}, L_{s4} and L_{s3}, L_{s6} are auxiliary circuit inductors. The clamping capacitor C_{s1} and C_{s2} help to clamp of the voltage of a main inverter switch voltage by storing energy whenever one of these switches is turned off. Inductors L_{s1}, L_{s4}

and L_{s3}, L_{s6} are responsible to limit the rate of *di/dt* during a switching transition. The auxiliary circuits allow each of the four main inverter switches to turn on with ZVS. The main inverter switches do not need help to turn off with ZVS since the rate of voltage rise (*dv/dt*) is limited by the capacitor across each switch. It should be noted that C_1, C_3, C_4 and C_6 can be just the output capacitance of a switching device or the sum of such a capacitance and an external capacitor.

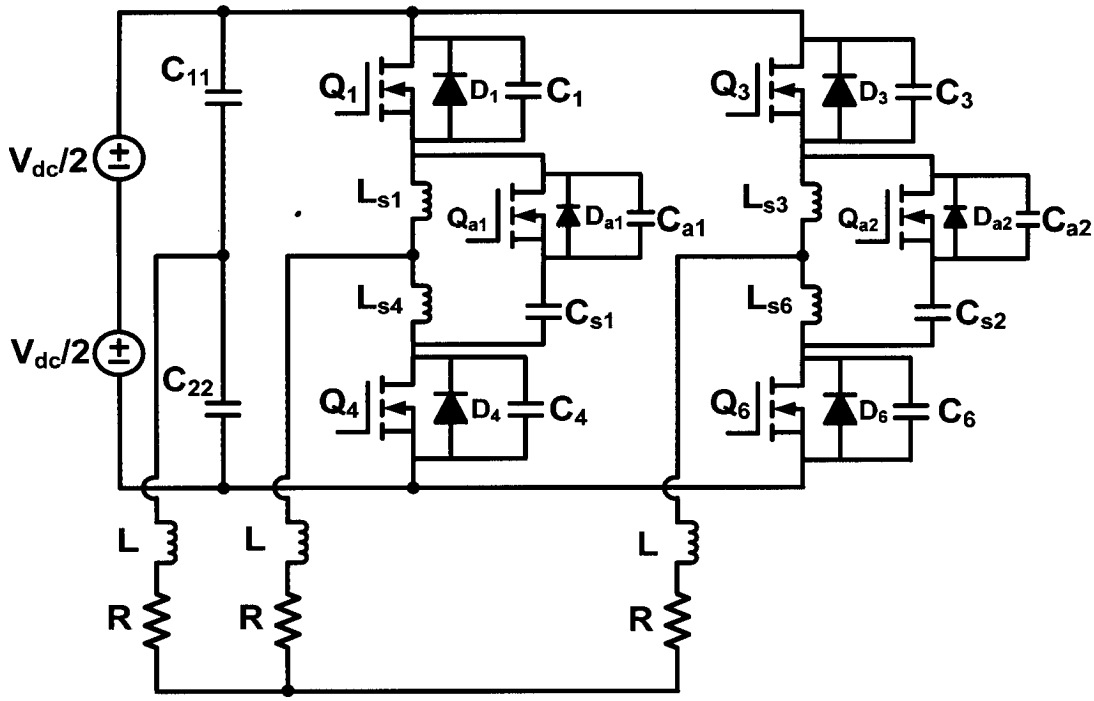


Figure 2.1. Proposed three-phase inverter

2.3 PWM Operation

The proposed inverter can produce three-phase sinusoidal output voltages if a valid PWM method is used to produce appropriate gating signals that will turn the inverter switches

on and off at the proper instants. Although there are numerous PWM techniques that can be implemented in inverters in general and in the proposed inverter, it will be assumed throughout this thesis that the inverter operates with sinusoidal PWM (SPWM), which is the one of the simplest possible methods of PWM. This will be done for simplification as the focus of the thesis is not on PWM methods and a detailed review of these methods is outside the scope of this thesis. The PWM method that will be used in this thesis will be briefly reviewed, however, to better understand how the proposed inverter can produce sinusoidal voltages.

Consider a conventional six-switch inverter, as shown in Figure 2.2 and the line-to-line output voltage waveform shown in Figure 2.3(a) [89]. This line-to-line output voltage (which is the voltage between two output phases, before the output inductor filters) can be produced by very low frequency switching. This waveform can be considered to be a sinusoid with low order harmonic frequency components according to Fourier Analysis theory, as shown in Figure 2.3(b). If this voltage is applied to the load (along with two other identical waveforms that are spaced 120^{o} apart), then the filter inductors will block most of the harmonic frequency components so that the current through the load (and thus the voltage across the load resistances), will be sinusoidal with some distortion, as shown in Figure 2.3(c).

The harmonic current of the output line-to-line voltage can be improved if notches are placed in the square-wave voltage waveform of Figure 2.3(a) at appropriate locations, as shown in Figure 2.3(d). This alters the harmonic content of the line-to-line voltage waveform so that the frequency of the harmonic components is increased, as shown in

Figure 2.3(e). If the line-to-line voltage waveform of Figure 2.3(d) is fed to the load, along with the two other line-to-line voltage waveforms, then the current through the load will have less distortion than the waveform shown in Figure 2.3(c), as can be seen in Figure 2.3(f).

The key to producing sinusoidal output waveform is to determine how to "chop up" the output line-to-line voltage waveform. With SPWM, this can be done as shown in Figure 2.4 [89]. Figure 2.4(a) shows a sinusoidal modulation signal and a triangular carrier signal. The gating signal of a switch in an inverter leg, such as the one shown in Figure 2.4(b), can be determined from the intersections of the modulating and carrier waveforms. For the signal shown in Figure 2.4(b), this has been done by making the signal high whenever the sinusoidal modulating waveform is greater than the triangular carrier signal and low otherwise. The gating signal for the other switch in the same inverter leg can be determined by making the signal low whenever the sinusoidal modulating waveform is greater than the triangular carrier signal and high otherwise. The gating signals of the switches in the second inverter leg can be determined by using a modulating waveform that has been shifted by 120^{o} in one direction with respect to the one shown in Figure 2.4(a), while the gating signals of the switches in the third inverter leg can be determined by using a modulating waveform that has been shifted by 120^{o} in the opposite direction. It is with these gating signals that line-to-line output voltage waveforms like the one shown in Figure 2.4(c). It should be noted that the amplitude of the fundamental component of the line-to-line voltage waveform is directly proportional to the amplitude of the sinusoidal modulating waveform.

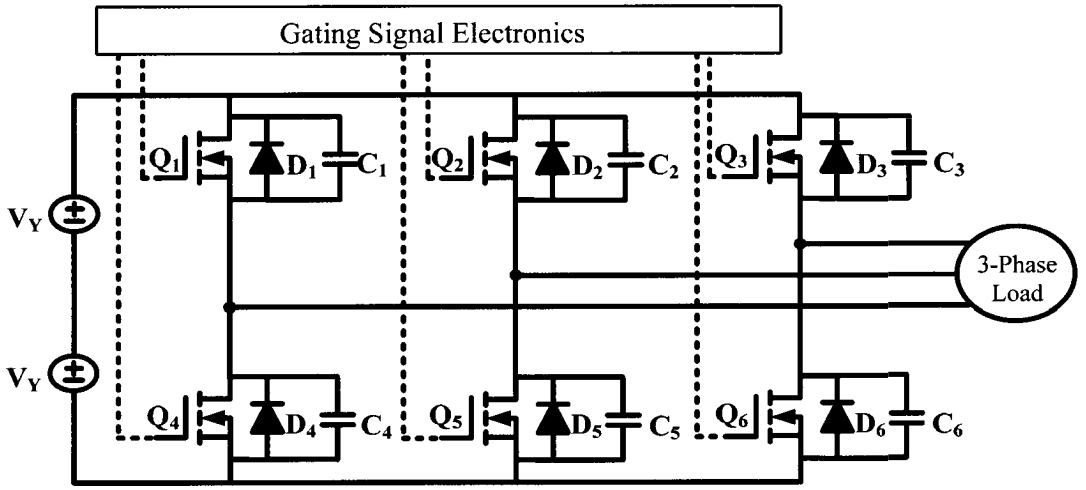


Figure 2.2. Conventional six-switch three-phase inverter

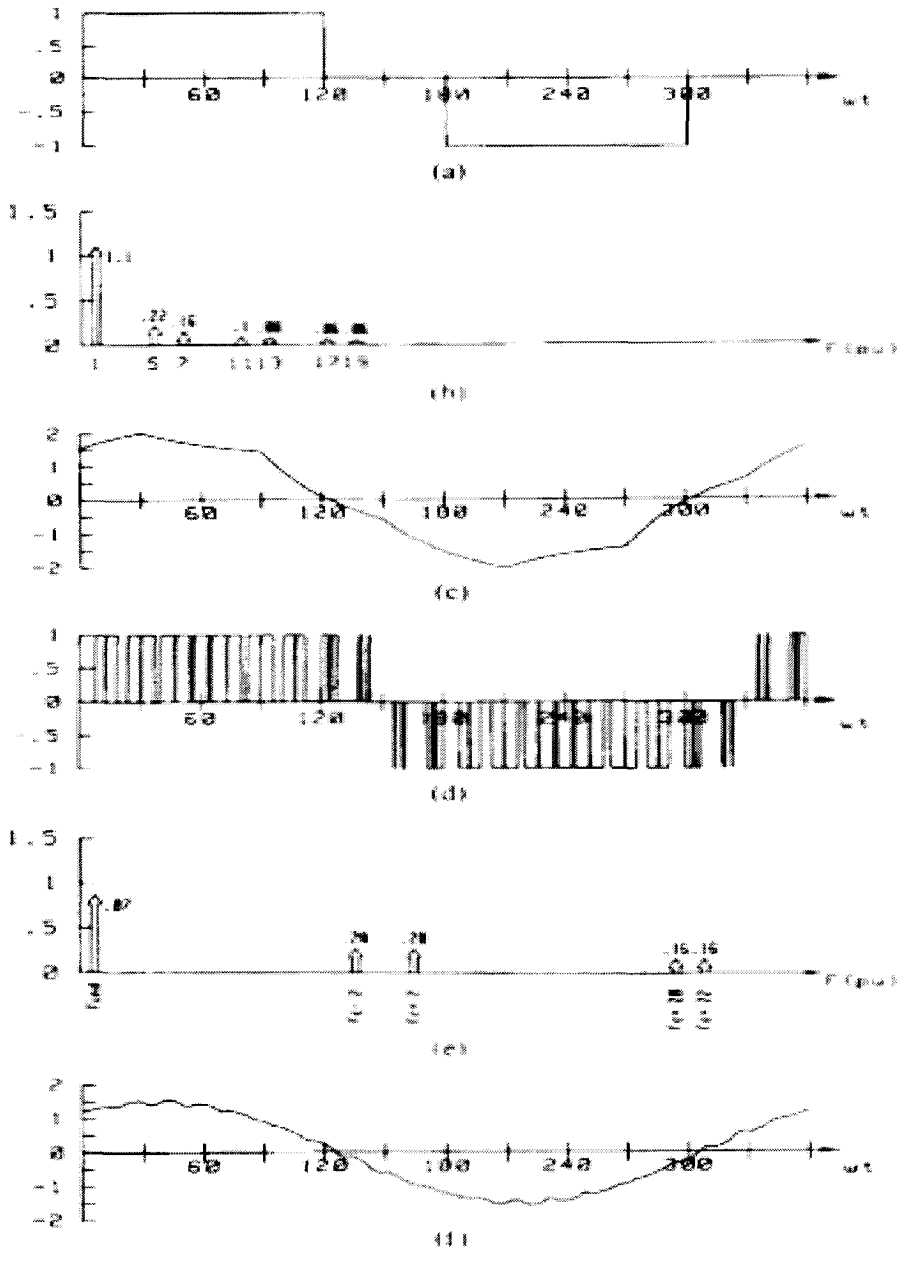


Figure 2.3. Inverter voltage and current waveforms with six-step and sinusoidal PWM (SPWM) operation. (a) Square wave output line-to-line voltage. (b) Line-to-line voltage spectrum (square-wave). (c) Output line current (square-wave). (d) SPWM output line-to-line spectrum (SPWM). (f) Output line current (SPWM). [89]

The SPWM method can be used in the proposed reduced switch rectifier if a modification is made. This modification is the phase difference of the signal related to the two inverter legs that have switches. In a conventional six-switch inverter, this phase difference is 120°, but in the reduced switch inverter, it is 60°. This can be explained with reference to Figure 2.5 and Figure 2.6.

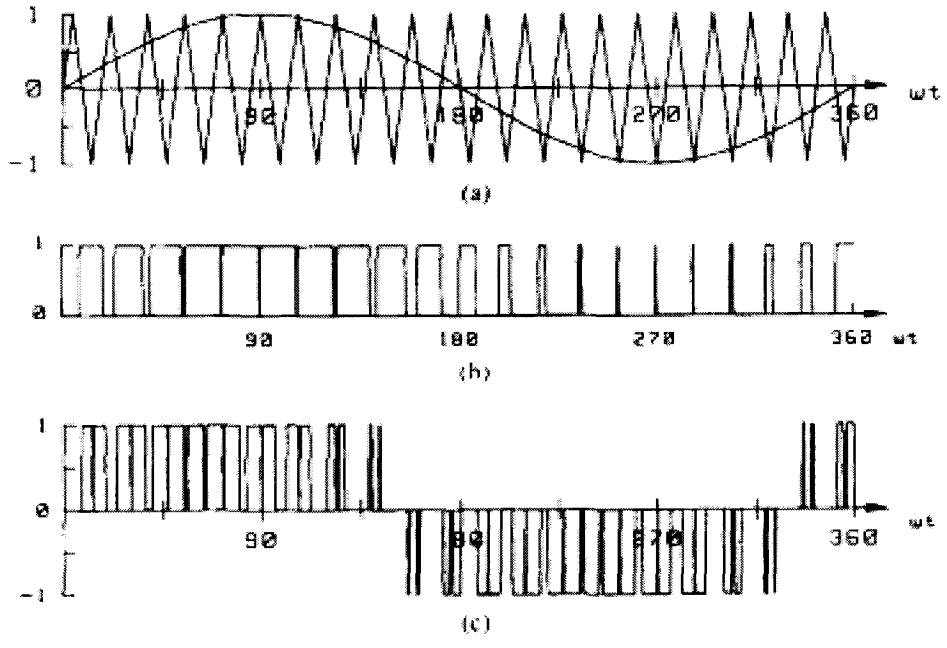


Figure 2.4. Sinusoidal PWM (SPWM). (a)SPWM scheme. (b)VSI switch Q_1 gating signal (c)AC term. [89]

Fig. 2.6(a) shows a conventional three-phase system with a three-phase voltage source feeding a three-phase load. The addition of a voltage V_z, that is opposite in phase and equal in amplitude to V_b to all phases, as shown in Figure 2.6(b) results in a zero sequence component that does not affect the current flow in the system if the star (or neutral) point remains floating - the currents I_a, I_b and I_c still represent a balanced positive sequence

three-phase system. The result of adding voltage V_z, to each phase can be seen in the phasor diagram shown in Figure 2.6(c) - the phase voltage V_b is cancelled and phase voltages V_a and V_c are changed into voltages V_x and V_Y. The magnitude of voltages V_x and V_Y is greater than that of the original phase voltages V_a and V_c by a factor of $\sqrt{3}$, and the phase difference between V_x and V_Y is 60 degrees. Figure 2.6 (d) shows the equivalent circuit when the original phase voltages are replaced by voltages V_x and V_Y.

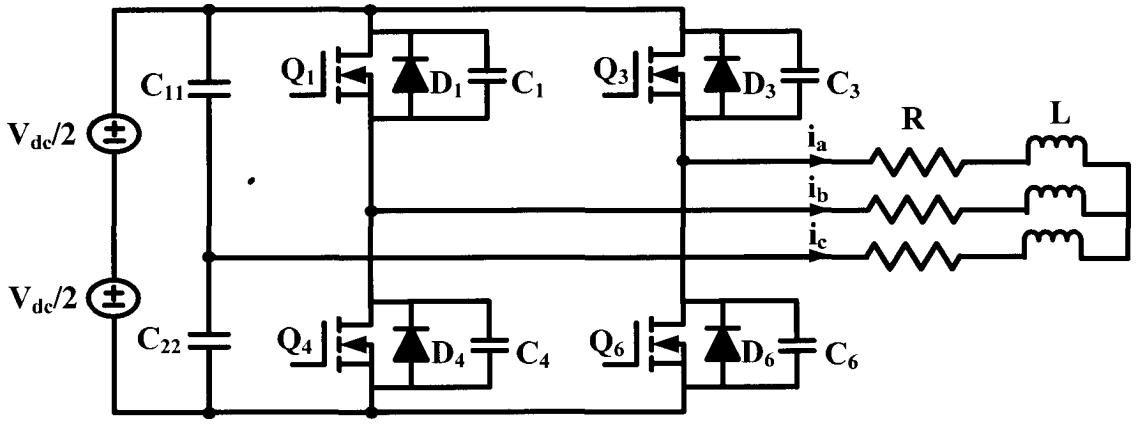


Figure 2.5. Reduced switch three-phase inverter

The current in the phase that is coming from the center of the split-capacitor bank i_c is the result of the currents i_a and i_b in the two controlled phases (refer to Figure 2.5). If currents i_a and i_b are sinusoidal, then current i_c must also be sinusoidal according to Kirchoff's Current Law because the sum of the three currents flowing into a three-phase load must be zero. As a result, current i_c is left "alone" as it will naturally be sinusoidal as well.

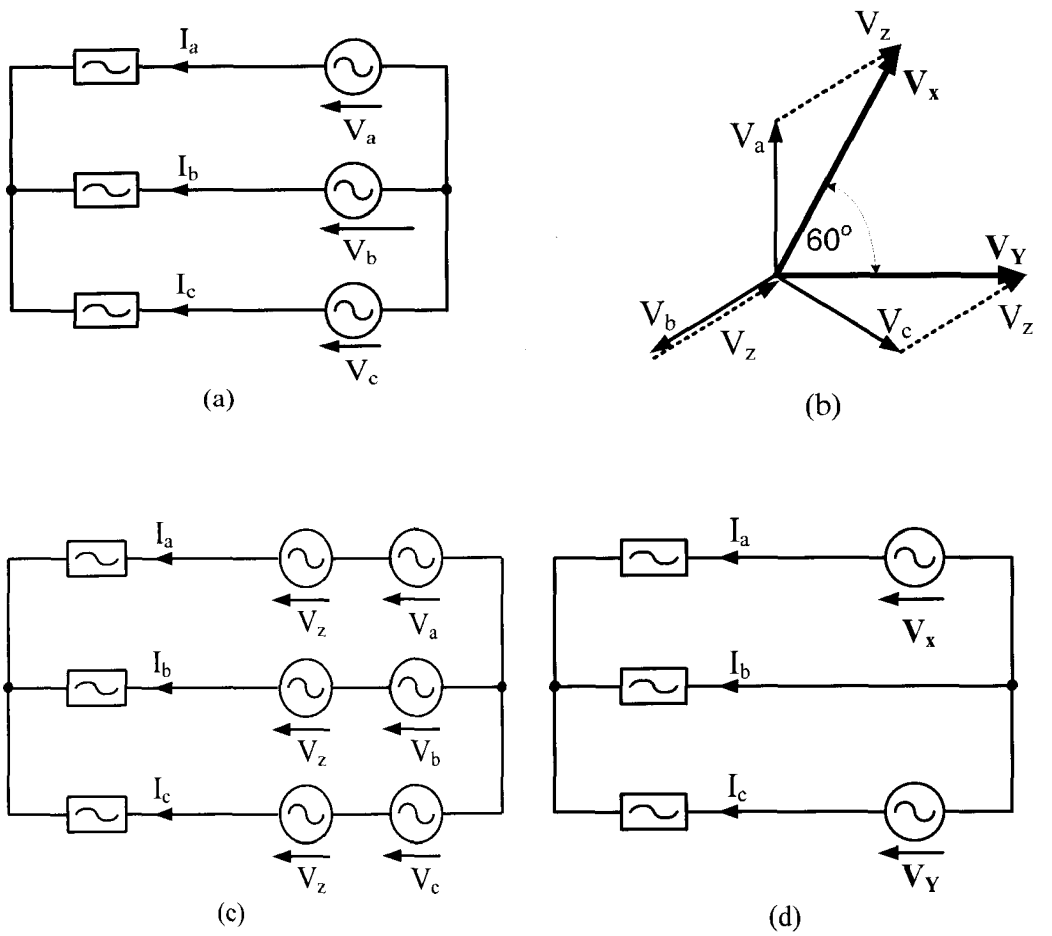


Figure 2.6. Supplying three-phase load from two voltage sources with 60° phase shift

2.4 Converter Operation

The quality of the output waveform improves as the switching frequency of the inverter is made higher. For the SPWM method discussed in the previous section, this can be achieved by increasing the frequency of the triangular carrier signal relative to that of the sinusoidal modulating waveform. Higher switching frequency operation, however, results

in more switching losses, thus the need for ZVS operation, and the need for auxiliary circuits that will have the inverter switch do just that. In this section, the various modes that the inverter encounters while it is going through a switching cycle during steady-state operation are explained. It should be noted that the main focus of this explanation is on the operation of the auxiliary circuits and that a switching cycle is considerably smaller than the period of the output waveforms.

A mathematical analysis of each mode that the inverter goes through during a switching cycle will also be performed. Some assumptions have been made to simplify the analysis, including the following: It is assumed that the circuit operates in steady state; the inverter components are ideal; and the voltage across capacitors C_{s1}, C_{s2} and the current through the output inductors are constant during the switching period. The proposed inverter has nine operating intervals for a half cycle of output current. The current waveforms of components C_{s1}, L_{s1} and L_{s4} are shown in Figure 2.7 and the equivalent circuit for each interval is shown in Figure 2.8. For the sake of simplicity, the discussion below will refer to only one of the two inverter legs with switches, but it is applicable to the other leg as well.

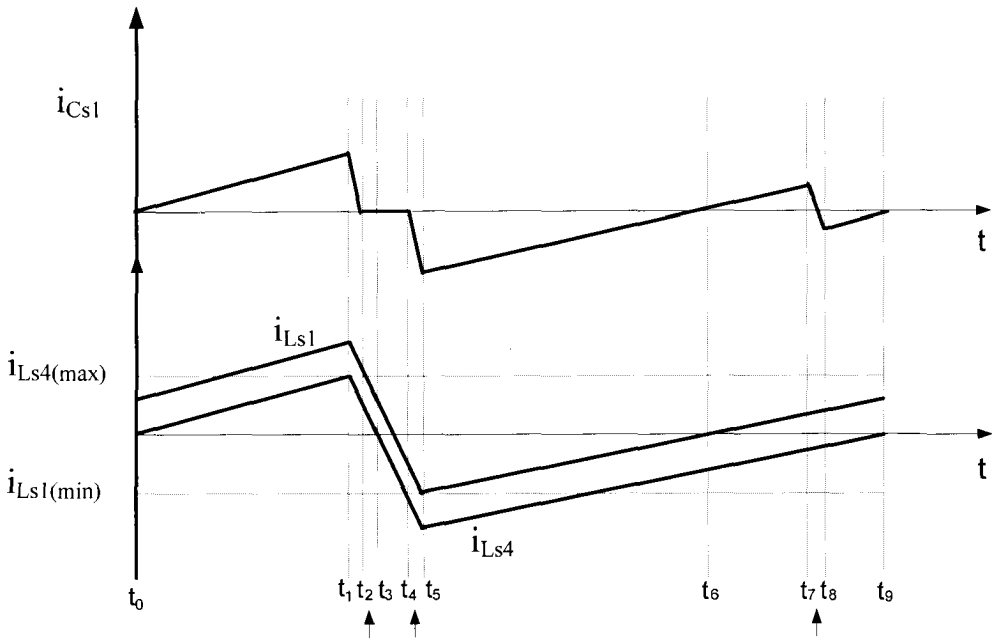


Figure 2.7. Current waveforms of the snubber elements C_{s1}, L_{s1} and L_{s4}

1) Interval-1(t_0-t_1):

The description begins with the interval when the auxiliary switch Q_{a1} is turned on. During this interval, the output current i_a, is delivering energy to the source via diode D_1. At the same time, additional current, i_{Ls4}, is flowing in the loop consisting of L_{s1}, Q_{a1}, C_{s1} and L_{s4}. At the end of this interval, the current through inductor L_{s4} reaches its maximum value $i_{Ls4\ (max)}$. The current i_{Ls1} is the sum of i_{Ls4} and i_a. This stage precedes a switching transition of main switch Q_4. At time t_0, current i_{Ls4} becomes positive and increases linearly. This current is ultimately responsible for the ZVS turn-on of Q_4. The key equations that describe the operation of the inverter during this interval are:

$$i_{Ls4}(t) = \frac{V_{Cs1}}{L_s}.t \tag{2.1}$$

$$i_{Ls1}(t) = i_{Ls4}(t) + i_a \tag{2.2}$$

$$v_{C4}(t) = E + V_{Cs1} \tag{2.3}$$

$$v_{CA1}(t) = 0 \tag{2.4}$$

where $E = \frac{V_{dc}}{2} + \frac{V_{dc}}{2}$ and $L_s = L_{s1} + L_{s4}$

2) Interval-2(t_1-t_2):

Interval-2 begins when auxiliary switch Q_{a1} is turned off. The current i_{Ls4} begins to charge the capacitance C_{a1} from 0 towards $(E + V_{Cs1})$ and to discharge C_4 from $(E + V_{Cs1})$ towards *0*. The key equations that describe the operation of the inverter during this interval are

$$v_{C4}(t) = -\frac{i_{Ls4(max)}}{2C_4}.t + (E + V_{cs1}) \tag{2.5}$$

$$v_{Ca1}(t) = \frac{i_{Ls4(max)}}{2C_{a1}}.t \tag{2.6}$$

$$i_{Ls4}(t) = i_{Ls4(max)} \tag{2.7}$$

$$i_{Ls1}(t) = i_{Ls4(max)} + i_a \tag{2.8}$$

3) Interval-3(t_2-t_3):

This interval starts when C_4 is fully discharged and current begins to flow through the anti-parallel diode across Q_4, D_4. As soon as this happens, Q_4 can be turned on with ZVS. Inductors L_{s1} and L_{s4} each have a voltage E across them so that so both currents i_{Ls1} and i_{Ls4} decrease linearly, according to

$$i_{Ls4}(t) = -\frac{E}{L_s}.t + i_{Ls4(max)} \tag{2.9}$$

4) Interval-4(t_3-t_4):

This interval begins when i_{Ls4} reverses direction and ramps up while i_{Ls1} continues to ramp down. This interval ends when i_{Ls1} also changes direction. The key equations that describe the operation of the inverter during this interval are

$$i_{Ls4}(t) = -\frac{E}{L_s}.t \tag{2.10}$$

$$i_{Ls1}(t) = i_{Ls4}(t) + i_a(t) \tag{2.11}$$

5) Interval-5(t_4-t_5):

Interval-5 starts when current i_{Ls1} begins to charge C_1 from 0 towards (E + V_{Cs1}) and to discharge C_{a1} from (E + V_{Cs1}) towards 0. The key equations that describe the operation of the inverter during this interval are

$$v_{C1}(t) = \frac{i_{Ls1}(min)}{2C_1}.t \tag{2.12}$$

$$v_{Ca1}(t) = -\frac{i_{Ls1}(min)}{2C_{a1}}.t + (E + V_{Cs1}) \quad (2.13)$$

$$i_{Ls1}(t) = -i_{Ls1}(min) \quad (2.14)$$

$$i_{Ls4}(t) = -i_{Ls1(min)} - i_a \quad (2.15)$$

6) Interval-6(t_5-t_6):

This interval begins when C_{a1} discharges to 0 and current begins to flow through diode D_{a1}. This allows auxiliary switch Q_{a1} to be turned on with ZVS. Currents i_{Ls1} and i_{Ls4} decrease due to the voltage V_{Cs1} applied by the capacitor C_{s1}. The key equations that describe the operation of the inverter during this interval are

$$i_{Ls1}(t) = \frac{V_{Cs1}}{L_s}.t \quad (2.16)$$

$$i_{Ls4}(t) = i_{Ls1}(t) - i_a \quad (2.17)$$

$$v_{C1}(t) = E + V_{Cs1} \quad (2.18)$$

7) Interval-7(t_6-t_7):

This interval begins when current i_{Ls1} changes its direction and flows through switch Q_{a1}. Currents i_{Ls1} and i_{Ls4} continue to increase linearly. The key equations that describe the operation of the inverter during this interval are

$$i_{Ls1}(t) = \frac{V_{Cs1}}{L_s}.t \quad (2.19)$$

$$i_{Ls4}(t) = i_{Ls1}(t) - i_a \quad (2.20)$$

$$v_{C1}(t) = E + V_{Cs1} \quad (2.21)$$

8) Interval-8(t_7-t_8):

This interval starts when main switch Q_4 is turned off. At this instant, the current through C_{s1} changes direction, moving from Q_{a1} to D_{a1}. Capacitor C_4 charges from zero to $(E + V_{Cs1})$ and capacitor C_1 discharges from $(E + V_{Cs1})$ to zero. The key equations that describe the operation of the inverter during this interval are

$$v_{C4}(t) = \frac{i_a}{2C_4} . t \tag{2.22}$$

$$v_{C1}(t) = -\frac{i_a}{2C_1} . t + (E + V_{Cs1}) \tag{2.23}$$

$$i_{Ls1}(t) = \frac{V_{Cs1}}{L_s} . \Delta t_7 \tag{2.24}$$

where $\Delta t_7 = D.T_s + \frac{i_{Ls1(min)} L_s}{V_{Cs1}}$

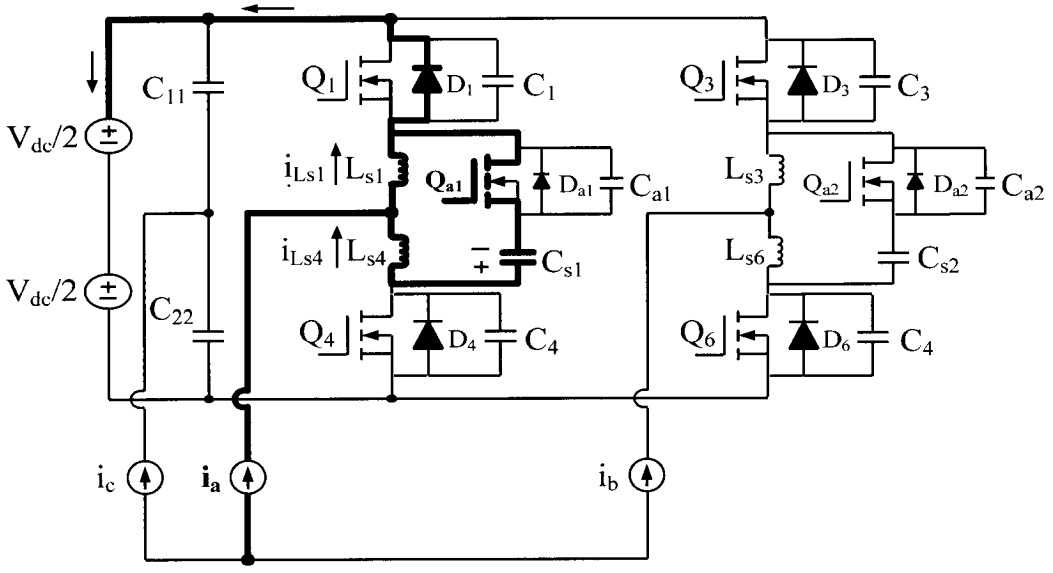
9) Interval-9(t_8-t_9):

This interval begins when C_1 is discharged to 0 and current starts to flow through diode D_1, while C_4 is charged to $(E + V_{Cs1})$. During this interval, i_{Ls4} continues to decrease and i_{Ls1} continues to increase. At the instant when i_{Ls4} reverses and moves from D_{a1} to Q_{a1}, Interval-1 begins. The key equations that describe the operation of the inverter during this interval are

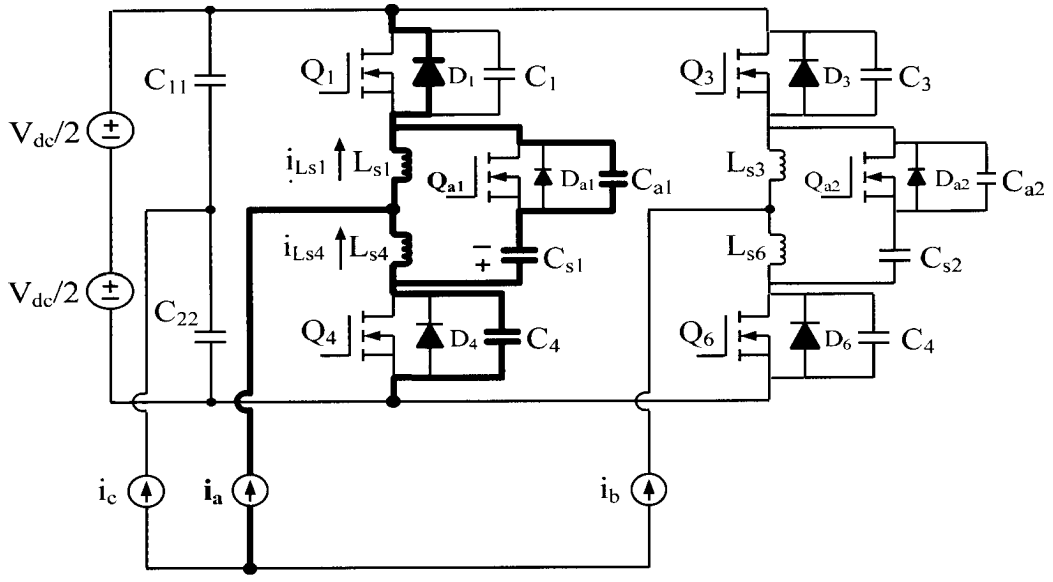
$$i_{Ls1}(t) = \frac{V_{Cs1}}{L_s} . t + \frac{V_{Cs1}}{L_s} . \Delta t_7 \tag{2.25}$$

$$i_{Ls4}(t) = -i_a + i_{Ls1}(t) \tag{2.26}$$

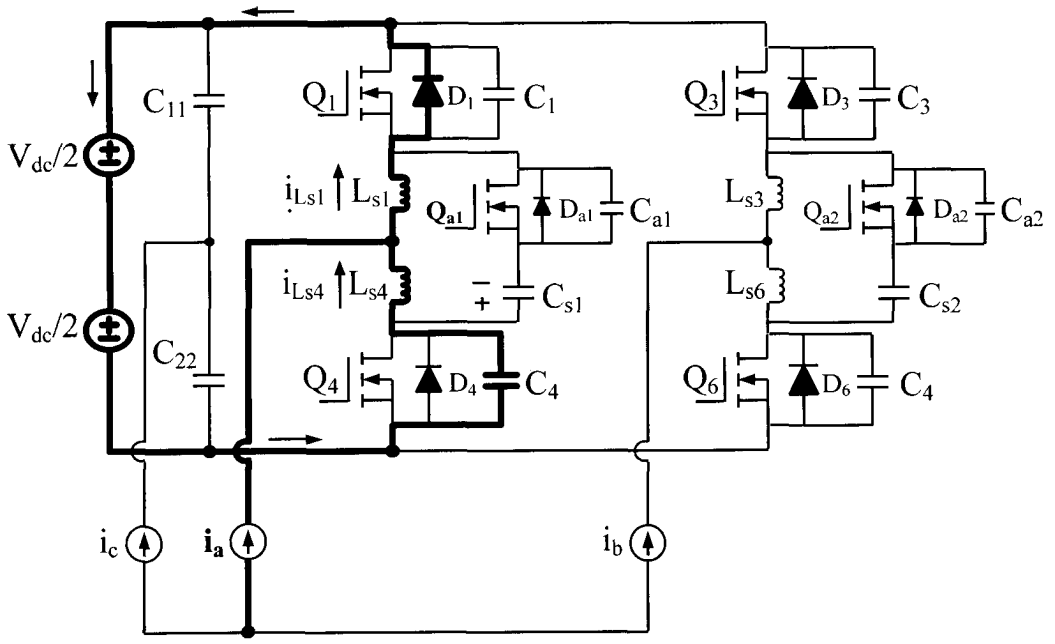
Three transition intervals, Intervals 2, 5, and 8, are very short. In Figure 2.7, $i_{Ls4(max)}$ denotes the final current value of the auxiliary switch Q_{a1} just before this switch is turned off to initiate the ZVS turn-on of a main switch.



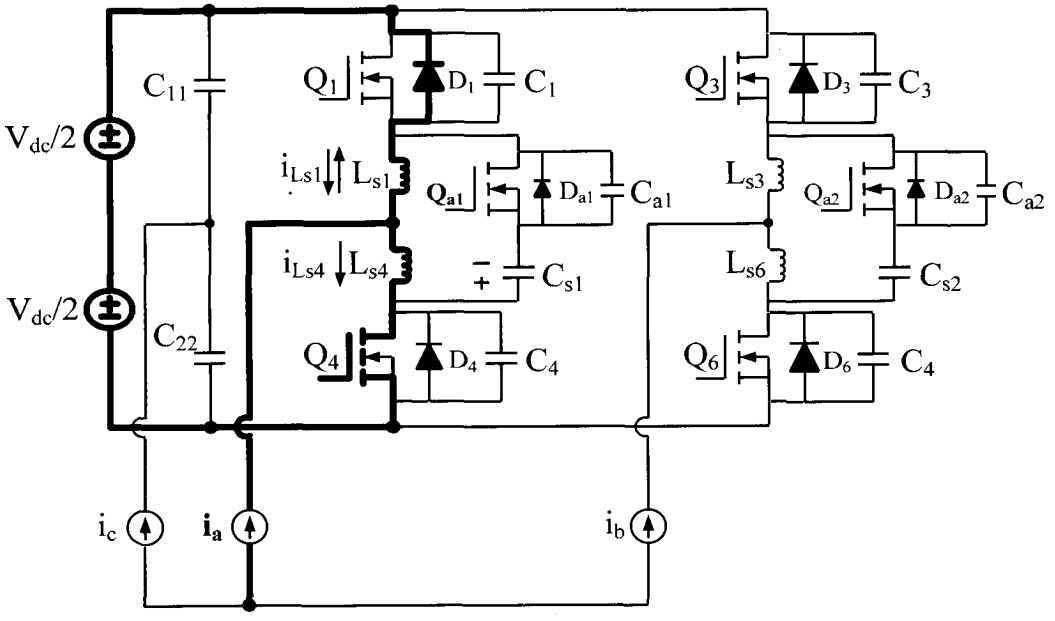
(a) Interval-1 (t_0-t_1)



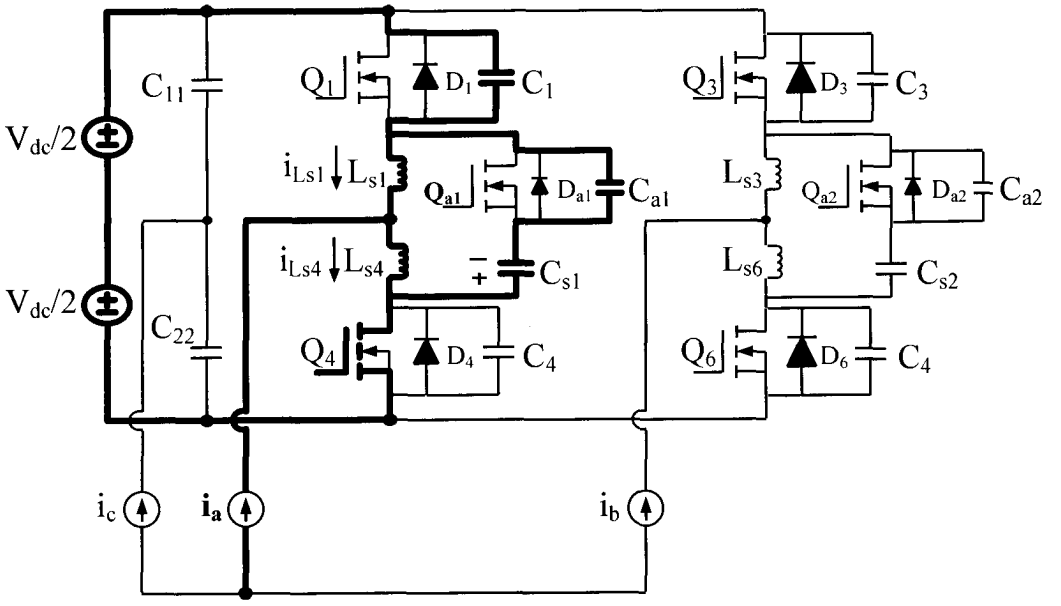
(b) Interval-2 (t_1-t_2)



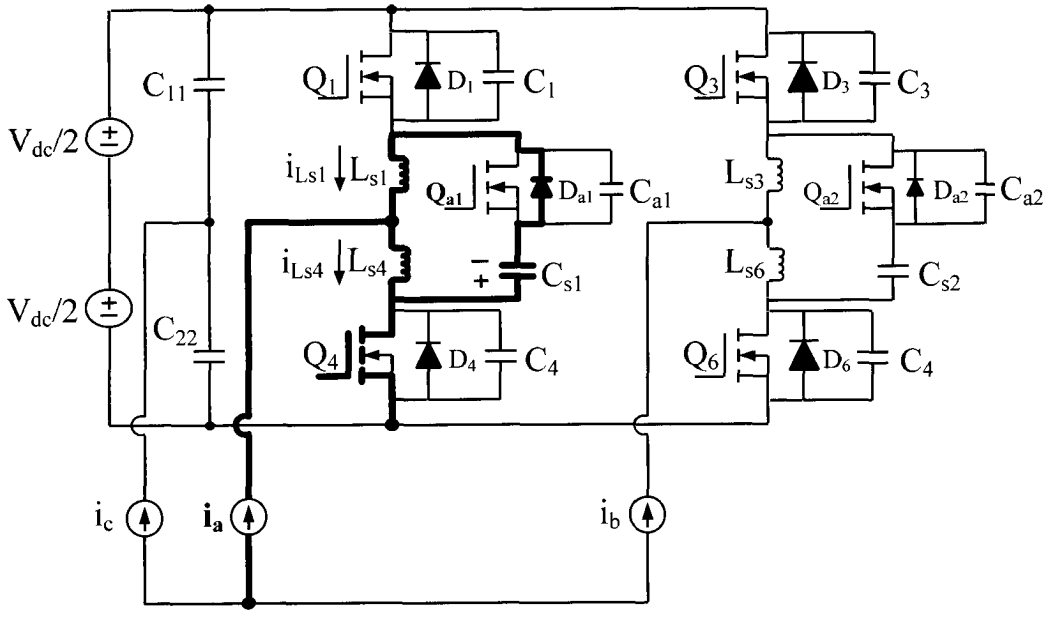
(c) Interval-3 (t_2-t_3)



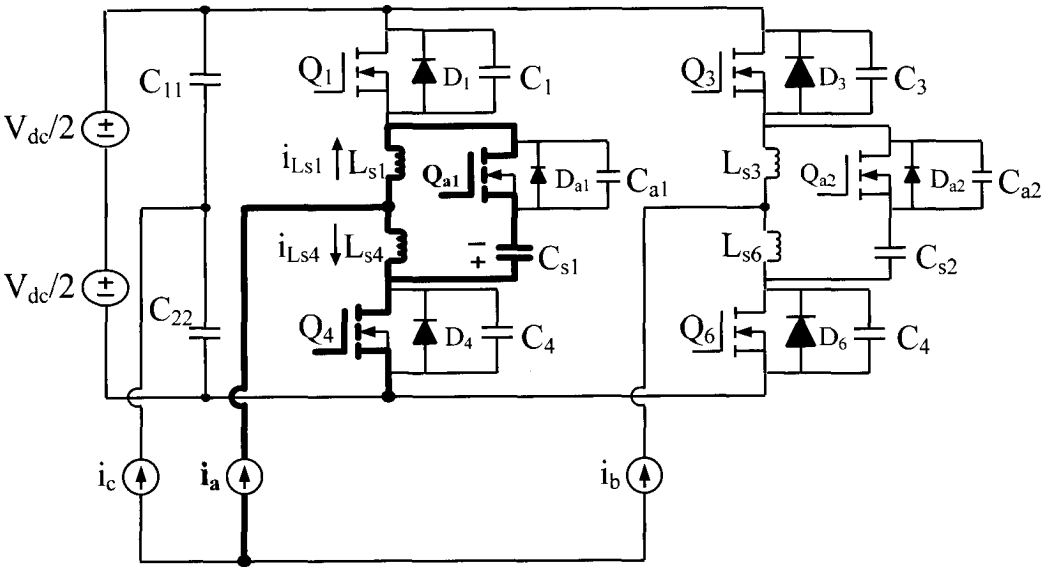
(d) Interval-4 (t_3-t_4)



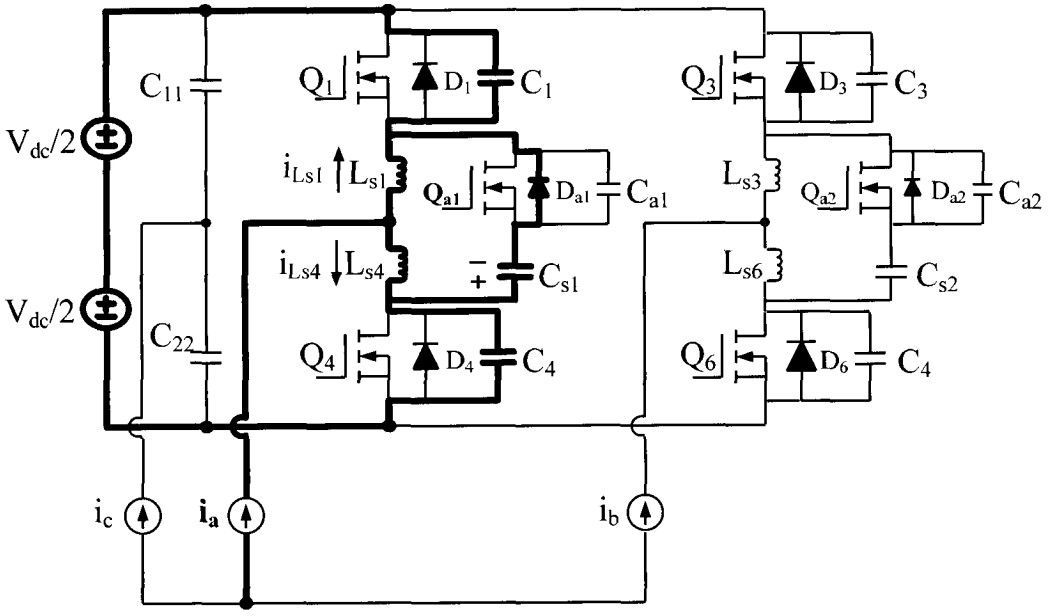
(e) Interval-5 (t_4-t_5)



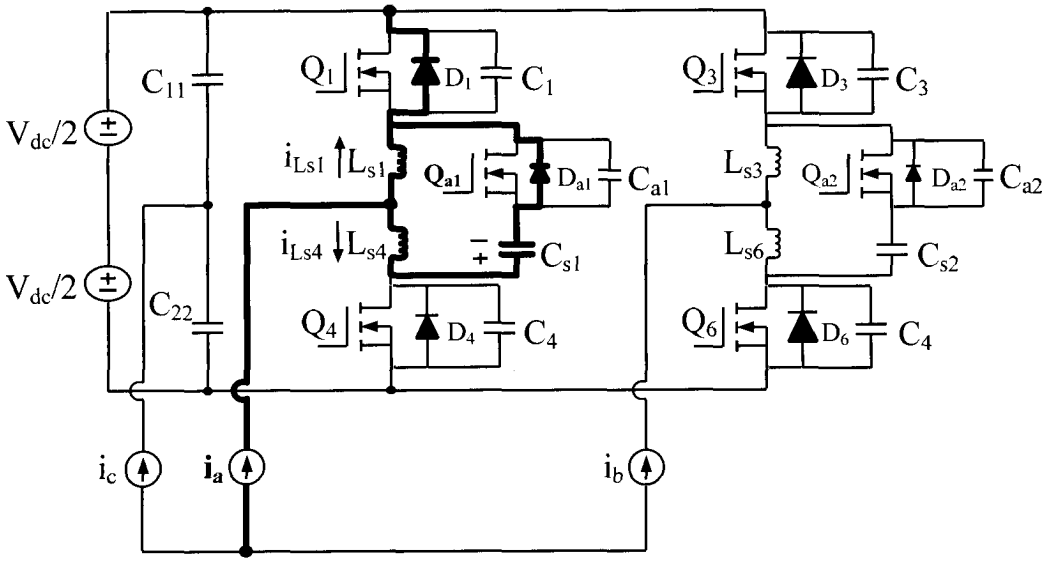
(f) Interval-6 (t_5-t_6)



(g) Interval-7 (t_6-t_7)



(h) Interval-8 (t_7-t_8)



(i) Interval-9 (t_8-t_9)

Figure 2.8. Operation Intervals. (a) Interval-1 (t_0-t_1). (b) Interval-2 (t_1-t_2). (c) Interval-3 (t_2-t_3). (d) Interval-4 (t_3-t_4). (e) Interval-5 (t_4-t_5). (f) Interval-6 (t_5-t_6). (g) Interval-7 (t_6-t_7). (h) Interval-8 (t_7-t_8). (i) Interval-9 (t_8-t_9).

2.5 Inverter Features

The proposed inverter has the following important features:

- It has most of the benefits of a conventional three-phase inverter, but at a reduced cost as it has four main power switches instead of six.
- The main inverter switches can be turned on with ZVS with the help of an auxiliary circuit in each leg. Its main switches can be turned off with ZVS due to the presence of a capacitor across each switch that helps slow down the rise in voltage that occurs

whenever a main switch is turned off. Since the overlap of voltage and current that would otherwise occur whenever a main inverter switch undergoes a switching transition is significantly reduced (in the case of the turn-on transition it is close to zero and as voltage across the switch is almost zero) so too are switching losses.

- The switch in each auxiliary circuit also operates with ZVS.

- Since the auxiliary circuit operates for a small fraction of a switching cycle, the device that is used for the auxiliary switch can be a smaller, lower power rated, cheaper device than a main inverter switch device.

- The auxiliary circuits that are connected to each inverter leg do not interfere with the inverter's ability to produce a sinusoidal three-phase output voltage unless the switching cycles are very small. Extremely small switching cycles means that the duration of auxiliary circuit operation becomes significant relative to the switching cycle so that the output voltage pulses that appear before the filter inductors may be distorted. Since very small switching cycles are due to converter operation with very high switching frequencies that cannot be used with hard-switching inverters (because of their switching losses), this phenomenon is not a concern.

- A very attractive feature is that the presence of the auxiliary circuits in the inverter does not interfere with the inverter's ability to operate as a rectifier (ac-dc converter) as well as an inverter. This is unlike many other previously proposed ZVS-PWM inverters that cannot operate with ZVS unless they operate only as inverters. This feature is important because it allows the inverter to be implemented in applications

where there is a need for the bidirectional flow of power. Such applications include application where there is battery storage (the same converter can be used to charge the battery or to allow the battery to supply power to the mains) or in small wind energy systems. It should be noted that the details of rectifier operation will be not discussed in the thesis as the converter waveforms and modes of operation are identical to those produced by inverter operation.

The main limitation that the proposed inverter has when compared to the conventional three-phase inverter is it can handle the maximum power. This is because it has fewer main power switches so that each main switch is subjected to more current stress than is a main switch in a conventional three-phase converter when the converter tries to deliver the same amount of power.

2.6 Conclusion

In this chapter, a new three-phase inverter was proposed. The inverter is based on a reduced switch topology that can produce three-phase sinusoidal output voltages. A PWM method that allows the new inverter to produce these voltages was presented, and the various modes of operation that the inverter goes through during a single switching period were explained and a mathematical analysis of each mode was performed. The result of the analysis will be used in the succeeding chapters of this thesis. Finally, the salient features of the proposed inverter were stated.

Chapter 3

Analysis and Design of the Proposed Inverter

3.1 Introduction

In this chapter, an analysis of the proposed inverter, related to its ZVS operation, is presented. The results of the analysis are then used as part of a design procedure to ensure that the main converter switches operate with ZVS. The design procedure is demonstrated with an example that shows how the value of certain key components can be selected.

3.2 Minimum Current Required for ZVS

Consider the inverter leg that has switches Q_1 and Q_4. The process that allows for the zero-voltage switching (ZVS) turn-on of one of these main switches is initiated by turn-off of the auxiliary switch Q_{a1}. For example, say that the switch that is to be turned on is Q_4. When Q_{a1} is turned off (Interval-2), the energy that is in inductors L_{s1} and L_{s4} discharges switch output capacitance C_4 and charges auxiliary switch output capacitance C_{a1}, as the current that was flowing through Q_{a1} must have a path to flow through (refer to Figure 2.8(b)). Once switch output capacitance C_4 is fully discharged, current starts to flow through the body-diode of Q_4, which clamps the voltage across this device to zero (neglecting the body-diode's forward voltage drop) and thus allows the switch to be

turned on with ZVS. A similar process allows Q_1 and Q_4 to be turned on with ZVS with the help of Q_{a1}, and switches Q_3 and Q_6 to be turned on with the help of Q_{a2}.

Q_4 can turn on with ZVS only when there is sufficient energy in L_{s1} and L_{s4} to discharge C_4 and charge C_{a1}. Current must be flowing through the body-diode of a switch while it is being turned on and this is not possible without the discharging of C_4 and the charging of C_{a1}. Since the energy stored in L_{s1} and L_{s4} must be sufficient to make the voltage across C_4 go from $(E+V_{Cs1})$ to zero and make the voltage across C_{a1} go from zero to $(E+V_{Cs1})$, the following condition can be formulated based on these energy considerations,

$$L_s \cdot i_{Ls4(max)}^2 \geq (C_{a1} + C_4)(E + V_{Cs1})^2 \tag{3.1}$$

where V_{Cs1} is the voltage value across C_{s1} (approximately constant during a switching period), E is the dc-bus voltage, and $L_s = L_{s1}+L_{s4}$. Assuming that $V_{Cs1} \ll E$, then eqn. (3.1) can be written as,

$$i_{Ls4(max)} \geq E. \sqrt{\frac{C_{a1}+ C_4}{L_s}} \tag{3.2}$$

The aim of the following analysis will be to find the necessary conditions to satisfy (3.2) over the whole period of the line frequency. Since the time required for switch Q_4 to turn on with ZVS is negligible compared to the switching period, therefore, only Interval-6 and Interval-7 will be considered in the analysis.

Considering Interval-6 and Interval-7, an expression for current $i_{Ls4}\ (t)$ can be obtained from eqns. (2.17) & (2.20)),

$$i_{Ls4}\ (t) = -\frac{V_{Cs1}}{L_s}.t + i_a \tag{3.3}$$

It can be seen from eqn. (3.3) that $i_{Ls4}\ (t)$ is dependent on the voltage across the active-clamp capacitor C_{s1}, and the per phase load current i_a. The next steps in the analysis are, therefore, to determine expressions for these parameters that can be substituted in eqn. (3.3).

From the mathematical analysis of the modes of operation presented in Chapter-2, the average current of C_{s1} can be written as

$$i_{Cs1(avg.)} = \frac{1}{T_s}\left[\int_{t_5}^{t_7}\left(\frac{V_{Cs1}}{L_s}t - i_{Ls1(min)}\right)dt + \int_{t_7}^{T_s}\left(\frac{V_{Cs1}}{L_s}t - i_{Ls1(min)} - i_a\right)dt\right] \tag{3.4}$$

where T_s is the switching period. Since the time between the activation of Q_{a1} and the turning on of Q_4 is negligible compared to the switching period, therefore, the following simplifications can be made

$$t_5 \approx t_1 = 0 \tag{3.5}$$

$$t_7 - t_5 = D\,.\,T_s \tag{3.6}$$

where D is the time interval of Interval-6 and Interval-7. From eqn. (3.5) and (3.6), the following expression can be written

$$t_7 = D\,.\,T_s \tag{3.7}$$

Substituting eqn. (3.7) into (3.4) gives

$$i_{Cs1(avg.)} = \frac{1}{T_s}\left[\int_0^{D\,.T_s}\left(\frac{V_{Cs1}}{L_s}t - i_{Ls1(min)}\right)dt + \int_{D\,.T_s}^{T_s}\left(\frac{V_{Cs1}}{L_s}t - i_{Ls1(min)} - i_a\right)dt\right] \tag{3.8}$$

As the voltage across clamping capacitors C_{s1}, and C_{s2} are considered constant during the switching period, thus the following statement can be derived,

$$\frac{d}{dt}\left[\frac{1}{C_{S1}}\int_0^{T_s} i_{Cs1}\,dt + V_{Cs1}(t=0)\right] = Constant \tag{3.9}$$

Taking derivative on both side of eqn. (3.9) yields,

$$\frac{d^2}{dt^2}\left[\frac{1}{C_{S1}}\int_0^{T_s} i_{Cs1}\,dt\right] = 0 \tag{3.10}$$

From eqn. (3.10) it can be seen that the average current of C_{s1} in a switching period is zero. Since the average current of C_{s1} is zero, eqn. (3.8) can be solved to give the following expression for V_{Cs1}.

$$V_{Cs1} = \frac{2.L_S}{T_s}\left[i_{Ls1(min)} + i_a(1-D)\right] \tag{3.11}$$

The next steps in the analysis are to determine i_a and D.

If the per phase load current i_a is a sinusoidal function and in phase with the per phase output voltage, then the following expression can be derived from conventional pulse width modulation theory [90],

$$i_a(\omega t) = \frac{E.m_a}{2.Z_{out}} . \sin \omega t \tag{3.12}$$

where m_a is the modulation index for leg-A (containing switch Q_1 and Q_4), Z_{out} is the per phase load impedance, which can be given by

$$Z_{out} = R + j\,(2 * \pi * f * L) \tag{3.13}$$

R is the per phase load resistance, f is the output voltage frequency, and L is the per phase load inductance.

To determine an expression for D for eqn. (3.11), the inverter per phase output voltage must be found. This voltage can be expressed from the standard equation [91], which is given by

$$v_a = E\left(D - \frac{1}{2}\right) \tag{3.14}$$

where v_a is the inverter per phase output voltage. From eqn. (3.14), D can be written as

$$D = \frac{v_a}{E} + \frac{1}{2} \tag{3.15}$$

The inverter per phase output voltage is given by

$$v_a(\omega t) = \sqrt{2} . v_{a(rms)} . \sin \omega t \tag{3.16}$$

where ωt is related to the line period. The rms output voltage can be written as

$$v_{a(rms)} = \frac{E.m_a}{2.\sqrt{2}} \tag{3.17}$$

where m_a is the modulation index for leg-A (contain switch Q_1 and Q_4), which can be written as [90],

$$m_a = S_1\,(t) = \frac{V_{ta}\,(t)}{\frac{V_{dc}}{2}} \tag{3.18}$$

From eqn. (3.15), (3.16), and (3.17), D can be determined to be

$$D(\omega t) = \frac{m_a}{2}.\sin\omega t + \frac{1}{2} \tag{3.19}$$

Since expressions for i_a (eqn. (3.12)) and D (eqn. (3.19)) have been determined, these expressions can be substituted into eqn. (3.11) to give the following for the capacitor voltage V_{Cs1}

$$V_{Cs1}(\omega t) = \frac{2.L_S}{T_S}\left[i_{Ls1(min)} + \frac{E.m_a}{4.Z_{out}}\sin\omega t - \frac{E.\,m_a^2}{4.Z_{out}}.sin^2\,\omega t\right] \tag{3.20}$$

From eqn. (3.3) and (3.20), an expression for i_{Ls4} can be obtained as

$$i_{Ls4}(\omega t) = 2i_{Ls1(min)} - \frac{E.\,m_a^2}{2.Z_{out}}.sin^2\,\omega t \tag{3.21}$$

To guarantee that the inverter switches turn on with ZVS, the minimum value of current i_{Ls4} obtained from eqn. (3.21) must be greater than the value obtained from eqn. (3.2). As in eqn. (3.2) the value of V_{Cs1} is neglected, thus the value of i_{Ls4} provided by eqn. (3.2)

will be less than the value of i_{Ls4} provided by eqn. (3.21). Thus the condition shown in eqn. (3.2) will be considered, as this is the worst-case condition for the circuit for the design procedure.

3.3 Minimum Time-Interval Required for ZVS

During Interval-3, the supply voltage appears across L_s. As a result, current i_{Ls4} ramps down linearly and becomes negative during this interval. Q_4 should be turned on before i_{Ls4} ramps down to zero to achieve ZVS because by this time, the output capacitance of Q_4, C_4, is fully discharged and current is flowing through the body-diode of Q_4, D_4. If this is not done the circuit goes back into Interval-2 and the voltage across Q_{a1} builds up again.

From the above discussion, it can be seen that for the ZVS of Q_4 its body capacitor should be discharged fully and the voltage across Q_4 reduces to zero following eqn. (2.5), during Interval-2, which can be written as,

$$V_{C4} = (E + V_{cs1}) - \frac{i_{Ls4}}{2C_4}(t_2 - t_1) = 0 \tag{3.22}$$

where

$$(t_2 - t_1) = \frac{(E+V_{cs1})}{\frac{i_{Ls4}}{2C_4}} \tag{3.23}$$

In order to achieve ZVS for the switch Q_4, it is necessary to have at least the time interval shown in eqn. (3.23) to fully discharge the capacitor C_4.

3.4 Design Procedure

A systematic procedure is needed to design the proposed inverter so that it can be implemented in a way that satisfies certain desired criteria. This involves selecting appropriate values for the clamping capacitors C_{s1}, C_{s2}, and inductors L_{s1}, L_{s4} and L_{s3}, L_{s6} so that the following key design objectives are achieved.

(i) The current and voltage stresses of the inverter switches should be kept as low as possible.

(ii) The conduction period of the auxiliary switches should be as low as possible to decrease the auxiliary switching losses.

3.4.1 Converter Specifications

The converter is to be designed according to the following specifications:

$E = \frac{V_{dc}}{2} + \frac{V_{dc}}{2} = 400$ V	bus voltage;
$m_a = 0.866$ (for switch Q_1 and Q_4)	modulation index;
$P_{out} = 1500$ VA	output power;
$V_{out} = 120$ V	r.m.s output voltage
$\hat{\imath}_a = 5.9$ A	output current (per phase);
$f_s = 25$ kHz	switching frequency;
$f = 60$ Hz	output frequency;
$L = 500$ uH	load inductance (per phase);
$R = 30$ ohm	load resistance (per phase);

The above values are chosen considering the worst-case situation when the inverter is running under full load condition. The voltage and current ratings of the main switches are to be chosen to be 500 volts peak and 5 amperes r.m.s respectively. It is customary to have at least 10% tolerance with the ratings.

It should be noted that the converter will be designed so that it begins to lose its ZVS ability when operating with less than 40% of the full load current. It is a standard practice not to design a converter to operate with ZVS under very light load conditions (i.e. close to no-load) as the losses created by the auxiliary circuit would exceed the losses that are trying to be saved. When the load dips below the 40% level, the main inverter switches begin to turn on with some voltage across them. It is only when the load is very light, close to no-load, that the main inverter switches turn on with significant voltage across them.

3.4.2 Choice of Inductors L_{S1} and L_{S4}

L_{s1} and L_{s4} should be chosen to satisfy eqn. (3.2), to ensure that the main converter switches turn on with ZVS when the load is at least 40% of full load. They should also be chosen to minimize the reverse recovery losses in the body-diodes of the main switches, such as diode D_4. Reverse recovery losses can be decreased by gradual decrement of current from the diode D_4. However, it's important to have an overview on the reverse recovery phenomenon of diode to make this concept clear.

An ideal diode conducts current only in the forward direction and never in the reverse direction. However, in reality, when a diode is reverse-biased, the stored minority carriers in the device must return to the opposite material. It takes time for the electrons to move from the p-material back to the n-material and the holes to move from the n-material to the p-material. During this time the current flowing through a diode is decreased to zero, and may momentarily become negative before finally becoming zero, as shown in fig. (3.1). This negative current is referred to as reverse-recovery current in the power electronics literature since it flows through the device during the time t_{rr} needed by the diode to "recover" from its previous current conduction state. This reverse-recovery current can lead to power losses in the diode due to the overlap of voltage and current that exists while the diode is recovering. These adverse effects can be significant in high-frequency applications, and thus fast-recovery diodes with short reverse recovery times (t_{rr}) are widely used in high-frequency converters.

Referring to Interval-3 of converter operation, the time in which current is fully diverted from the body-diode, D_4, to the main switch Q_4 is given by eqn. (2.9), which is reproduced here,

$$i_{Ls4}(t_3 - t_2) = -\frac{E}{L_s}.(t_3 - t_2) + i_{Ls4(max)} = 0 \qquad (3.24)$$

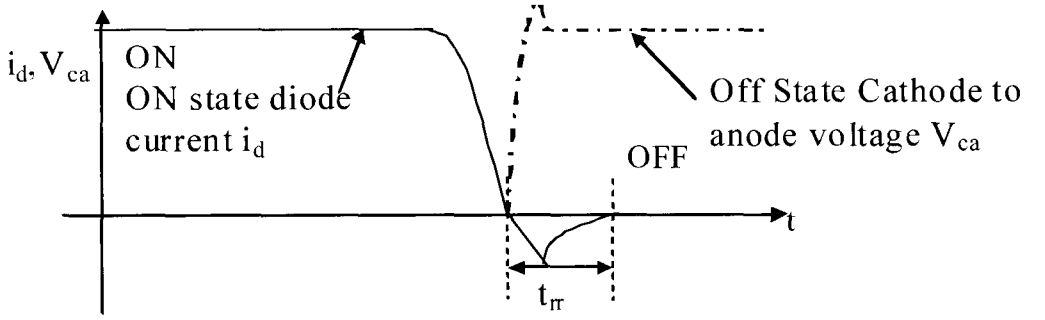


Figure 3.1 Reverse recovery current in a diode.

Rearranging eqn. (3.24) results in

$$(t_3 - t_2) = \frac{i_{Ls4(max)}}{E} L_s \tag{3.25}$$

The duration of this (t_3-t_2) interval of operation given by eqn. (3.25) should be made such so that that it is at least three times greater than the reverse recovery time of the body-diode of a main power switch, (t_3-t_2) > $3t_{rr}$ where t_{rr} is the reverse recovery time for the diode. This will ensure the gradual removal of charge from the diode, and thus the elimination or near elimination of diode reverse recovery current (and thus the losses associated with it).

Substituting t_{rr} into eqn. (3.25) yields

$$(t_3 - t_2) = \frac{i_{Ls4(max)}}{E} L_s > 3t_{rr} \tag{3.26}$$

Rearranging eqn. (3.26) results in

$$i_{Ls4(max)} > \frac{3t_{rr}\,E}{(L_{s1} + L_{s4})} \tag{3.27}$$

From eqn. (3.2) (with the left-hand side of the equation equal to 40% of $i_{Ls4(max)}$) and (3.27), the following expression can be obtained

$$(L_{s1} + L_{s4}) > \frac{(3t_{rr})^2}{2C_4} \tag{3.28}$$

This equation takes into account the ZVS condition (that ZVS occurs when the converter is operating above 40% of full load) and the reverse recovery criterion. If the value of t_{rr} is chosen as *80 nsec* (a typical reverse-recovery time for MOSFET body-diodes), and E = *400 volts*, C_4 = *5nF*, then, from eqn. (3.28),

$$(L_{s1} + L_{s4}) \geq 5.76\,\mu H \tag{3.29}$$

Since $L_{S1} = L_{S4}$,

$$L_{s1} = L_{s4} \geq 2.88\,\mu H \tag{3.30}$$

Based on this condition, a value of $L_{S1} = L_{S4} = 3\,\mu H$ is used. As larger inductor sizes will result in the physical converter circuit becoming more bulky and heavy, so a value near the lower boundary level for ZVS operation has been chosen for L_{S1} and L_{S4}.

3.4.3 Choice of Capacitor C_{s1}

The maximum voltage across the main switch Q_4 is given by

$$V_{Q4\,(max)} = (E + V_{cs1}) + i_{Ls4}\, Z_{eq} \tag{3.31}$$

Substituting eqn. (3.2) into (3.31) results in

$$V_{Q4\,(max)} = E + E\sqrt{\frac{2C_4}{C_{S1}}} \tag{3.32}$$

From eqn. (3.32), it can be seen that if the value of C_{s1} is increased, $V_{Q4\ (max)}$ will decrease. On the other hand as the value of C_{s1} increased, the on-time of the auxiliary switch (t_{aux}) is increased, which results in lower conduction losses. So, to choose an appropriate value for the clamping capacitor (C_{s1}) a trade-off is needed to ensure that the key design objectives that were described in Section 3.4 are satisfied.

To ensure that this happens, it is necessary to have graphs of characteristic curves that show the relationship between the on-time of the auxiliary switch (t_{aux}) and the active-clamp capacitor (C_{s1}), the main switch voltage stress ($V_{Q4(max.)}$) and the active-clamp capacitor (C_{s1}), and the main switch peak current ($I_{Q4(peak)}$) versus the active-clamp capacitor (C_{s1}). Such graphs are shown in Figures 3.2, 3.3, and 3.4 respectively.

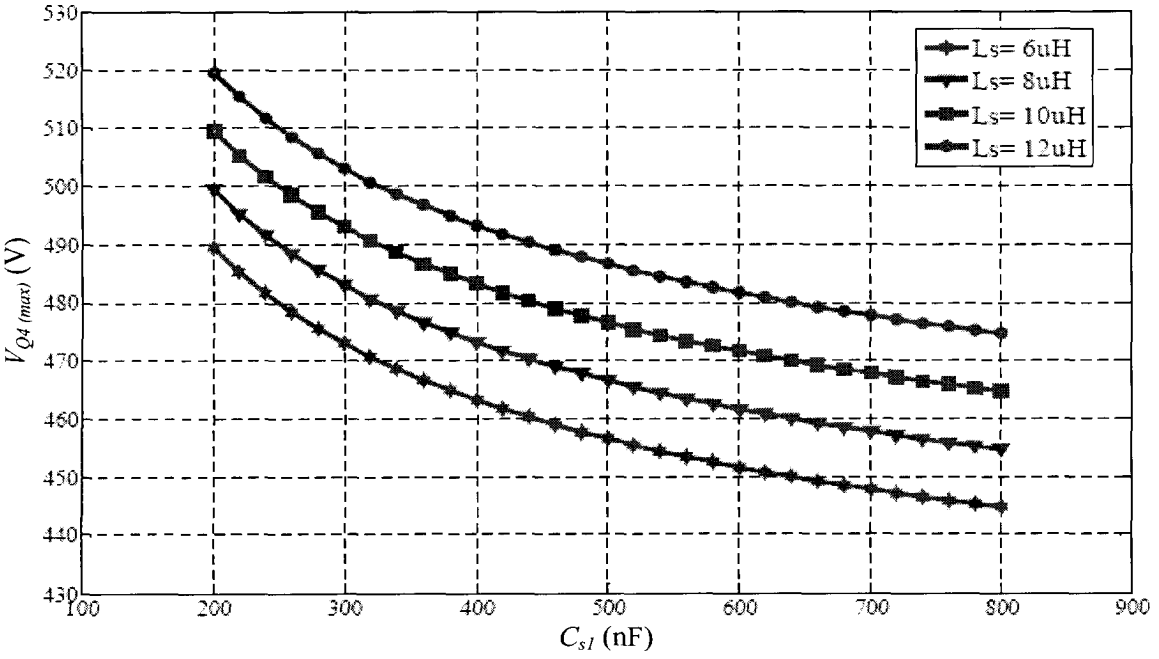


Figure 3.2 Switching stress of switch, Q_4 versus clamping capacitor, C_{s1}

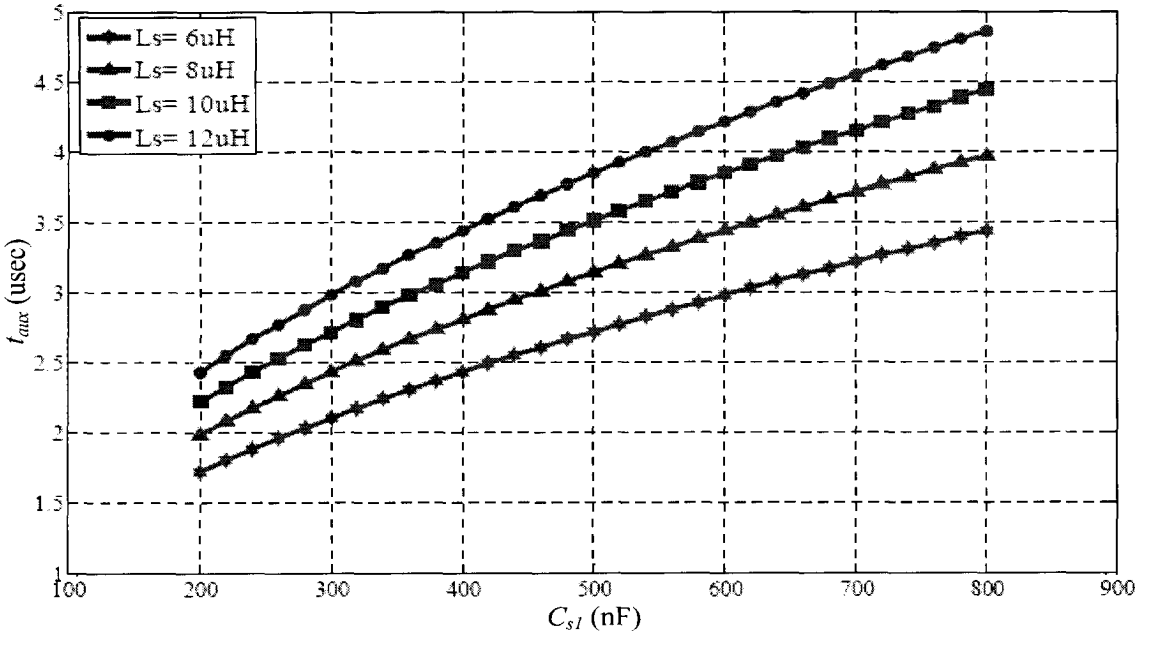


Figure 3.3 On-time of auxiliary switch, Q_{a1} versus clamping capacitor, C_{s1}

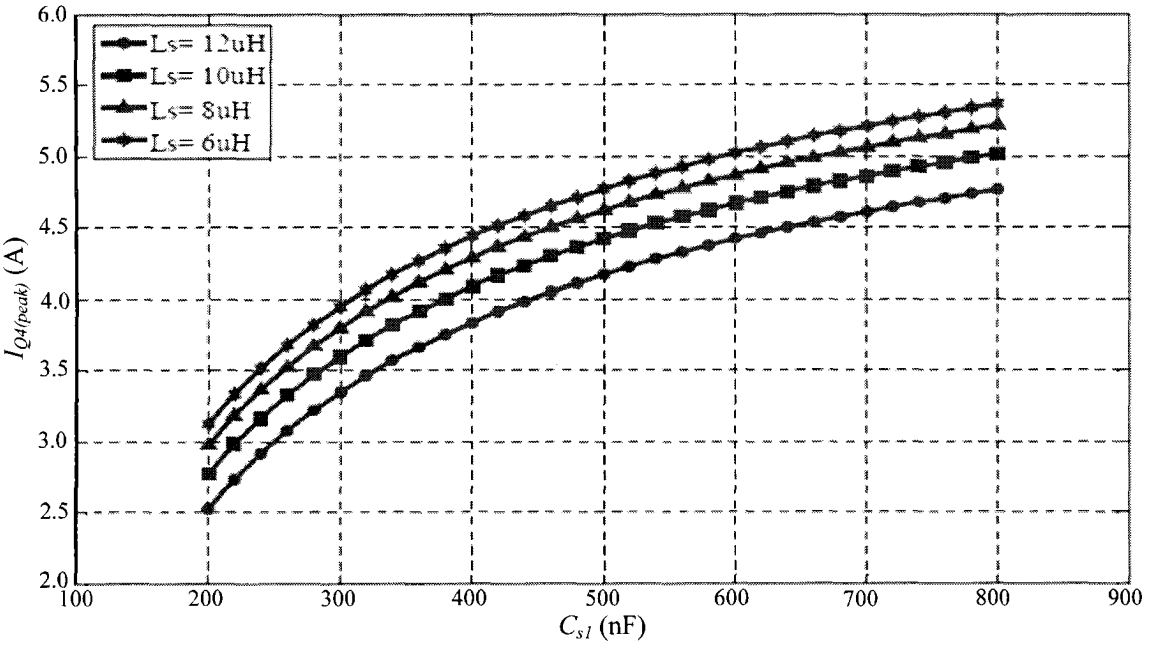


Figure 3.4 Peak current of switch, Q_4 versus clamping capacitor, C_{s1}

From Fig. 3.2 it can be seen that the main switch peak voltage ($V_{Q4(max)}$) is decreased as the clamping capacitor (C_{s1}) value is increased. Moreover, the main switch peak voltage ($V_{Q4(max)}$) is increased as the value of L_S is increased. However, $L_S = 6\ \mu H$ gives the best result to minimize the main switch voltage stress. If the clamping capacitor value is chosen within *500 nF* to 600 *nF* with $L_S = 6\ \mu H$, then the main switch peak voltage is within the 10% tolerance level; whereas $L_S = 8\mu H$, $L_S = 10\ \mu H$, *and* $L_S = 12\ \mu H$ would not be good choices as they are more likely to result in main switch peak voltage that are not within the 10% tolerance level.

From Fig. 3.3, it can be seen that the on-time of auxiliary switch, Q_{a1} is increased as the clamping capacitor (C_{s1}) value is increased. Moreover, the on-time of auxiliary switch, Q_{a1} is increased as the value of L_S is increased. If the clamping capacitor value is chosen within *500 nF* to 600 *nF* with $L_S = 6\ \mu H$, then the on-time of auxiliary switch is just 2.5 μsec to 3 μsec which is considerably low to minimize the conduction losses in the auxiliary switch and also to maintain all the condition for ZVS operation. A clamping capacitor value within *500 nF* to 600 *nF* with $L_S = 6\ \mu H$ also results in a low on-time for the auxiliary switch.

In Fig. 3.4, it can be seen that the peak-current of the main switch ($I_{Q4(peak)}$) is increased as the clamping capacitor (C_{s1}) value is increased. Moreover, the peak current of the main switch ($I_{Q4(peak)}$) is decreased as the value of L_S is increased, and thus a trade-off between switch voltage stress may need to be considered. However, if a clamping capacitor value is chosen within *500 nF* to 600 *nF*, the peak-current does not vary that much for various values of L_s. A clamping capacitor value of 500 *nF* is, therefore, an appropriate value for the converter that will fulfill the design objectives stated in Section 3.4.

3.5 Conclusion

In this chapter, an analysis of the proposed inverter, related to its ZVS operation, was presented. The results of the analysis were used as part of a design procedure to ensure that the main converter switches operate with ZVS. The design procedure was demonstrated with an example that showed how the value of certain key components can be selected.

Chapter 4
Simulation Results

4.1 Introduction

In the previous chapter of this thesis, it was shown how certain key components related to the auxiliary circuits of the proposed converter can be selected so that the inverter switches can operate with ZVS. In this chapter, results obtained from computer simulation that demonstrate the feasibility of the proposed inverter with the component values that were selected in the previous chapter are presented. PSIM, a recognized commercially available power electronics simulation software package, is used to perform the simulation. Simulations were performed for different load operating conditions to see if the inverter can maintain its ZVS ability as predicted or if over consideration need to be taken into account in the design of the inverter.

4.2 Simulation Results

Simulations were carried out to verify the feasibility of the proposed inverter. At first, the inverter was simulated with 100% load and the following specifications: Bus voltage $E = 400\ V$, output power $P_0 = 1500\ VA$, switching frequency $f_s = 25\ kHz$. After that, the inverter was simulated with 50% load and 30% load respectively. For all the load conditions, the inverter was implemented with the following parameters that were determined in the previous chapter: $L_{s1} = L_{s4} = L_{s3} = L_{s6} = 3\ \mu H$, $C_{s1} = C_{s2} = 500\ nF$, $L = 100\ \mu H$, $R = 30ohm$.

Figure 4.1 to Figure 4.6 show the simulation results that were done for 100% load. Figure 4.1 shows the voltage and current waveforms of the main switch Q_1. From the figure it can be seen that the switch Q_1 turns on with ZVS - that the current is following through the body diode of Q_1 when the switch is supposed to be turned on. As a result, the voltage across the switch is zero when it is about to be turned on and thus it can turn on with ZVS. Figure 4.2 to Figure 4.6 show the voltage and current waveforms of switches Q_4, Q_3, Q_6, Q_{a1}, and Q_{a2} respectively. In all these cases, the switches are turned on with ZVS, which confirms the inverter's ability to operate with all its switches turning on with ZVS.

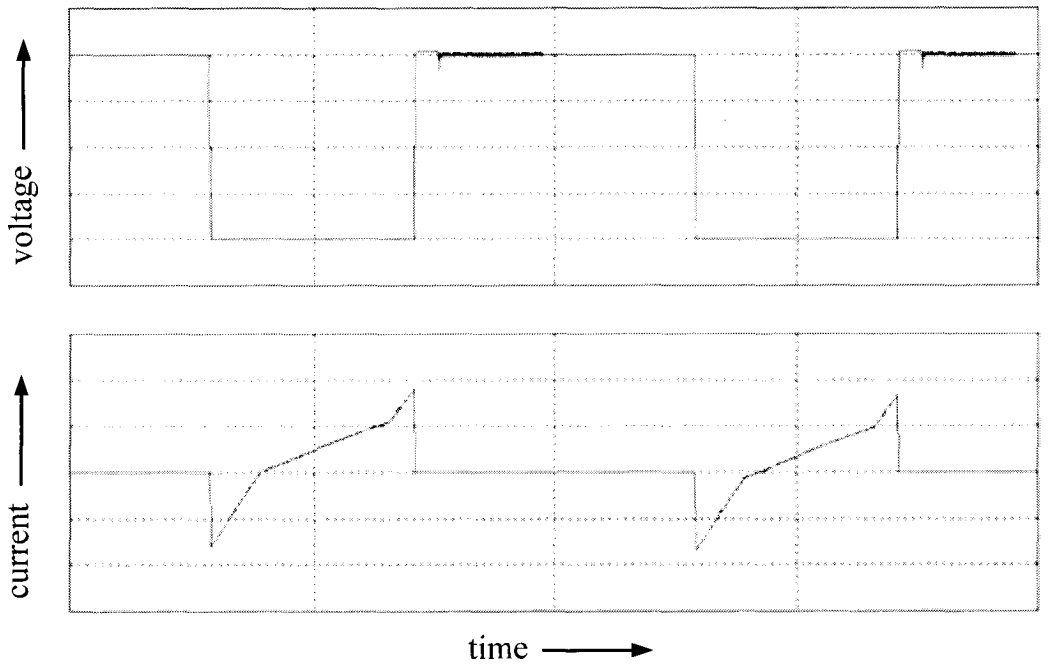


Figure 4.1. Voltage and current wave forms of switch, Q_1 (100 V/div, 3 A/div, 4μs/div)

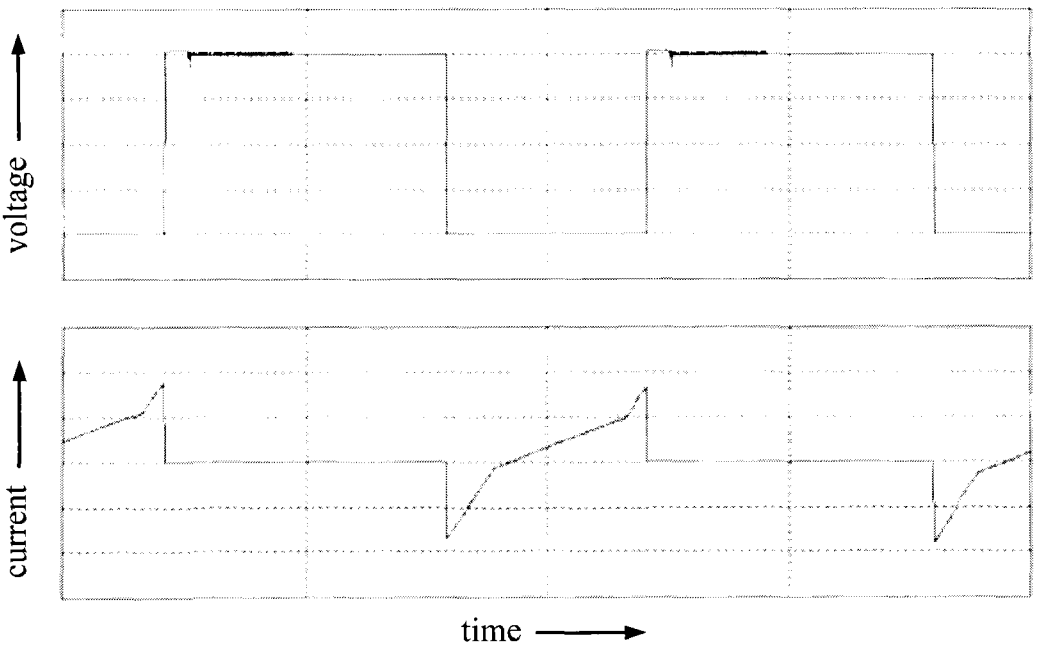


Figure 4.2. Voltage and current wave forms of switch, Q_4 (100 V/div, 3 A/div, 4μs/div)

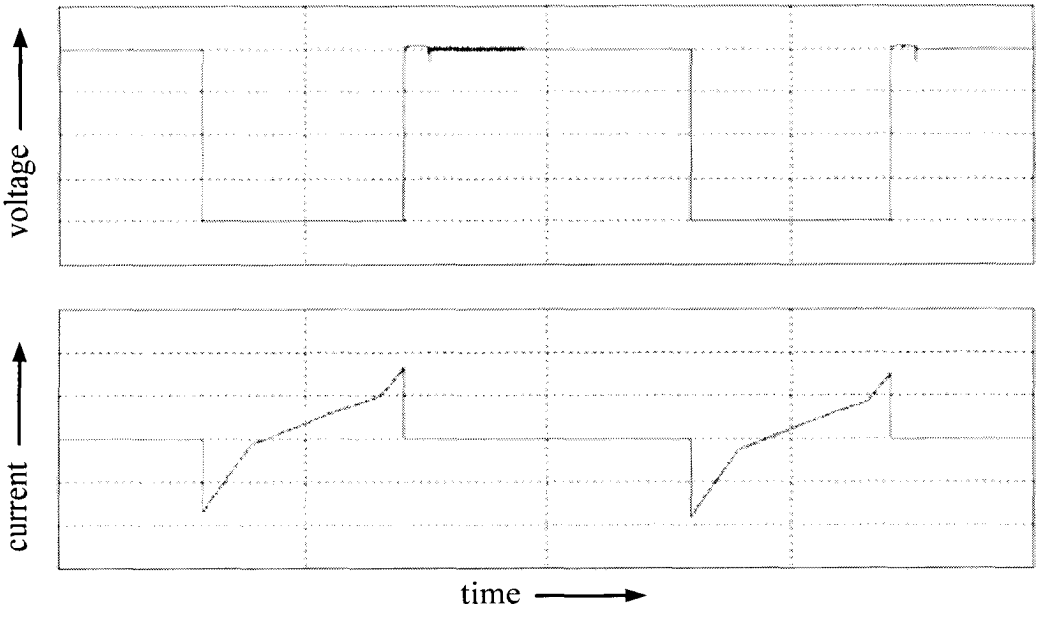


Figure 4.3. Voltage and current wave forms of switch, Q_3 (100 V/div, 3 A/div, 4μs/div)

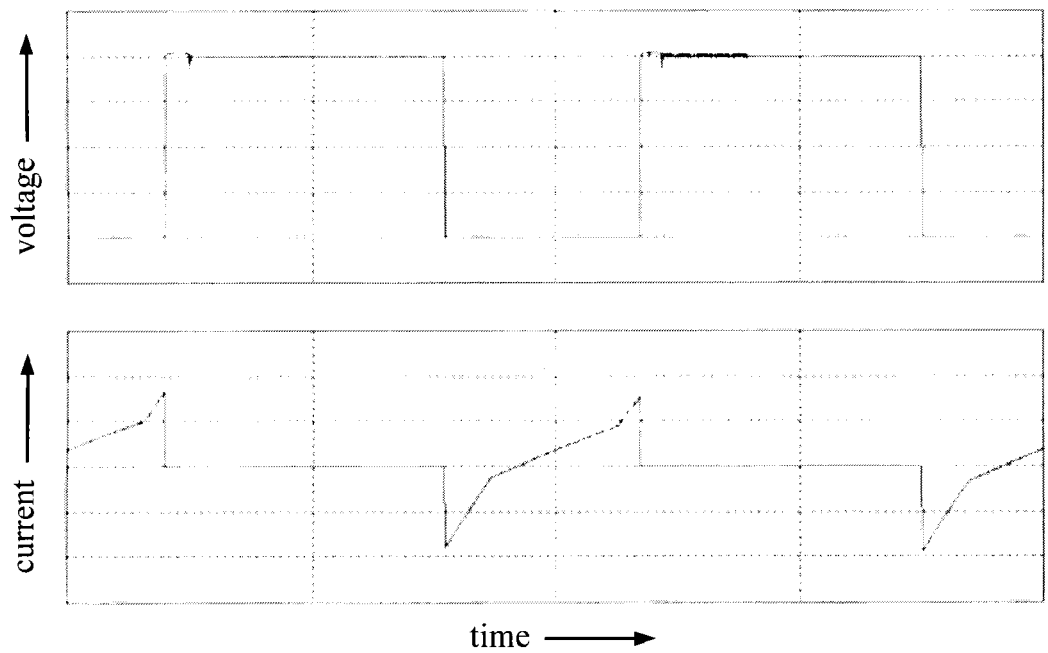


Figure 4.4. Voltage and current wave forms of switch, Q_6 (100 V/div, 3 A/div, 4μs/div)

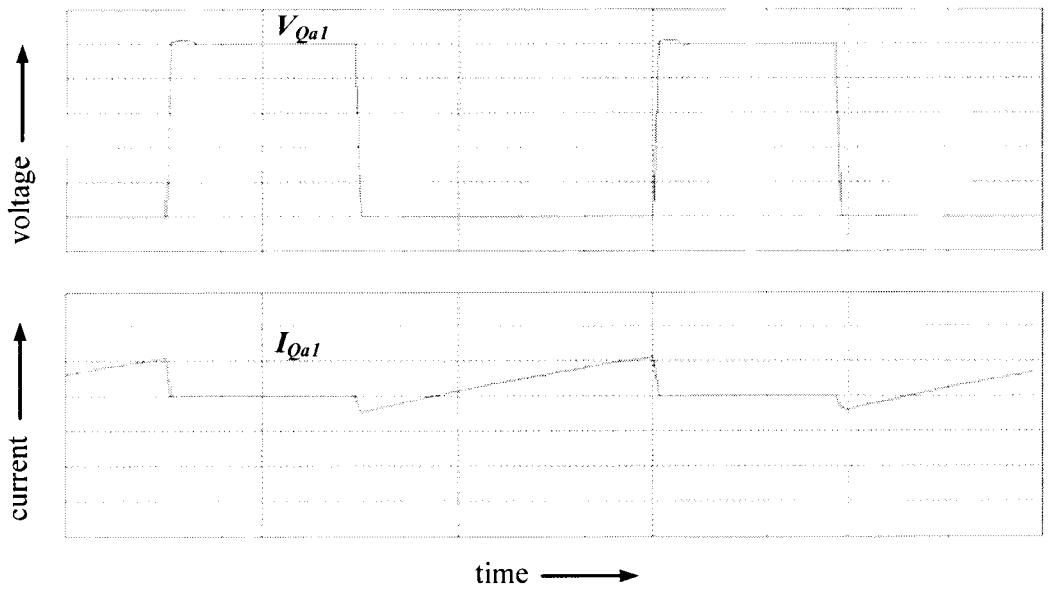


Figure 4.5. Voltage and current wave forms of switch, Q_{a1} (20 V/div, 4 A/div, 8μs/div)

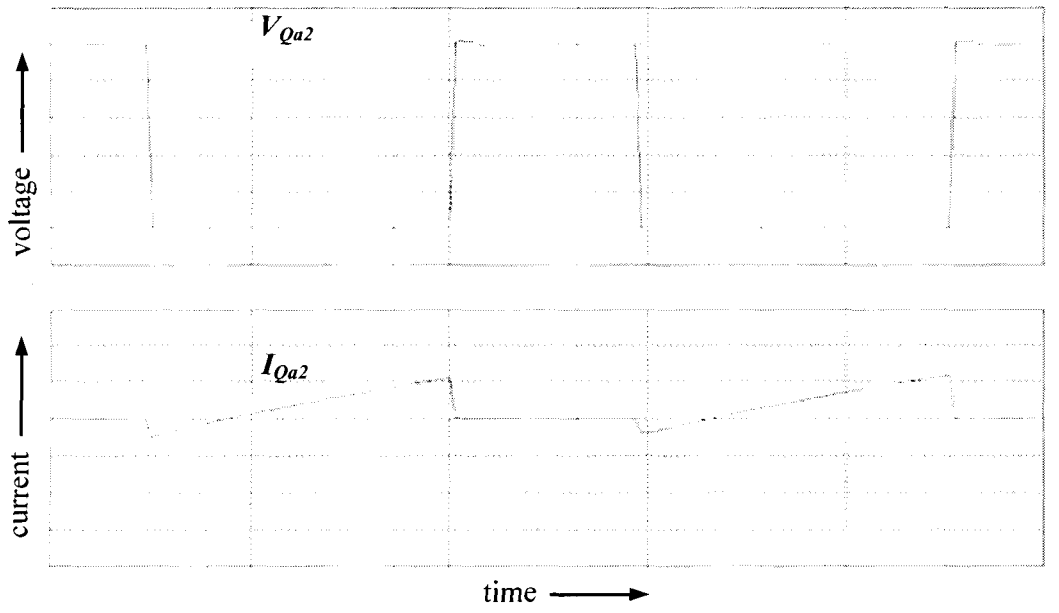


Figure 4.6. Voltage and current wave forms of switch, Q_{a2} (20 V/div, 4 A/div, 8μs/div)

Figure 4.7 to Figure 4.10 show simulation results for the main inverter switches for the case when the inverter is operating with 50% load, and Figure 4.11 to Figure 4.14 show simulation results for the main inverter switches for the case when the inverter is operating with 30% load. When these two sets of results are compared to those shown in Figure 4.1 to Figure 4.4, it can be seen that the negative current through the main switches, which is an indication of ZVS operation, is largest for the case when the inverter is operating with 100% load and non-existent for the case when the inverter is operating with 30% load.

When the converter is operating with 30% load, the inverter switches do not have the ability to turn on with ZVS, and thus turn on with switching losses. This is consistent with

the way that the inverter was designed in Chapter 3 to allow the main inverter switches to operate with ZVS as long as the load is greater than 40% of full load. As can be seen from the simulation results, the inverter switches can operate with ZVS at 50% load, but not at 30% load. This confirms the validity of the design procedure.

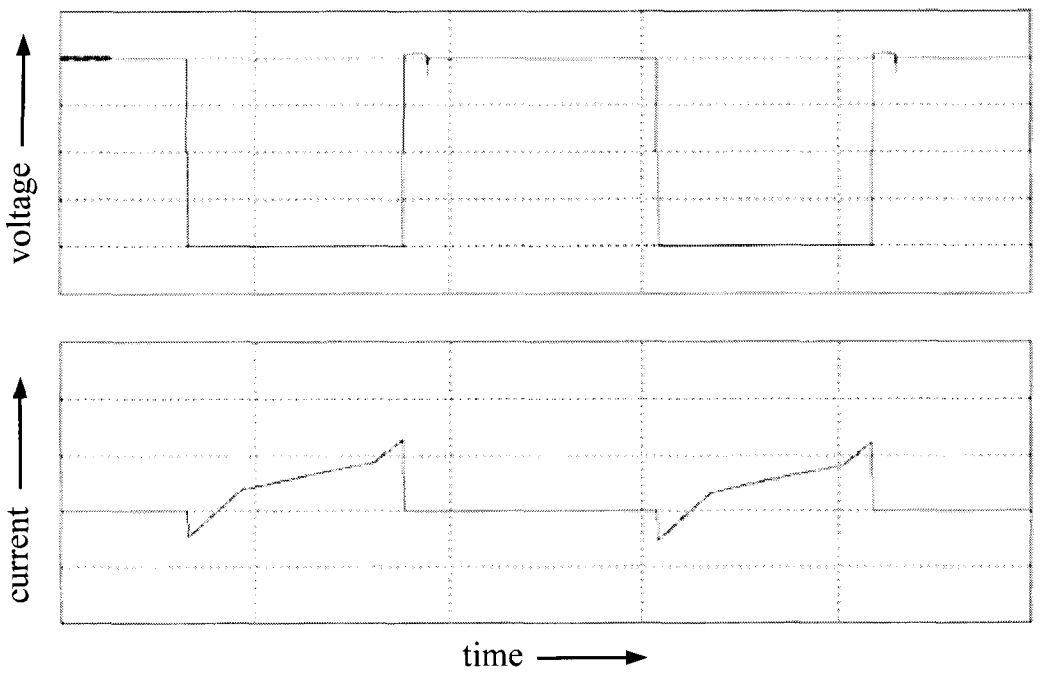


Figure 4.7. Voltage and current wave forms of switch, Q_1 (100 V/div, 3 A/div, 4μs/div)

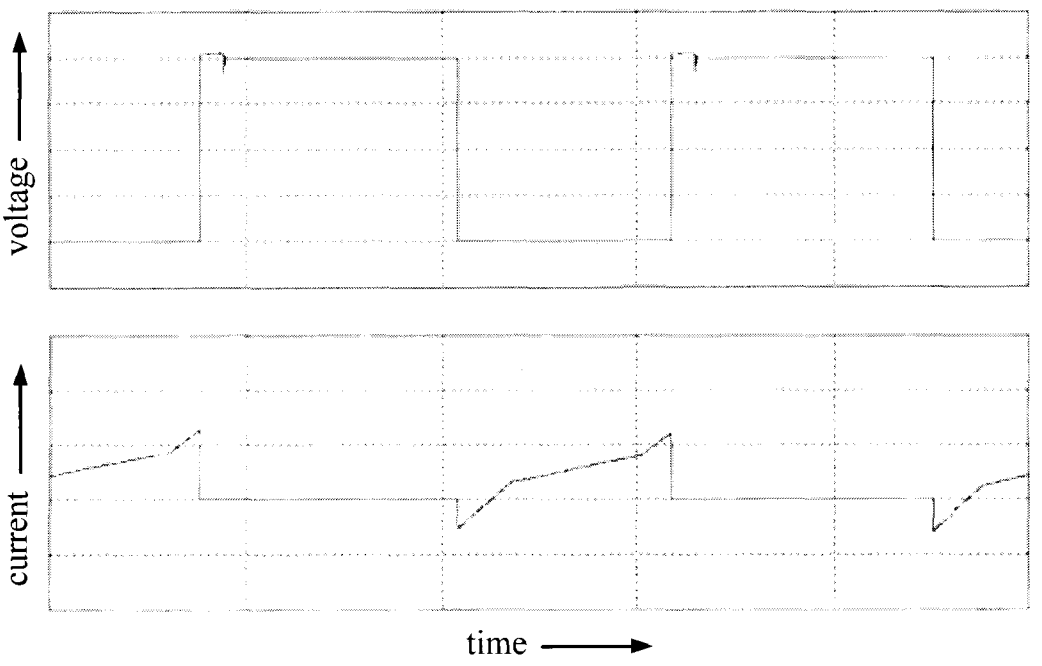


Figure 4.8. Voltage and current wave forms of switch, Q_4 (100 V/div, 3 A/div, 4μs/div)

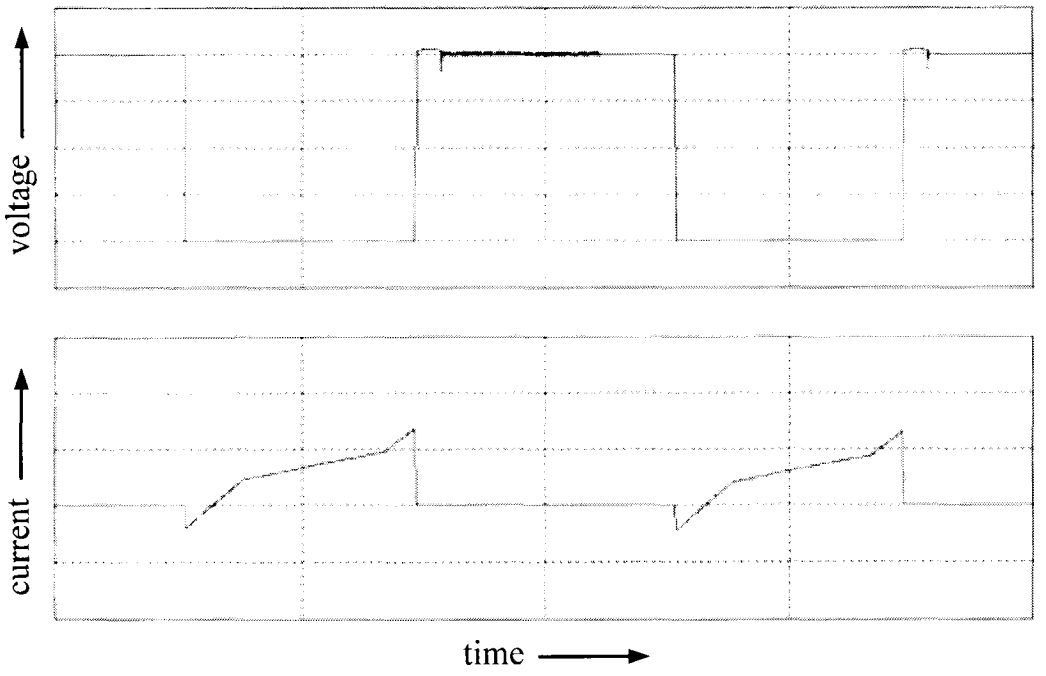


Figure 4.9. Voltage and current wave forms of switch, Q_3 (100 V/div, 3 A/div, 4μs/div)

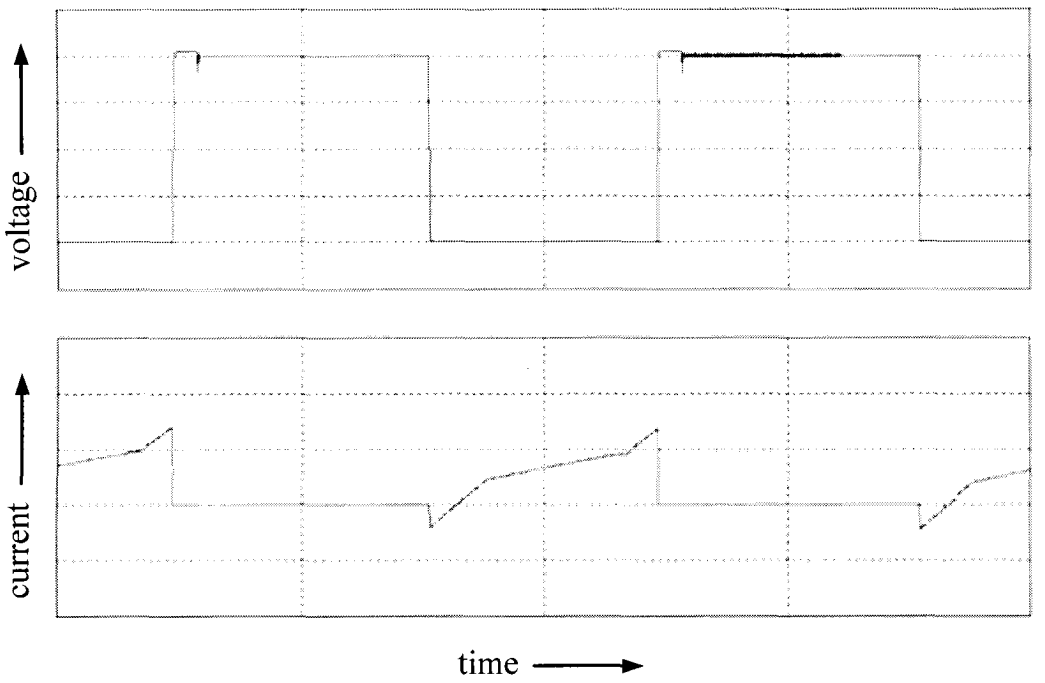


Figure 4.10. Voltage and current wave forms of switch, Q_6 (100 V/div, 3 A/div, 4μs/div)

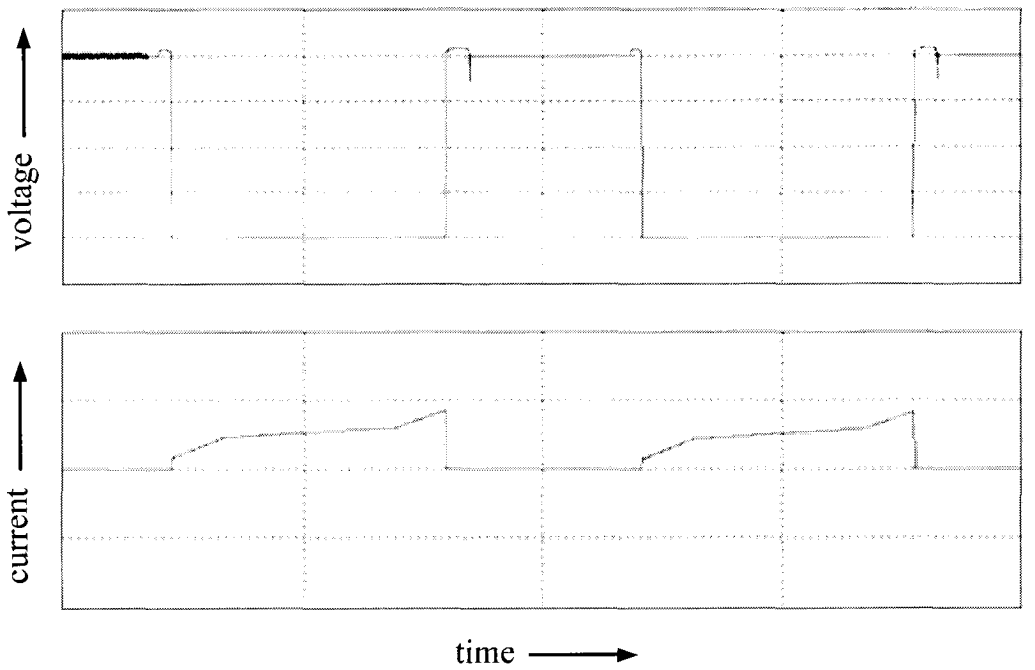


Figure 4.11. Voltage and current wave forms of switch, Q_1 (100 V/div, 3 A/div, 4μs/div)

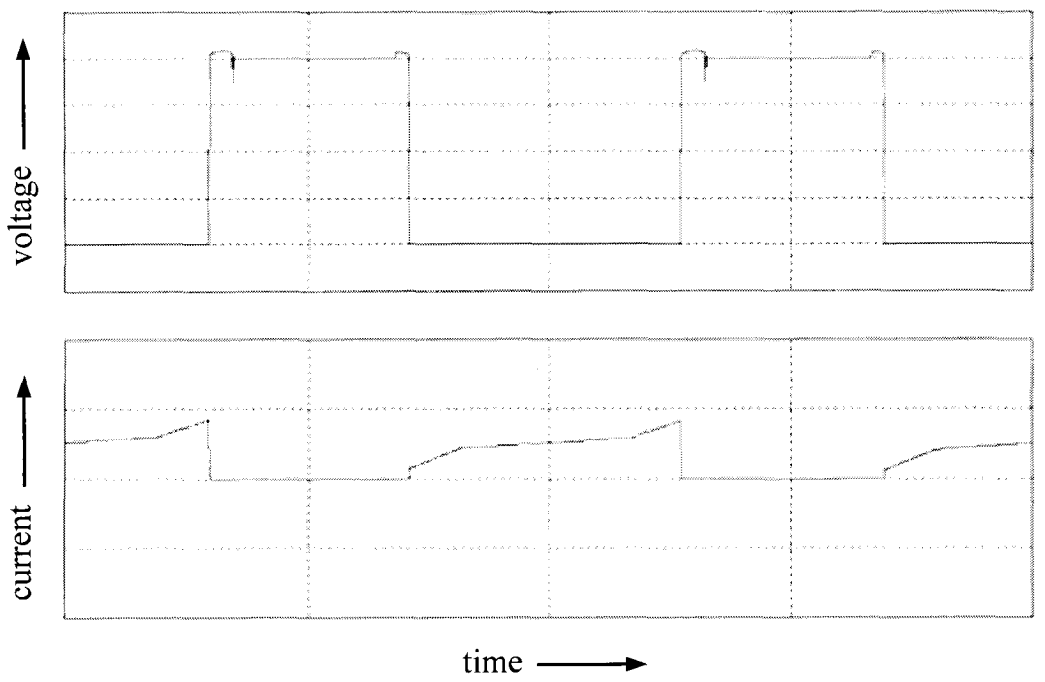


Figure 4.12. Voltage and current wave forms of switch, Q_4 (100 V/div, 3 A/div, 4μs/div)

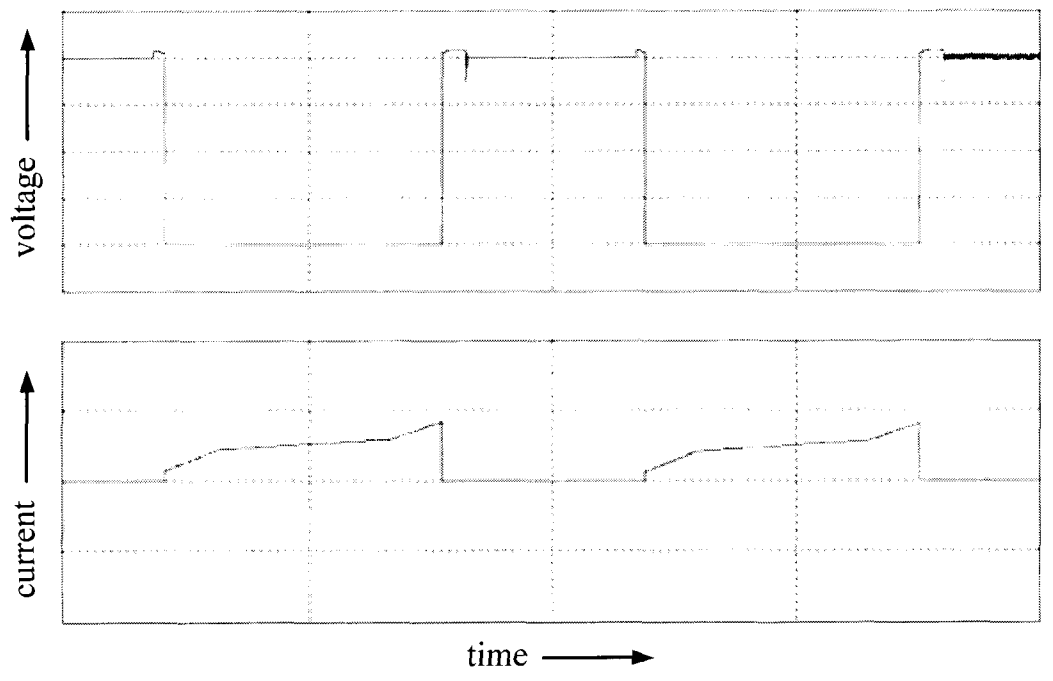


Figure 4.13. Voltage and current wave forms of switch, Q_3 (100 V/div, 3 A/div, 4μs/div)

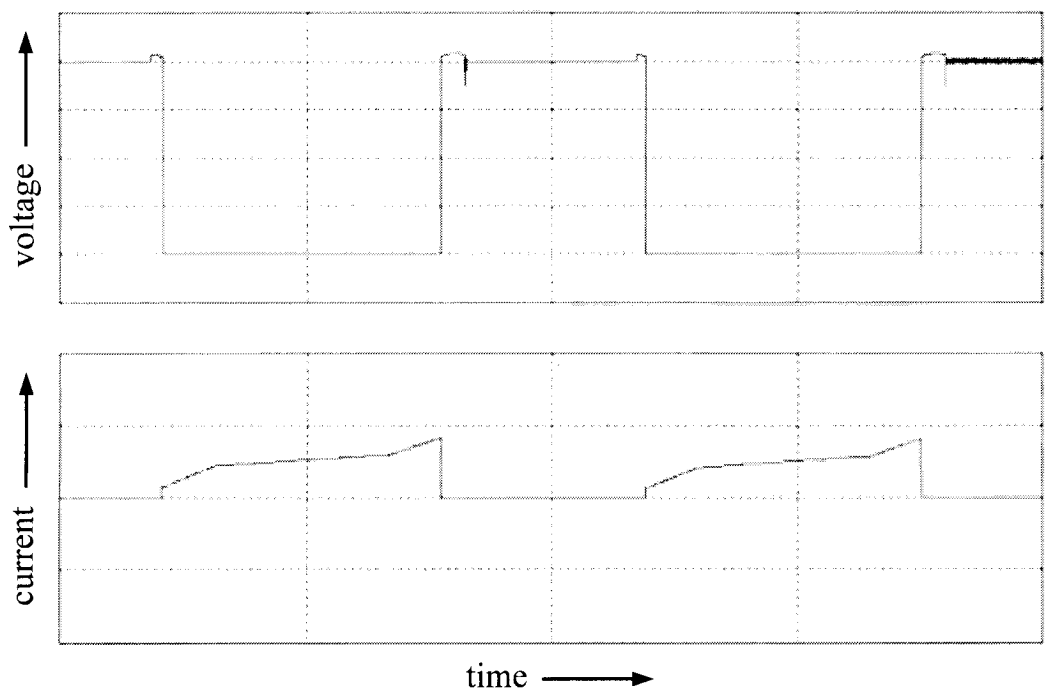


Figure 4.14. Voltage and current wave forms of switch, Q_6 (100 V/div, 3 A/div, 4μs/div)

Figure 4.15 shows the three-phase output voltage of the proposed inverter. It can be seen that the presence of an auxiliary circuit in each inverter leg does not interfere with the inverter's ability to produce a balanced three-phase output voltage like a conventional three-phase inverter.

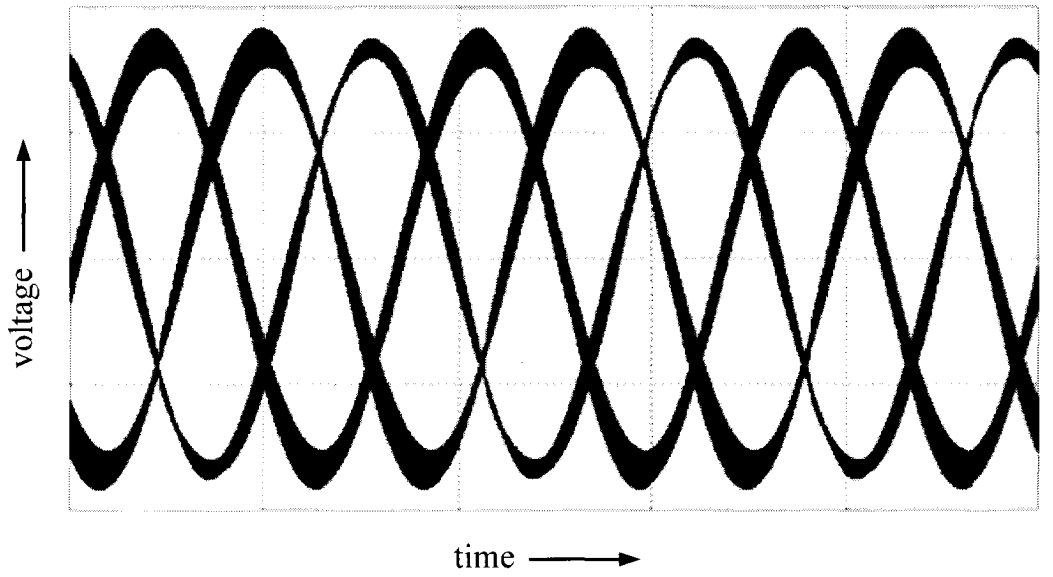


Figure 4.15. Three-phase output voltage (100 V/div, 10 ms/div)

Figure 4.16 shows simulation results of the current through the inductors L_{s1} and L_{s4} when the converter is operating with 100% load. Since the currents through these inductors are critical parameters in the design of the inverter auxiliary circuits, which are the "mechanism" that helps the inverter switches to operate with ZVS, and since the design of the auxiliary circuit is based in part on the Interval equations that were derived in Chapter 2, a test was made to confirm the validity of these equations. This test involved writing a MATLAB program (Appendix-A) that used the necessary Interval equations to generate real-time graphs of the currents in inductors L_{s1} and L_{s4}, as shown in Figure 4.17, so that the validity of the equations can be confirmed against the PSIM simulation results. It can be seen that there is a close match between the PSIM results of Figure 4.16 and the MATLAB results of Figure 4.17.

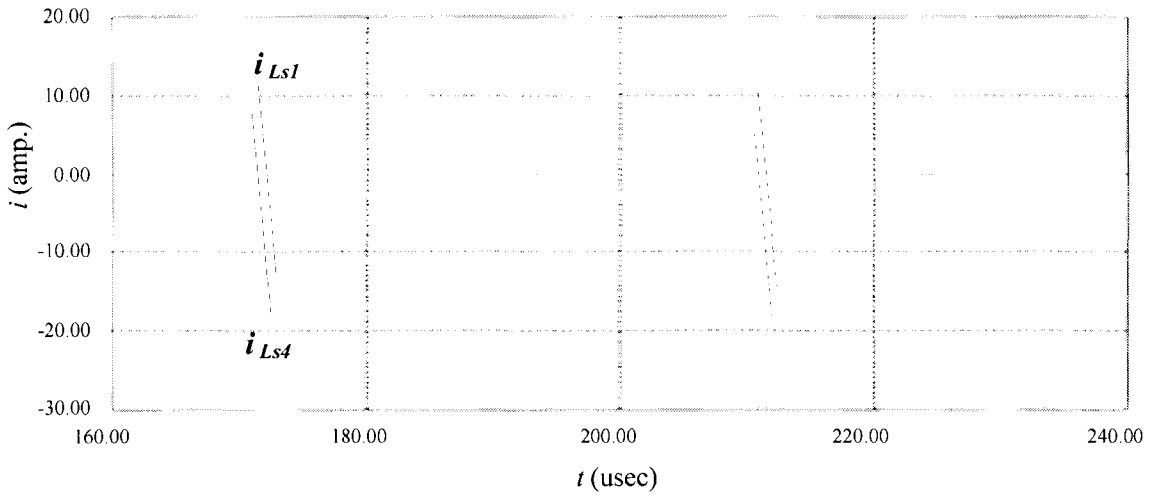


Figure 4.16. Current through L_{s1} and L_{s4} (in PSIM)

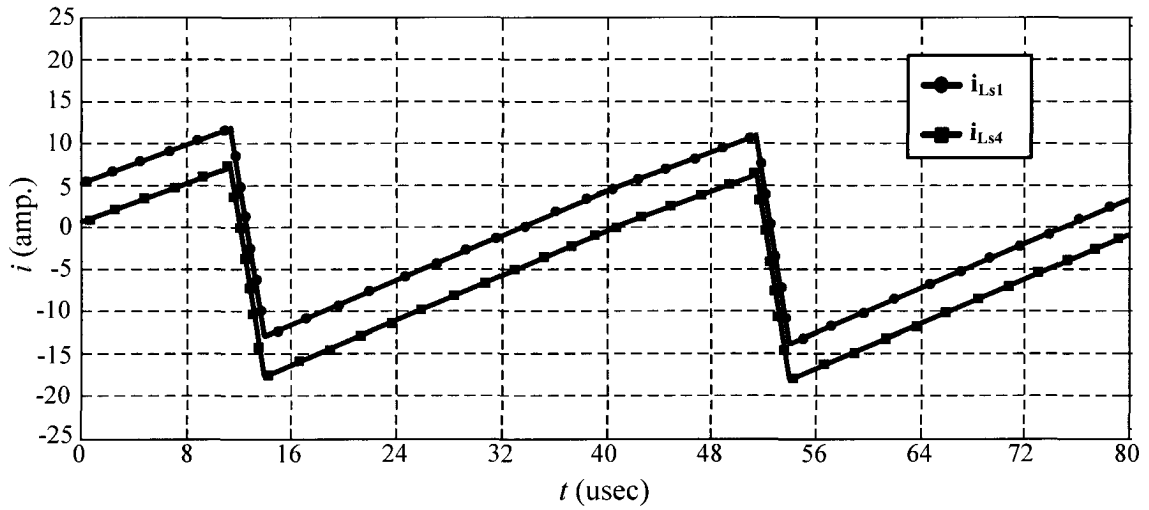


Figure 4.17. Current through L_{s1} and L_{s4} (in MATLAB)

In order to further validate the Interval equation that were derived in Chapter 2, a comparison of the peak voltage stress of the main inverter switches obtained using the MATLAB program and that obtained by simulation using PSIM was made for the case

when the inverter was operating with 100% load current. The comparison is shown in Table 4.1. It can be seen that there is a close match between the two sets of results.

Switch	Analytical Switching Stress	Simulated Switching Stress
Q_1	456.57 V	458.50V
Q_4	456.57 V	462.70V
Q_3	456.57 V	461.25V
Q_6	456.57 V	460.75V

Table 4.1. Switching Stress

4.3 Conclusion

In this chapter, the operation of the proposed inverter was examined using PSIM, a recognized commercially available power electronics software package. The results obtained from the simulation confirmed the feasibility of the proposed inverter. Based on these results, observations were made as well as a comparison between the simulated and analytical results. The simulated and analytical results were found to be in good agreement.

Chapter 5
Conclusion

5.1. Summary

Dc-ac inverters convert a dc input voltage into a desired ac output voltage and are widely used in many industrial applications, including utility grid interfaces, motor drives, and wind energy systems. Because of their widespread use, there has been considerable interest to try to make them more efficient to conserve energy. One way of doing so is to reduce the losses that are generated by the switching of the inverter devices as they help convert the dc input voltage into an ac output. As a result, there has been considerable research into implementing inverters with so-called soft-switching - zero-voltage and zero-current switching techniques that make either the voltage across a switch or the current through it zero at the time of a switching transition (from on to off or off to on). Since the power dissipated in a switch is related to the amount of overlap of voltage and current during a switching transition, making either the switch voltage or switch current zero at this time can result in a significant reduction in switching losses.

The focus of this thesis has been on a new, reduced switch, zero-voltage switching (ZVS), three-phase dc-ac inverter. The proposed inverter has the following attractive features:

- It has most of the benefits of conventional three-phase inverter, but at a reduced cost as it has four main power switches instead of six.

- The main inverter switches turn on with ZVS with the help of an auxiliary circuit in each leg, and turn off with ZVS due to the presence of a capacitor across each switch.
- The switch in each auxiliary circuit also operates with ZVS.
- Since the auxiliary circuit operates for a small fraction of a switching cycle, the device that is used for the auxiliary switch can be a smaller, lower power rated, cheaper device than a main inverter switch device.
- The auxiliary circuits that are connected to each inverter leg do not interfere with the inverter's ability to produce a sinusoidal three-phase output voltage.
- The inverter can also operate with ZVS even if it is operated as a rectifier (ac-dc converter), which makes it very useful for applications that require a bidirectional power flow.

In this thesis, an extensive literature review of previously proposed soft-switched inverters was performed in Chapter 1 and the strengths and weaknesses of each type were stated. The new inverter was then presented in Chapter 2 and its operation was explained in detail. A PWM method was reviewed to show how a reduced switch inverter can produce three-phase sinusoidal output waveform, and how the use of an auxiliary circuit in each of the two converter legs with switches allows these switches to turn on with ZVS. Since auxiliary circuits are placed at the inverter leg instead of at the dc bus, as is the case with many previously proposed ZVS inverters, the proposed inverter can also operate as a ZVS rectifier if needed.

The steady-state operation of the new inverter was analyzed in Chapter 3. As a result of the analysis, the boundary for ZVS operation was determined and graphs of key steady-state characteristic curves were generated. The graphs provided insight as to the relations between certain key parameters and were used as a part of a design procedure that was demonstrated with an example.

The feasibility of the proposed converter was confirmed in Chapter 4 with simulation results obtained from PSIM, a widely used, commercially available software simulation package for power electronics. It was shown that the inverter switches can operate with ZVS under various load conditions while providing sinusoidal three-phase ac output voltages. The validity of the analysis in Chapter 3 and the interval equations in Chapter 2 were confirmed by comparing results obtained from PSIM with analytical results obtained from a MATLAB program. The MATLAB program was based on the analysis that was performed in Chapters 2 and 3 and generated auxiliary circuit waveforms that closely matched those obtained from PSIM.

5.2. Conclusions

The following can be concluded based on the work that was done in this thesis:

- It is possible to model the ZVS operation of the converter in a well-defined manner so that its steady-state characteristics can be accurately determined and used in its design.

- The operation of the auxiliary circuits will not interfere with the inverter's ability to produce a three-phase sinusoidal output voltage as long as the auxiliary circuits operate for only a fraction of the switching cycle of the inverter.
- A number of trade-offs or compromises must be considered in the design of the auxiliary circuit. The most significant of these include a compromise between the length of auxiliary circuit operation time and the ability of the inverter switches to operate with ZVS and the length of auxiliary circuit operation time and the peak voltage stresses of the inverter switches.

5.3. Contributions

The following are the main contributions of this thesis to the power electronics literature:

- A new three-phase reduced switch ZVS-PWM inverter was presented in this thesis. The new converter has many attractive features, as listed above.
- The ZVS operation of the inverter was analyzed so that the steady-state characteristics of the converter were established. This allows for a solid understanding of the operation of the inverter.
- A design procedure that can be used in the selection of key inverter components was presented. The procedure can be used to ensure that the main inverter switches turn on with ZVS.
- The feasibility of the converter and the validity of the analysis were confirmed with simulation results. This confirmation proved that the inverter can be used in practical applications.

5.4. Future Work

The main future work that needs to be considered is experimental work. The simulation work confirmed the feasibility and operation of the converter, but an experimental prototype needs to be built to further confirm converter operation. Given the work that has been done for this thesis (especially the analytical and simulation work), there is little doubt that the proposed inverter will actually "work", but experimental work is needed to establish how well the inverter will do so.

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Appendix A

Flowchart of program to generate real-time graphs of the currents in inductors L_{s1} and L_{s4}

The flowchart program is done based on the interval equations that were derived in Chapter 2 to confirm the validity of these equations. The flowchart is shown in fig. A.1. The program is done assuming the initial condition of i_{Ls4} is equal to zero (refer to fig. 2.7). In the first Interval a loop is run with changing the value of t according to eqn. 2.1 as long as it touched the maximum value of i_{Ls4} (refer to eqn. 3.2).

In Interval-2 (with initial condition $i_{Ls4} = i_{Ls4(max)}$) the maximum value of i_{Ls4} holds (with changing the value of t) as long as the output of eqn. 2.5 come to zero (refer to fig. 2.7). In Interval-3 (with initial condition $i_{Ls4} = i_{Ls4(max)}$ and $v_{C4} = 0$) a loop is run with changing the value of t according to eqn. 2.9 as long as the output of eqn. 2.9 come to zero (refer to fig. 2.7). In Interval-4 (with initial condition $i_{Ls4} = 0$) a loop is run with changing the value of t according to eqn. 2.10 as long as it touched the minimum value of i_{Ls1}(refer to eqn. 3.2). In Interval-5 (with initial condition $i_{Ls1} = i_{Ls1(min)}$) a loop is run with changing the value of t according to eqn. 2.13 as long as the output of eqn. 2.13 come to zero (refer to fig. 2.7).

In Interval-6 (with initial condition $v_{CA1} = 0$) a loop is run with changing the value of t according to eqn. 2.16 as long as the output of eqn. 2.16 come to zero (refer to fig. 2.7). In Interval 7,8 and 9 (with initial condition $i_{Ls1} = 0$) a loop is run with changing the value of t according to eqn. 2.26 as long as the output of eqn. 2.26 come to zero (refer to fig. 2.7).

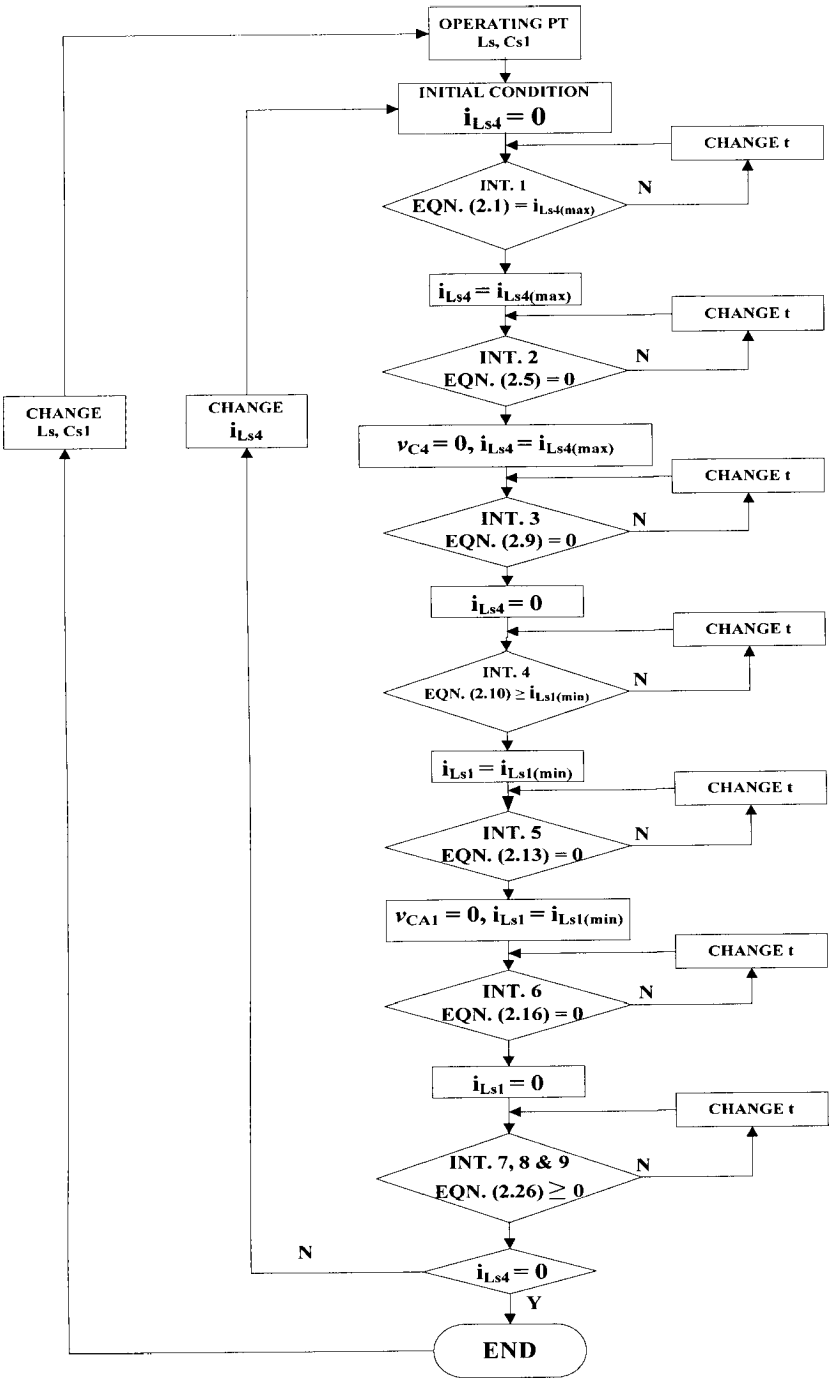

Figure A.1. Flowchart of program to generate real-time graphs of the currents in inductors L_{s1} and L_{s4}