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Breakdown transients in high-k multilayered MOS stacks: role of the oxide-oxide thermal boundary resistance

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In this work, breakdown transients of multilayered gate oxide stacks were analyzed to study the impact of the interfaces between oxides on the heat dissipation considering an electromigration-based progressive breakdown model. Using two distinct measurement setups on four different sets of samples, featuring two layers and three layers of Al_2O_3 and HfO_2 interspersed, the breakdown transients were captured and characterized in terms of the degradation rate. Experimental results show that the number of oxide-oxide interfaces present in the multilayered stack has no visible impact on the breakdown growth rate among our samples. This strongly supports the interpretation of the bulk materials dominating the heat transfer to the surroundings of a fully formed conductive filament that shows no electrical differences between our various multilayered stack configurations.

I. INTRODUCTION

Over the last 50 years, advances in the Silicon (Si) industry have led to a process of miniaturization of the electronic devices that is not yet finished. Such a downscaling trend is of vital importance for the nanoelectronics industry, and in order to keep it going, the search for new materials capable of overcoming the limitations of the Si/SiO_2 system is currently on the spotlight[1,2]. It is in this context that innovative materials such as high dielectric constant (high-k, HK) insulators have been intensively studied as an alternative to the Si/SiO_2 system and represent the starting point in the development of more complex, multi-layered oxides in current and future integration technologies[3,4].

For Metal-Oxide-Semiconductor (MOS) devices under nominal operation (a regime of low voltage and high electric fields) the wear out process of the thin dielectric leads to the so called time dependent dielectric breakdown (BD)[5]. Such a phenomenon results in a loss of performance or even the catastrophic failure of the device. Therefore, to make reliable predictions over the device lifetime that meet the industry standards, the BD dynamics must be well understood. In this regard, several authors have focused on the BD statistics of the modern metal gate (MG)/HK/SiO_X/Si stacks from a defect centered perspective[6–9], and it is also known that progressive BD (PBD) is the main BD phenomenon in nanofilms ($< 50\ nm$)[10].

Micro-structural damage within the MOS stack has been observed during the PBD regime. Such damages consist in the creation of one or multiple conductive filaments (CF) as a consequence of the migration of Si atoms from the bulk of the stack, or metallic ions coming from the metal gate, as suggested by electron microscopy studies on the BD spot[8,11,12].

Recent papers studied the heat dissipation in resistive switching devices after the electroforming of CF indicating that the heat produced by carrier energy loss is dissipated mostly at the interfaces of the CF where the electron transport in and out of the filament is limited by an energy barrier[13–16].

Therefore the phenomenology of the heat dissipation in nano-scaled structures is well defined and experimentally assessed for a variety of different materials. Nevertheless the role of the involved interfaces in the PBD growth remains unclear. In order to gain a better understanding of such mechanism, in this paper we investigate the energy transfer from the BD path to its surroundings in multi-layered MOS stacks with different interlayer interfaces. We considered MOS stacks consisting of two and three alternating layers of Aluminium oxide (Al_2O_3) and Hafnium dioxide (HfO_2) and evaluated their impact on the heat dissipation by measuring the growth rate of the PBD.

II. EXPERIMENTAL

The samples under study are illustrated on Figure 1. These are MOS capacitors fabricated on a highly dopped ($\rho = 7-13\ m\Omega\ cm$) n-type (100) Czochralski Silicon substrate, and toped with 200 nm Ni electrode deposited by magnetron sputtering. For the insulating layer we considered a multilayered stack of two compounds, Al_2O_3 and HfO_2 (grown by atomic layer deposition) structured in four different ways. This selection of materials aims to combine the benefits of each oxide: Al_2O_3 is widely known to have a wide band oxide thus ensuring low leakage currents, whereas HfO_2 has a high dielectric constant that allows high capacitance per unit area.

Sample A is formed by a 10 nm Al_2O_3 layer next to

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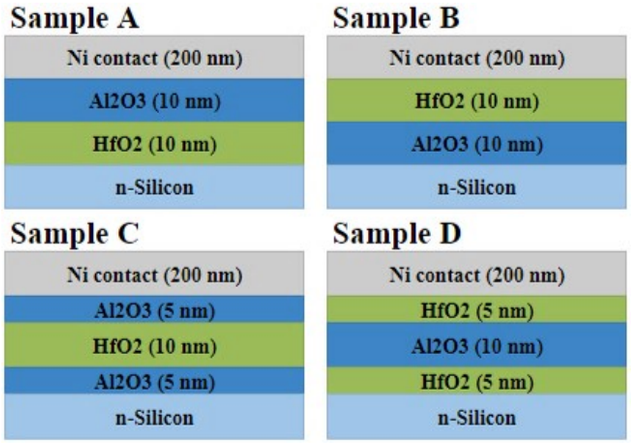

FIG. 1. Representation of the samples used. The multilayered oxide stack is composed of combinations of HfO_2 and Al_2O_3. The total oxide thickness remains constant for all the samples: 20 nm. Figure is not to scale.

the Ni contact, followed by a 10 nm HfO_2 layer. Sample B is similar, with inverted oxide stack order. These two samples present three different interfaces: metal-oxide, oxide-oxide and oxide-silicon. Similarly, Sample C (D) is made of 5 nm Al_2O_3 (HfO_2), 10 nm HfO_2 (Al_2O_3) and 5 nm Al_2O_3 (HfO_2), for a total of four interfaces (an oxide-oxide interface is added). More information about the fabrication process can be found in Reference 17.

C-V measurements (at 200 Hz and 500 KHz) were performed using devices with an area of 1.44×10^4 μm^2, obtaining values of the capacitance in accumulation that matches the theoretical calculations for each sample (used values for the dielectric constant are $\epsilon_r = 9 \times \epsilon_0$ for Al_2O_3 and $\epsilon_r = 25 \times \epsilon_0$ for HfO_2[17]), confirming that the thickness of the samples are consistent with those shown on Figure 1. Parallel conductance (G_p) peak shows similar values for all cases, indicating that the density of interface states are similar for all the set of samples (results not shown).

Being the Si surface exposed in the ALD chamber to high-temperature in an oxygen-containing environment, it may be possible to oxidize the Si. In this case, a SiO_2 interlayer (IL) of ≈ 1 nm may be present, which is small compared to the oxides under study. However, it is worth highlighting that the presence of this native oxide, which slightly affects the capacitance of the device, will not affect the conclusion of the paper. A deep analysis of this effect is included in Section IV.

Constant voltage stress (CVS) experiments were conducted at different voltages to study the BD characteristics of the samples. For this purpose, two different measurement setups were used. The first one, based on a Keithley 2636B source/measurement unit (SMU) and a triaxial-chuck probe station, allowed us to capture the current-time (I-t) curve with negligible series resistance and a leakage current background around 100 fA. This setup can register the wear-out stages of the sample during CVS, resolving several orders of magnitude of current at the cost of a relatively low time resolution of around 20 ms.

The second measurement setup uses a Femto high-bandwidth transimpedance amplifier (TIA) model DHPCA-100 and an Agilent digital sampling osciloscope (DSO) MSO−X 3024A to bias the device and record the amplified current trace, respectively. The advantage of this setup is that the time resolution is of the order of a few microseconds. As drawback, only a limited current range can be resolved, depending on the amplifier's gain: the values employed for our measurement were 10^6 and 10^7 V/A. Further details about this setup can be found in References 18 and 19. All measurements were carried out at the dark and at room temperature conditions.

During CVS experiments in multilayered gate stacks it is worth noting that the voltage drop on each layer shall create an associated electric field below the layer's BD field. Therefore the stress voltage applied to a multilayered gate oxide stack must be chosen based on the layer material, considering their intrinsic BD field and the ratio of the equivalent oxide thickness (EOT). Assuming that there is no surface charge at the interface, the oxide field is different for each material. By applying the Gauss Law it is possible to determine the voltage drop in each dielectric layer[20]

$$V_i = \eta_i V_G, \tag{1}$$

where V_G is the voltage applied to the stack and η_i is a coefficient that involves EOT and dielectric constants. In the case of Al_2O_3 (and similarly for HfO_2),

$$\eta_{Al_2O_3} = \frac{t_{Al_2O_3}\epsilon_{HfO_2}}{(t_{Al_2O_3}\epsilon_{HfO_2} + t_{HfO_2}\epsilon_{Al_2O_3})}, \tag{2}$$

where $t_{Al_2O_3}$ (t_{HfO_2}) represents the sum of the thickness of all sub-layers of Al_2O_3 (HfO_2) in the stack. Calculated values of V_i for our samples are showed in Table I for V_G = 10 V. The first row shows the voltage drop, while the second one presents the electric field for each layer. It can be seen that the electric field values are lower than the BD field (E_{BD}), being $E_{BD} \sim$ 10 - 30 MV/cm for Al_2O_3 (depending on the thickness[21]), and $E_{BD} \sim$ 5.5 - 13 MV/cm for HfO_2[22–24].

III. RESULTS

Figure 2 shows I-t measurements performed on Sample D with the SMU setup using gate voltages (V_G) of 9, 9.5 and 10 V. As expected, the curves are consistent with those found in the literature[18,19,25]. First, the initial current increases with voltage due to the voltage dependence of the conduction mechanism (direct tunneling[26], Fowler-Nordheim tunneling[27], and Schottky emission[28]) through

Gate bias = 10 V	Sample A		Sample B		Sample C			Sample D		
Layer	Al_2O_3 10 nm	HfO_2 10 nm	HfO_2 10 nm	Al_2O_3 10 nm	Al_2O_3 5 nm	HfO_2 10 nm	Al_2O_3 5 nm	HfO_2 5 nm	Al_2O_3 10 nm	HfO_2 5 nm
V_i (V)	7.35	2.65	2.65	7.35	3.67	2.65	3.67	1.32	7.35	1.32
E_{Field} (MV/cm)	7.35	2.65	2.65	7.35	7.35	2.65	7.35	2.65	7.35	2.65

TABLE I. Voltage drops and electric field for each layer when 10 V are applied on the gate contact while bulk is grounded.

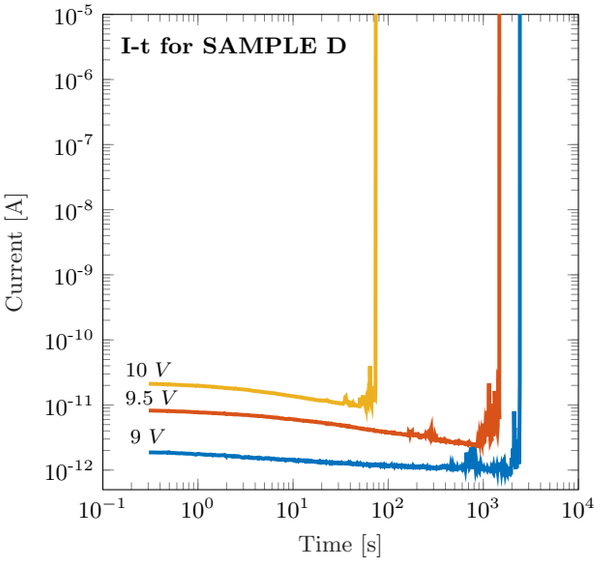

FIG. 2. Current-time curves for sample D obtained with the SMU setup. The curves are consistent with the literature, but the BD occurs so fast that the SMU cannot resolve the transient beyond the 100 pA level.

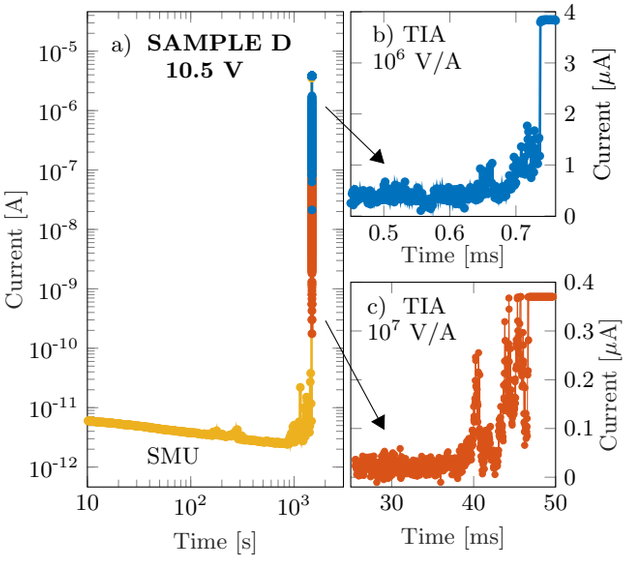

FIG. 3. a) I-t curve obtained superimposing the measurements acquired with the different setups, at same applied voltage of 10.5 V. b) and c) show typical breakdown transients captured by means of a TIA @ gain of 10^6 and 10^7 V/A, respectively. These resolve a specific range of current but allow to see the evolution of the breakdown with improved time resolution.

the dielectric layer. Second, three different stages can be found in each transient: an initial phase in which the current remains constant or slowly decreases (due to charge trapping). Then a second stage where the leakage current exhibits a noisy and progressive growth. Finally the catastrophic failure of the devices occurs during the last stage, which involves an abrupt jump of the current level up to the compliance limit. Also, it can be noticed that, as the biasing voltage decreases, the wear-out stage becomes longer. Given that the time resolution of this setup is in the order of 20 ms, it is unable to properly resolve the current transient during the last phase, showing an abrupt transition in the current level. Therefore, a different measurement setup is required to capture the details of the current transient during this stage.

Because of this requirement, the second measurement setup (TIA) was used. Figure 3 shows a typical measurement on a fresh device. It exhibits three different measurements superimposed to clarify the methodology. The evolution of the BD transient was captured with a μ-s time resolution, current levels ranging from a few nA to μA. It is worth noting that the current range depends on the gain of the TIA (see Figure 3 (b) and (c) for details). Using this methodology all set of samples were studied. Figure 4 (a) and (b) shows typical measurements for sample B.

It is widely accepted that the evolution of the PBD can be quantified by the slope of the current during the BD event, i.e. the degradation rate (DR), as defined in Reference 29, DR = dI_{BD}/dt. Figure 5 shows the DR extracted from measurements of 20-30 devices of each set of samples at 10.5 V calculated in the range of μA as showed in Figure 3 (b). Although the results have a large dispersion (as expected from previous results reported in the literature[29,30]), no significant difference on the mean value has been found between the different samples (see Figure 5). It's also worth mentioning that the variability in sample A is large compared with B-D. Negative and positive bias voltages were used, finding no difference on the morphology of the BD transient for different polarities.

Due to the presence of high-k/Si IL, one may argue that a poor structural quality is responsible for the results observed in Figure 5. In fact, we observe that the

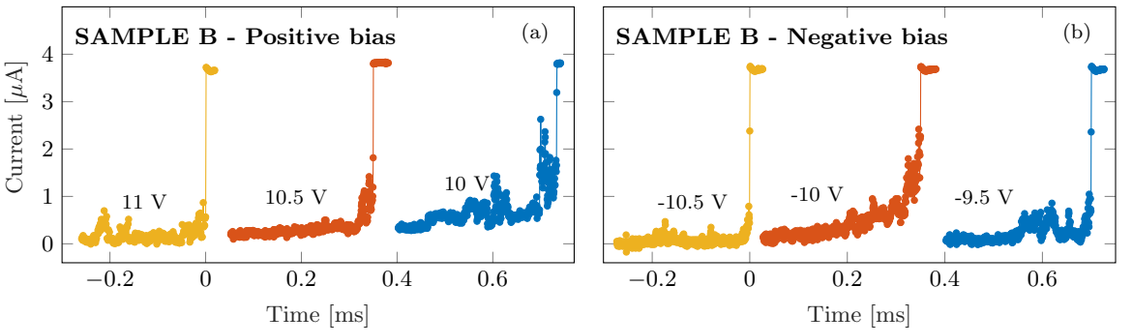

FIG. 4. Typical breakdown transients (I-t) acquired using the TIA setup with gain 10^6 V/A for Sample B. Although the stress runs were a few seconds long, only the last section (a few hundreds of micro seconds around the oscilloscope trigger to capture the current increase) is shown. (a) shows positive bias whereas (b) shows negative bias. Traces are arbitrarily displaced in the x-axis for clarity purposes.

gate stack quality in terms of interface states, border traps, and leakage current affects only the first phase of the current-time measurements, and does not influence the PBD regime. In our samples, the initial defect density is sufficiently low and the MOS samples have to be stressed at high voltage for long times to increase the defect density within the dielectrics beyond the percolation threshold for BD in order to observe within reasonable times the onset of PBD. Moreover, the impact of the IL on the BD growth dynamics for our experimental conditions is negligible[31].

IV. ANALYSIS

The interpretation of the results presented in Figure 5 relies on the understanding of the mechanisms involved in the PBD regime. Recently, the main physical mechanism behind the PBD effect in ultra thin dielectrics was identified[29]. The basic idea is that the PBD transient is due to an electro-migration effect promoting diffusion of the cathode or anode atoms into the gate dielectric in the region of the BD spot. Since the area of the BD spot is of the order of 1-50 nm^2, the current density through it is in the range of 200-10000 MA/cm^2. Such current levels may trigger diffusion/electro-migration of atomic species in the BD spot, providing a simple model to interpret the experimental results.

This interpretation of the current growth during PBD is supported by independent papers[5,19,32,33] in different MOS stacks. After the BD event, in Si-based MOS stacks with metal gates it is observed that the BD spot is characterized by the formation of a Si-rich or a metal-rich region in the gate dielectric in correspondence with the BD spot (i.e. a CF). This evidence goes in strong favor of the hypothesis of electromigration as the major cause of the formation of a CF through the stack, connecting the electrodes. The PBD regime has been shown to be a generalized process in single and bi-layered MOS stacks[10,25,30] where the BD current growth rate is strongly related to the thermal conductivity of the dielectric layer. Taking into account that the interfaces in nanoscaled devices may play a role in the heat dissipation[16] and that the stack composition of our sets of samples show different number of interfaces, the contribution of the thermal boundary at the interfaces must be considered in the analysis of the experimental data of Figure 5.

To model the temperature in the BD spot, it is reasonable to assume spherical symmetry around a source power at the center of the dielectric layer, which electrical power is proportional to $I_{BD}V$[5,10]. The capability of the system to transfer this heat to the surroundings of the BD spot may depend on two aspects: (i) the thermal properties of the bulk materials, and (ii) the thermal behavior of the interfaces. This can be characterized by a thermal resistance for the bulk (ρ_{bulk}) and other one for the interface (ρ_{int}), i.e. a thermal boundary resistance[14] expressed per unit area with units m^2K/W.

But first, the thermal system of a bilayered oxide must be interpreted. In a scenario where the center of the BD spot is considered as the heat source during PBD[29], a first order approximation can consider that both oxides involved contribute to dissipate the heat in a symmetrical way. Considering that the boundaries of the sample are symmetrical at T_{amb}, the equivalent thermal model of a two layer device shall be represented as a parallel of thermal resistances, as shown in Figure 6. Under the strong approximation of spherical symmetry[29], the thermal resistance of one oxide film is defined $R_{th} = 1/t_{ox}k$, where t_{ox} is the oxide's thickness and k its thermal conductivity. Considering one thermal resistance per layer connected in parallel, the equivalent thermal resistance of the oxide stack yields:

$$\frac{1}{R_{th_{eq}}} = \frac{1}{R_{th_{\mathrm{Al_2O_3}}}} + \frac{1}{R_{th_{\mathrm{HfO_2}}}}, \tag{3}$$

$$k_{eq} = \frac{k_{\mathrm{Al_2O_3}} t_{\mathrm{Al_2O_3}} + k_{\mathrm{HfO_2}} t_{\mathrm{HfO_2}}}{t_{tot}}, \tag{4}$$

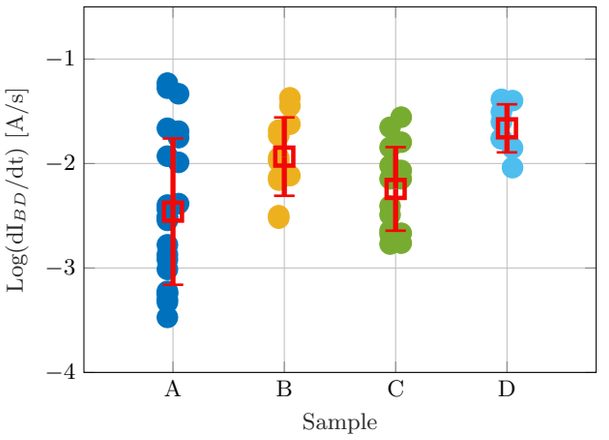

FIG. 5. Values of the degradation rate obtained for each sample. Both positive and negative bias are included. To convert the transient duration into DR, we use $I_{BD} = 1$ μA. The mean values are similar for every sample, although they present a large dispersion.

where k_{eq} is the equivalent thermal conductivity of the bulk oxide considering the contribution of both layers. A way of quantifying the physical impact of the thermal boundary resistance of the interface is comparing it to the equivalent boundary resistance of a dielectric layer with thickness t and thermal conductivity k, i.e. $\rho = t/k$. This way, the overall contribution of the interface can be compared to the influence of the bulk oxides in complex multilayered stacks as those discussed in this work, by adding it's contribution to that of the bulk materials[14]. Using the $R_{th_{eq}}$ calculated with Equation 3, we can obtain an equivalent boundary resistance for the bulk oxide $\rho_{Bulk} = t_{tot}/k_{eq}$ (with t_{tot} being the total thickness of the stack) and add it to the boundary contribution of the interface between oxides itself. Considering this series of thermal boundary resistances, one can derive:

$$\rho_{tot} = \rho_{bulk} + N \times \rho_{int} = \frac{t_{tot}}{k_{eff}}, \tag{5}$$

where N is the number of interfaces in the multilayered system of constant physical thickness $t_{tot} = t_{Al_2O_3} + t_{HfO_2}$. Solving Equation 5 for the effective thermal conductivity k_{eff} of the system, it is straightforward to see that adding interfaces shall contribute to lower k_{eff}. The thermal boundary resistance between various solids has been reported by independent studies. Depending on the materials involved, the values spread over a wide range between 10 and 200 MW/m^{2}K[13–15]. Since there are no reported results on the thermal boundary resistance between Al_2O_3 and HfO_2, we assume a value of 100 m^{2}K/MW. It is worth pointing out that changing this value across the reported range does not affect the interpretation of our results.

The values of k_{eff} are shown on Table II for different number of interfaces, as for the set of samples used in this paper (see Figure 1). This simple comparison highlights that the increase in the number of interfaces in the oxide stack should impact its ability to conduct heat (i.e. k_{eff} decreases as function of the number of interfaces between HfO_2 and Al_2O_3). In this framework, it is worth analyzing how this may affect the PBD of mulitlayered stacks.

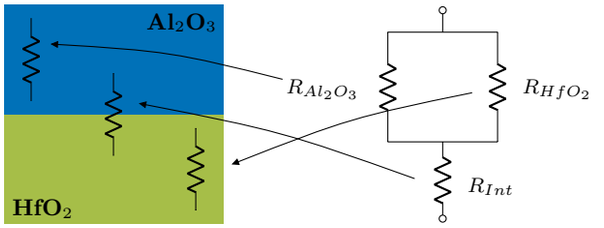

FIG. 6. Representation of the equivalent thermal circuit for the oxide stack of sample A. The center of the breakdown spot is considered as the heat source. Both oxides contribute to dissipate the heat in a symmetrical way. The interface also contributes to the total dissipation capacity of the device.

Finally, as a SiO_2 IL of ≈ 1 nm may be present in the set of samples, its influence on k_{eff} must be analyzed in terms of an increase of the thickness and/or adding an interface to the stack. On both cases, a negligible influence is observed. By considering the bulk effect of 1 nm of SiO_2 at the Si interface k_{eff} remains unchanged, while if the interface is taking in account, it is observed an increase of 1.2 % , and 3.4 % depending if the interface of the gate contact is considered.

A. Physical model of the progressive breakdown

A detailed analysis of the PBD model is required in order to determine if the interfaces play a role on the BD transient. According to the model from Reference 29, the DR depends on the thickness (t_{ox}) and the thermal conductivity (k) of the dielectric layer:

$$\frac{dI_{BD}}{dt} = \frac{eV}{k_B T}\frac{f_1}{t_{ox}^2} D I_{BD}, \tag{6}$$

where I_{BD} represents the BD current, e the elemental charge, V the gate voltage, k_B the Boltzmann constant, T the average conducting filament temperature and D the atomic diffusivity of the electrode's species involved. $f_1 = n_e \lambda_e \sigma_e$ is a constant for electro-migration, with n_e being the electron density, λ_e the electron mean free

Number of interfaces	k_{eff} $\left[\frac{W}{mK}\right]$
0 (only bulk effect)	1.35
1	0.81
2	0.57

TABLE II. Values for k_{eff} calculated with Equation 5, considering different number of interfaces.

path and σ_e the cross-section for the electron-atom collision, which is the basic mechanism for momentum transfer from the conduction electron of the metal to the diffusing atom. Inner dielectric temperature is an essential parameter in some mechanisms behind the electric current through that dielectric (Poole-Frenkel emission[34], ionic conduction[35], nearest-neighbor hopping conduction, Mott-hopping conduction[36]). In some publications, the classical heat equation is solved[37]. Obviously, at the considered scale, a more accurate model for the Fourier's law should be employed[38,39]. In spite of these facts, we have modeled the temperature by means of the expression:

$$T = \frac{f_2 V I_{BD}}{2\pi t_{ox} k} + T_{amb}, \tag{7}$$

where f_2 is the fraction of the energy eV per electron lost at the BD spot, T is the local temperature at the electrode which provides the dominant diffusing atomic species and k is the thermal conductivity of the dielectric. So if the value of k changes due to the contribution of the interfaces, so it does the magnitude of $\mathrm{dI}_{BD}/\mathrm{dt}$. In our previous works, the effect of the thermal conductivity on the current growth rate was reported for different HK-based MIM[10,40] and MOS[29] devices. The objective was to compare the BD transients among sets of samples of identical oxide thickness and electrodes, that only differ in their HK oxide materials, Al_2O_3 or HfO_2. In such studies, Al_2O_3 based devices showed much lower dI_{BD}/dt than their HfO_2 counterparts. Considering that the thermal conductivity of HfO_2 has been reported around 0.9 W/mK[41] and for amorphous Al_2O_3 around 1.8 W/mK[42], a difference of a factor 2 between materials can severely modify the experimental dI_{BD}/dt[29,40,43].

Within this framework, we will study the impact of the additional interfaces on the BD characteristics exhibited by the current transients presented in this paper. By deriving an effective thermal conductivity for the multilayered case by considering Equation 5 (See Table II), a clear decrement by a factor of ∼2 can be seen as the number of oxide-oxide interfaces increases from 0 (single layer case) to 2. In this context, if the interfaces do play a role on the BD transient, a variation in the thermal conductivity of the stack should correlate with a change in DR, as it can be seen from Equations 6 and 7. Nevertheless this is not observed in the experimental data reported in Figure 5, where a negligible, if none at all, dependency of DR on the number of interfaces is presented. This indicates that oxide-oxide interfaces do not affect DR, and hence, nor the temperature of the CF. A possible explanation to this phenomenon can be made based on the power dissipation in the CF, as it could be argued that once formed, the power dissipation will be driven by the electrical characteristics of the BD path itself, with little if none influence of the added interfaces in the multilayered structure. But to properly address this aspect, we should discuss the transport characteristics of the CF.

B. Characteristics of the breakdown path

Heat dissipation by electron relaxation at the interfaces occurs when an energy barrier exists between the filament and one of the electrodes[16]. This feature is determined by the geometry and the electrical properties of the CF[44]. Therefore, it is imperative to study the carrier transport through the BD path, which is related to its structural characteristics[10], in samples with different number of interfaces in order to validate the analysis from previous sections. To compare the CF of the different samples, the conduction mechanism has been analyzed in terms of the quantum point contact (QPC) model. The QPC model assumes that the BD conduction takes place through a CF which is narrow enough to consider it as a quasi-1D system. Modeling the constriction of the CF as a potential barrier (Figure 7 (c)) and using the finite-bias Landauer formula, a V-I characteristic can be derived[45]:

$$V = \frac{2}{\alpha e} sinh^{-1}\left[\frac{h\alpha\ sinc\left(\pi k_B T \alpha\right)}{4e\ exp(-\alpha\Phi)} I\right], \tag{8}$$

where $\alpha = t_b\ h^{-1}\ \pi^2\sqrt{2m^*/\Phi}$, Φ is the barrier height, t_b the barrier width at $E = 0$, m^* the electron effective mass in the constriction and k_B and h are the Boltzmann and Planck constant. On Figure 7 (a), typical V-I curves for Sample D are shown. They were obtained by applying a ramped current stress while measuring the resulting voltage drop across the device with a Keithley SMU. By fitting the experimental data with Equation 8, the CF can be characterized trough the values of Φ and t_b. Black curves correspond to the measurement, while the blue dashed lines are the QPC model results (Equation 8).

The results of each fit for both samples (A and D) are plotted together in Figure 7 (b), which shows the evolution of the barrier height (Φ) and width (t_b) as s function of the current compliance for each sweep. It is observed that, as reported in previous works[46,47], both Φ and t_b reduces as the current level increases, suggesting a progressive degradation of the CF during the successive V-I sweeps. Fitting values are in good agreement with the previously reported results on similar structures[47,48].

It is worth noting that a clarification regarding the use of the QPC model is required. Although within Landauer's conduction model the transport process through the constriction is inherently elastic[30] (see Figure 7 (c)), it can consider the Joule heating in the regions around a scattering center present in the CF[44]. At this point it is worth highlighting that the assumption of power dissipation taking place inside the dielectric layer at the constriction is reasonable based on independent experiments. Takagi *et al*[49] have shown that the electrons tunneling through defects responsible for stress induced leakage current (SILC) in thin oxynitrides do lose a large

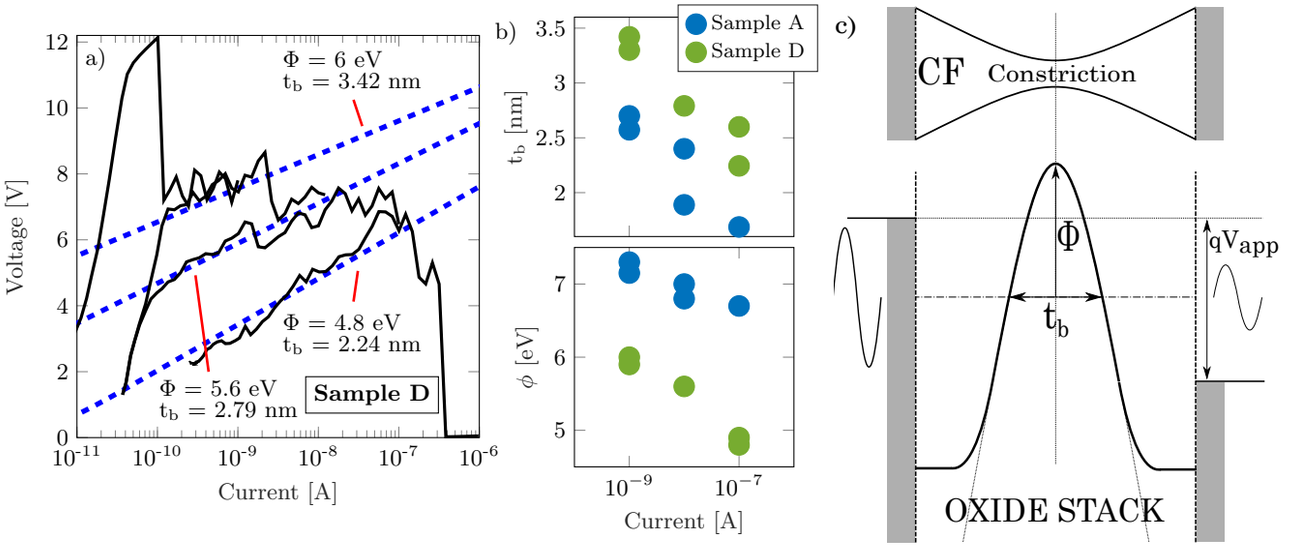

FIG. 7. (a) Successive V-I sweeps and respective fits -according to the QPC model- for sample D. (b) Plot for the different parameters obtained through the QPC fit: t_b represents the width of the CF while Φ the barrier height (see Equation 8). (c) Diagram of the barrier in the narrowest point of the conductive filament and the corresponding energy band. The different model parameters are displayed.

fraction of their energy in the oxide. That is, the electron tunneling through SILC defects is inelastic, with a large fraction of electron energy lost due to defect relaxation, as shown by Blochl and Stathis[50]. It is reasonable to assume that a similar effect takes place during electron transport through the BD spot. Furthermore, Sorée *et al*[51,52] link the dissipation to the presence of phonons in the vicinity of this constriction, where inelastic processes occur.

Figure 7 reveals that the transport characteristics can be represented by the same features. Although the number of interfaces in the gate stack is different on both set of samples (sample A has one Al_2O_3/HfO_2 interface while sample D has two), the carrier transport characteristics across the insulators are virtually the same for both stacks, suggesting a similar structural composition of the CF. Linking this observation to the results of Figure 5, where the BD dynamics are characterized by very similar DR for all our sets of samples, it is safe to say that the dissipated power in the vicinity of the BD spot is being transferred to its surroundings at similar rates in all cases. In this way, the temperature profiles around the conductive filament remain unaltered despite the number of interfaces in our samples, consistently with the physical mechanisms that describe the progressive current growth under the PBD regime.

V. SUMMARY

In this paper, we have shown that the PBD event occurs in the case of MOS devices consisting of two and three layers of aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) by means of a high-bandwidth setup. To clarify the role of the interfaces in the heat dissipation from the BD path to its surroundings, a systematic analysis of the BD transients was performed in those samples. Taking into account the literature, the BD current growth rate was proposed as an adequate magnitude to measure the heat dissipation during the BD event since it is strongly related to the thermal conductivity of the dielectric layer. Overall results showed no differences in the PBD growth rate indicating a negligible impact of the interfaces on the temperature profiles around the CF despite the number of interfaces.

Although the role played by material interfaces in the heat dissipation in nanoscaled devices is well documented, our results show no clear impact of oxide-oxide interfaces on the BD transients. This suggests that the capabilities of the stack to dissipate the heat produced during BD, which drives the PBD growth, away from the BD path are solely defined by the bulk materials involved.

This observation goes in strong favor of the formation of a CF (probably due to atom electromigration from the electrodes) with electrical characteristics that are not influenced by the number of oxide interfaces in the multilayered stack. This concept was shown by QPC model fits, consistent with the idea of a variable energy barrier at the center of the filament constriction. The case of partially formed percolation paths is considerably different, since most of the power is dissipated at the interfaces within the percolation path itself and the surrounding insulator, where energy barriers limit the carrier transport into and out of the filament.

In addition to their relevance for the scaling of gate dielectrics in modern CMOS devices, our results may provide a basic framework for different applications of ultrathin dielectrics, in particular for the electrically induced resistive switching effects which have been proposed as the basis for future semiconductor non-volatile memories.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Sample A

Ni contact (200 nm)
Al2O3 (10 nm)
HfO2 (10 nm)
n-Silicon

Sample B

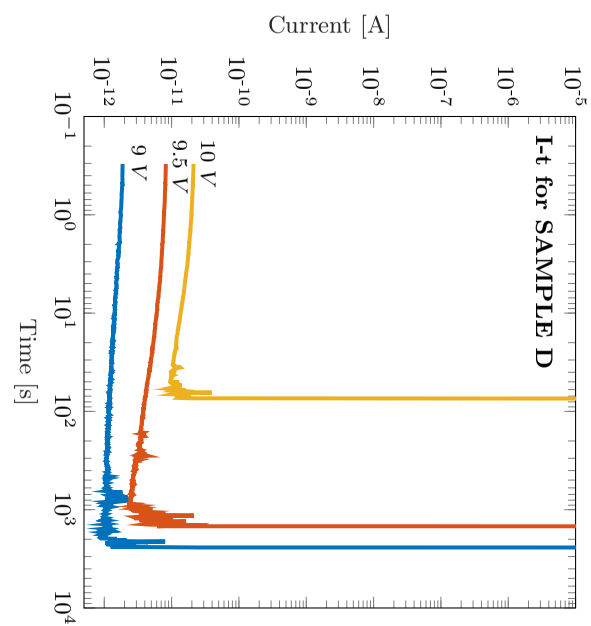
Ni contact (200 nm)
HfO2 (10 nm)
Al2O3 (10 nm)
n-Silicon

Sample C

Ni contact (200 nm)
Al2O3 (5 nm)
HfO2 (10 nm)
Al2O3 (5 nm)
n-Silicon

Sample D

Ni contact (200 nm)
HfO2 (5 nm)
Al2O3 (10 nm)
HfO2 (5 nm)
n-Silicon



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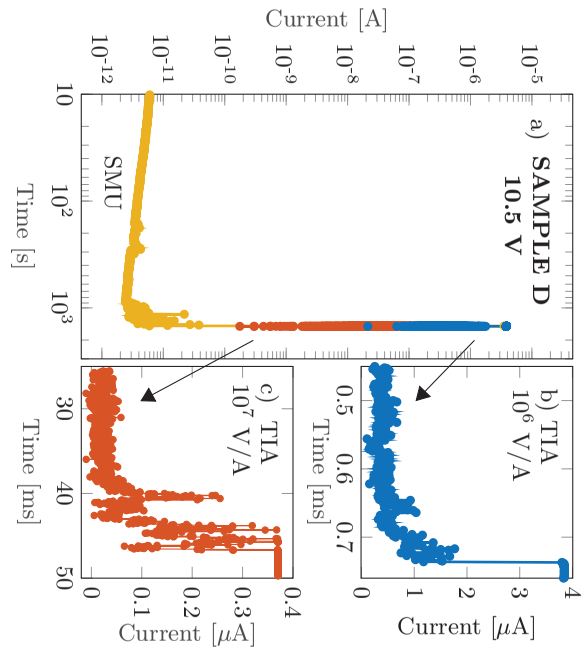

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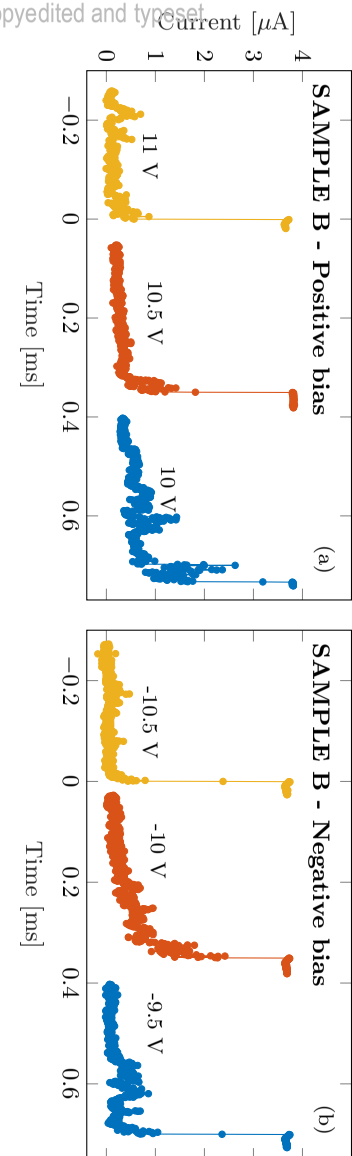

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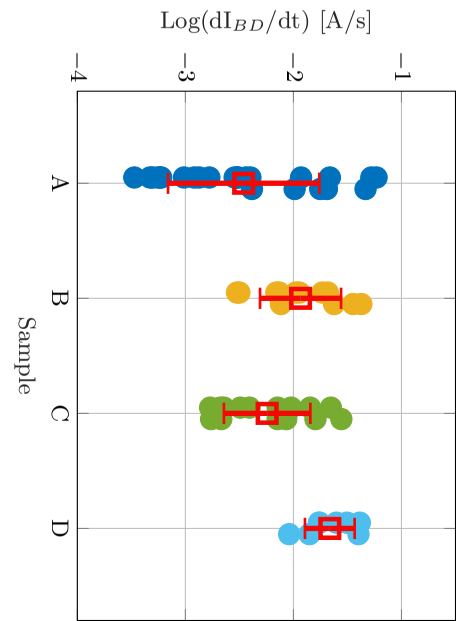

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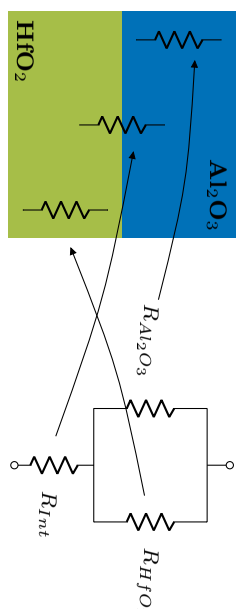

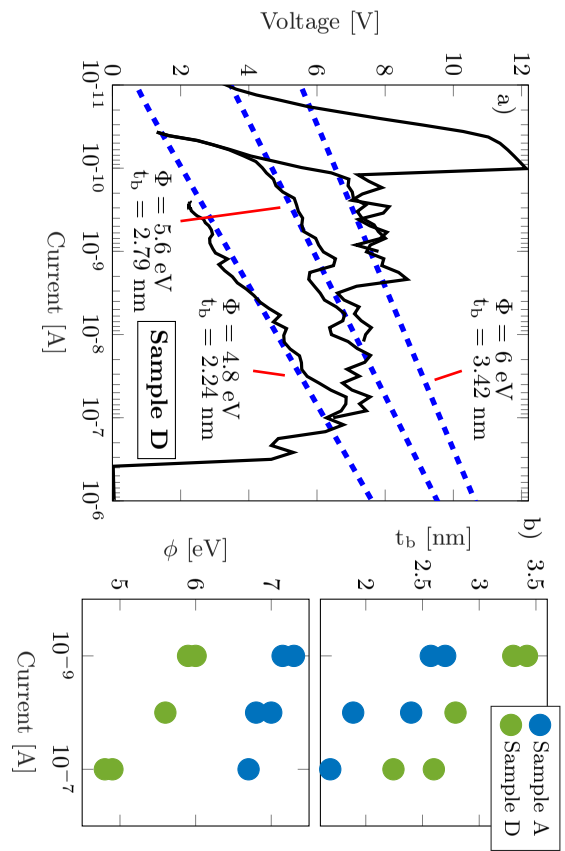

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