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Nicola Zanatta*, Tommaso Caldognetto*, Giorgio Spiazzi†, and Paolo Mattavelli*

*Department of Management and Engineering, University of Padova, Vicenza, Italy
†Department of Information Engineering, University of Padova, Padova, Italy
nicola.zanatta.2@phd.unipd.it, tommaso.caldognetto@unipd.it, giorgio.spiazzi@unipd.it, paolo.mattavelli@unipd.it

***Abstract*—This paper proposes a two-stage isolated dc-dc converter for electric vehicle charging applications, where high efficiency over a wide range of battery voltages is required. It employs a first pre-regulation stage and a second half-bridge LLC stage, integrated with the first. The second stage is always operated at resonance, ensuring very high efficiency. The first pre-regulation stage is responsible for the desired input-to-output voltage conversion ratio and the zero-voltage switching operation of all the switches. This allows low conversion losses even with voltages that may vary over a wide range. The conversion structure is shown considering a first experimental prototype that interfaces a 750-V dc-link with an output bus with nominal voltage range 250V-500V. The implemented module is rated 5 kW and achieves a peak efficiency of 98.0% at 3 kW output power.**

***Index Terms*—battery charger, buck-boost, dc-dc converter, DCX, fast-charging, resonant LLC, pre-regulation, soft-switching.**

I. Introduction

DC-DC converters with galvanic isolation are crucial in the development of effective electric-vehicle (EV) battery charging systems [1]–[4]. The resonant LLC converter is commonly adopted in many applications for its simple structure and efficient power conversion [5], [6]. LLC resonant converters can achieve zero-voltage switching (ZVS) operation for the primary-side switches and zero-current switching (ZCS) operation for secondary-side switches, but performance significantly degrades at input or output voltage levels that do not allow near-resonance operation [2], [6]. This is often the case in the considered application, represented in Fig. 1, where battery state of charge variations due to typical mission profiles may bring to wide ranges of operating voltages [2], [7]–[9]. The literature reports approaches to overcome the limitations of the frequency-modulated LLC converter [2], [8]–[10]. An LLC structure reconfigurable for half-bridge or full-bridge operation is proposed in [11], but smooth transitions between the configurations may be complex to achieve. A reconfigurable topology employing an additional LCL-T resonant tank and with smooth transitions between the configurations is proposed in [12], in which a careful design of the additional resonant tank is required to limit the related losses. An interleaved LLC is proposed in [9], achieving wide voltage regulation. A solution using input-parallel and output-series partial power processing (PPP) and resonant CLLC-type DCXs is proposed in [13], considering a narrower range of operating voltages with respect to the one considered herein. The topology is characterized by low switching losses on the output switches, but it requires an active rectification with very low conduction losses and a relatively high number of devices.

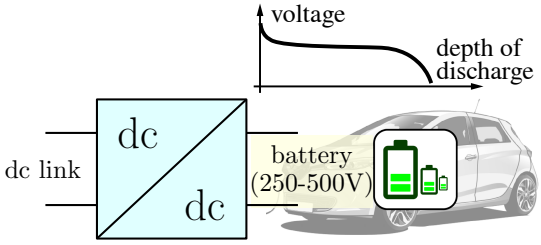

Fig. 1: EV-charging application.

The conventional LLC-type DCX design has been widely investigated in the literature. Partial power conversion solutions show potential advantages to accommodate wide operating voltage ranges for applications like in Fig. 1, at the cost of a higher number of components, a more complex design of DCXs stages, and more complex modulations [13]–[15].

Input voltage regulation is one of the most suitable solutions in case of wide input and output voltage regulation for its simplicity and low component count [8], [16], [17]. In this paper, a two-stage conversion structure is considered, analyzed, and experimentally evaluated. The structure, shown in Fig. 2, is composed of a first, pre-regulation stage and a second stage based on the LLC resonant converter. The principle is to operate the second stage at the operating condition that ensures maximum efficiency, namely, at resonance, and exploit the pre-regulation stage to impose such optimal operating condition for the second, LLC stage. Minimum leakage inductance L_r is desired for the LLC operated in DCX mode, which can sim-

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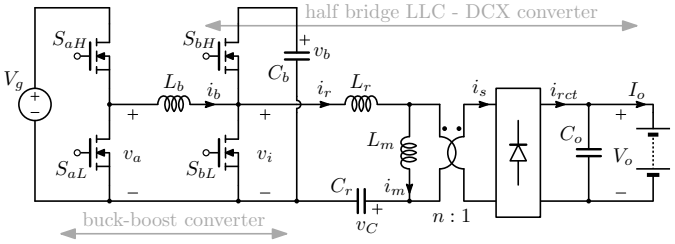


Fig. 2: Two-stage converter with pre-regulation & LLC stage.

plify the transformer design process, reduce winding losses, and reduce the resonant capacitor voltage stress. Such a design consideration allows to achieve nearly constant voltage gain even with some parameter mismatches. The pre-regulation stage can also help in achieving zero-voltage turn-on (ZVS) of the switches that drive the second stage over a wide range of output voltages [2], [8]. Of course, the exploitation of latest wide-bandgap power semiconductors allows to further reduce semiconductor loss [18]. Despite of the presence of an additional stage, some valuable characteristics are highlighted and shown in terms of overall conversion efficiency. In particular, light-load low voltage operation is possible with limited efficiency degradation, which is instead difficult to achieve considering the LLC topology.

In the following, the topology is introduced, in Sect. II, analyzed in terms of main loss contributions, in Sect. III, and experimentally evaluated, in Sect. IV. Conclusions are reported in Sect. V.

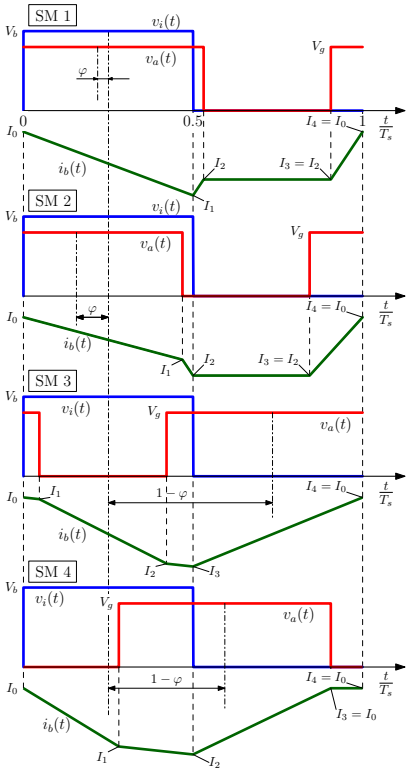
II. Converter Structure and Operation

A. Converter Description and Operation

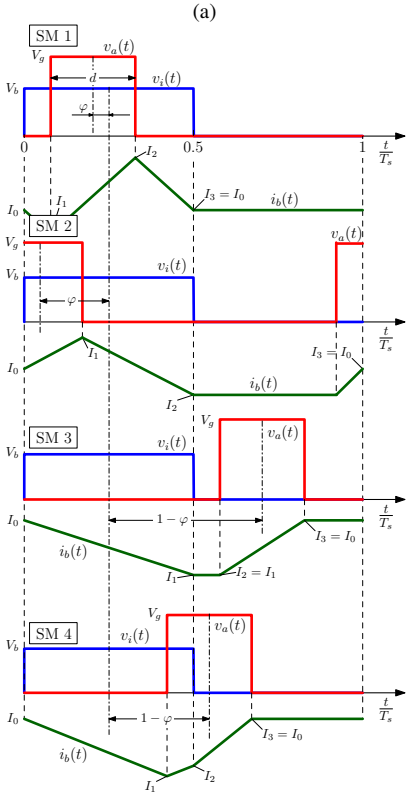
The two-stage topology is displayed in Fig. 2. Its peculiarity is the integration of the two power switches S_{bH} and S_{bL} of the buck-boost stage as primary switches of the half-bridge LLC [17], [19]–[21]. In order to exploit the high performance of the LLC stage working as dc-transformer (DCX) [15], the right-leg (S_{bH} and S_{bL}) duty cycle is fixed at 50%. Whereas, the two remaining degrees of freedom, that is, the duty cycle d of the left-leg referred to the upper switch S_{aH} and the phase shift φ between the driving signals of the two legs, can be used to adjust *i*) the inductor current at switching instants, which is important for ZVS constraints, and *ii*) the output voltage, which is important to allow operation at resonance of the LLC stage. Therefore, the total voltage gain of the structure can be computed as the product of the voltage gain of the pre-regulation buck-boost and the half-bridge LLC working as DCX:

$$M = \frac{V_o}{V_g} = \frac{V_b}{V_g} \cdot \frac{V_o}{V_b} = M_{BB} \cdot M_{LLC} = 2d \cdot \frac{1}{2n} = \frac{d}{n} \quad (1)$$

Remarkably, the voltage gain is a function of the duty-cycle d of the left leg only. Whereas, the phase-shift φ represents a degree of freedom that can be used to shape the piece-wise linear current i_b to ensure ZVS of the four switches.



(a)



(b)

Fig. 3: Main converter waveforms for different phase shift values. (a) Boost case; (b) buck case.

TABLE I: Boundaries and corresponding switching instants.

(a) Boost operation mode (i.e., $d \geq 0.5$)

SM	Boundaries	Switching instants $4 \cdot t_1/T_s$	$4 \cdot t_2/T_s$	$4 \cdot t_3/T_s$
1	$\frac{1-2d}{4} \leq \varphi < \frac{2d-1}{4}$	2	$1-4\varphi+2d$	$5-4\varphi-2d$
2	$\frac{2d-1}{4} \leq \varphi < \frac{3-2d}{4}$	$1-4\varphi+2d$	2	$5-4\varphi-2d$
3	$\frac{3-2d}{4} \leq \varphi < \frac{1+2d}{4}$	$1-4\varphi+2d$	$5-4\varphi-2d$	2
4	$\frac{1+2d}{4} \leq \varphi < \frac{5-2d}{4}$	$5-4\varphi-2d$	2	$5-4\varphi+2d$

(b) Buck operation mode (i.e., $d < 0.5$)

SM	Boundaries	Switching instants $4 \cdot t_1/T_s$	$4 \cdot t_2/T_s$	$4 \cdot t_3/T_s$
1	$\frac{2d-1}{4} \leq \varphi < \frac{1-2d}{4}$	$1-4\varphi-2d$	$1-4\varphi+2d$	2
2	$\frac{1-2d}{4} \leq \varphi < \frac{1+2d}{4}$	$1-4\varphi+2d$	2	$5-4\varphi-2d$
3	$\frac{1+2d}{4} \leq \varphi < \frac{3-2d}{4}$	2	$5-4\varphi-2d$	$5-4\varphi+2d$
4	$\frac{3-2d}{4} \leq \varphi < \frac{3+2d}{4}$	$5-4\varphi-2d$	2	$5-4\varphi+2d$

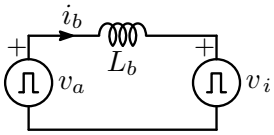


Fig. 4: Equivalent circuit for inductor current analysis.

Two main operation modes may be distinguished, namely, boost mode, when $d > 0.5$, and buck mode, when $d < 0.5$. For each operation mode, phase shift variations give rise to four different shapes of the inductor current i_b, herein refereed to as switching modes (SM). The total eight SMs, depending on the values of d and φ, are displayed in Fig. 3a and Fig. 3b. Table Ia and Table Ib report an analytical description of the SMs, which is useful for the analysis of the converter operation.

B. Inductor Current Derivation

The equivalent circuit in Fig. 4 can be referred to for the derivation of the current i_b through the inductor L_b. Source voltages v_i and v_a model the voltages imposed by the half-bridges in Fig. 2, according to Table I.

The instantaneous inductor current i_b in the time domain can be computed as:

$$i_b(t) = I_0 + \frac{1}{L_b}\int_{t_0}^{t} (v_a(\tau) - v_i(\tau))\ \mathrm{d}\tau \tag{2}$$

where $I_0 = i_b(t_0)$ is the initial value of the inductor current, $t_0 < t$. Being the inductor current waveform piecewise linear, (2) can be computed as:

$$i_{b_k}(t) = i_b(t_{k-1}) + \frac{v_{L_b}(t)}{L_b} \cdot (t - t_{k-1})\ , \quad t \in [t_{k-1},\, t_k) \tag{3}$$

for $k = 1, 2, 3, 4$, let us call I_k the inductor current values $i_b(t_k)$ and V_{L_k} the constant inductor voltage in $[t_{k-1},\, t_k)$. The initial value $I_0 = i_b(t_0)$ is calculated imposing the capacitor charge balance during the conduction phase of S_{bH}, between $t = 0$ and $t = T_s/2$, thus:

$$I_o = \frac{2n}{T_s}\int_0^{T_s/2} i_b(t)\ \mathrm{d}t = \frac{n}{2T_s}\sum_{k=1}^{N} \Delta t_k (I_{k-1} + I_k) \tag{4}$$

where $\Delta t_k = t_k - t_{k-1}$ and $N = 1, 2$ or 3 is the number of current piecewise in the considered half-period, depending on the SM. Observing that $I_k = I_{k-1} + V_{L_k}\Delta t_k / L_b$ and $\sum_{k=1}^{N} \Delta t_k = T_s/2$, (4) yields:

$$I_o = n\frac{I_0}{2} + \frac{n}{2L_bT_s}\sum_{k=1}^{N} V_{L_k}\Delta t_k(\Delta t_k + 2\Delta t_{k+1} + 2\Delta t_{k+2}) \tag{5}$$

with $\Delta t_k = 0$ for $k > N$. Equation (5) allows to determine the initial value I_0, once the output current is known.

An additional parameter worth computing is the inductor rms current:

$$i_b^{\mathrm{rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_b^2(t)\ \mathrm{d}t} = \sqrt{\frac{1}{T_s}\sum_{k=1}^{4}\int_{t_{k-1}}^{t_k} i_{b_k}^2(t)\ \mathrm{d}t} \tag{6}$$

where $i_{b_k}(t) = I_{k-1} + \dfrac{V_{L_k}}{L_b}t$, $t \in [t_{k-1},\, t_k)$, it yields:

$$i_b^{\mathrm{rms}} = \sqrt{\frac{1}{T_s}\sum_{k=1}^{4}\left[I_{k-1}^2\Delta t_k + \frac{I_{k-1}V_{L_k}}{L_b}\Delta t_k^2 + \left(\frac{V_{L_k}}{L_b}\right)^2\frac{\Delta t_k^3}{3}\right]} \tag{7}$$

The equations reported above can help to properly define the modulation parameter φ, as demonstrated in the following sections.

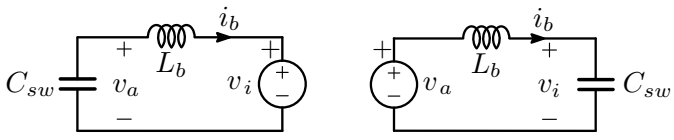
III. Main Loss Contributions

Since all the diodes of the DCX-LLC can achieve ZCS turn-off and, with a proper modulation of the phase shift φ, ZVS turn-on can be achieved for all the active switches, the main loss components include conduction losses of MOSFETs and diodes, magnetic components losses, and MOSFETs turn-off losses. Phase-shift modulation has a significant impact on both MOSFETs switching and conduction losses and inductor losses. The ac resistance and the ferrite losses of the inductor should be accurately took into account in the design of the component to allow a convenient exploitation of the phase-shift modulation. Instead, the transformer losses of the LLC are not affected by φ variations. Besides, optimal design for maximum efficiency of the LLC transformer is facilitated by the fixed operation at nominal conditions ensured by the pre-regulation stage.

In the following, the ZVS conditions for switching losses minimization, the conduction losses evaluation of the inductor and the transformer, and the design procedure of the magnetic components are discussed.

A. Conditions for Zero-Voltage Switching Operation

Switching losses mainly depend on the switches output capacitance C_{oss}, the inductor current at switching instants



(a) Turn-on S_{aH} and S_{aL} (b) Turn-on S_{bH} and S_{bL}

Fig. 5: Equivalent circuits during ZVS transients.

$t_{0\div4}$, and the chosen dead-times. To minimize such a loss contribution ZVS at turn-on is necessary [22]. This poses minimum switched current constraints for ZVS, which can be determined as discussed in [22]–[24].

Fig. 5 shows equivalent circuits for the analysis of the SMs in Fig. 3. Generators v_i, in Fig. 5a, and v_a, in Fig. 5b, are set as per the considered SM, resulting in different minimum current conditions, function of the input and output voltages. By the methods in [23], [24], the minimum current condition for the ZVS of the left leg (refer to Fig. 5a) can be calculated by solving iteratively the expression for $t_{\mathrm{ZVS}} \leq t_{\mathrm{dead}}$:

$$t_{\mathrm{ZVS}} = \int_0^{V_g} \frac{C_{sw}(v_a)}{\sqrt{i_{\mathrm{ZVS}}^2 + \frac{2}{L_b}\int_0^{v_a} C_{sw}(v)(v_i - v)\,\mathrm{d}v}}\,\mathrm{d}v_a \qquad (8)$$

where t_{ZVS} is the duration of the transition with an initial inductor current i_{ZVS}, and C_{sw} is the equivalent charge capacitance at the switching node [23]. Equation (8) can be adapted to the equivalent circuit in Fig. 5b by substituting V_g with V_b and v_i with v_a, respectively.

By this approach, ZVS regions for all the switches in the output-current, output-voltage (i.e., duty cycle d), and phase-shift space can be computed, as displayed in Fig. 6a. Fig. 6b shows the ZVS region at minimum output voltage. Notably, ZVS is achieved over the whole range of transferred power and output voltages. In Fig. 6a and Fig. 6b, red lines highlight those points where ZVS is achieved for all the switches with minimum inductor rms current, that relates to the minimum phase-shift values to achieve ZVS. Such an inductor current computed as in (7) is shown in Fig. 6c.

It is worth remarking that, absence of ZVS turn-on makes switching losses amount to become a predominant portion of the total converter losses, especially in high-voltage applications [25]. For this reason ZVS turn-on is aimed herein, especially at low output voltages, where state-of-the-art LLC topologies present significant efficiency degradations due the lost of ZVS [2].

B. Conduction Losses Estimation

Generally, the conduction losses of a magnetic element can be modeled summing its dc losses, related to the windings dc resistance R^{dc} and the dc value of the current i^{dc}, with its ac losses, which can be estimated by considering the rms of the first M ac frequency components $i^{\mathrm{ac_m}}$ and related ac winding resistances. Therefore, the conduction losses related

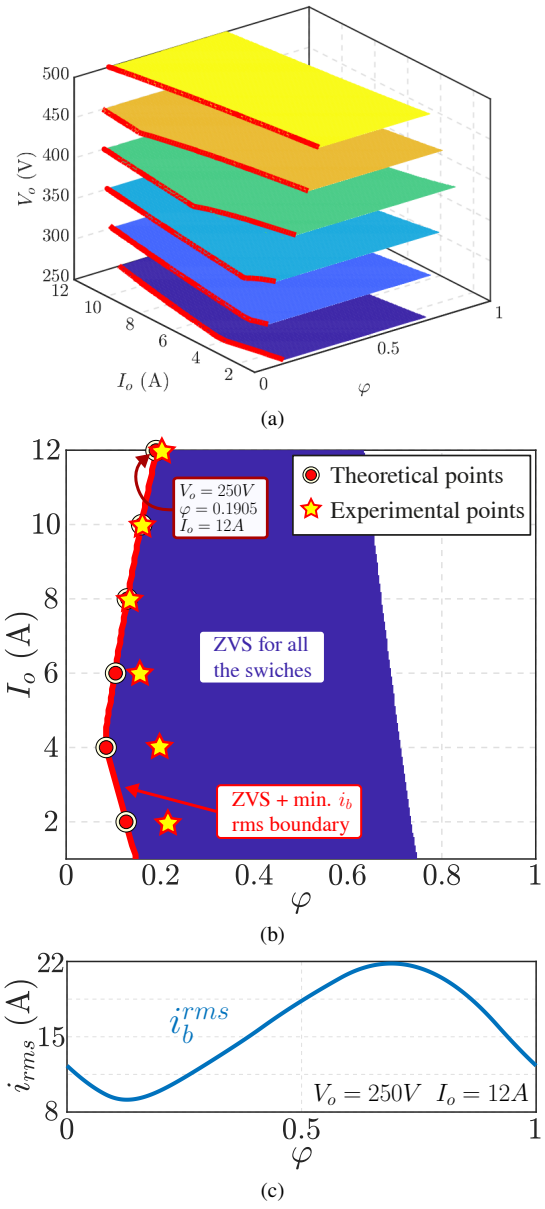


Fig. 6: ZVS regions: (a) whole output voltage range; (b) $V_o = 250\,\mathrm{V}$. (c) Inductor rms current, $V_o = 250\,\mathrm{V}$ and $I_o = 12\,\mathrm{A}$. Converter parameters in Table II.

to the inductor L_b can be modeled as:

$$P_{L_b}^{\mathrm{cond}} = R_b^{\mathrm{dc}} \cdot i_b^{\mathrm{dc}\,2} + \sum_{m=1}^{M} R_b^{\mathrm{ac_m}} \cdot i_b^{\mathrm{ac_m}\,2} \qquad (9)$$

Equation (9) is adopted for the estimation of the winding losses of the inductor in Sect. IV. In the considered case, the number of harmonics for an acceptable estimate is set $M = 3$. Instead, the conduction losses of the transformer of the LLC stage are not affected by any modulations. The LLC behaves as a DCX and the winding losses of the transformer can be simplified as:

$$P_{\mathrm{Tr}}^{\mathrm{cond}} = R_{\mathrm{Tr}}^{\mathrm{ac_1}} \cdot i_r^{\mathrm{rms}\,2} \qquad (10)$$

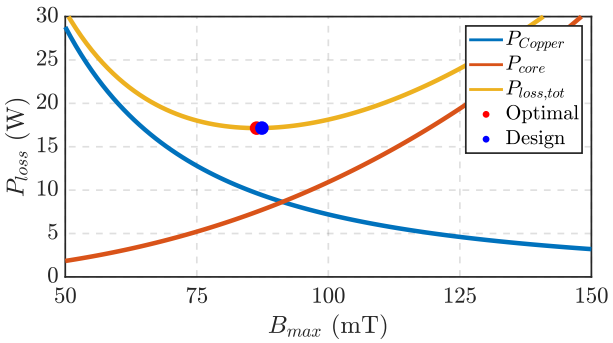


Fig. 7: P-B plot for transformer design at $V_o^{\text{nom}} = 400\,\text{V}$ and $P_o^{\text{nom}} = 5\,\text{kW}$. The design point is obtained with two parallel litz wires $500 \times 71\,\mu\text{m}$ each and number of turns $N_p = N_s = 17$.

where $R_{\text{Tr}}^{\text{ac}_1}$ is the ac resistance of the windings referred to the primary side at fundamental frequency and i_r^{rms} is the rms value of the resonant current.

C. Transformer Losses Minimization

Magnetic losses include winding loss and core loss, both of which should be carefully estimated for overall minimum losses. The transformer design procedure adopted herein is based on [26]. Once the magnetic core is selected, with given magnetic volume V_c, window winding area W_a, core cross-sectional area A_c, Steinmetz parameters K_c, α and β, and maximum window filling factor k_u of the transformer (typ., assume $k_u \leq 40\%$), it is possible to calculate the winding and core losses as:

$$\begin{cases} P^{\text{cond}} = RF\rho_w V_w k_u J_0^2 \\ J_0 = \dfrac{\sum VA}{K_v f_s k_f B_{max} k_u A_p} \\ P^{\text{core}} = V_c K_c f^{\alpha} B_{max}^{\beta} \end{cases} \tag{11}$$

where P^{cond} is the total copper loss, ρ_w is the copper resistivity, V_w is the total windings volume, $RF = R^{\text{ac}}/R^{\text{dc}}$ is the resistivity factors for the selected litz wire at fundamental frequency [26], J_0 is the current density, $\sum VA$ is the power rating of the transformer, K_v is the waveform factor, f_s is the fundamental frequency, B_{max} is the peak flux density, k_f is core stacking factor, $A_p = AcW_a$ is the area product of the core and P^{core} is the core loss given by the Steinmetz equation with parameters K_c, α and β. The total loss of the transformer is then computed as $P^{\text{cond}} + P^{\text{core}}$ and must be lower than the thermal dissipation capability of the component, which can be estimated during the design phase.

Fig. 7 reports the results using (11), showing a total loss of 17 W at nominal conditions, namely, $V_o = 400\,\text{V}$ and $P_o = 5\,\text{kW}$. A corresponding prototype of the transformer was implemented using a core PQ50/50 N87 and two parallel litz wires $500 \times 71\,\mu\text{m}$, resulting in a measured total power loss of 21 W at the same nominal conditions.

TABLE II: Prototype parameters.

Parameter	**Symbol**	**Value**	
Input voltage	V_g	750	V
Output voltage	V_o	250-500	V
Nominal power	P_o^{nom}	5	kW
Switching frequency	f_s	200	kHz
Leakage inductance	L_r	1.8	µH
Magnetizing inductance	L_m	180	µH
Inductance	L_b	30	µH
Turns ratio	n	1	-
Resonant capacitance	C_r	290	nF
S_{aH}, S_{aL}	SCT3040KR, SiC MOSFETs		
S_{bH}, S_{bL}	G3R30MT12K, SiC MOSFETs		
Output Rectifier	SK20KDD12SCp, SiC diodes		

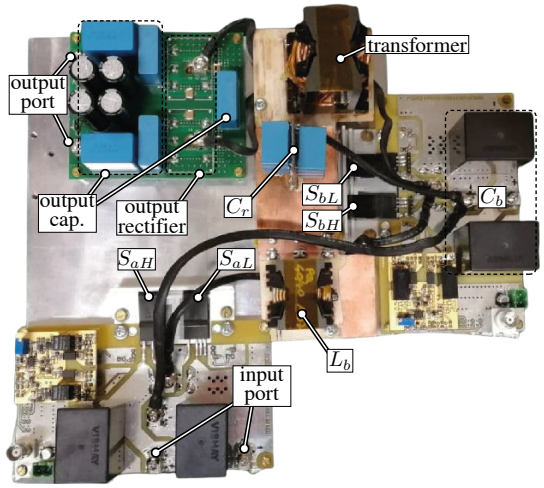


Fig. 8: Experimental prototype.

IV. Experimental Results

The experimental prototype displayed in Fig. 8 of a 5-kW module with parameters in Table II has been implemented and evaluated. Fig. 9 shows the converter efficiency over the entire output voltage range, and in particular at the minimum, nominal, and maximum voltage, namely, 250 V, 400 V, and 500 V, respectively. Efficiency measurements were performed by means of a Keysight PA2203A power analyzer. The measured peak efficiency at minimum output voltage is 97.25%, while at maximum output voltage is 97.9%, which are both very close to the absolute maximum efficiency of 98.0% measured in nominal conditions. A loss breakdown over the considered wide output voltage range of operation is reported in Fig. 10. The loss breakdown has been validated experimentally by means of thermal measurements. The total discrepancy among estimations based on the described models and the collected measurements results lower than about 10% of the measured total power loss.

Finally, Fig. 11 shows the converter waveforms at the point $V_o = 250\,\text{V}$, $P_o = 3\,\text{kW}$, arbitrarily selected. Notably, ZVS

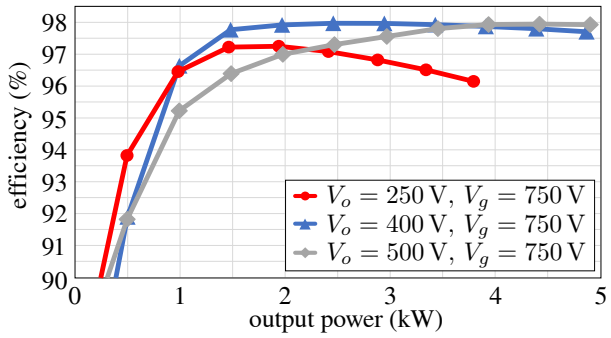


Fig. 9: Measured efficiency at minimum, nominal, and maximum output voltage.

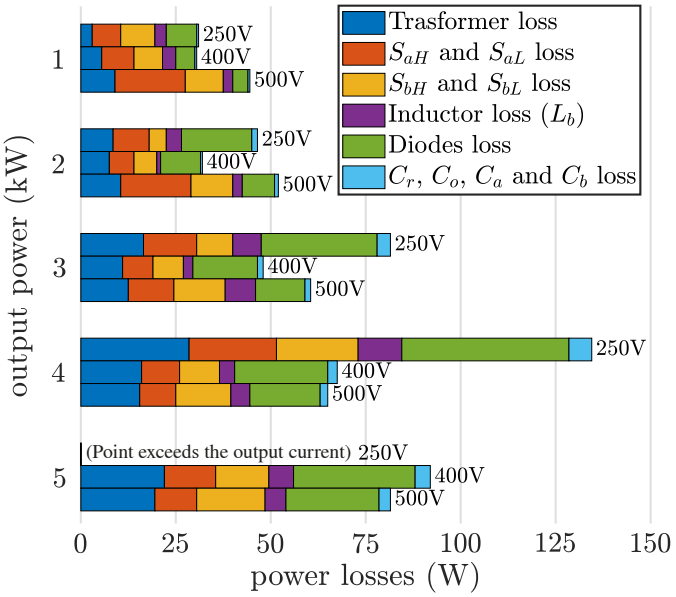


Fig. 10: Loss breakdown.

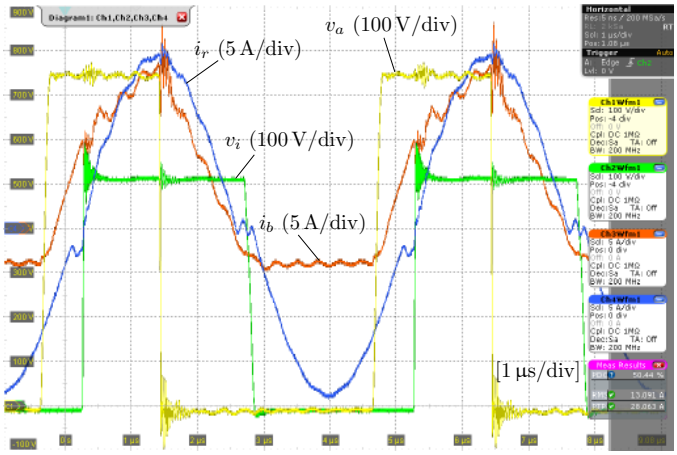


Fig. 11: Converter waveforms at $V_o = 250\,\mathrm{V}$, $P_o = 3\,\mathrm{kW}$. Soft-switching transitions, $\varphi = 0.2$.

for all the switches is achieved with an experimental, minimum phase-shift of 0.2, whereas the theoretical minimum phase-shift is 0.19 (see Fig. 6b). The complete set of minimum phase-shifts for ZVS at minimum output voltage is visible in Fig. 6b.

V. Conclusion

The work analyzes a two-stage topology composed of a pre-regulation stage with buck-boost features and a second stage based on the LLC converter. The two stages share part of the switching components. It is shown that, by a coordinated operation of the two stages, the switched currents can advantageously combine to have ZVS over a wide range of output voltages, while limiting rms currents. Experimental results on a 5-kW module show a peak efficiency of 98.0% at 3 kW transferred power. An output voltage range of 250-500 V is considered, which may be easily extended ≥ 1 kV by the series connection of more modules.

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