Stability and startup of non linear loop circuits

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Abstract. The reliable analysis of DC operating point in circuits with positive feedback topology is often challenging, and frequently performed with ad hoc methods. These techniques are often error prone and lead to the frequent use of sub-optimal or unnecessary additional circuits for the stabilization or determination of the operating point (startup circuits). We present a simple and reliable technique for the determination of "stable" circuit solutions, that is based on the use of available circuit simulators and hence takes advantage of accurate device models. The method has been experimentally validated on a self-biasing current generator fabricated with a standard 0.18 μm CMOS process.

Keywords: Self Biasing, Operation Point, Analog Circuits

1 Introduction

In the realm of electronic circuits containing active devices, the determination of the operating point is a basic step of the design process. It is one of the few engineering techniques requiring the solution of an inherently non-linear physical system. Since non-linear systems cannot generally be solved in closed form, the electronic designer has to resort to approximate solutions, numerical analysis tools or, sometimes, clever ad hoc tricks. In fact, this intrinsic non-linearity is seldom a problem, since most circuits are *designed* to have an operating point that can be easily determined.

However, some applications demand the use of circuits for which the computation of the operating point is non trivial. The typical case is a circuit with a positive feedback such as the well known Eccles-Jordan flip-flop. These circuits can have a few operating points, some of which "unstable". Due to the mentioned non-linearity, the analysis of these circuits can be challenging; furthermore, in this case commonly used circuit simulators, such as SPICE, often provide unreliable information, since they can converge to the "unstable" solution.

General methods have been developed for the non-linear analysis of active circuits[1–3], but are generally too abstract, provide poor physical insight on circuit operation, and are of little help to the circuit designer. As a consequence, non-linear circuits are usually analysed with simple pencil and paper methods[4].

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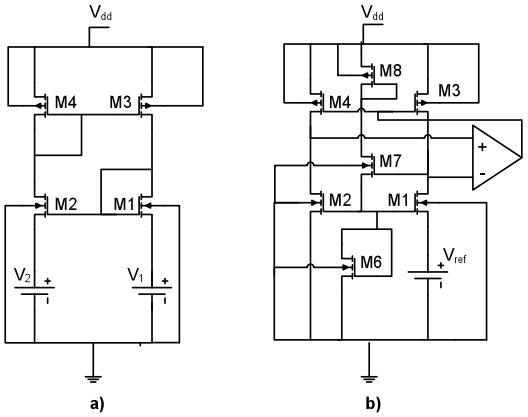

Fig. 1. Self-biased current generator: simplified proof of concept circuit (a) and complete circuit (b); M6, M7 and M8 are needed to set the bias point of M1 (a native transistor with negative threshold voltage); the operational amplifier imposes $V_{DS_{M3}} = V_{DS_{M4}}$ improving the accuracy of the upper current mirror; since in the complete circuit $V_2 = 0$ no generator is connected in series with M2.

These calculations are constrained to the use of crude first-level device models, which can lead to grossly approximated solutions, missed solutions and also to spurious solutions. Another common way to investigate the stability properties of circuits is the use of (time consuming) transient simulations, but these can also provide unreliable information in case of circuits with widely separated time constants (ill-conditioned systems). In order to overcome these shortcomings, we propose a method that is able to find the operating points and the stability properties of many commonly used non-linear feedback circuits.

2 Problem definition

A non-linear time-independent circuit (i.e., without capacitors and inductors) can be described with a system of equations $F(\mathbf{x}) = \mathbf{0}$, where the vector $\mathbf{x}$ is composed by node voltages and/or branch currents. The system can have an unknown number of solutions $\mathbf{x_i}$. Most circuits have only one solution, but circuits with more than one solution are well known. Eccles-Jordan circuits generally have three solutions, one of which is "unstable".

We must note that even the "stability" of the solution is not a well-defined concept. Solutions of time-independent circuits cannot be "stable" or "unstable". Indeed, unstable solution are not solutions at all. A formal definition of "stable solution" can be found in [5]: a solution of $F(\mathbf{x}) = \mathbf{0}$ is *potentially stable* if it is possible to build — adding capacitors between nodes and inductors in series to the branches of the given circuit — an augmented circuit which is *robustly stable* in the time domain. *Robustly stable* means that the stability is not compromised by the addition of another set of sufficiently small capacitors and inductors to

the given circuits (i.e. the values of the first set of capacitors and inductors must not be critical). Solutions which are not potentially stable are unstable.

Many non-linear circuits with more than one solution are based on a positive-feedback loop topology, like, for example, self-biased current generators, in which two current-controlled current generators are connected back-to-back in a positive-feedback loop. We will take this circuit as an example for illustrating the method (Fig.1a).

Transistors M3 and M4 form a linear current mirror, duplicating the current fed into the drain of M4 (I_{in_um}) onto the drain of M3 (I_{out_um}). This current mirror provides a linear relationship between its input and output:

$$I_{out\_um} = k_{um} I_{in\_um}, \tag{1}$$

where k_{um} depends on the geometry of M3 and M4. On the other hand, the lower mirror (M1, M2, V1, and V2) provides a nonlinear relationship between the input current (the drain current of M1, I_{in_lm}) and the output (the drain current of M2 I_{out_lm}):

$$I_{out\_lm} = f(I_{in\_lm}). \tag{2}$$

The ratio of the input to the output current k_{lm} depends on the input current. At equilibrium we must have

$$k_{um} = 1/k_{lm}. \tag{3}$$

If k_{lm} is a monotonic function of the input the (3) can be satisfied for a single set of circuit currents. However, as [4] points out, both mirrors of the circuit provide zero current when fed with a zero input and hence another equilibrium point exists, with all null currents (where k_{lm} is undefined). For this reason most designers of self-biased current generators include a startup circuit which forces the circuit to the desired solution, avoiding the zero-current one [6–8].

However, the above discussion is oversimplified. Simulating the circuit (with a UMC .18 μm CMOS technology, and with identically sized M3 and M4) we find that if $\beta_1 > \beta_2$ and $V_1 > V_2$, where $\beta_i = \mu C_{ox} W_i/L_i$ (W_i and L_i are transistor width and length, μ is carrier mobility and C_{ox} is the gate oxide capacitance per unit area) are referred to transistors M_i, the circuit undergoes a transient ending at the equilibrium point with non-zero currents. Hence, no startup circuit seems required. Instead, if $\beta_1 < \beta_2$ and $V_1 < V_2$ the circuit never settles in the equilibrium point suggested by eq.(3), and no startup circuit can help. For the other possible configurations ($\beta_1 < \beta_2$ and $V_1 > V_2$; $\beta_1 > \beta_2$ and $V_1 < V_2$) eq. (3) is never verified and no equilibrium point is possible.

3 Proposed solution

To solve this problem we developed a technique that provides valuable information on the equilibrium points of nonlinear circuit. If we can consider a nonlinear circuit as a closed loop of nonlinear blocks (Fig. 2a), we can cut open the loop

and insert the circuitry shown in Fig. 2b. Even if the method can be adapted to cuts in any branch, we will discuss only the most useful case, when the current flowing in the severed branch is non zero. The case of zero current is indeed simpler, but less general. The independent current source sends in the circuit a test current I_t which gives rise to a voltage V_p across its terminals. The voltage-controlled generator imposes the same voltage V_p to node B, the other end of the cut loop. Obviously, when the current I_v sinked by the voltage generator is equal to I_t, the original uncut circuit is in equilibrium. The two sides of the cut could be directly connected without altering the branch currents and the node voltages. Hence if we plot I_v vs. I_t, equilibrium points can be identified as the intersections between the $I_v(I_t)$ curve and the $I_v = I_t$ line. In addition, the derivative $\partial I_v/\partial I_t = \lambda$ at the equilibrium point enables us to determine the stability of the equilibrium point.

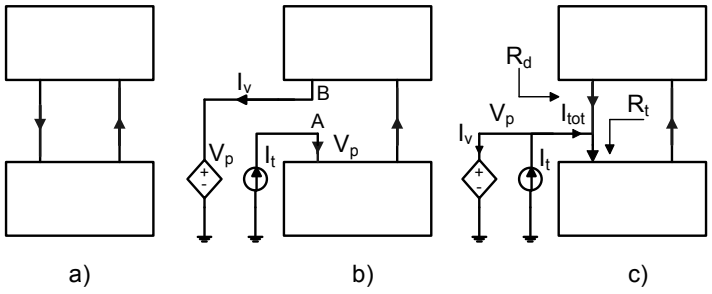

Fig. 2. Non-linear loop analysis

Let us call R_t the differential resistance seen by the I_t generator: if the test current increases by ΔI_t, the voltage V_p increases by $\Delta V_p = R_t \Delta I_t$. The current I_v, instead, increases by $\Delta I_v = \lambda \Delta I_t$. Since the nodes A and B are at the same voltage, we connect them and redraw the circuit as in Fig. 2c. The total differential resistance seen between nodes $A \equiv B$ and ground (as shown in Fig. 2c) can be written as:

$$R_d = \frac{\Delta V_p}{\Delta I_{tot}} = \frac{R_t \Delta I_t}{\Delta I_t - \lambda \Delta I_t} = \frac{R_t}{1 - \lambda} \tag{4}$$

where ΔI_{tot} is indicated in Fig. 2c. From (4) we can conclude that if $\lambda > 1$ this solution is unstable. Let us underline that we assumed $R_t > 0$, which is the typical situation is practical circuits, but the method can in theory be easily generalized to any initial sign of R_t. Furthermore, λ is the small-signal DC loop gain, and hence the fact that values in excess of 1 lead to instability is well known.

Hence, the practical application of the method consists of cutting open a loop, inserting the proper generators and performing a DC simulation of the circuit with an input current sweep. The analysis of circuit Fig. (1a) (for which

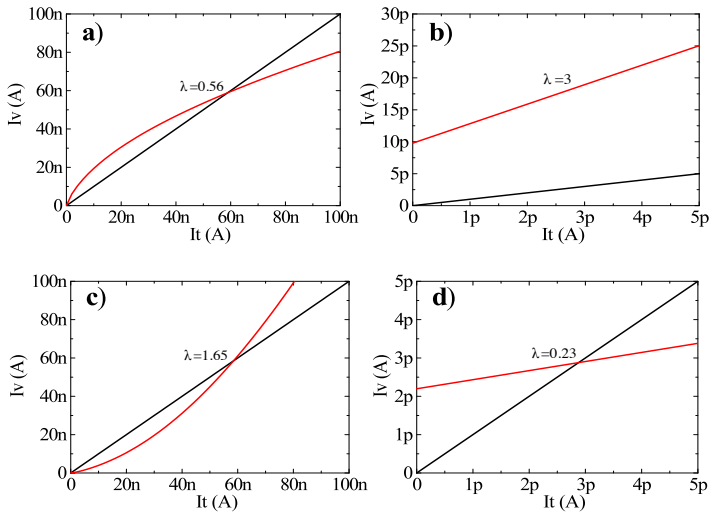

Fig. 3. SPECTRE dc sweep of circuit of Fig. 1, cut at the drain of M3: current generator to gate-drain of M1, voltage generator to M3 drain. $\beta_1 > \beta_2$ and $V_1 > V_2$(a); particular of low current region (b); $\beta_1 < \beta_2$ and $V_1 < V_2$(c); particular of low current region (d) (λ is the derivative of the current at the intersection; the black straight lines are $I_V = I_t$, while the red lines show the simulation results.

is $R_t > 0$) leads to the results of Figures 3a-b, which show that a single and stable operating point is obtained only for $\beta_1 > \beta_2$ and $V_1 > V_2$. It is worth noticing that in this case no equilibrium point exist at $I_t = 0$ and hence no startup circuitry is needed. Figures 3c-d show instead that for $\beta_1 < \beta_2$ and $V_1 < V_2$ the solution is unstable, and another stable solution is present for very small currents. Therefore, with the use a circuit simulator equipped with accurate device models we can learn that often some pencil-and-paper results, such as the zero-current stable solution, can indeed be artifacts due to the use of too simplistic device models.

Furthermore, this approach provides valuable physical insights on the circuit. Since the $I_v(I_t)$ relationship provided by the simulations can be interpreted as the input-output characteristic of an amplifier, a designer can usually devise modifications to the circuit which can modify it in a foreseeable manner. Hence, the above analysis not only can provide evidence of bias or stability problems, but is also a tool for their solution.

The circuit of Fig. 1(b) has been designed and fabricated, using native transistors (with threshold voltage < 0) for M1 and M2. In this version of the circuit M1 was not diode-connected and a proper bias circuit was added in order to bias M1 in saturation. V_1 and V_2 were set to 335 mV and 0, respectively. Using the proposed method, we obtained the results of Fig. 4(left). The current in M1 is about 7 nA, and the operating point is stable. This is confirmed by measurements

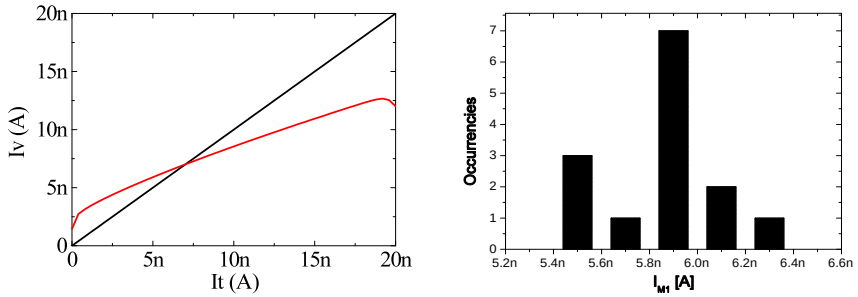

Fig. 4. I_v vs. I_t for the complete circuit of Fig. 1(b) (left) and I_{M1} distribution in 14 samples of the Fig.1(b) circuit (right).

on 15 samples realized in a 0.18 μm UMC CMOS technology. Fig.4(right) shows the current distribution in 14 working samples; the mean current is 5.85 nA ($\sigma = 0.24$ nA) and no start up problems were observed.

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