CHARACTERIZATION OF THE SUBSTRATE NOISE SPECTRUM FOR MIXED-SIGNAL ICs

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ABSTRACT

This paper presents a simplified analytical model of the substrate noise generated by digital circuitry that captures the most relevant frequency domain characteristics and relates them with parameters of the digital circuit and the package. Simulations and experimental results are used to validate the analytical model.

1. INTRODUCTION

The integration of digital and analog circuits in the same silicon die is conditioned and limited by the noise levels generated in the digital section in conjunction with the increasingly demanding performance requirements of the analog and Radio Frequency (RF) sections. Despite these difficulties, there is a strong trend towards the CMOS mixed-signal integration of the whole system in a single chip. In this context, substrate noise coupling from digital to analog/RF sections is one of the most important issues to solve. Though the digital and analog sections of the chip employ different power supply connections, the digital noise is transmitted through the substrate to the analog sensitive circuitry, degrading its performance [1,2]. Many analog and RF circuits operate in narrow frequency bands. A strategy to reduce noise impact is to reduce it in these frequency bands. This motivates our study of the relation between the digital noise and the factors that determine its spectral characteristics.

Substrate noise power spectrum, $S_N(\omega)$, can be defined as a linear transformation of the switching current demanded by digital gates $I_s(t)$, which spectrum is $S_{Is}(\omega)$. The linear transformation is formulated by the substrate noise transfer function $H(\omega)$, from the digital power supply nodes to the victim substrate node,

$$S_N(\omega) = S_I(\omega) \cdot \left|H(\omega)\right|^2 . \qquad (1)$$

The analysis of the substrate noise spectrum can be divided in the analysis of each of the terms of (1): $S_{Is}(\omega)$ and $H(\omega)$, where the latter term depends on the IC+package parasitic component values and the former term depends on the statistics of the input vectors sequence, the deterministic characteristics of the individual current waveforms of the gates and the digital circuit topology.

2. DIGITAL SWITCHING CURRENT SPECTRUM

The digital switching current waveform can be considered a random process, where each pair of successive input vectors (that constitute a *transition vector*) selects one among the elements of the ensemble of all the possible switching current waveforms of the digital circuit.

2.1 Switching current spectral analysis using Markov Chains

Since the second input vector of a transition vector will be the initial condition for the next transition vector, the stochastic process representing the switching current waveform has a memory effect. Markov Chains can be used to model this type of processes [3,4]. In this context, each possible transition vector is considered a state of the system. For an N input digital circuit, there are $K = 2^{2N}$ possible states. Each state s_i, $1 \le i \le K$, has an associated switching current waveform $g_i(t)$ and a probability of state occurrence p_i. The expected current waveform for this random process is the ensemble average, given by

$$\mu_g(t) = \sum_{i=1}^{K} p_i g_i(t) , \qquad (2)$$

and the probabilistic *variance waveform* is defined as:

$$\sigma_g^2(t) = \sum_{i=1}^{K} p_i g_i^2(t) - \mu_g^2(t) . \qquad (3)$$

From a given present state, there are only 2^N allowed future states, due to the memory characteristic. The state probabilities and their associated transition probabilities are combined into a single matrix that models the overall system: the *state transition probability matrix* **P**. This matrix is composed of $K \times K$ elements. Each element p_{ij} represents the conditional probability of future state j being the current state i, $\mathbf{P}(i,j) = P\left\{s_j \left| s_i \right.\right\}$. The PSD of a signal generated by a system with memory modeled by a Markov Chain using a state transition probabilities matrix **P** is, [4]:

$$S(f)=\frac{1}{T}\sum_{i=1}^{K}p_i\left|\widetilde{G}_i(f)\right|^2+\frac{2}{T}\mathbb{R}\left[\sum_{i=1}^{K}\sum_{j=1}^{K}p_i\widetilde{G}_i^*(f)\widetilde{G}_j(f)P_{ij}(f)\right] \quad (4)$$
$$+\frac{1}{T^2}\sum_{m=-\infty}^{+\infty}\left|\sum_{i=1}^{K}p_iG_i\left(\frac{m}{T}\right)\right|^2\delta\left(f-\frac{m}{T}\right)=S_{cont}(f)+S_{disc}(f)$$

In the above expression the dependence on the current waveforms and its probabilities is explicitly shown. The last term of (4) is a discrete spectrum, $S_{disc}(f)$. The two first terms form a continuous spectrum, $S_{cont}(f)$, which corresponds to the Fourier transform of the switching current covariance function. The $\widetilde{G}_i(f)$ functions are the Fourier transform of $\tilde{g}_i(t)$, defined as the departure-from-the-mean of the current waveform for each state:

$$\tilde{g}_i(t)=g_i(t)-\sum_{j=1}^{K}p_jg_j(t)\,. \quad (5)$$

The middle term of (4) incorporates temporal correlations due to memory effects through the state transition probabilities represented by $P_{ij}(f)$, defined as:

$$P_{ij}(f)=\sum_{n=1}^{+\infty}p_{ij}(n)\exp(-j2\pi nfT)\,, \quad (6)$$

where $p_{ij}(n)$ denotes the probability that current waveform $g_j(t)$ happens n cycles after current waveform $g_i(t)$. These probabilities are the elements of the n^{th} power of the state transition probabilities matrix $\mathbf{P}^n$. Note that $p_{ij}(1) = p_{ij}$. When memory effects are ignored the switching current PSD of (4) simplifies to:

$$S(f)\approx\frac{1}{T}\sum_{i=1}^{K}p_i\left|\widetilde{G}_i(f)\right|^2+\frac{1}{T^2}\sum_{m=-\infty}^{+\infty}\left|\sum_{i=1}^{K}p_iG_i\left(\frac{m}{T}\right)\right|^2\delta\left(f-\frac{m}{T}\right) \quad (7)$$

This expression summarizes two important characteristics of the switching current spectrum: 1) it is composed by two terms: an *impulse train term* with an envelope that corresponds to the squared modulus of the Fourier transform of the ensemble average current waveform, and a *continuous term*, which in this simplified expression is completely determined by the averaged summation of the $\tilde{g}_i(t)$ waveforms spectra; 2) the dependence of these two terms with the digital switching frequency is different: the continuous term power scales linearly with the digital switching frequency whereas the impulse train term power scales quadratically with it.

The switching current PSD (4) can be normalized, resorting to the following expression:

$$S(f)=\sigma_0^2S_{C_{II}}^{norm}(f)+\frac{\mu_0^2}{T}\sum_{m=-\infty}^{+\infty}S_{R_{\mu\mu}}^{norm}\left(\frac{m}{T}\right)\delta\left(f-\frac{m}{T}\right), \quad (8)$$

where μ_0^2 and σ_0^2 are the RMS values of the expected current waveform and the variance waveform, respectively, and $S_{C_{II}}^{norm}(f)$ and $S_{R_{\mu\mu}}^{norm}(f)$ are the normalized PSD of the covariance function and the expected waveform autocorrelation function, respectively. Considering that the normalized versions of the covariance PSD and the mean waveform PSD have a similar magnitude although they may have different spectral profiles, the relative level of the discrete term with respect to the continuous term can be approximated, for low frequencies by:

$$\frac{S_{disc}(f)}{S_{cont}(f)}\approx\frac{1}{T}\cdot\frac{\mu_0^2}{\sigma_0^2}=\frac{1}{T}\cdot\frac{R_{\mu\mu}(0)}{R_{\sigma\sigma}(0)}\,, \quad (9)$$

2.2 Generalized current waveforms

Some general characteristics of the digital switching current spectrum can be derived from generalized current waveforms matched to the expected current waveform. In [2] the ensemble average of the switching current waveform of typical digital circuits is generalized using an exponential waveform given by:

$$\overline{I_s(t)}=K\left[\exp\left(-t/t_f\right)-\exp\left(-t/t_r\right)\right],\ 0\le t\le T\,, \quad (10)$$

where K is an amplitude parameter and t_f and t_r are the fall and rise time parameters, respectively. This time expression has the following Laplace Transform representation:

$$\overline{I_s(s)}=\frac{K\left(1/t_r-1/t_f\right)}{\left(s+1/t_f\right)\left(s+1/t_r\right)}\,, \quad (11)$$

that corresponds to an over-damped 2nd order system, having two poles with real roots. Another expected current waveform model widely employed consists on a triangle.

3. SUBSTRATE NOISE TRANSFER FUNCTION

The substrate noise transfer function, H(ω) from the current source to the victim node *Vxf* is derived from the circuit model of Fig. 1. This circuit model captures the most relevant elements necessary to characterize the digital circuit noise generation [5]. It is composed of three sections: the package and power supply rails, the active elements of the digital circuitry (the circuit network) and the substrate network. The circuit network consists of a current source, Ic(t), that represents the digital circuit switching current waveform and a set of parasitic elements, Rcir and Ccir, that model the non-switching gates parasitics as a complex impedance. The substrate network is composed by the digital substrate to digital ground impedance Rc, VDD to substrate impedances Rwell and Cwell due to the wells, and the substrate

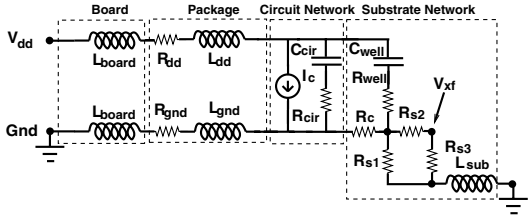

Figure 1. Macromodel of DAC test chip.

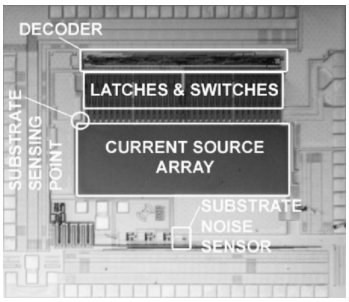

Figure 2. DAC test chip floorplan.

impedance between the aggressor digital circuit and the victim circuit substrate node and other nodes of the substrate: Rs1, Rs2 and Rs3. In most cases substrate is biased in the analog section by a connection to the analog ground, and therefore Lsub represents the package model of the connections from on-chip analog ground to board ground. Table 1 shows the components values for a test circuit shown in Fig. 2:

Table 1. Macromodel Components

Comp.	Value	Comp.	Value
R_{dd}=R_{gnd}	14.28	R_{s3}	838.0 Ω
R_c	100.0	L_{sub}	1.200 nH
R_{well}	750.0	L_{vdd}	1.642 nH
R_{cir}	240.0	L_{gnd}	1.773 nH
R_{s1}	39.59 Ω	C_{well}	31.63 pF
R_{s2}	2075 Ω	C_{cir}	1131.1 pF

4. TEST CHIP IMPLEMENTATION AND EXPERIMENTAL RESULTS

A test chip (DAC, Fig. 2) has been used to validate experimentally the substrate noise spectrum analytical model results.

4.1 Chip-Level Model Implementation

The DAC test chip has been fabricated in a 0.35µm CMOS process on high-resistivity (10Ω/cm^2) p-substrate and encapsulated in a CQFP64 package. In this work, only the combinational decoder of the DAC is activated. This circuit connected directly to the chip inputs allows a direct control of the input sequence to study its implications on the substrate noise continuous PSD term. The test chip contains a substrate sensor, which is based on a two stage amplifier with low gain (3.4 dB), but enough BW to measure substrate noise up to 1 GHz.

The substrate noise transfer function is derived from the chip-level macromodel of the test IC shown in Fig. 1. The PCB, package, and IC different parasitics elements that contribute to the overall V_{DD}-V_{SS} impedance have been taken into account to calculate the model component

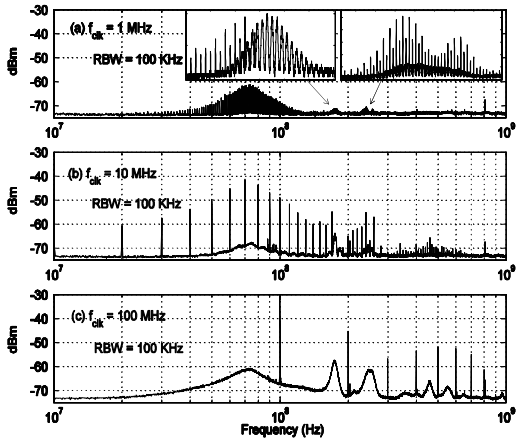

Figure 4. DAC substrate noise PSD for different

values. Guard rings in the analog section have been also considered. The substrate resistances have been obtained with SubstrateStorm tool from Cadence.

4.2 Experimental Results

Fig. 3 shows the substrate noise measured at the substrate sensor output using a spectrum analyzer. Resonance peaks at 74.6 MHz, 176 MHz and 250 MHz are observed. The first one coincides with the IC model resonance. It raises the substrate noise level when it is excited by switching current of the digital decoder. The second and third resonances (zoomed in Fig. 3(a)) are due to the data pattern generator used in the experiment. We consider these resonance peaks as measurement artifacts, and therefore they are not included in the noise generation model. One of the most important characteristics of the substrate noise power spectral density is its strong dependence on the digital circuit clock frequency or data rate. In Fig. 3, the continuous and discrete terms scale by $1/T_{clk}$ and $1/T_{clk}^2$, respectively, as it is predicted by (4).

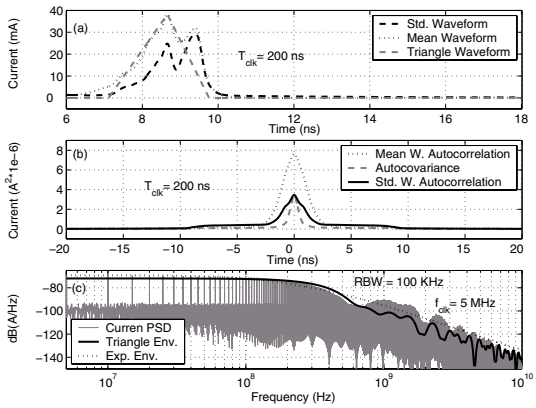

Figure 3. Simulation Results: (a) Time domain representation of mean, std. deviation and triangular current waveforms. (b) Autocorrelation waveforms. (c) current waveforms spectra.

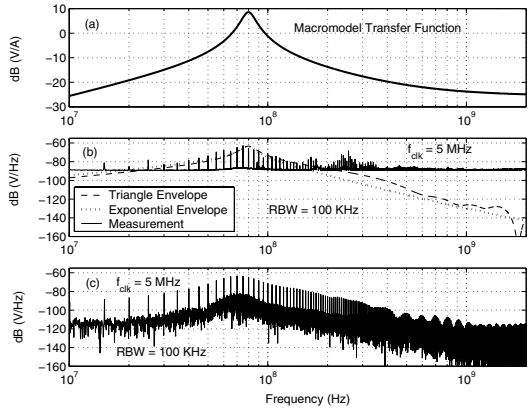

Figure 5. (a) DAC chip substrate noise transfer function (b) Experimental and model substrate noise PSD comparison. (c) Full layout transistor level simulation.

According to the theoretical development of section 2, the most important characteristics of the substrate noise spectrum can be calculated from the digital circuit activity and the whole chip model. First, the statistical characteristics of the IC digital section switching current are obtained from time domain simulations using a long pseudorandom sequence of input vectors applied with a cycle time of 200 ns (data rate = 5 MHz). Fig. 4(a) shows the mean and standard deviation current waveforms for the DAC input decoder and Fig. 4(b) the mean waveform autocorrelation, the $\tilde{g}(t)$ waveform covariance, and the standard deviation waveform autocorrelation. From these data we obtain the mean and the standard deviation waveforms RMS values μ_0 = 2.77 mA and σ_0 = 1.86 mA, respectively. These data implies that the relative level between the continuous and discrete terms of the power spectra predicted by (9) yields a difference of 70.44 dB between the two terms, which closely matches the 73.5 dB of difference[1] observed at the first impulse frequency on the current PSD graph of Fig. 4(c).

An additional investigation that has been carried out is about the accuracy of simplistic models of the substrate noise discrete term. These models use triangular or exponential waveform, matched to the expected current waveform.

Secondly, the substrate noise transfer function is calculated from the simplified circuit model of the whole chip. Fig 5(a) shows the substrate noise transfer function from the digital power supply current to the sensing point of the test chip labeled *Vxf* in Fig. 1. Fig. 5(b) shows the product of this transfer function and the spectral envelope of the two expected current waveform models (triangular and exponential), superimposed to the experimental substrate noise spectrum measured for a data rate of 5 MHz. The experimental data is limited by the maximum spectrum analyzer noise floor. The results shown in Fig. 5(c) correspond to a full chip transistor level simulation including a substrate model. These results allow extending the model validation to low and high frequencies, where the substrate noise PSD is below the spectrum analyzer noise floor.

[1] Note that 50 dB has been added to the discrete term value since RBW = 100KHz.

5. CONCLUSION

In this work, the frequency domain behavior of the substrate noise generated by the digital section of a mixed-signal IC has been analyzed. We have derived a simple but general analytical expression that captures the most relevant characteristics of substrate noise and relates them with circuit and design parameters. Substrate noise spectrum is composed of a discrete and a continuous term. Both terms are derived from the aggressor digital circuit current supply waveform. The spectrum of this waveform is shaped by the transfer function from the power supply nodes to the substrate node of interest to produce the final substrate noise spectrum. The modeling and analysis process has been applied to a mixed-signal circuit and a good agreement is achieved between model expressions, experimental measurements and full layout transistor level simulations (including a substrate model).

6. ACKNOWLEGMENT

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