A Low-Power RF Front-End for 2.5 GHz Receivers

L. Moreno[1], D. Gómez[1], J.L. González[1], D. Mateo[1], X. Aragonès[1], R. Berenguer[2], H. Solar[2]

[1]Electronic Engineering Department
Universitat Politècnica de Catalunya
Barcelona, Spain
jl.gonzalez@upc.edu

[2]Centro de Estudios e Investigaciones Técnicas de Gipúzcoa
RFIC Design Group
San Sebastián, Spain
rberenguer@ceit.es

***Abstract*—This paper presents a low power and low cost front end for a direct conversion 2.5 GHz ISM band receiver composed of a 16 kV HBM ESD protected LNA, differential Gilbert-cell mixers, and high-pass filters for DC offset cancellation. The whole front-end is implemented in a 2P6M 0.18 μm RFCMOS process. It exhibits a voltage gain of 24dB and a SSB noise figure of 8.4dB which make it suitable for most of the 2.5 GHz wireless short-range communication transceivers. The achieved power consumption is only 1.06mW from a 1.2V power supply.**

I. INTRODUCTION

The 2.5 ISM band is very suitable for new wireless short-range communication applications requiring very low-power devices [1]. The radios for such applications require extremely low-power operation. This paper presents a low-cost implementation of the RF front-end of a low-power direct conversion receiver using frequency shift-keying (FSK) for the 2.5 GHz ISM band. The direct conversion receiver (DCR) architecture is selected for its simplicity and low power consumption [2]. However two important drawbacks must be overcome: output DC offset and flicker noise. In the proposed receiver those issues are solved by using DC blocking capacitors between the LNA and the mixer inputs and by inserting a high-pass filter (HPF) at the output of the mixer. System simulations show that cut-off frequencies below 25 kHz do not highly degrade SNR and receiver BER, since the FSK modulated signal presents low energy around DC whereas flicker noise content is significantly large around DC.

Section II describes the front-end architecture and the designed RF circuits. Performed measurements and achieved power consumption is reported in section III. Section IV deals with the gain switching circuitry in order to improve dynamic range of the receiver. Finally section V discusses substrate noise related issues since the radio will be integrated along with a noisy digital section.

II. FRONT-END BLOCKS

Fig. 1 shows the receiver block diagram. It is composed of a single-ended LNA connected to two fully differential double-balanced down-conversion mixers for I/Q signal

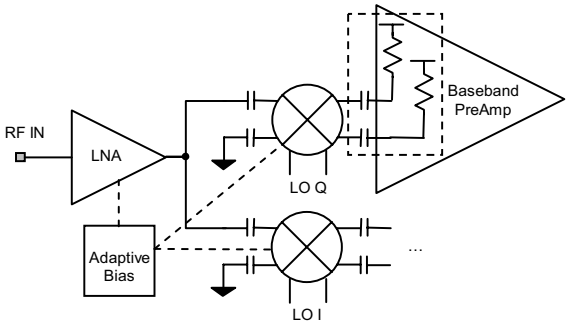

Figure 1. Direct conversion receiver front-end.

generation. The DC canceling HPF is implemented by reusing the biasing resistors of the baseband section pre-amplifiers (or the channel filters input stage) along with series capacitors at the output of the mixers.

A. LNA

The single-ended, inductively degenerated common source amplifier topology was selected for the LNA (see Fig. 2), which avoids the use of a transformer at the input and minimizes the power consumption and occupied area. Its input section has been optimized to minimize the amplifier noise figure. 50-Ohms input matching has been implemented with a Π network composed by the LNA gate inductor and the parasitic capacitance of the ESD protection diodes. This way input matching and ESD protection are obtained at the same time. Those diodes are implemented with p+/n-well and n+/p-sub diodes and exhibit a quality factor of around 75 in reverse mode operation. Due to ESD requirements, the big diodes dimensions degrade the noise figure of the LNA, but since they, as well as the input pad parasitics, are incorporated from the beginning in the optimization process such negative effect is minimized. LNA ESD protection is completed by the inclusion of several power clamps between V_{DD} and ground to avoid reverse operation of the diodes during ESD stress in the PS and ND operation modes [3]. The output section is implemented with a cascode stage and a choke inductor that resonates with the capacitive input impedance of the mixers. For the gate and source inductors, an optimized layout has

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been used with decreasing stripe width in the direction to the center of the spiral for maximizing the quality factor [4], which is 16.9 and 19, respectively. A not optimized, less area consuming inductor is used at the output.

Aggressive biasing is used in the LNA input transistor (and the mixer transconductors as well) to obtain very low power consumption, resulting in an overdrive voltage of only 40 mV. Such a low overdrive voltage would compromise the linearity and the performance with temperature and process variations. Innovative adaptive biasing system that simultaneously compensates temperature and process variations [5], and a dual gain mode, detailed in section IV, allows extending the dynamic range of the front-end.

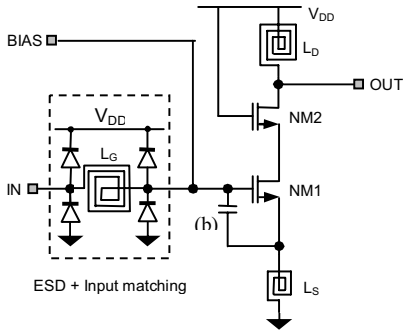

Figure 2. Schematic of the single ended LNA with ESD protections.

B. Mixer and DC blocking high-pass filter

The mixer has a conventional double balanced topology (see Fig. 3) with bleeding current sources implemented using PMOS transistors connected to the common source of the differential switches [6]. The biasing of the bleeding transistors is adjusted to optimize the gain and NF. The two differential RF inputs are connected to the LNA and ground, respectively, using 3 pF DC blocking capacitors. The output section includes a resistive load in parallel with a capacitor to additionally reject the LO. The mixer outputs are connected to a large series capacitor of 62.3 pF implemented with two stacked MIM capacitors occupying a total area of 200 μm × 100 μm (note that four of such capacitors are needed, one at each differential output of the I and Q mixers). They form a high-pass filter along with the bias resistors of the following amplifier with a cut-off frequency of 15 kHz.

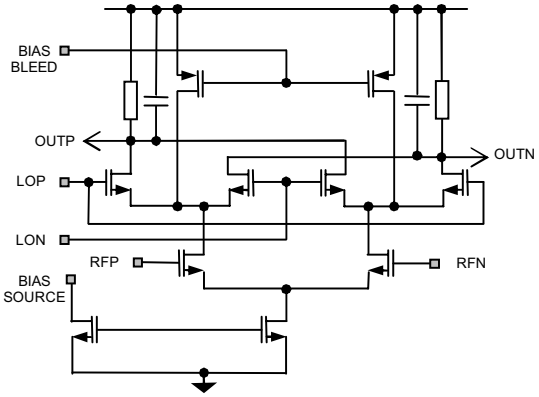

Figure 3. Schematic of the double-balanced mixer.

III. Experimental Results

The front end has been implemented in a test chip shown in Fig. 4. Only one of the two mixers has been fabricated. The loading effects of the other one is modeled with an on-chip capacitor that mimics the mixer input impedance. The baseband preamplifier is substituted by an output buffer to drive the external 50 Ohms loads. The two first big LNA ESD diodes are placed around the RF IN pad, and the other two between L_D and L_G as shown in Fig.4. Those diodes and the mentioned power clamps provide a measured ESD protection level at RF_IN of the LNA higher than +16kV according to the HBM ESD MIL-STD 883 test standard. Both leakage and power supply currents were monitored after each ESD stress pulse. Fig. 5 shows the measured leakage current of the RF input for different ESD stress levels. As it can be noticed, no damage is observed in the ESD devices and the RF input transistor of the LNA. The total chip area is 1.1×1.0 mm^2 (excluding pads). The chip is measured using on-wafer probes. The LNA is implemented also in another test chip with a 50 Ohms passive output matching network instead of the mixer, which allows the characterization of the LNA alone. The results from the LNA characterization provide a NF of 4.3 dB, a S_{11} and S_{21} of -23 dB and 1 dB, respectively, at 2.45 GHz, with a power consumption of 550 μA drawn from a 1.2 V power supply. The CP1dB and IIP3 are -4.1 dBm and 1 dBm, respectively. The low S_{21} obtained is due to the fact that that the LNA output is optimized for matching the mixer input and not to the passive 50 Ohms output network used in the LNA alone test chip.

Since the previous results were quite good, the bias voltage of the LNA used in the front-end test chips was reduced even more. The total current consumption of the front end was set to 608.4 μA, from which 341.7 μA correspond to the LNA and 266.6 μA to the mixer. Since there will be two mixers in the final front-end the total power consumption would be 1.06 mW for V_{DD} = 1.2 V.

The complete front end measured conversion gain and NF for various mixer bleeding bias voltage (*V_BLEED*) is shown in Fig. 6 for an IF frequency of 10 MHz, which was the minimum frequency of the noise figure measuring system (Agilent PSA E4443A + MAURY MICROWAVE MT7618E

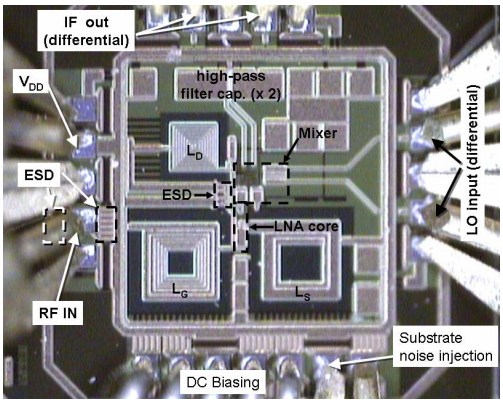

Figure 4. Test chip including the receiver front-end.

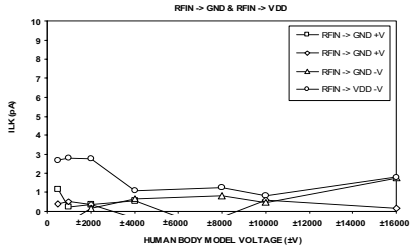

Figure 5. Leakege current measurments after ESD stress.

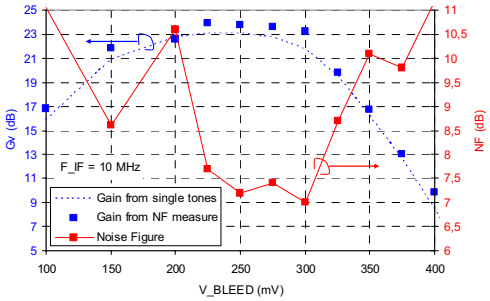

Figure 6. Front-end gain and measured DSB NF at IF = 10 MHz .

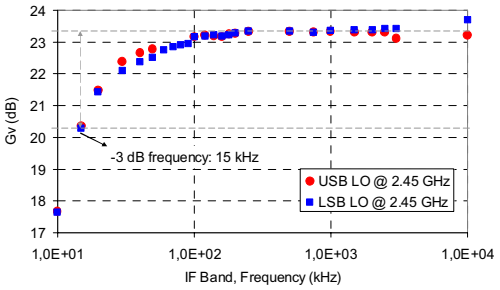

Figure 7. Measured front end conversion gain for the band central channel.

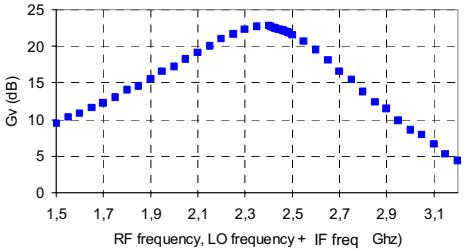

Figure 8. Front-end conversion gain *vs* RF in frequency.

noise source). The noise figure measurement uncertainty was 0.9 dB. Nevertheless, since a good agreement between simulation and measurements is obtained, full chip extracted simulations results are used to extend the NF analysis to lower output frequencies. The simulated NF for the optimum *V_BLEED* at 1MHz output frequency is 8.9 dB. The front-end conversion gain, corrected with the losses of the 50 Ohms output buffer, is shown in Fig. 7 and 8, for a sweep of IF and RF frequencies, respectively. Fig. 7 shows the symmetry between the two sidebands of the mixer and the cut-off frequency of the HP filter. Fig. 8 shows that the gain variation across all the 2.5 GHz ISM band is ±0.4 dB. CP1dB and IIP3 are found to be -30.5 dBm and -21.5dBm, respectively. Since the LNA is single ended, the IIP2 is also measured, resulting in -5.0 dBm. All these measurements have been done with a LO power of -9 dBm, which was found to be the optimum oscillator amplitude value. The oscillator is connected to the differential chip LO pads using an RF balun and differential GSGSG probes. After correcting the balun and cable losses and using the measured mixer input port LO impedance (obtained with a Network Analyzer) the differential LO signal amplitude corresponding to the -9 dBm provided by the generator is 246.22 mV_p. The RF to IF and LO to IF isolations were also measured. Table I summarizes the results.

TABLE I. SUMMARY OF THE RECEIVER FRONT-END RESULTS

Parameter	***Value***	***Parameter***	***Value***
Power consumption	1.06 mW	Power cons. LNA	410 µW
S_{11} @ 2.45 GHz	-20 dB	G_v @ V_{LO}=246 mV	22.5 ±0.4 dB
NF @ IF =10 MHz (measured)	7 dB	NF @ 1MHz (simulated)	8.9 dB
CP1dB	-30.5 dBm	IIP3 IIP2	-21.0 dBm -5.0 dBm
LO to RF isolation	-70 ±2 dB	LO to IF isolation	-44 ±2 dB

Specifically in terms of power consumption, the whole RF front-end of the presented receiver uses just 1.06mW. The baseband circuitry power consumption (not shown in this work) is 2.26mW, what gives a total of 3.32mW for the whole receiver chain, while receivers of other 1Mbps "cable replacement" radios use much more power: 5.4mW [8], 10mW [9] or 9mW [10].

IV. GAIN SWITCHING CIRCUITRY

The aggressive biasing approach used to achieve a very-low power consumption results in a lower than required CP1dB. In order to increase the receiver dynamic range, a gain switching strategy was devised to cut-down 20 dB the front-end gain. This technique is implemented by commutating the biasing resistor of the mixer RF inputs.

All the capacitive impedance of that node will be resonated by the LNA drain inductor (L_D). Therefore, the LNA voltage gain is set by the product of the LNA tranconductance and the parallel combination of the L_D inductor losses, the real parts of the mixer input impedance and LNA drain output impedance, and the biasing resistors connected at the mixer RF input transistors gates. By switching the mixer RF input biasing resistors between a lower and higher value, the gain is changed from a low to a high value.

The lower value resistor is implemented with a NMOS transistor biased in linear region (see Fig. 9) when the digital gain switching control signal is 'high'. For the 'low' level the transistor is in weak inversion, offering a large drain-to-source resistance. Since the switching transistor adds some parasitic

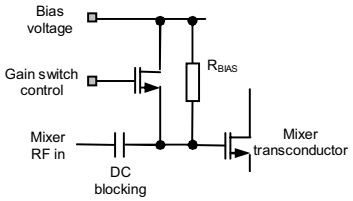

Figure 9. Gain switching circuitry at the biasing of the mixer RF input.

capacitance, the output section of the LNA was resized to resonate this additional capacitance as well. Fig. 10 shows the simulated conversion gain (G_v) in the two modes. In the lower gain mode, the CP1dB is increased up to -13 dBm at the expenses of a NF @ 1 MHz of 22.4 dB.

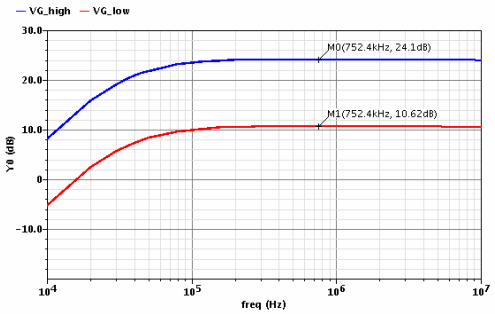

Figure 10. Simulated dual gain of the receiver front end.

V. Substrate Noise Impact on the LNA

The substrate noise spectrum generated by the digital radio is composed of harmonics at multiples of the clock frequency, that in our case is 16 MHz, and it extends up to a few hundreds of MHz. There is also a continuous term between the noise harmonics due to random logic activity that may be important at low frequencies [6]. The LNA will be operating at 2.45 GHz, far away from the most important substrate noise harmonics. However, substrate noise at low frequencies can mix with strong interferers in adjacent channels due to non linearities in the LNA. The result of this mixing are intermodulation products that appear at the LNA output as co-channel interference. We have performed an innovative experiment to evaluate the sensitivity of the single ended LNA to substrate noise harmonics. The maximum allowable substrate noise has been experimentally determined in the LNA alone test-chip[1], by injecting a low frequency noise tone in the substrate through a dedicated pad connected to a p+ diffusion, while driving the LNA input with an interferer. Fig. 10 shows a measurement of the LNA output when a 16 MHz tone (emulating the first harmonic of the clock) is injected into the substrate and a strong interferer located at 16 MHz from the wanted channel is fed into the LNA input. The interferer power is set to -40 dBm, a reasonable maximum allowable power for adjacent channels at > 3MHz separation. The combination of the low frequency substrate noise tone and the interference produces an intermodulation product at the frequency of the wanted channel that, when measured at the output, must be smaller than -88 dBm + G_v to fulfill a typical co-channel interference spec. Our experiment showed that, to reach this limit, the substrate tone generator must deliver as much as 14 dBm of output power, which corresponds to more than 1 V_{rms} at the substrate. Given that these are not realistic levels for substrate noise, we conclude that the proposed LNA, even being single-ended, would not be affected significantly by substrate noise, and a differential architecture is therefore not needed.

[1] Due to a modelling error in the passive output matching network, the LNA alone test chip has a peak gain at a frequency lower than expected.

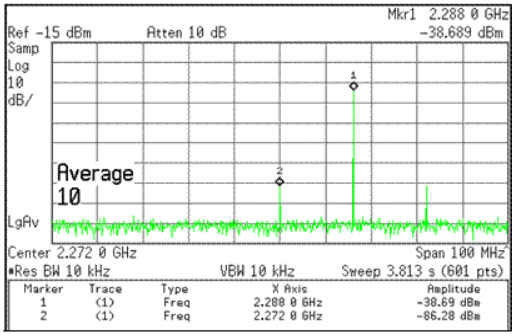

Figure 11. Co-channel interference generated by an intermodulation of adjacent channel interference and low frequency substrate noise.

VI. Conclusions

In this paper a RF receiver front-end implementation in 0.18 µm CMOS process for low-power 2.5 GHz radio standards is presented. The low power consumption required for such radios is achieved using a direct-conversion architecture composed of a single ended LNA and double-balanced active mixers. DC-offset and flicker noise problems are solved using and on-chip high-pass filter. The LNA input includes the ESD diodes that are re-used to implement a Π matching network along with the input transistor gate inductor. The bias circuitry of the active mixers is also re-used to implement a dual-gain control mode that reduces by 15 dB the overall voltage conversion gain of the receiver front-end, which relaxes linearity requirement for strong input signals. The overall power consumption is 1.06 mW, outperforming the existing literature for low power radios at 2.5 GHz.

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