Comparison of Modulations and Dc-Link Balance Control Strategies for a Multibattery Charger System Based on a Three-Level Dual-Active-Bridge Power Converter

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***Abstract*— This paper focuses on the study of a charger for two batteries connected in series. From the three-phase grid, the batteries are charged through a three-level neutral-point-clamped (NPC) ac-dc converter in cascade with a three-level NPC dual-active-bridge converter. The system provides galvanic isolation and allows bidirectional power flow. A simple control strategy to charge the batteries is considered, based on the regulation of the common- and differential-mode components of the batteries charging currents. In addition, the proposed control system regulates the total dc-link voltage and the dc-link voltage balance in the two systems dc-links. This work is particularly focused on the comparison of the charger performance under two competitive ac-dc converter modulations, in terms of the ac-side voltage harmonic content, the number of switching transitions, the dc-link voltage balance, and the charging current control capacity. Simulation results with the performance comparison are provided and the merits and demerits of each option are highlighted.**

Keywords*— Battery charger, capacitor voltage balance, dual-active-bridge, multilevel converter, nearest-three space-vector modulation, neutral point clamped, virtual vector pulse-width modulation.

I. INTRODUCTION

Battery chargers (BCs) are required in many applications, from domestic to industrial systems. At present, among these applications, it is worth highlighting the importance of the BCs for electric vehicles.

BCs for electric vehicles are typically classified into different categories [1]: supplied from a single- or a three-phase power grid; on- or off-board; with or without galvanic isolation (GI); uni- or bidirectional power flow (BPF) capacity; and with two-level or multilevel (ML) technology. From the topological point of view, BCs are usually implemented with an ac-dc stage connected in cascade with a dc-dc stage [1].

A BC has been proposed in [2], shown in Fig. 1, composed of a three-level ac-dc converter fed from a three-phase ac-grid and connected in cascade to a three-level dual-active-bridge (DAB) dc-dc converter. The DAB converter is then connected to two batteries in series. The system controls the charging currents of the batteries and the balance of both dc-links. Also, it provides GI and BPF capabilities.

The system is complex and involves many degrees of freedom. It is, therefore, worth exploring the different control options in order to optimize its performance. In this work, the performance of the BC under two different pulsewidth modulations (PWM) for the ac-dc converter are compared, in terms of the ac-voltage harmonic content, the number of commutations per switching period (i.e., switching losses), dc-link voltage balancing, and charging current control capability.

In order to quantify the performance of the system, four figures of merit (FoMs) have been defined, obtaining different values depending on the modulation used by the ac-dc converter. The FoMs are the percentage of ripple in the dc-link voltages (rr_{vCa1} and rr_{vCa2}), the harmonic content of the synthesized line-to-line voltage v_{ab} (THD_{vab}), the number of commutations per fundamental period generated in the ac-dc converter, and the steady-state error present in the charging currents (e_{iB1} and e_{iB2}). To ensure proper performance, two requirements are established for the system, which must be met, i.e., rr_{vCa1}, rr_{vCa2}, e_{iB1}, and e_{iB2} must be less than 1.5 %.

The paper is organized as follows. Section II presents the battery charger topology. Section III and Section IV define the general BC control structure and the two considered PWMs for the ac-dc converter, respectively. Section V presents the analysis through simulation of the BC performance and features under the two different PWM options. Finally, Section VI presents the conclusions.

II. BATTERY CHARGER TOPOLOGY

The BC topology under study is presented in Fig. 1 [2]. An ac-dc stage implemented with an inductive filter (L_{ac}) and a three-level three-phase neutral-point-clamped (3L-3P-NPC) ac-dc converter is sourced from a three-phase grid with phase voltages e_a, e_b, and e_c, and line cable resistance R_{ac}. The 3L-3P-NPC converter is connected to a dc-link (A-side dc-link) which is built using the capacitors C_{a1} and C_{a2}, in parallel with bleeding resistors R_{Ca1} and R_{Ca2}. Following, a dc-dc stage is connected in cascade, implemented with a three-level NPC

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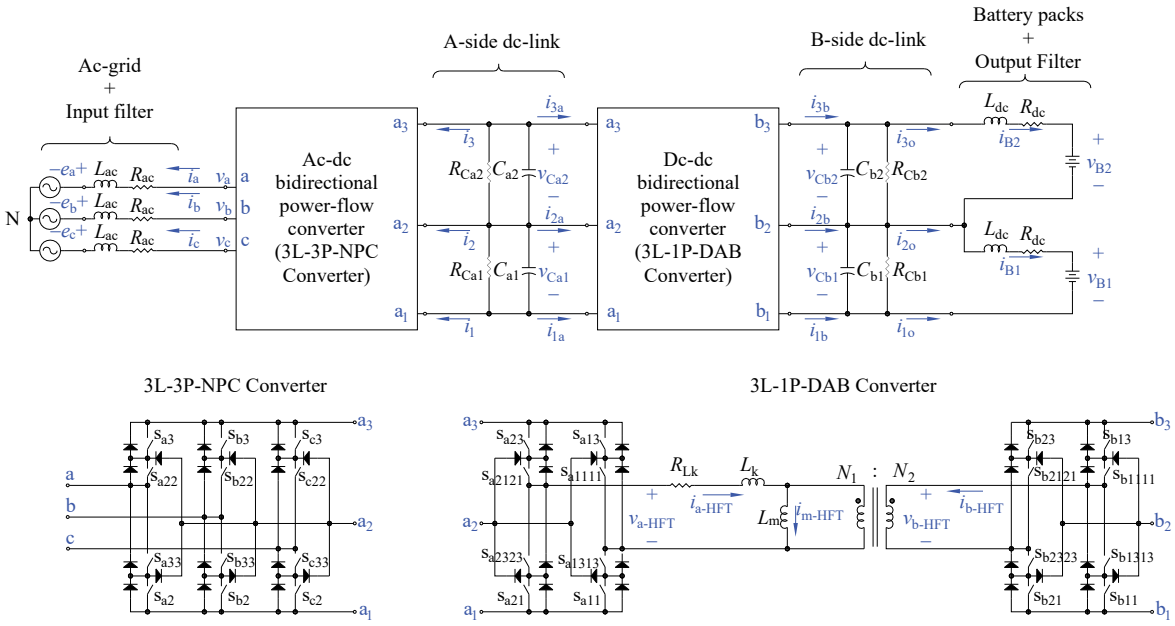


Fig. 1. Battery charger topology [2].

dual-active-bridge (3L-1P-DAB) dc-dc converter. The 3L-1P-DAB converter includes a high-frequency transformer (HFT) with winding resistance R_{Lk}, leakage inductance L_k, and magnetizing inductance L_m. The transformer turns ratio is designated as t_r. This stage is connected to a second dc-link (B-side dc-link) with capacitors C_{b1} and C_{b2} and their respective bleeding resistors R_{Cb1} and R_{Cb2}. Finally, two battery packs with voltages v_{B1} and v_{B2} are connected to the B-side dc-link with wires characterized by their inductance L_{dc} and resistance R_{dc}. Both the 3L-3P-NPC and the 3L-1P-DAB converters feature BPF capability.

III. Control System Description

The full scheme of the control system for the BC is shown in Fig. 2(a). The control goals are, first to regulate the charging currents of the batteries by properly controlling the B-side dc-link voltages, second to regulate the A-side dc-link (total voltage and balance), and third to regulate the power factor of the grid connection.

The controller of the 3L-3P-NPC converter is in charge of regulating the total A-side dc-link voltage (v_{DCa}) and controlling the reactive power exchange with the grid (power factor control) and can be also in charge of keeping balanced the A-side dc-link capacitor voltages (v_{Ca1}, v_{Ca2}). The controller of the 3L-1P-DAB converter is in charge of controlling the charging currents of the batteries (i_{B1}, i_{B2}) and can be also in charge of keeping balanced the A-side dc-link capacitor voltages (v_{Ca1}, v_{Ca2}). Therefore, the A-side dc-link capacitor voltage balancing can be carried out only by the 3L-3P-NPC converter, only by the 3L-1P-DAB converter, or concurrently by both converters. The user can decide which option to choose to keep this voltage balance.

A. 3L-3P-NPC Converter Control

A conventional voltage-oriented control on the dq frame is implemented in the 3L-3P-NPC converter, as shown in Fig. 2(b), which is implemented according to [3]. The total voltage of the A-side dc-link (v_{DCa}) is controlled through a PI compensator (v_{DCa}-Compensator) which supplies the current reference of the d component of the grid current (i_d) which is also regulated by a PI compensator (id-Compensator). On the other hand, the q component of the grid current (i_q) is regulated by a PI compensator (iq-Compensator), to control the power factor of the grid (typically a unity power factor). The id- and iq-Compensators produce the d and q components of the grid voltages which are converted into α-β variables to then obtain the modulation index $m = \text{sqrt}(v_\alpha+v_\beta)$ and the reference angle $\theta = \text{atan}(v_\beta/v_\alpha)$ [3].

The A-side dc-link voltage balance compensator shown in Fig. 2(c) is also implemented. This PI compensator generates a signal that represents the control effort (k_2) required to reduce to zero the dc-link unbalance $v_{Caimb} = v_{Ca1} - v_{Ca2}$ [4].

As shown in Fig. 2(a), the signals m, θ, and k_2 enter the modulator block to generate the leg duty ratios of connection to each dc-link point. Finally, a distributor block produces the corresponding switching signals (switching functions) that determine the control signals of the converter switches.

B. 3L-1P-DAB Converter Control

The control scheme for this converter is shown in Fig. 2(d) and 2(e) [5]. The switching strategy for this converter is illustrated in Fig. 3 and it is based on the modification of switching angles for a given shape of the voltages on the primary and secondary sides of the HFT [5]. Fig. 3 shows the waveforms of the voltages on the primary and the secondary side of the HFT ($v_{a\text{-HFT}}$, $v_{b\text{-HFT}}$); the voltage of the inductance L_k (v_{LK}), and the current $i_{a\text{-HFT}}$. In this strategy, five levels are

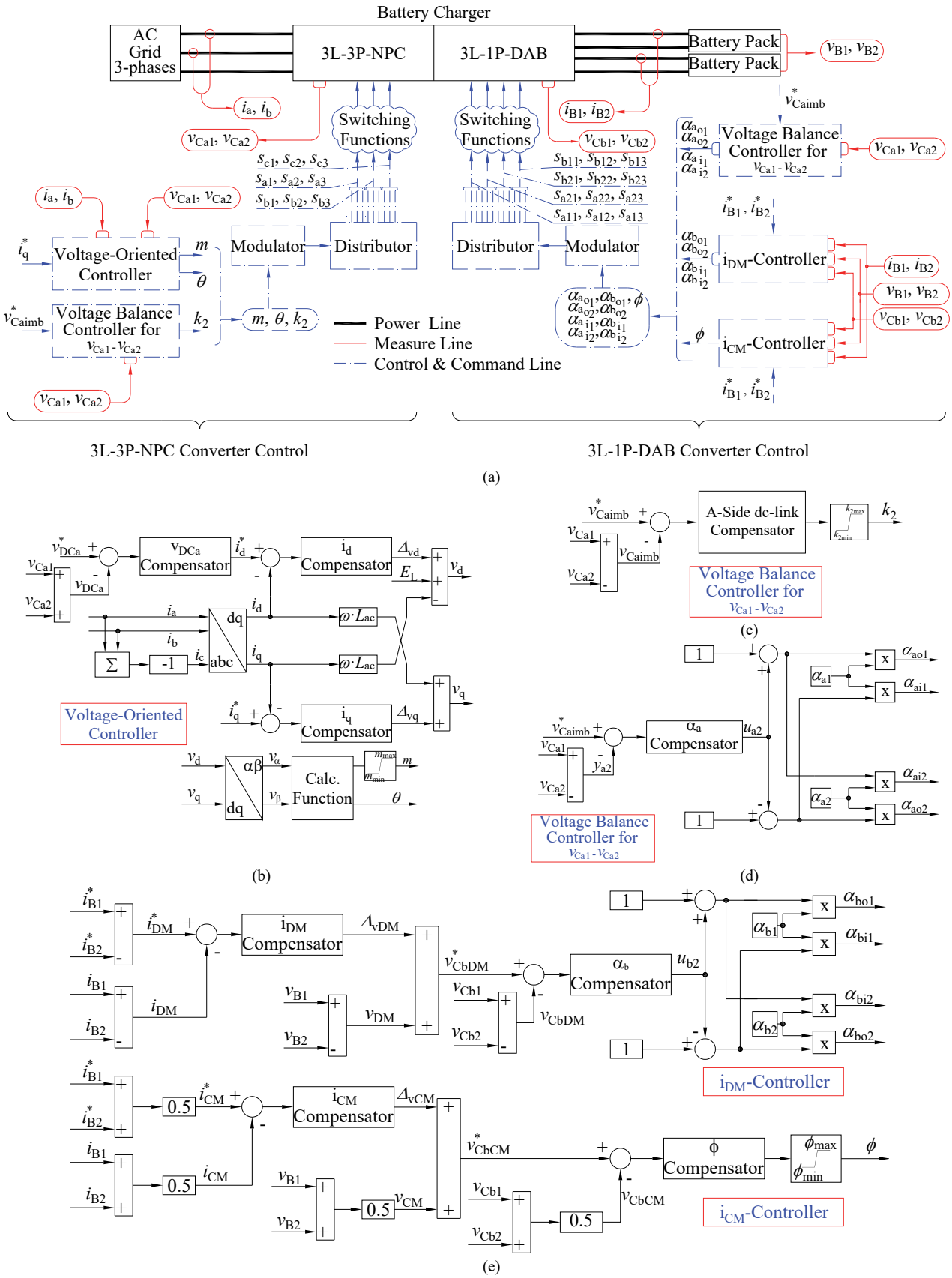


Fig. 2. Control system diagrams [2]. (a) General battery charger control diagram. (b) Voltage-oriented controller for the 3L-3P-NPC converter. (c) A-Side dc-Link voltage balancing control of the 3L-3P-NPC converter. (d) A-Side dc-Link voltage balancing control of 3L-1P-DAB converter. (e) Control scheme of the 3L-1P-DAB converter for i_{DM} and i_{CM} regulation.

produced in the voltages $v_{a\text{-HFT}}$ and $v_{b\text{-HFT}}$. The power transfer between the A- and B-side of this converter and voltages v_{Ca1}, v_{Ca2}, v_{Cb1}, and v_{Cb2} are regulated through phase-shift angle ϕ and switching angles α_{ao1}, α_{ao2}, α_{ai1}, α_{ai2}, α_{bo1}, α_{bo2}, α_{bi1}, and α_{bi2}.

In order to control the currents, i_{B1} and i_{B2} are converted into their corresponding DM- and CM- components which are regulated through the PI compensators, i.e., i_{DM}-Compensator and i_{CM}-Compensator, respectively [2]. This controller is seen in the diagram presented in Fig. 2(e). The i_{CM}-Compensator provides the reference of the CM voltage v_{CM}, i.e., the total B-side dc-link voltage. Then, to control v_{CM}, the power transfer is regulated through the control of the DAB phase shift angle ϕ, using a PI compensator (ϕ-Compensator). That is, the CM current i_{CM} is controlled by regulating the total B-side dc-link voltage through the phase shift angle ϕ regulation.

As the controller provides the option of having different charging currents for each battery pack, there is a need to regulate the DM current component [2].

The i_{DM}-Compensator provides the reference of the DM voltage, i.e., the B-side dc-link voltage imbalance, which is regulated employing a PI compensator (α_b-Compensator). The output of this controller generates the modification of the switching angles α_{bo1}, α_{bi1}, α_{bo2}, α_{bi2} to properly inject or extract electric charge towards or from the neutral point b_2 (see Fig. 1) over a switching period, to lead the system to the reference v^*_{DM}, i.e., the reference B-side dc-link voltage unbalance that provides the desired DM current component.

IV. Modulations for the 3L-3P-NPC Converter

In this work, two different modulations are considered as possible candidates to operate the 3L-3P-NPC converter: a nearest-three-vectors space-vector modulation (NTV-SVM) and a virtual-vector pulsewidth modulation (VVPWM). Both are defined in detail in the following two subsections.

A. NTV SVM

The NTV SVM modulation has been extensively used in the literature, both for conventional and multilevel converters [6]–[8]. This modulation chooses the voltage vectors closest to the reference voltage vector in the space-vector diagram (SVD), achieving a low harmonic content in the output ac voltage. The NTV SVM modulation algorithm is defined in (1)–(4). The initial modulating signals, representing the normalized value of the desired phase voltages, are defined in (1). In (3), these modulating signals are modified introducing a common-mode component: the term $-(mod_{max} + mod_{min})/2$ is used to be able to maximize the maximum amplitude of the fundamental ac voltage in the linear modulation range [9] and the term k_2, provided by the dc-link voltage imbalance compensator in Fig. 2(c), is used to regulate the dc-link capacitor voltage balance. Variable k_2 has to be limited so that $k_2 \in [-1 - mod_{min}, 1 - mod_{max}]$. Finally, in (4), the values of the leg x ($\in \{a, b, c\}$) duty ratio of connection to dc-link point y ($\in \{1, 2, 3\}$), designated as d_{xy}, are calculated. Fig. 4 shows the leg duty-ratio pattern for $k_2 = 0$ over a line cycle.

This modulation can be carrier-based implemented through the comparison of the three modulating signals (mod'_x) in (3) to

$$\begin{aligned} mod_a(\theta) &= (2/\sqrt{3})\cdot m\cdot\cos(\theta) \\ mod_b(\theta) &= (2/\sqrt{3})\cdot m\cdot\cos(\theta - 2\cdot\pi/3) \\ mod_c(\theta) &= (2/\sqrt{3})\cdot m\cdot\cos(\theta + 2\cdot\pi/3) \end{aligned} \quad (1)$$

$$\begin{aligned} mod_{max}(\theta) &= \max[mod_a, mod_b, mod_c] \\ mod_{min}(\theta) &= \min[mod_a, mod_b, mod_c] \end{aligned} \quad (2)$$

$$mod'_x(\theta) = mod_x - (mod_{max} + mod_{min})/2 + k_2, x \in \{a,b,c\} \quad (3)$$

$$\begin{aligned} &\text{if } mod'_x(\theta) \geq 0 \\ &\quad d_{x1}(\theta) = 0 \\ &\quad d_{x2}(\theta) = 1 - d_{x3}(\theta) \\ &\quad d_{x3}(\theta) = mod'_x \\ &\text{else} \\ &\quad d_{x1}(\theta) = -mod'_x(\theta) \\ &\quad d_{x2}(\theta) = 1 - d_{x1}(\theta) \\ &\quad d_{x3}(\theta) = 0 \\ &\text{end.} \end{aligned} \quad (4)$$

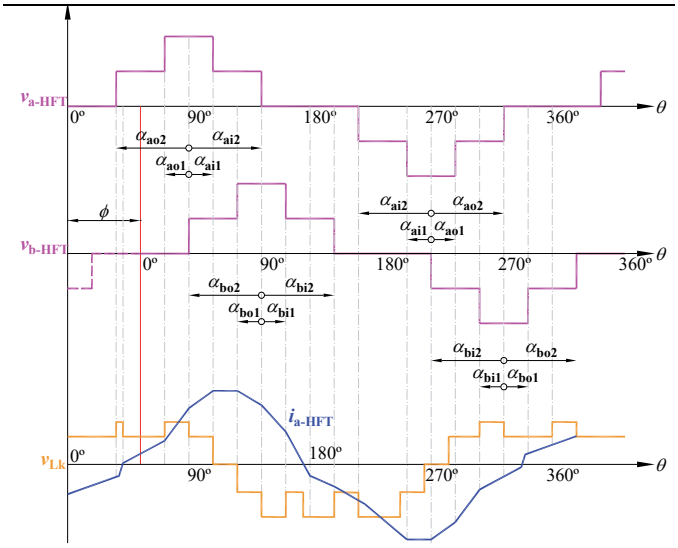


Fig. 3. Voltage waveform $v_{a\text{-HFT}}$, $v_{b\text{-HFT}}$, v_{Lk}, and $i_{a\text{-HFT}}$ for the switching strategy in [5].

two triangular carriers (car_1 and car_2), as shown in Fig. 5. If mod'_x is located above car_2, the leg x is connected to the dc-link point 3 (a_3 in Fig. 1). If mod'_x is located in between both car_2 and car_1, the leg x is connected to the dc-link point 2 (a_2 in Fig. 1). Finally, if mod'_x is located below car_1, the leg x is connected to the dc-link point 1 (a_1 in Fig. 1).

As it is well known, for this modulation strategy with high modulation indexes and low power factors, the balancing of the dc-link capacitor voltages in every switching cycle is not possible, leading to capacitor voltage oscillations at three times the fundamental frequency [9].

B. VVPWM

The VVPWM is based on the construction of a set of special space vectors in the SVD, called virtual vectors, which are defined as a linear combination of certain switching states [10]. Each virtual vector involves an average zero neutral-point current in every switching cycle. In this way, if the reference voltage vector is synthesized with these virtual vectors, the

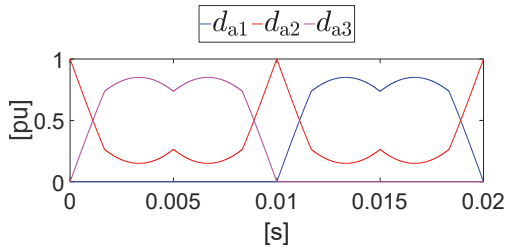


Fig. 4. Leg duty-ratio pattern of the NTV SVM for $m = 0.85$ and $k_2 = 0$. The three waveforms correspond to leg "a". The duty ratios for legs "b" and "c" are the same but phase-shifted $\pm 2\pi/3$ respectively.

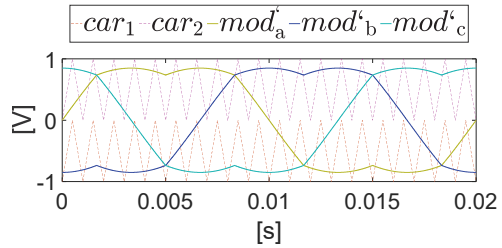


Fig. 5. Carrier-based implementation of the modulation pattern in Fig. 4.

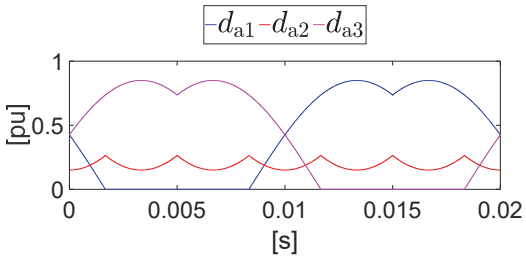


Fig. 6. Leg duty-ratio pattern of the VVPWM for $m = 0.85$ and $k_2 = 0$. The three waveforms correspond to leg a. The duty ratios for legs b and c are the same but phase-shifted $\pm 2\pi/3$ [10].

balance of the voltages of the dc-link capacitors will be guaranteed in each switching cycle [9]–[11].

$$\begin{aligned} d_{x1}(\theta) &= (mod_{\max} - mod_x) / 2 \\ d_{x2}(\theta) &= 1 - d_{x1}(\theta) - d_{x3}(\theta) \\ d_{x3}(\theta) &= (mod_x - mod_{\min}) / 2 \end{aligned} \tag{5}$$

$$m' = \frac{m}{1 + k_2 \cdot \frac{v_{Ca_2} - v_{Ca_1}}{v_{DCa}}} \Rightarrow r = \frac{m'}{m} = \frac{1}{1 + k_2 \cdot \frac{v_{Ca_2} - v_{Ca_1}}{v_{DCa}}} \tag{6}$$

$$\begin{aligned} d'_{x1}(\theta) &= d_{x1} \cdot (1 - k_2) \cdot r \\ d'_{x2}(\theta) &= 1 + [- d_{x1} - d_{x3} + k_2 \cdot (d_{x1} - d_{x3})] \cdot r \\ d'_{x3}(\theta) &= d_{x3} \cdot (1 + k_2) \cdot r. \end{aligned} \tag{7}$$

In practice, the modulation can be implemented through the use of (1), (2), and (5)-(7). In (5), the basic form of the leg duty ratios is calculated, without considering the control action determined by the closed-loop capacitor voltage balancing control. Although the modulation strategy features in principle capacitor voltage balance in all operating conditions, the converter non-idealities can still cause slight capacitor voltage unbalances. Thus, the closed-loop capacitor voltage balance control in Fig. 2(c) is necessary. Its output control parameter k_2 modifies the value of the open-loop leg duty cycles in (5) as indicated in (7) [4]. The correction factor r defined in (6) is necessary to avoid perturbing the intended modulation index value through the capacitor voltage balancing action when both dc-link capacitor voltages are different [4].

V. Simulation Results

Simulations have been carried out with the lossless model which is shown in Fig. 1, using MATLAB-Simulink. The BC is connected to a three-phase ac grid with 400 Vrms line-to-line and f = 50 Hz. Both converters in the BC operate with a switching frequency f_s = 10 kHz. The converter parameter values are listed in Table I. The initial A-side dc-link capacitor voltages are $v_{Ca10} = v_{Ca20} = 400$ V. The A-side dc-link voltage reference is set at $v^*_{DCa} = 800$ V. The initial voltages of the B-side dc-link capacitors (v_{Cb10}, v_{Cb20}) are imposed by the voltages of each battery pack (v_{B1}, v_{B2}). Charging current references (i^*_{B1}, i^*_{B2}) are set to 100 A.

Two operating scenarios were generated according to the type of modulation used by the 3L-3P-NPC converter. In scenario 1, the 3L-3P-NPC converter operates with NTV SVM and in scenario 2, the 3L-3P-NPC converter operates with VVPWM. The system features and performance under each scenario are studied in three cases. In case 1, only the 3L-3P-NPC converter is in charge of balancing v_{Ca1} and v_{Ca2}. In case 2, only the 3L-1P-DAB converter is in charge of this task. Finally, in case 3, both converters are in charge of balancing v_{Ca1} and v_{Ca2}.

Fig. 7 presents the simulation results for scenario 1, depicting the value of voltages v_{Ca1} and v_{Ca2}, leg "a" duty ratios (d_{a1}, d_{a2}, and d_{a3}), and switching angles of the 3L-1P-DAB converter corresponding to side A (α_{ao1}, α_{ao2}, α_{ai1}, and α_{ai2}), with the system in steady-state operation. Fig. 7(a) corresponds to case 1, Fig. 7(b) corresponds to case 2, and Fig. 7(c) corresponds to case 3. Fig. 8 presents analogous results for scenario 2 under the three cases.

From Fig. 7, the values of the percentage of ripple in the dc-link voltages (rr_{vca1} and rr_{vca2}) are calculated and summarized in Table II. It can be seen that the requirement of the maximum 1.5% allowed ripple percentage is not met in any of the cases of scenario 1. However, and according to the results in Fig. 8, this requirement is met in all cases of scenario 2. On the other hand, case 2 of scenario 2 is the one with the lowest percentage. In Fig. 7, it can be observed the existence of a low-frequency harmonic component of around three times the line frequency (150 Hz) in the capacitor voltages v_{Ca1}, and v_{Ca2}, which is consistent with [9], since the 3L-3P-NPC converter uses an

TABLE I. Converter Parameter Values

Parameters	Value
R_{ac}	10 mΩ
L_{ac}	1 mH
$R_{Ca} = R_{Cb}$	10 kΩ
$C_a = C_b$	800 μF
L_k	25 μH
L_m	10 H
R_{Lk}	50 mΩ
t_r	1
R_{dc}	20 mΩ
L_{dc}	1 mH

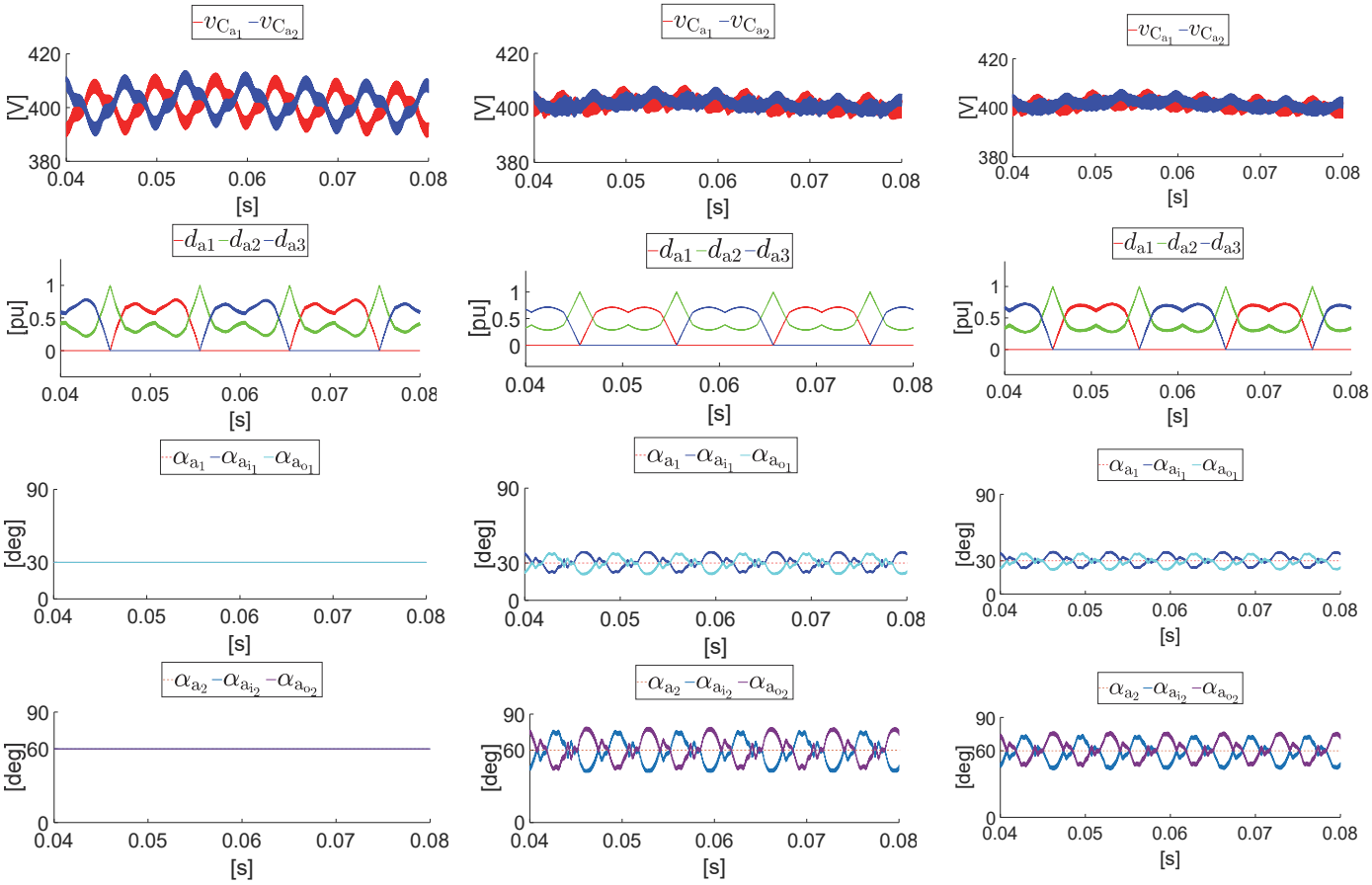


Fig. 7. Simulation of the BC under scenario 1 in steady-state operation. At start-up, the initial voltages $v_{Ca10} = v_{Ca20} = 400$ V. Reference charging current $i^*_{B1} = i^*_{B2} = 100$ A. (a) Case 1. (b) Case 2. (c) Case 3.

TABLE II. SUMMARY OF rr_{vCa1} AND rr_{vCa2}

Scenarios	rr_{vCa1} and rr_{vCa2} in %	Cases		
		1	2	3
1	rr_{vCa1}	5.0	2.3	2.2
	rr_{vCa2}	5.0	2.4	2.1
2	rr_{vCa1}	1.2	1.1	1.2
	rr_{vCa2}	1.2	1.1	1.2

NTV SVM and, hence, capacitor voltage balance is achieved over one-third of the line period. On the other hand, in Fig. 8, as the VVPWM does not generate third-order harmonics (150 Hz) [10], dc-link voltages v_{Ca1} and v_{Ca2} do not present this harmonic component. According to Fig. 7 and Fig. 8 for both scenarios, the leg duty ratios do not saturate, which means that the 3L-3P-NPC converter still has a control margin, enabling a possible reduction of the capacity of the A-side dc-link. From Fig. 7(a), and Fig. 8(a) (case 1 in both scenarios) it is observed that the switching angles remain around their reference values; i.e., $\alpha_{a1} = 30^o$ and $\alpha_{a2} = 60^o$ (see Fig. 2 (d)) which is consistent since in this case, the 3L-1P-DAB converter controller is not responsible for balancing the voltages of the A-side dc-link and, therefore, it does not force any control action. However, when the BC operates under cases 2 and 3 of scenario 1, the 3L-1P-DAB converter is able to mitigate the 150 Hz voltage ripple present in voltages v_{Ca1} and v_{Ca2}, by properly modifying the switching angles (see Fig. 7(b) and Fig. 7(c)). On the other hand, no saturation is seen in these switching angles. Therefore, the 3L-1P-DAB converter still has a control margin, allowing a possible reduction in the capacitance of the A-side dc-link. The total harmonic distortion of the line-to-line voltage (THD_{vab}) and the number of switching transitions per fundamental period generated in the ac-dc converter have been calculated for all cases in both scenarios. The THD_{vab} in scenario 1 (3L-3P-NPC converter operated with NTV SVM) is around 41.25% and it is 50.23 % in scenario 2 (operate with VVPWM). Hence, the THD_{vab} is lower when NTV SVM is used [9], [11]. On the other hand, the number of switching transitions of the 3L-3P-NPC converter in scenario 2 is 4/3 the number of switching transitions in scenario 1, which implies that when operating with VVPWM, the switching losses increase [9], [11].

Fig. 9 shows the dynamics under step changes of the charging currents (i_{B1} and i_{B2}) under case 3. Fig. 9(a) presents the results for scenario 1 and Fig. 9(b) resents the results for scenario 2. At startup, the reference currents (i^*_{B1} and i^*_{B2}) are set to 100 A. Then at 150 ms, there is a step change of i^*_{B1} and i^*_{B2} taking the values 70 A and 130 A, respectively. Finally, at 250 ms, a second step change in i^*_{B1} and i^*_{B2} takes the final values of 130 A and 70 A, respectively. According to Fig. 9(a), it can be seen that the dynamics of the charging currents include

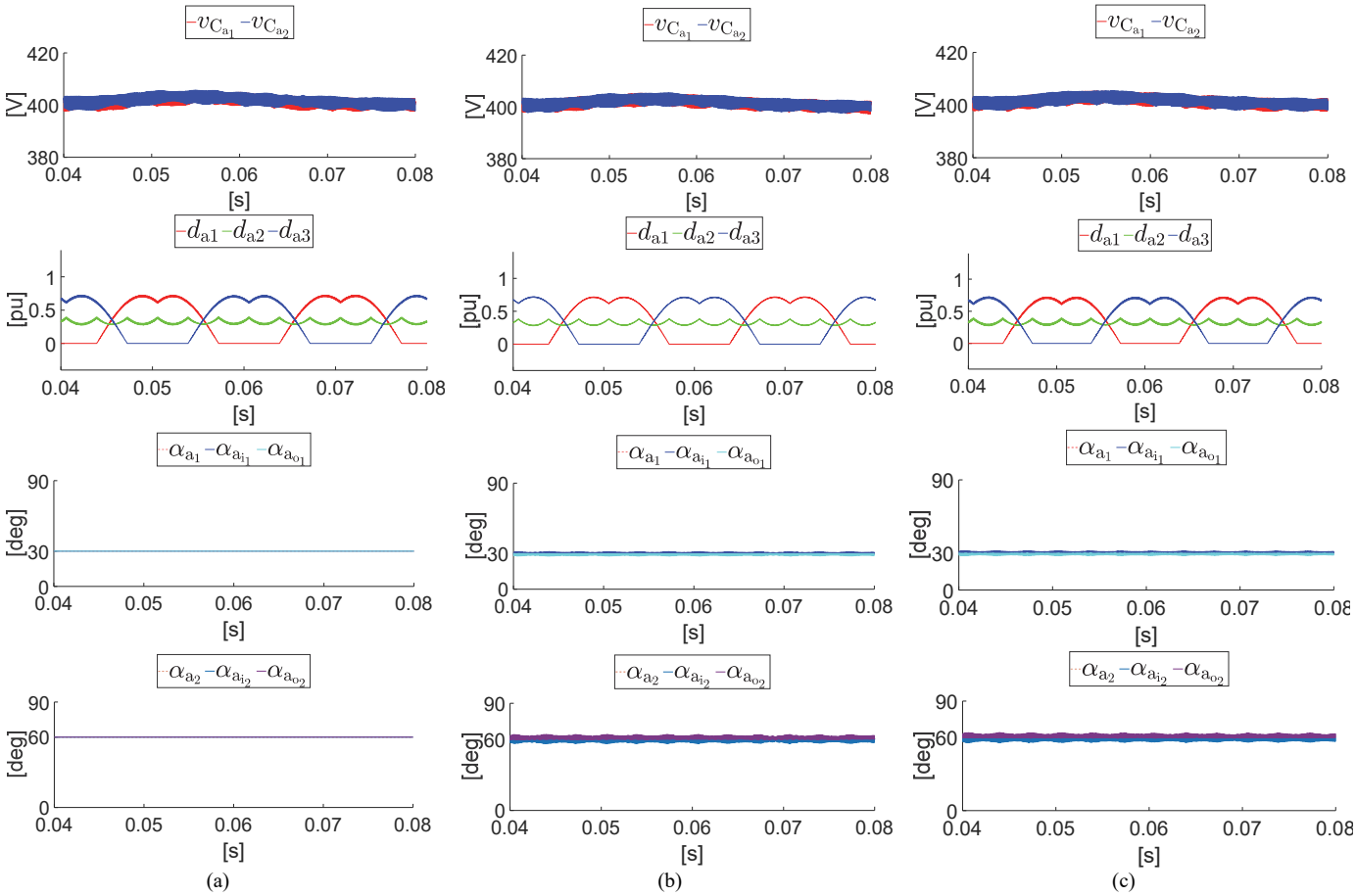


Fig. 8. Simulation of the BC under scenario 2 in steady-state operation. At start-up, the initial voltages $v_{Ca10} = v_{Ca20} = 400$ V. Reference charging current $i^*_{B1} = i^*_{B2} = 100$ A. (a) Case 1. (b) Case 2. (c) Case 3.

an oscillatory component at low frequency (150 Hz) that has been transferred along with the BC.

At the start-up of the system, the magnitudes of the oscillations are very small (around 1 A peak-to-peak) but after the step changes of the references (i^*_{B1} and i^*_{B2}), the magnitude increases (around 4 A peak-to-peak). On the other hand, in Fig. 9(b), under scenario 2, these oscillations are not present. From Fig. 9, the values of e_{iB1} and e_{iB2} are calculated for both scenarios. For scenario 1, e_{iB1} and e_{iB2} are equal to 4.6 % and for scenario 2, e_{iB1} and e_{iB2} are negligible. Therefore, the requirement to keep e_{iB1} and e_{iB2} below 1.5% is only met in scenario 2. The BC presents a better capacity to control charging currents when operating under scenario 2.

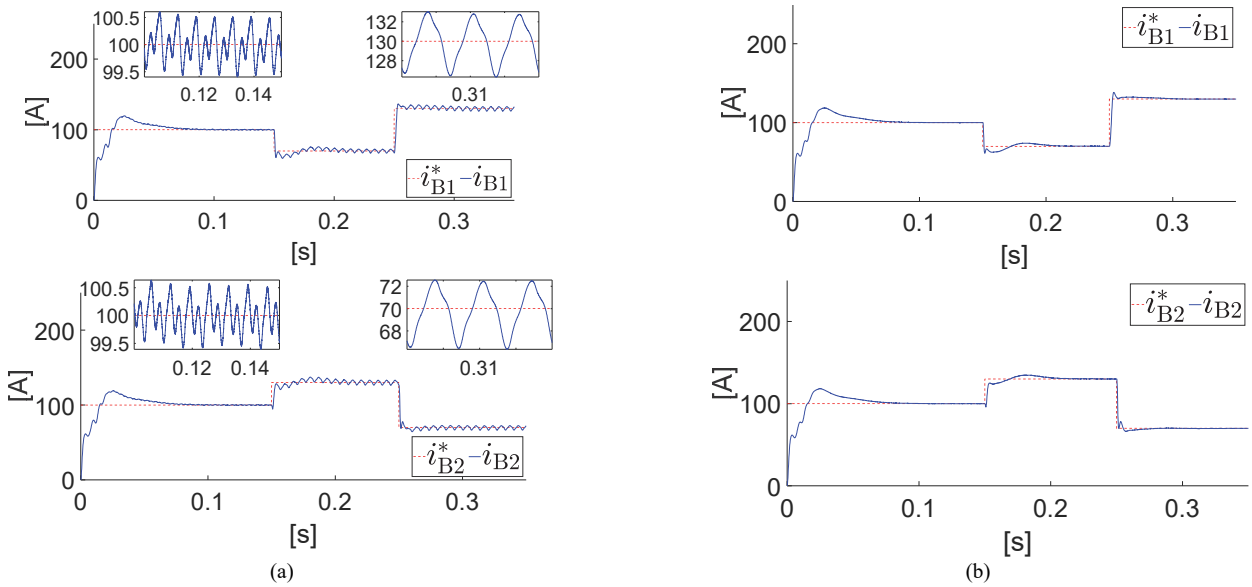
In summary, the simulation results show that, under scenario 2, the BC presents a better capacity, both for the balancing control of the A-side dc-link voltages, and the control of the charging currents (see Table II and Fig. 10). Furthermore, and according to Table II, it can be seen that rr_{vCa1} and rr_{vCa2} are the same for any cases whenever the system operates under scenario 2. On the other hand, under scenario 1, the BC presents lower harmonic distortion of the synthesized line-to-line voltages and lower switching losses in the 3L-3P-NPC converter.

VI. Conclusion

A BC configured with a three-phase three-level NPC ac-dc converter in cascade with a three-level NPC DAB dc-dc converter, and connected to two batteries in series, has been the focus of study in this work.

A control scheme has been selected for the complete system, including the total dc-link voltage control and the dc-link voltage balance control for the two dc-links. This control allows the independent regulation of the charging current of each battery bank, based on the regulation of the differential- and common-mode components of the charging currents.

A comparative study has been performed where the BC performance is analyzed under two possible modulation strategies for the 3L-3P-NPC converter. From this study, it can be concluded that with a VVPWM (scenario 2) the BC presents a larger capacity to balance the A-side dc-link capacitor voltages and to regulate the battery charging currents. Since in scenario 2 the ripple in the capacitor voltages is the same for cases 1, 2, and 3, with only one converter controlling the balancing is sufficient, releasing degrees of freedom that can be used to optimize other performance features, such as the losses in the dc-dc converter. On the other hand, with an NTV SVM (scenario 1), the system presents a reduction of the harmonic



(a) (b)

Fig. 9. Simulation of battery current control transients under case 3. Initial voltages $v_{Ca10} = v_{Ca20} = 400$ V. Reference charging current $i^*_{B1} = i^*_{B2} = 100$ A. Step-change in i^*_{B1} and i^*_{B2} at 150 ms and 250 ms. (a) Scenario 1. (b) Scenario 2.

distortion of the line-to-line voltages generated by the ac-dc converter and it also presents lower switching losses in this converter.

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